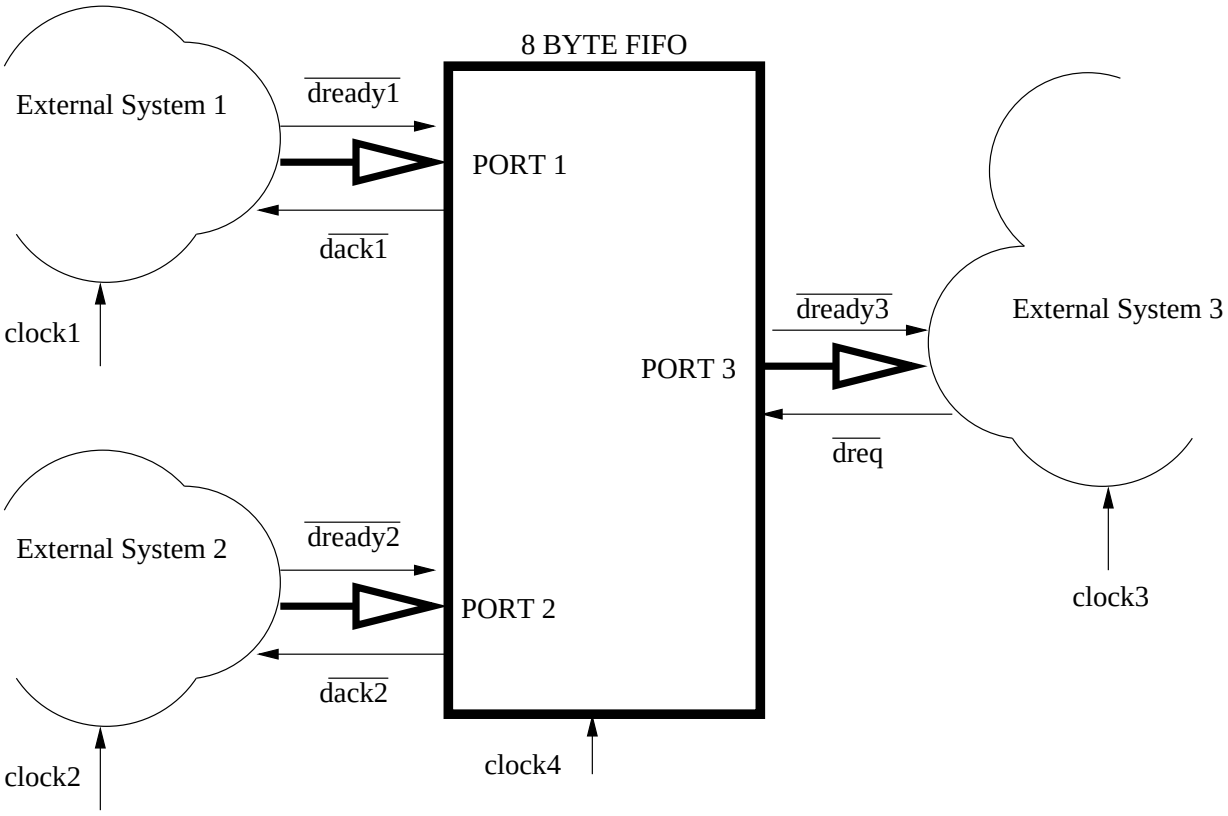
ECE 319 : Digital System Design : Fall 2018

Project III : Due: November 20, 2018.

Design a First-In-First-Out (FIFO) buffer that can store up to 8 data words received at port1 or port2 and deliver them in the same order at port3. Assume that each data word is 8-bit wide.



The external systems that provide data at port1 and port2 use the sender originated protocol and the system that requests data from port3 uses the receiver originated protocol.

Besides the system consisting of the data buffer, you should also design a test bench to simulate the three external systems. The first external system should read data from a file "proj3A.dat" and apply it to your system at port1 using proper handshake. The second external system should read data from the file "proj3B.dat" and apply it to port2 using handshake. The third external system will merely request data at port3 using proper handshake and copy it to its own register.

The four systems (your system and the three external systems simulated in the test bench) should use four independent clocks. To generate these clocks, copy the module *clocks* available on the coursesite to your file. Then instantiate it in your test bench to generate a reset signal as well as the four independent clocks.

To ensure the correct operation of your system under all circumstances, check it thoroughly by permuting application of the four clocks to the four modules.

Your system should have high throughput, i.e., it should respond to external requests as soon as it is possible. It should consume a small amount of power.

Submit a report on your design that includes at the minimum:

- Problem statement
- Design approach
- The complete design including datapath sketch and control state diagram(s).
- Verilog description of the design including a properly set-up test bench.
- Simulation results showing proper waveforms
- Any additional design enhancements you might have used to improve the speed or to reduce power.

Identify yourself clearly in the header of your report and Verilog file. Upload file proj3.v as well as your report to the coursesite by 11:59 PM, Nov 20. Late penalty applies to submissions after the due date. (For this purpose, the date stamp on the web submissions of the Verilog file is considered as the submission date).