

# EE5811 : FPGA LAB

## ASSIGNMENT 1

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EE20RESCH11012

## 1 Problem

Derive a Canonical SOP expression for a Boolean function  $F$ , represented by the following truth table

A	B	C	F(A,B,C)
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

## 2 Solution

### 2.1 KMAP Implementation

		$BC$			
		00	01	11	10
$A$	0	1	0	1	0
	1	1	0	1	0

Figure 1: SOP for F using KMAP

The given expression can be minimized using KMap as shown in Figure 1. Using implicants in figure, SOP terms obtained are:  $\bar{B}\bar{C} + BC$

### 2.2 Minimized SOP Expression

$$F = BC + \bar{B}\bar{C} \quad (1)$$

### 2.3 NAND Expression

To express the given SOP expression using NAND gates, we have

$$F(A, B, C) = BC + \bar{B}\bar{C} \quad (2)$$

$$F(A, B, C) = \overline{(\overline{BC + \bar{B}\bar{C}})} \quad (3)$$

$$F(A, B, C) = \overline{(\bar{B}\bar{C} \cdot \overline{\bar{B}\bar{C}})} \quad (4)$$

## 2.4 NAND Gate Implementation

Circuit diagram with NAND gates is shown below:

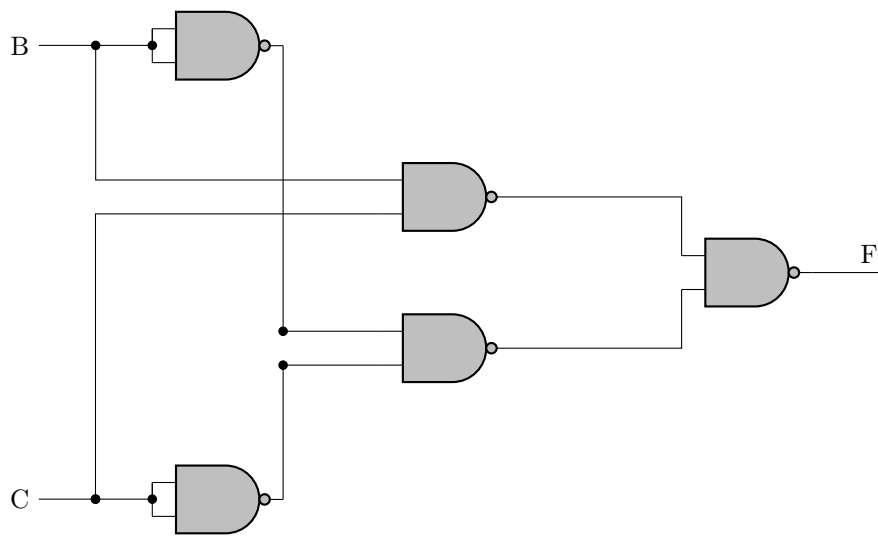


Figure 2: NAND gate implementation for  $F$