Superconducting qubit: Assembling a quantum processor - Leonardo DiCarlo

Hi! Today I will show you how we can assemble a quantum processor from circuit QED quantum hardware. I will focus on the approach to fault-tolerant quantum computing named Surface Code, which we pursue within QuTech.

Surface code calls for a 2-dimensional square lattice of qubits with only nearest-neighbor interactions In addition, these qubits must be individually addressable both for single-qubit gating and for measurement.

Currently, we are testing surface-code chips with 7, 17 and 49 qubits. We call these Surface-7, Surface-17, and Surface-49. We assemble all of these using a common approach that we believe scales to larger surfaces. I will now describe this approach using the specific example of Surface-17.

First we layout the square lattice of qubits. Let me symbolize the qubits by circles. Please disregard their assigned color, for now. To perform two-qubit conditional-phase gates between nearest neighbors, as presented by Adriaan, we add, first, a coupling bus resonator to interconnect them; and second, a dedicated flux-bias control line to each qubit.

To perform single-qubit gates, we follow the approach introduced by Brian, adding a dedicated microwave drive line to each qubit.

Finally, in order to measure each qubit individually, we add dedicated readout resonators. These readout resonators are coupled to diagonally running feedlines and probed independently using frequency division multiplexing as described by Niels.

You may have already noticed the crossing of transmission lines on the chip, which is not possible in a truly planar structure. For this, we make use of the third dimension, in the form of air-bridge crossovers. Cool stuff, isn't it?

Beautiful. So let's look at the totals for Surface-17: 17 qubits, 24 buses, 17 readout resonators, 17 flux lines, 17 microwave drive lines, and 3 feedlines. The grand total of ports connecting the quantum chip to the outside world is 40.

We call these ports vertical I/O ports because they connect to the outside world not via the edges of the planar chip, as traditionally done, but vertically. In one approach, which we purse together with Intel, the quantum chip is flipped and the ports connect directly to a multi-layer printed circuit board using a ball-grid array.

Achieving reliable vertical interconnect has been a key pursuit in our field over the last few years!

Now, let's go back to the colored circles representing our transmon qubits. Except on the edges, qubits couple to 7 objects: 4 buses, 1 readout resonator, 1 flux line, and 1 microwave

line. These interconnectivity requirements give our transmons a characteristic shape and nickmane, Starmon.

The colors we assign to the circles denote the qubit operating frequency, at which single-qubit gates are performed. In total, four frequencies suffice to control a surface-code of any size! This affords us significant savings in the microwave-frequency control electronics (which unfortunately, I don't have time to discuss here). But with regards to the quantum hardware, this repetition of qubit frequencies allows us critically to define an 8-qubit unit cell.

By exactly replicating this 8-qubit unit cell and performing the necessary truncation at the boundaries, we can build a surface code of arbitrary size!

In fact, we put together Surface-49 test chips in this very way, literally copy-pasting and truncating.

We believe this approach will scale to even larger surface codes, such as Surface-97. I leave you with the CAD drawing of such a future chip!