DBNG Measurements

Rubens Figueiredo

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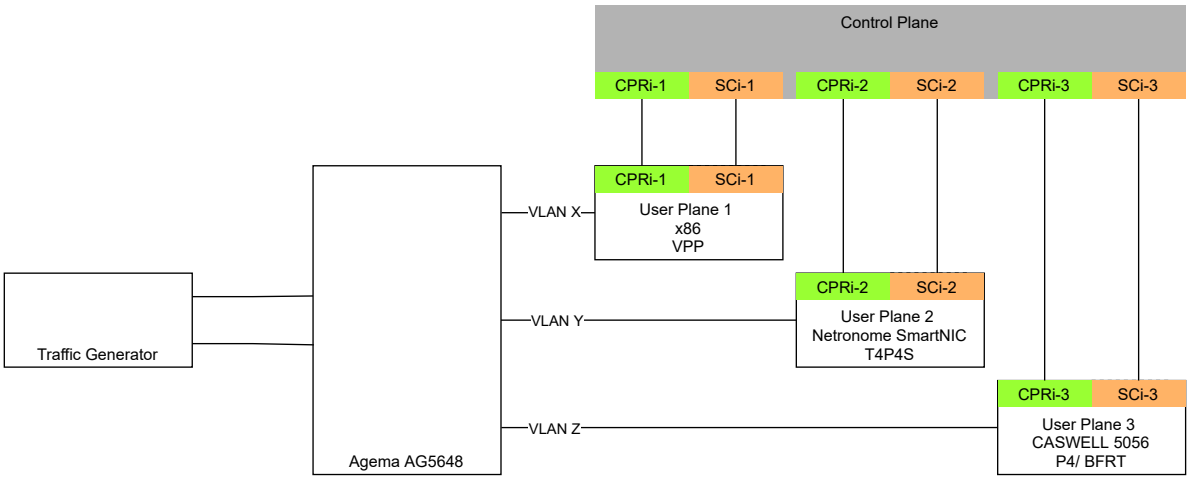

Figure 1: Planned testbed of the multiple dataplanes

Figure 1 shows the planned testbed for benchmarking the different platforms. The goal of the effort is to study the performance of different DBNG solutions based on different architectures.

The hardware under study is the following. These platforms where chosen as they provide 3 different solutions to deploy the DBNG-UP.

- **General purpose CPU** This shall be a general purpose x86, and the UP will run on VPP. Alternatively also deploy a T4P4S based DPDK container.
- **Netronome SmartNIC** The Netronome 4000, and the UP will run on a DPDK application compiled from T4P4S.
- **CASWELL 5056** A combination between the Intel Tofino ASIC and Stratix FPGA. The P4 pipeline will run on the Tofino, and the FPGA run the traffic shaping application.

The traffic generator deployment will be deployed as follows. The traffic generator under investigation to be deployed shall be the trex traffic generator, that shall be employed for the data traffic generation, and bngblaster for session setup.

The benchmarks shall be performed under the following variables. A set of 10 repeated measures for the duration of 45 seconds

- number of clients = [1, 50, 100, 500, 1000]
- Size of packets = [64, 128, 512, 1024, 1400]

The following measurements shall be taken.

- **Control channel throughput**: bngblaster provides output for the setup rate in CPS (clients per second). Pick up this measure, and evaluate the performance of sessions setup. Necessary to evaluate *only* the channel performance, and not the rest of the control plane. Find scalable solutions for the CP applications (accel-ppp, RADIUS, SQL)
- **Latency**: Employ STAMP [1] to capture accurate timestamps in the up/ downlink direction. For the P4 based platforms, this timestamping tool could be implemented in the dataplane, but in the VPP platform, a specific consumer needs to be handling the packets. Need to pay attention to the clock or system time information, to ensure accurate timestamps.
- **Jitter**: Using the latency information calculate the diff.
- **CPU utilization**

Further measurements will be taken based on the specific platform requirements.

The following results are to be expected and/ or validated.

- Low performance of the PCIe channel between the NIC and CPU with small packets [2]
- Inconsistency during Control Plane updates, batch vs rate [3]
- Effects on/of memory
- Effects on/of CPU
- Throughput/ Jitter/ Delay
- Overall Performance and main indicators

References

[1] G. Mirsky, G. Jun, H. Nydell, and R. F. Foote, "Simple Two-Way Active Measurement Protocol." RFC 8762, Mar. 2020.

[2] R. Neugebauer, G. Antichi, J. F. Zazo, Y. Audzevich, S. López-Buedo, and A. W. Moore, "Understanding pcie performance for end host networking," in *Proceedings of the 2018 Conference of the ACM Special Interest Group on Data Communication*, pp. 327–341, 2018.

[3] G. P. Katsikas, T. Barbette, M. Chiesa, D. Kostić, and G. Q. Maguire, "What you need to know about (smart) network interface cards," in *International Conference on Passive and Active Network Measurement*, pp. 319–336, Springer, 2021.