

# Proyecto Cerradura Electrónica

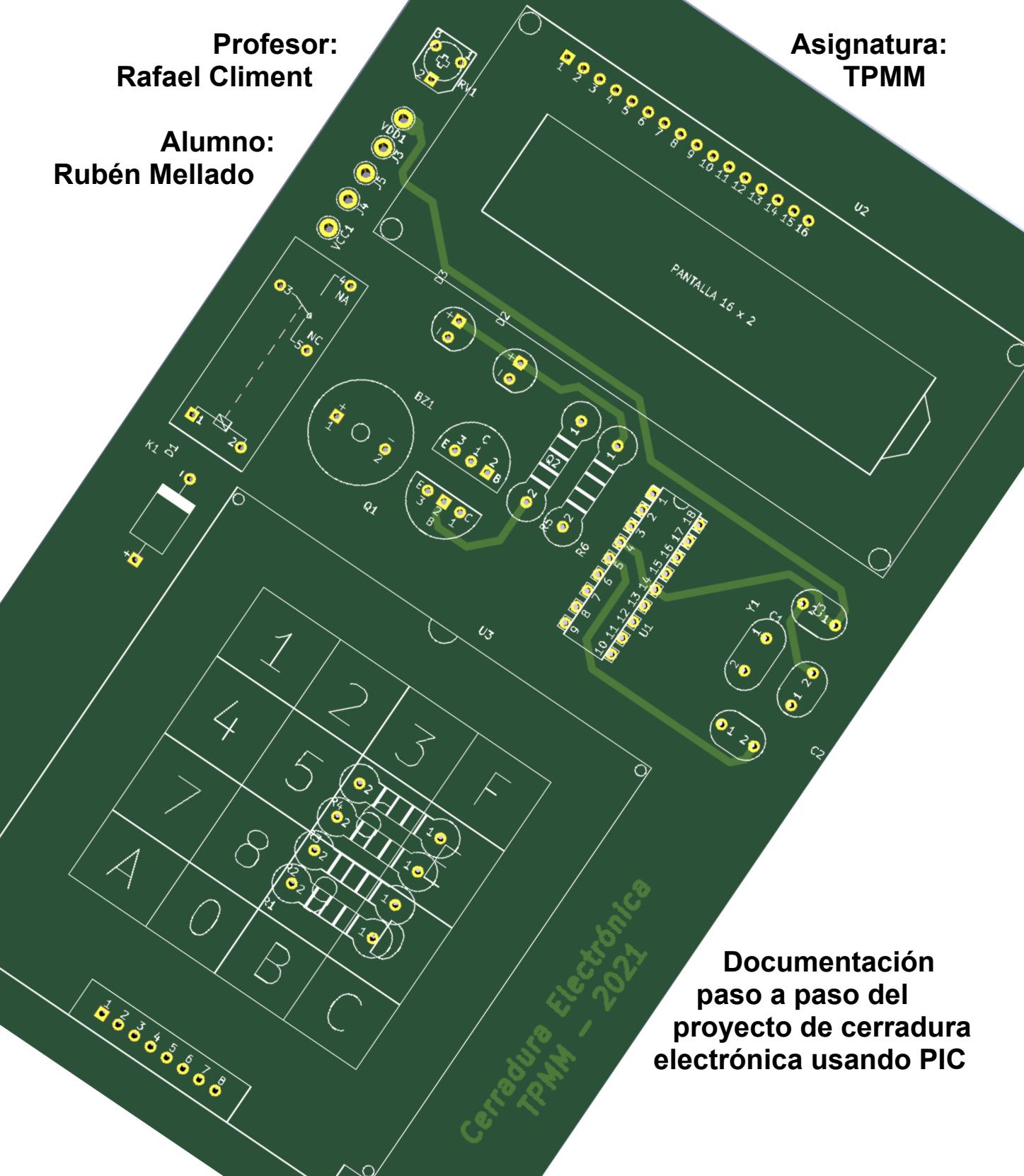
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TPMM



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## 1 - Memoria e introducción.

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Para finalizar el curso, hemos tenido que diseñar, montar y soldar, una placa PCB desde cero, con sus respectivos componentes.

El profesor Rafa nos facilita el diagrama esquemático de las interconexiones de los componentes, los cuales son necesarios para la realización completa de este proyecto.

Permitiéndonos la libertad de modificarlo con tal de mejorarlo, si es que este nos lo permite.

Tras esto, nuestro trabajo consistirá en realizar el diseño en un programa informático orientado al diseño de PCBs llamado KiCad, en su versión 5.0. Más tarde, comprar los componentes. Preparar la placa PCB. Montar los componentes en el circuito. Y por último documentarlo todo, en previsión de un posible montaje similar a futuro.

En este caso, no hemos elegido la versión que incorpora una fuente de alimentación 220v AC. Así que dependemos de tener previamente una fuente de alimentación regulada aparte, con tal de hacer funcionar el circuito de manera óptima.

Para las medidas de la placa, deberemos tener en cuenta las medidas y cantidad de componentes a colocar. Para este caso, Rafa el profesor, nos facilita una placa de PCB con las medidas de 100 mm x 160 mm.

### 1.1 - Memoria descriptiva.

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Lo que queremos hacer con la cerradura electrónica es facilitar la apertura de una puerta, sin necesidad de portar consigo un medio físico como lo sería una llave o una tarjeta RFID.

Esta permitirá la apertura de la puerta durante cierto tiempo delimitado en su código de configuración, tras haber introducido correctamente el código que permite abrirla.

En este caso, la hemos diseñado sin una fuente de alimentación incorporada, lo cual permite aligerar el peso, y facilitar su portabilidad. Cabe destacar, que permite así poder usar una fuente externa de inferior tensión, o sin necesidad de una entrada de 220V AC de un toma corriente de pared.

Por ejemplo para un uso en una autocaravana, o en una caseta de campo, que no disponga de alimentación eléctrica de acometida, pero sí de una fuente tipo panel solar con baterías.

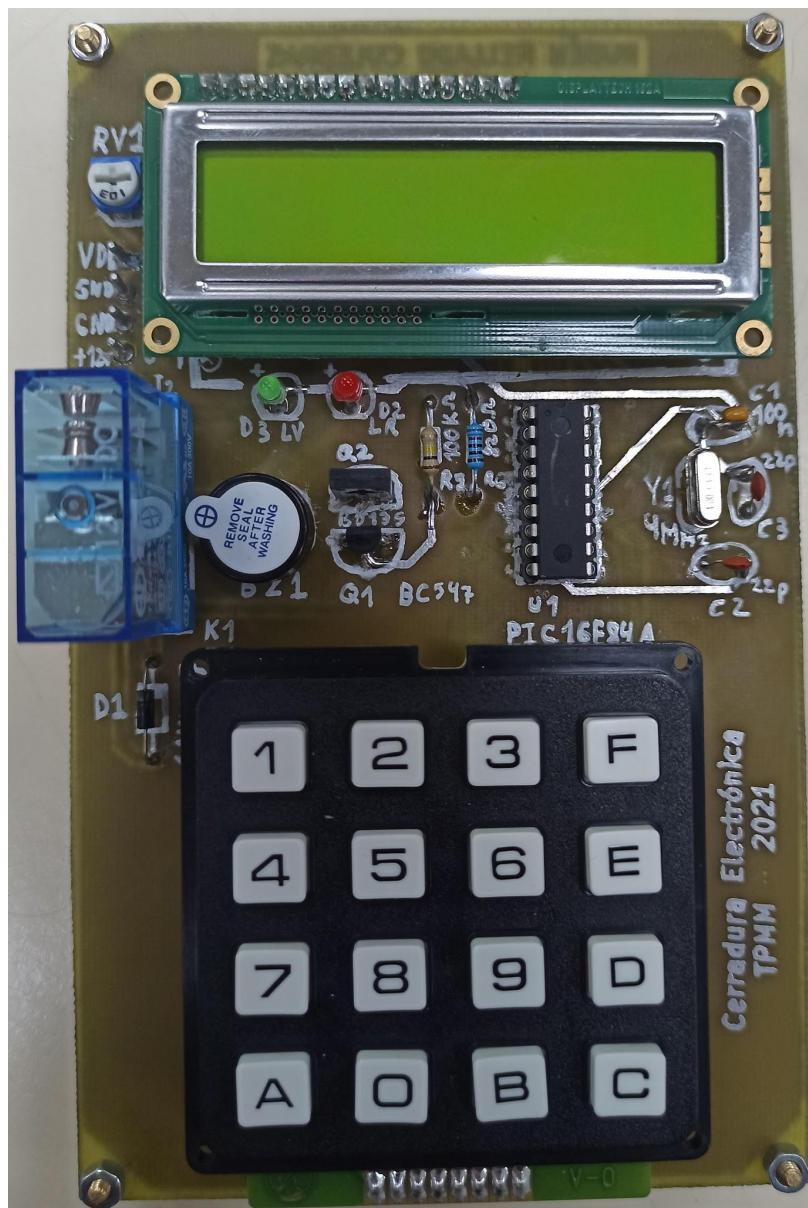
En esta hemos incorporado unos componentes para interfaz humana. Como son: el teclado, para poder introducir la secuencia de caracteres que componen la contraseña; y una pantalla LCD, para saber si se ha introducido correctamente esta.

Si se introduce correctamente la contraseña que introduciremos en el código del programa que contiene el PIC, este, enviará una señal de tensión que variará el estado actual del relé accionados mecánicamente, este activará el desbloqueo de la puerta de acceso, durante un tiempo preestablecido. Tras esto el relé volverá a su estado anterior, el de reposo.

Otros componentes visuales aparte de la pantalla LCD, son los 2 pilotos LED, el rojo indicando que la cerradura está cerrada, y el verde, indicando que la cerradura está abierta. Aparte del zumbador, que nos permitirá saber si se ha abierto la puerta, al activarse a la vez que el piloto LED verde.

Como preferencia de montaje, pondremos el teclado debajo de la pantalla. Y el resto de componentes donde mejor quepan, pensando en su posterior posible mantenimiento o reemplazo a futuro.

Todo esto, se va a alojar en una placa PCB de doble cara de pistas, con las dimensiones de 160mm x 100mm. La cual veremos su proceso para hacer las pistas y su revelado, más adelante.



## 1.2 - Información de la pantalla LCD.

Número pin	Nombre pin	Para que se usa ese pin
1	VSS	Negativo o GND
2	VDD	Voltaje de alimentación 5V (4.7V-5.3V)
3	V0	Variar la retroiluminación del LED con un potenciómetro externo
4	RS	Lee los comandos y datos registrados, según su estado (alto, bajo)
5	RW	En estado bajo escribe en el registro y en alto lee el registro
6	E	Cuando recibe un pulso de alto a bajo, habilita el envío de datos a los pines de datos
7	D0	Pines para datos 8 bits
8	D1	
9	D2	
10	D3	
11	D4	
12	D5	
13	D6	
14	D7	
15	A	Positivo del LED 5V
16	K	Negativo del LED 0V

La pantalla usada en este proyecto es del tipo LCD 16x2. Esta dispone de una buena resolución a la hora de ver los mensajes, para todos estos tipos de proyectos. Aparte de sus bajos precios, y su estandarización en la industria.

Para evitar sobrecalentamiento, y ahorrar en consumo eléctrico. Si vemos que permite su correcta lectura y visualización del texto mostrado, podemos optar por desconectar los terminales 15 y 16 de la pantalla, que son para la retroiluminación de esta.

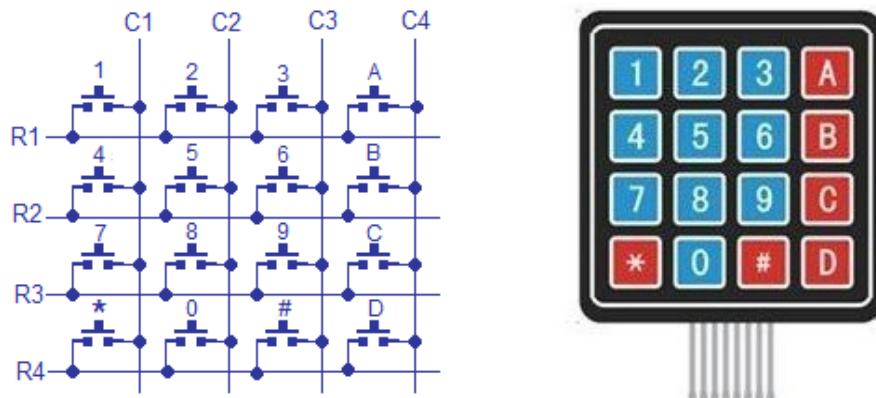


\* Para más información ir al capítulo 10 (Anexos), en [Pantalla LCD 16x2..](#)

### 1.3 - Información del teclado.

Es un teclado Hexadecimal completo. Formado por 16 teclas, que están formados por una matriz de 4x4, y con un conexiónado de salida de 8 pines en total.

Para la protección de este, se pone en 4 pines una resistencia, por ejemplo de 100 Ohmios, y los 4 siguientes tal cual están.



\* Para más información ir al capítulo 10 (Anexos), en [Teclado hexadecimal](#).

### 1.4 - Información del PIC.

Este componentes es un circuito integrado que se puede programar para muchos posibles usos. Este pequeño es altamente capaz de mover sobradamente este proyecto y aún le sobran pines para más posibles funciones a añadir en el circuito.

Debido a su éxito y expansión en el mercado, se puede encontrar con facilidad tanto proyectos de la comunidad, hojas de datos técnicos, posibles usos y aplicaciones, etcétera.

Requiere una tensión de 5V a la entrada, y un cristal de cuarzo externo, para poder usar el PIC.

Debido a su configuración interna, a la hora de usar un software para controlarlo, este facilita su programación, borrado, y reescritura, ya que es de tipo flash.

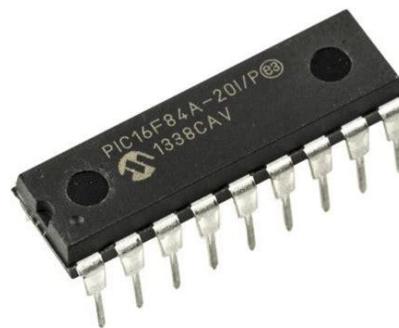
Es recomendable para poder modificar su código programado, colocarlo en la placa PCB, pero encima de un zócalo de pines, sin tener que soldar directamente el PIC a la placa. Esto permitirá su fácil extracción a futuro, mejora, o ampliación.

Tener en cuenta, que para este circuito, necesitaremos el uso de doble cara de pistas, ya que por este componente van a pasar varios buses, y si fuese a una cara, este nos haría tener que hacer muchos puentes o nudos.

Para todo esto, recordar que es un componente delicado, y hay que asegurarse de que no tenga ningún cortocircuito incondicional entre sus pines.

Una tabla de las entradas y salidas de cada pin que contiene el PIC que vamos a utilizar.

Número pin	Nombre y configuración en el PIC16F84A
1	RA2
2	RA3
3	RA4 / TOCKI
4	MCLR
5	VSS
6	RB0 / INT
7	RB1
8	RB2
9	RB3
10	RB4
11	RB5
12	RB6
13	RB7
14	VDD
15	OSC2 / CLKOUT
16	OSC1 / CLKIN
17	RA0
18	RA1



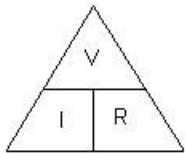
\* Para más información ir al capítulo 10 (Anexos), en [PIC16F84A](#).

## 1.5 - Cálculos de resistencias.

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Para usar LEDs en el circuito, al alimentarlo con una tensión de alimentación distinta a la nominal marcada por el fabricante, vamos a tener que hacer uso de resistencias en serie para cada uno, con tal de evitar el deterioro prematuro, y que se puedan quemar.

Según la ley de Ohm:



Por lo que si vamos a usar una fuente de 12V, y el LED requiere 2V (según el color), se quemará al conectarlo.

Los LED suelen funcionar con una corriente de entre 5mA y 40mA. A partir de 10mA suelen iluminar lo suficiente. Vamos a calcularlo para 15mA.

En el caso de que la resistencia calculada, no se venda comercialmente, deberemos ir a la inmediatamente superior. Por ejemplo, si da 300 Ω, deberemos ir a 390 Ω.

Entonces, hay que calcular la resistencia, y en este caso, vamos a calcularlo para un uso de 15mA pasando por el LED.

Si hacemos el cálculo, para conectar a 12V:

$$\frac{V_F - V_L}{I_C} = R \rightarrow \frac{12V - 2V}{15mA} = R \rightarrow \frac{10V}{0'015A} = R \rightarrow 670 = R$$

Por lo que la resistencia para conectar el LED a 12V de tensión de entrada, tendrá que ser de 670 Ω o superior, con tal de proteger al LED.

Si hacemos el mismo cálculo, pero para conectar a 5V:

$$\frac{V_F - V_L}{I_C} = R \rightarrow \frac{5V - 2V}{15mA} = R \rightarrow \frac{3V}{0'015A} = R \rightarrow 200 = R$$

Por lo que la resistencia para conectar el LED a 5V de tensión de entrada, tendrá que ser de 200 Ω o superior, con tal de proteger al LED.

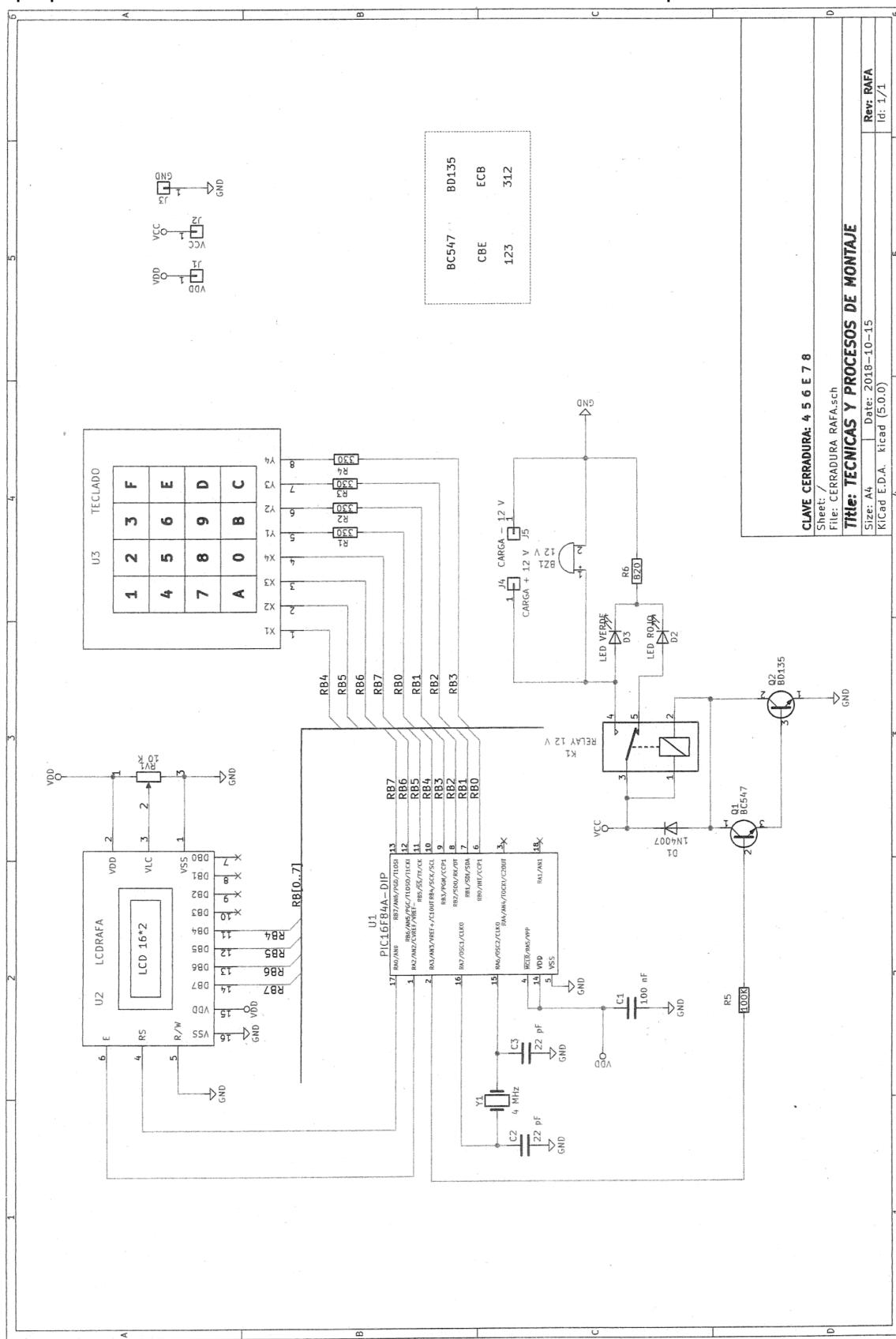
## **1.6 - Pasos que vamos a realizar.**

Nuestro trabajo consistirá en:

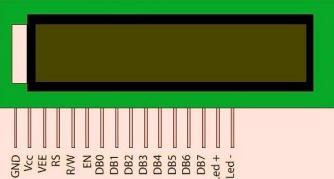
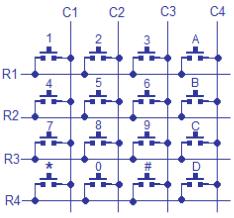
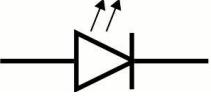
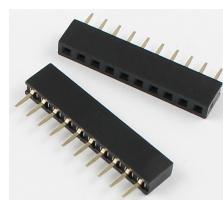
- Virtualizar el diagrama esquemático facilitado por Rafa.
- Tomar las medidas de los componentes reales.
- Diseñar y crear las huellas de los componentes.
- Asignar las huellas a los componentes.
- Diseñar el circuito final.
- Adaptar el diseño del circuito final, al tamaño de la placa.
- Comprar los componentes necesarios.
- Comprobar que sean de la medida de las huellas impresas.
- Revelar las pistas electrónicas.
- Estañar las pistas electrónicas.
- Retocar con el cutter las pistas que se hayan juntado en el revelado.
- Perforar la placa para poder colocar los componentes.
- Verificar que no haya continuidad o esté puentead a alguna pista.
- Colocar y soldar los componentes.
- Finalizar el montaje y testearlo.

## 2 - Diagrama esquemático de conexiones.

Aquí podemos ver la ubicación e interconexión de cada componente en el circuito.



## 2.1 - Símbolos de componentes

Símbolo	Descripción	Imagen
	Pantalla LCD 16 x 2	
	Teclado hexadecimal	
	Resistencia valor variable	
	Resistencia valor fijo	
	Diodo rectificador	
	Diodo LED	
	Zumbador acústico	
	Relé mecánico de 1 entrada	
	Pines para teclado y pantalla	

	Pines para el PIC	
	Espadines entrada tensión	
	PIC16F84A programable	
	Cristal oscilador de cuarzo	
	Condensador tantalio	
	Condensador cerámico	
	Transistor NPN	
	Placa de baquelita	
	Cableado	
	Puesta a tierra o GND	

## 2.2 - Tomar medidas de los componentes.

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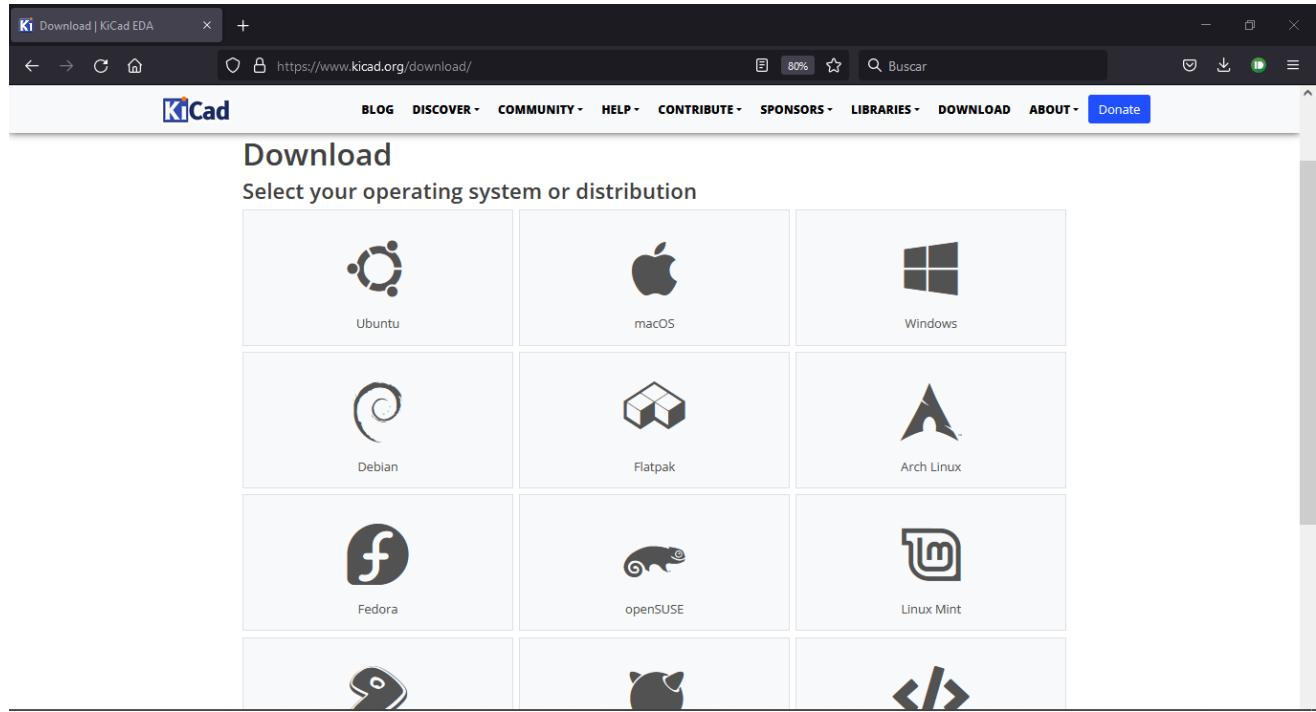
Este paso es importante para poder crear el dibujo de nuestros componentes en una librería del software del editor de PCBs en nuestro ordenador.

Con esto, conseguiremos que las medidas reales, pasen al dibujo de ordenador. Así al generar el archivo de PCB, los pines encajarán correctamente. Medido en mm.

Pantalla LCD 16 x 2	80mm x 36mm		Pines para teclado y pantalla y pic	2.54mm entre pines
Teclado hexadecimal	65mm x 69mm		Espadines tensión	5mm entre pines, por seguridad
Resistencia valor variable	7mm x 6mm		Cristal oscilador de cuarzo	11mm x 3mm 5mm entre pines
Resistencia valor fijo	14mm		Condensador tantalio	4mm
Diodo rectificador	14mm		Condensador cerámico	4mm
Zumbador acústico	14mm x 14mm		Diodo LED	2.54mm
Relé mecánico de 1 entrada	29mm x 11mm		Transistor NPN	5mm
PIC16F84A programable	23mm x 8mm 6mm entre las 2 filas		Placa de baquelita	160mm x 100mm

### 3 - Uso de software KiCAD para esquema y diseño.

Para descargar el software en cuestión, vamos a ir a la web oficial de KiCAD.



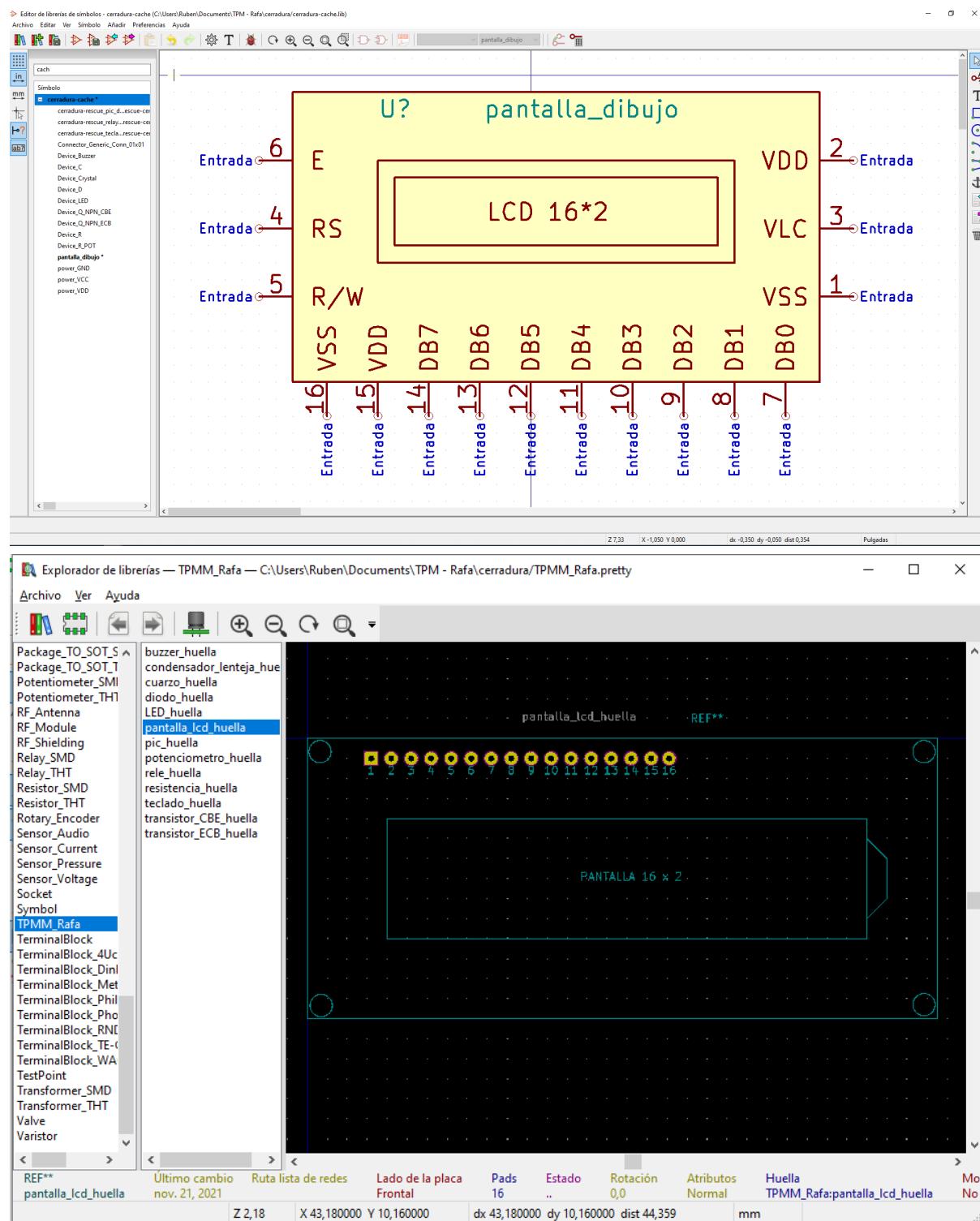
Se descarga el archivo para el sistema operativo desde el que vayamos a usarlo. En este caso, la versión 5.0.0 para Windows, es la que vamos a utilizar.

A screenshot of a web browser displaying the 'KiCad Downloads' page. The page lists various executable files for different versions of KiCad. The table includes columns for file name, date, and size. The file 'kicad-5.0.0-i686.exe' is highlighted with a blue border, indicating it is the selected download. Other files listed include kicad-5.1.2\_2-i686.exe, kicad-5.1.2\_1-x86\_64.exe, kicad-5.1.2\_1-i686.exe, kicad-5.1.1\_1-x86\_64.exe, kicad-5.1.1\_1-i686.exe, kicad-5.1.0\_1-x86\_64.exe, kicad-5.1.0\_1-i686.exe, kicad-product-4.0.2-x86\_64.exe, kicad-5.1.2\_1-i686.exe, kicad-5.0.1\_1-i686.exe, kicad-5.0.1\_1-x86\_64.exe, kicad-product-4.0.0\_rc2-x86\_64.exe, kicad-product-4.0.4-i686.exe, kicad-5.0.2\_1-x86\_64.exe, kicad-product-4.0.1-x86\_64.exe, kicad-4.0.7-i686.exe, and kicad-4.0.5-i686.exe.

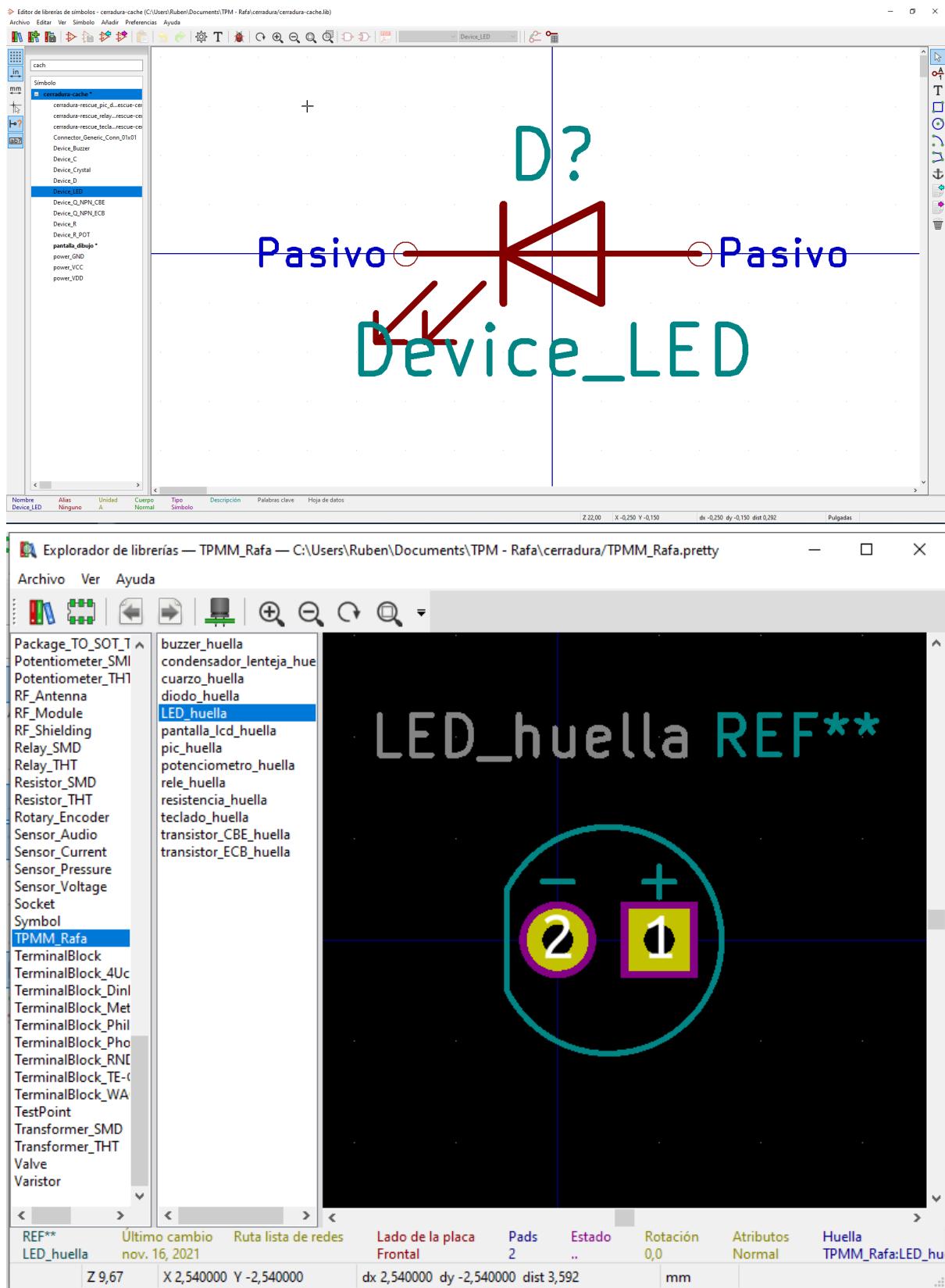
### 3.1 - Pasar medidas a la librería digital.

Creamos una librería propia, para no depender de las librerías que contenga el editor de PCBs. Así, almacenaremos aquí nuestros propios diseños de las huellas de cada uno de los componentes que vamos a usar.

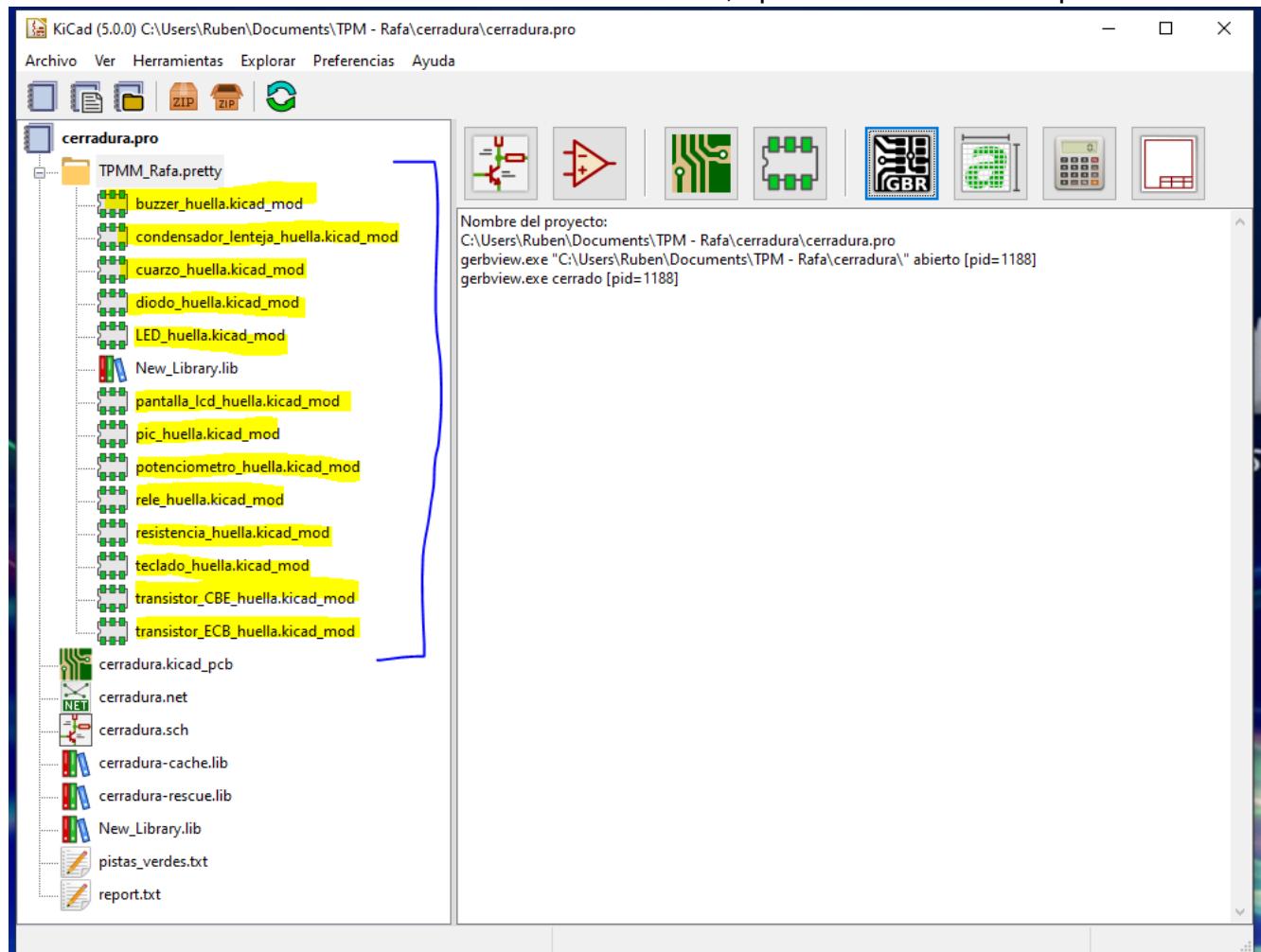
Aquí un ejemplo del símbolo en el esquema, y de la huella creadas para la pantalla:



Y aquí un ejemplo del símbolo en el esquema, y de la huella creadas para el LED:



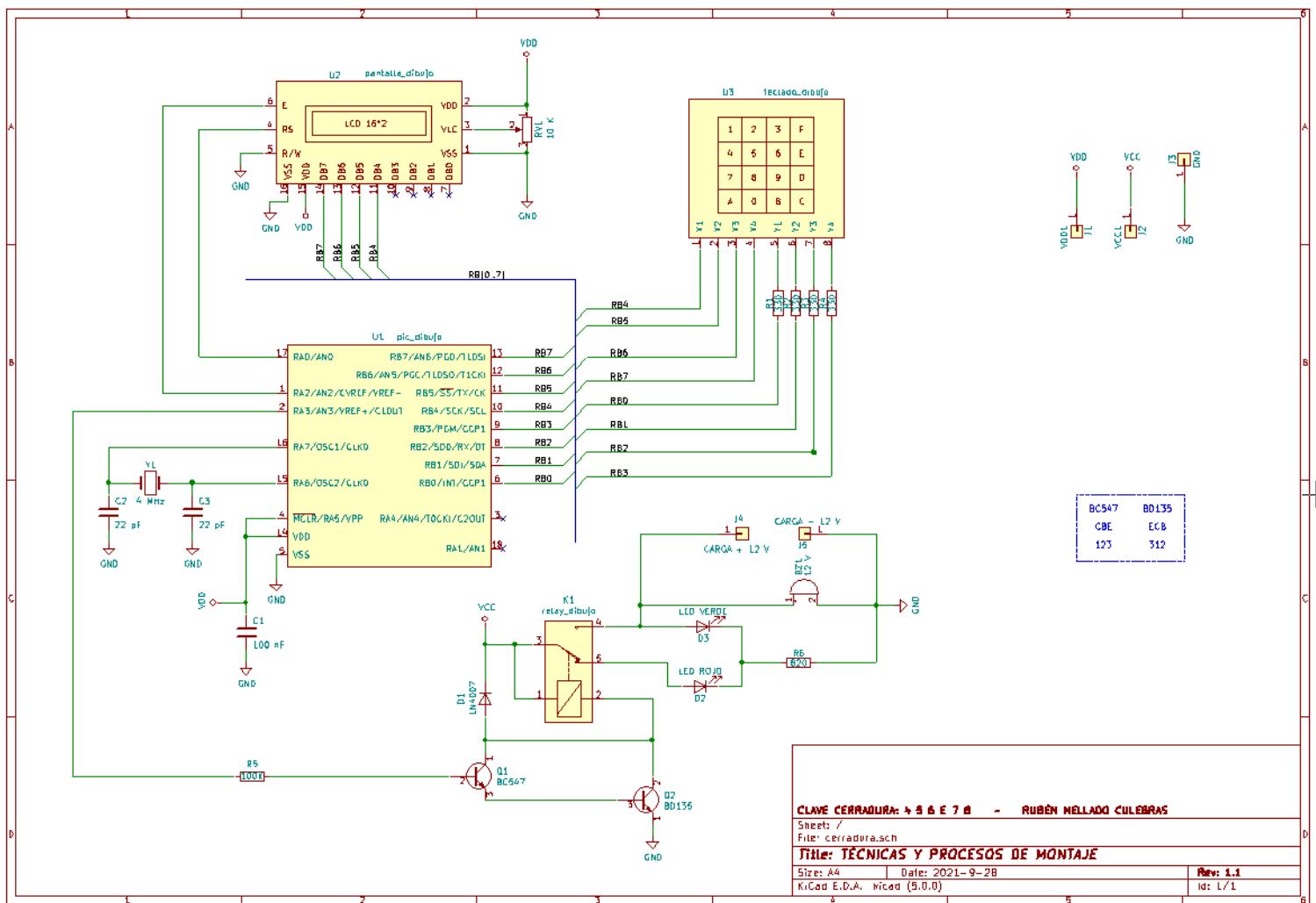
Tras haber creado todas las huellas necesarias, aparecerá una lista tal que así:



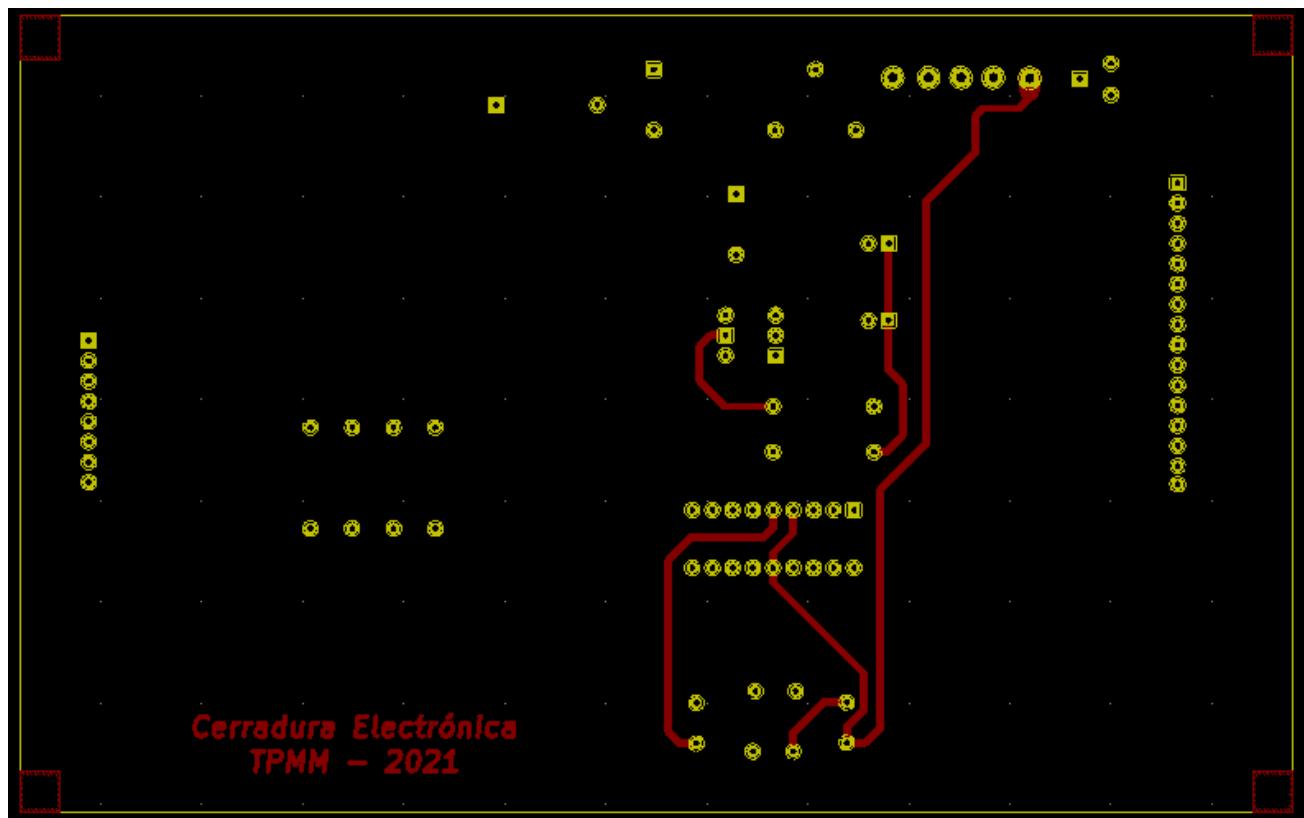
### 3.2 - Diseño del PCB y ruteado por ordenador.

Aquí vamos a ver los distintos planos que podemos encontrar al realizar el diseño del PCB para materializarlo físicamente al traerlo para luego llevarlo al mundo real.

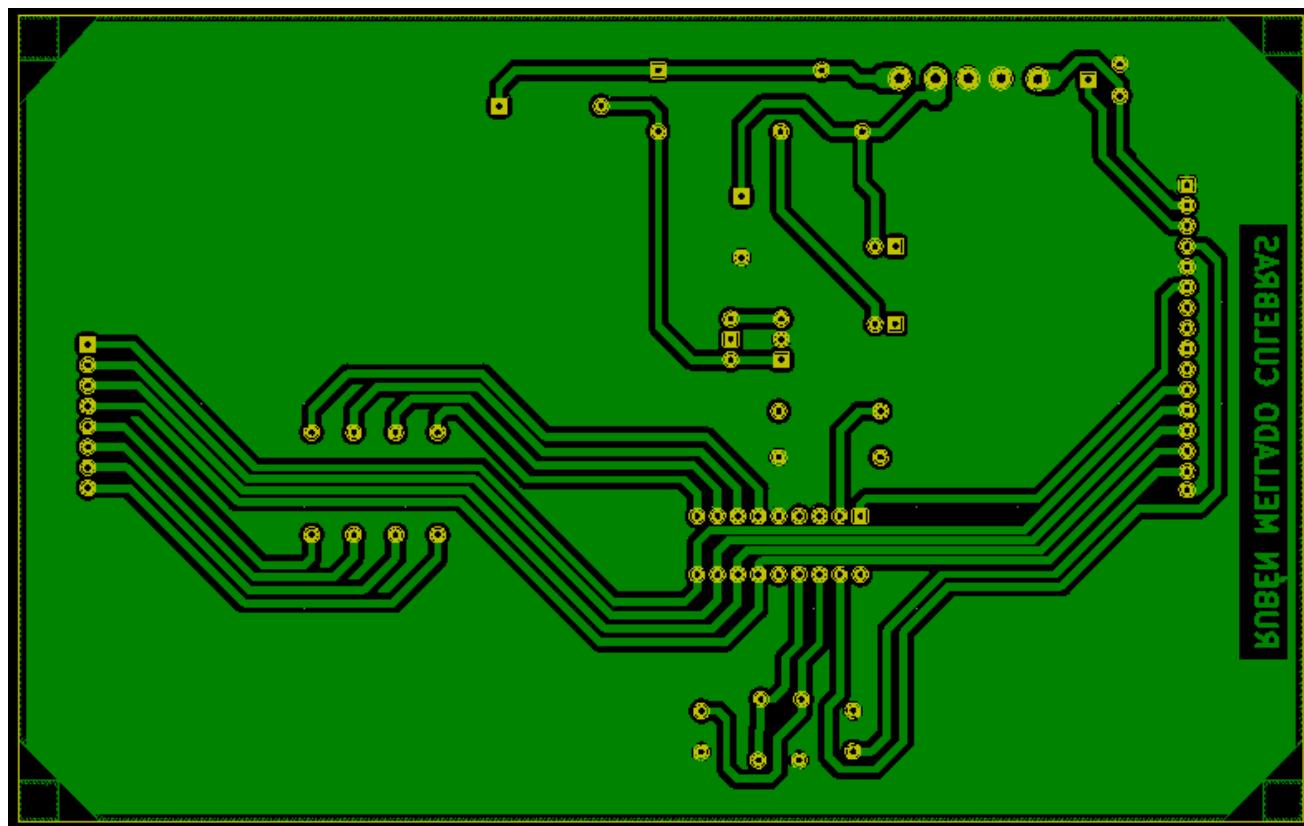
#### 3.2.1 - Plano general eléctrico.



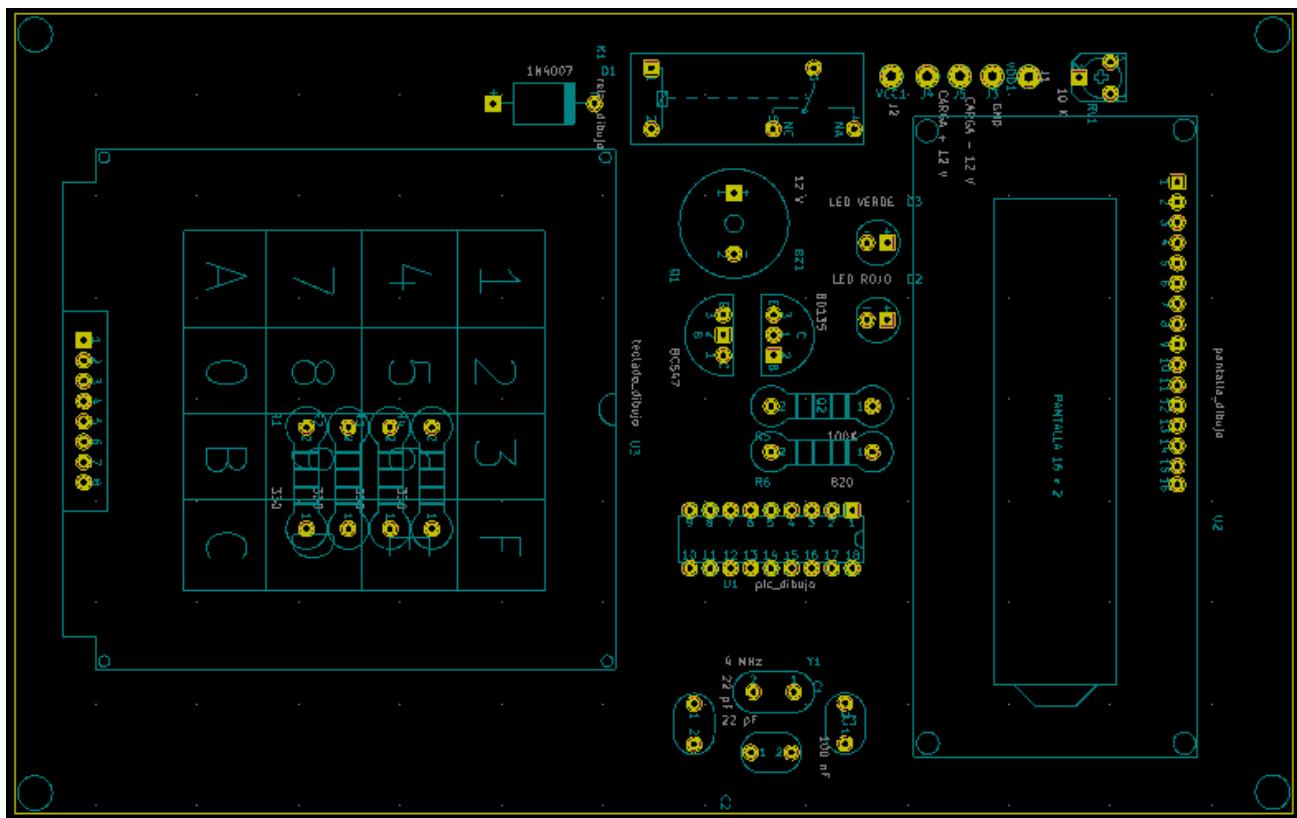
### 3.2.2 - Plano Top.



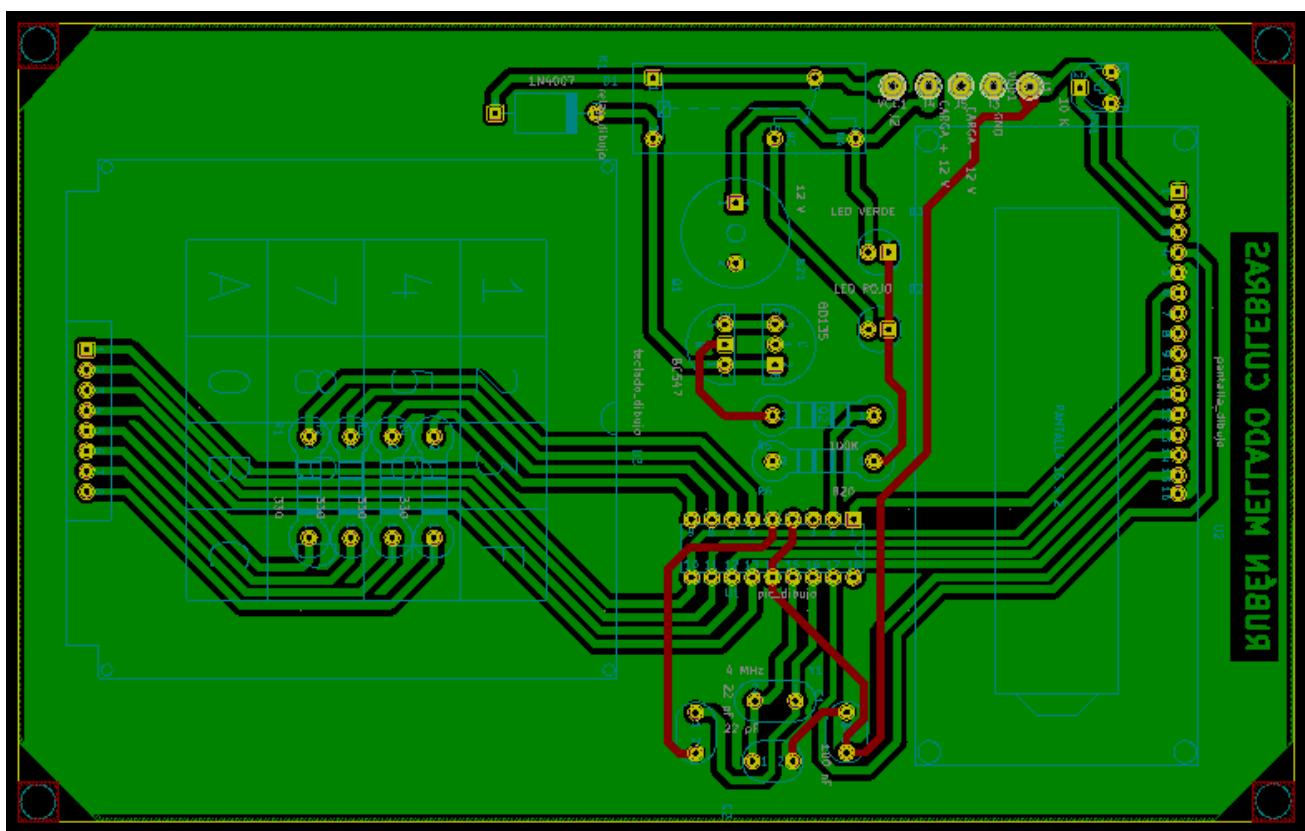
### 3.2.3 - Plano Bottom.



### 3.2.4 - Plano Componentes.

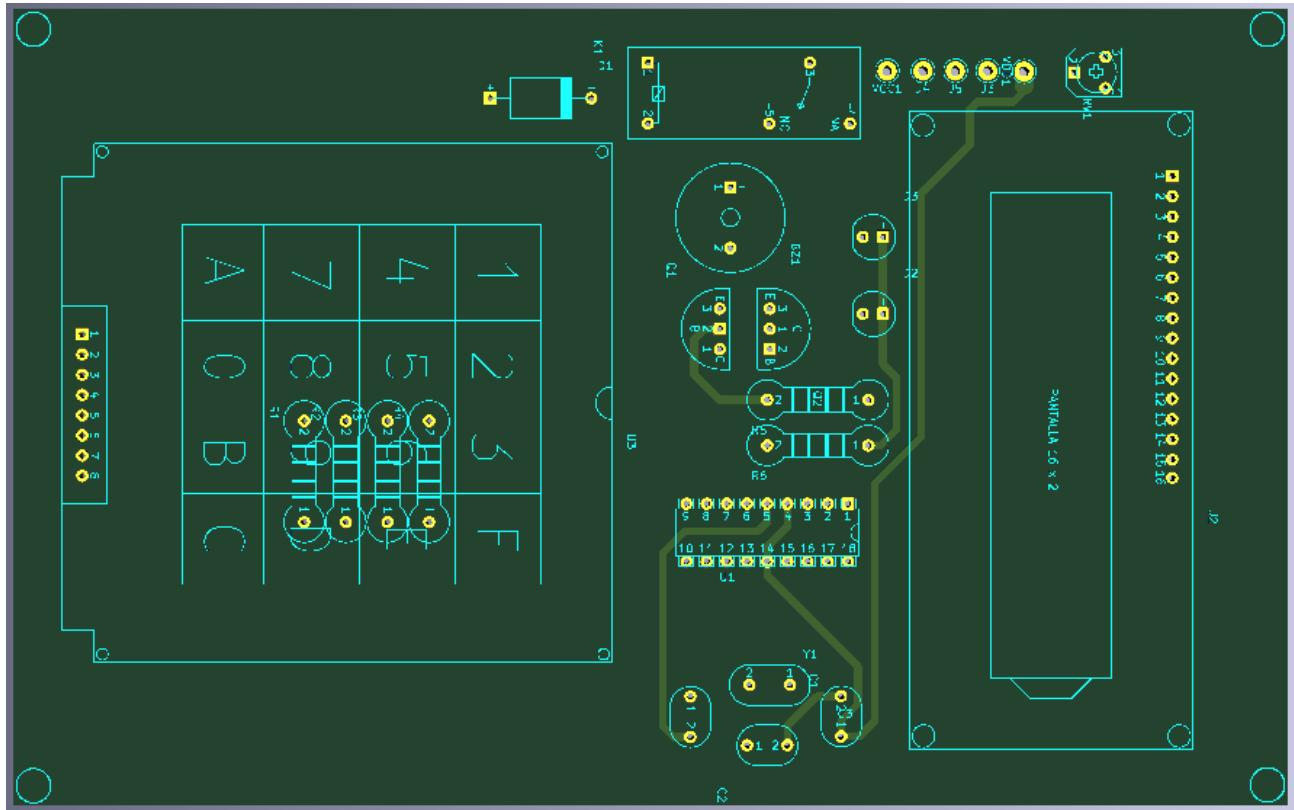


### 3.2.5 - Plano Top + Bottom + Componentes.

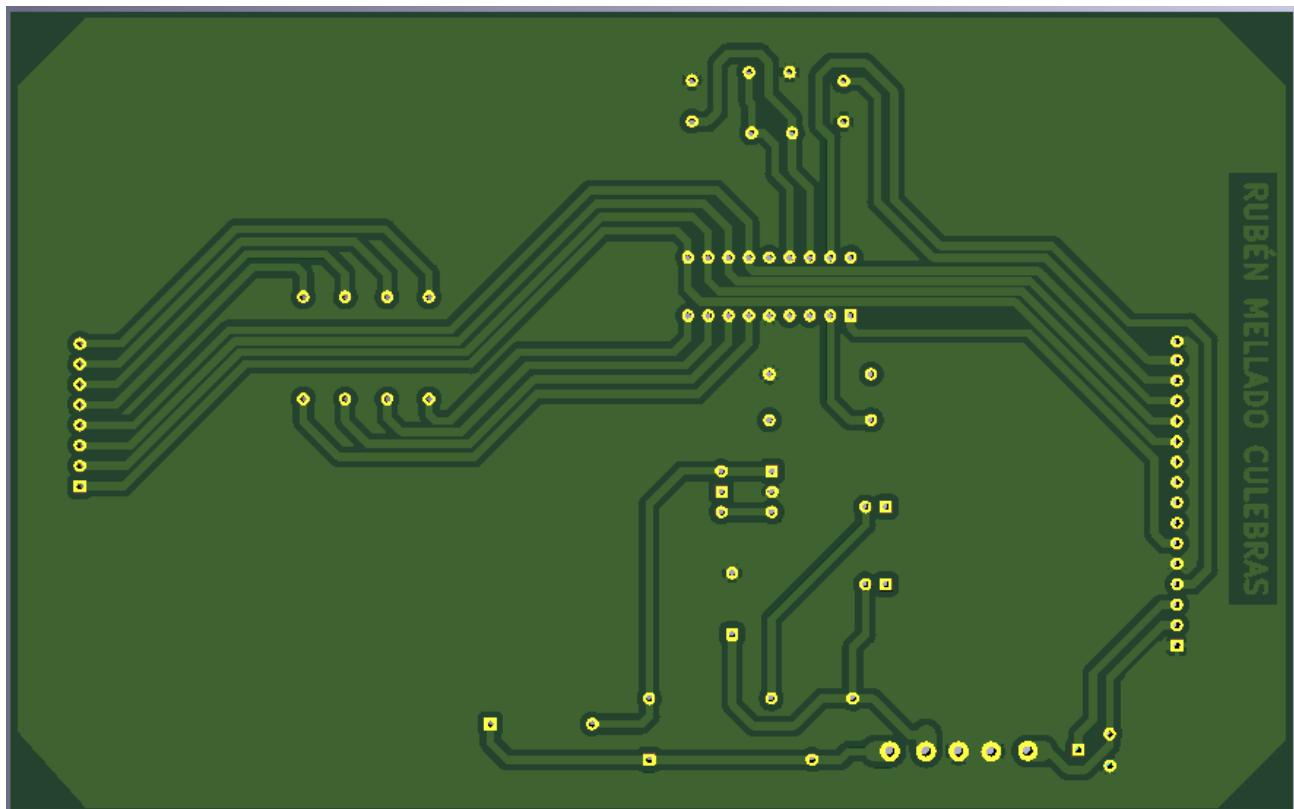


### 3.2.6 - Plano renderizado 3D.

Plano Top renderizado.



Plano Bottom renderizado.



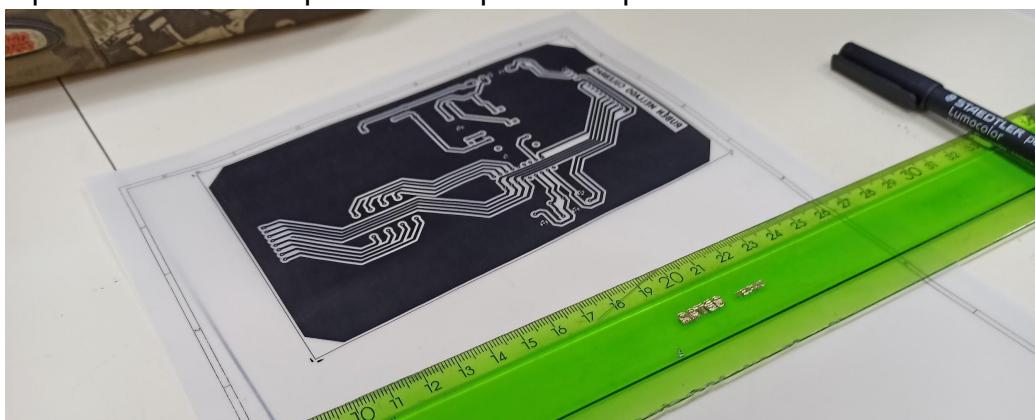
## 4 - Pasar el diseño a la placa PCB real.

En este paso, vamos a sacar de lo digital a la realidad, nuestro circuito diseñado para usarlo con componentes reales, con tal de que lo podamos manejar y tocar.

### 4.1 - Imprimir el circuito.

Primero tenemos que imprimir el circuito del ruteado (las 2 caras), en un papel especial transparente.

Tras esto, habrá que recortarlo dejando 1mm de margen en sus lados, para que al formar el “sobre”, se pueda introducir la placa de baquelita sin problema.



Cuando lo tengamos bien recortado, habrá que repasar las líneas que se hayan borrado un poco, con el rotulador permanente (si fuese necesario). Tras esto, ya podremos crear el sobre. Dejando en la parte interior, las caras del papel que tienen la tinta de la impresora.

Tras poner la placa de baquelita en el sobre, este lo pondremos en la insoladora. El tiempo necesario (2-4 minutos) para que se transfiera las pistas a la placa, las cuales veremos al revelarlo con los productos químicos.

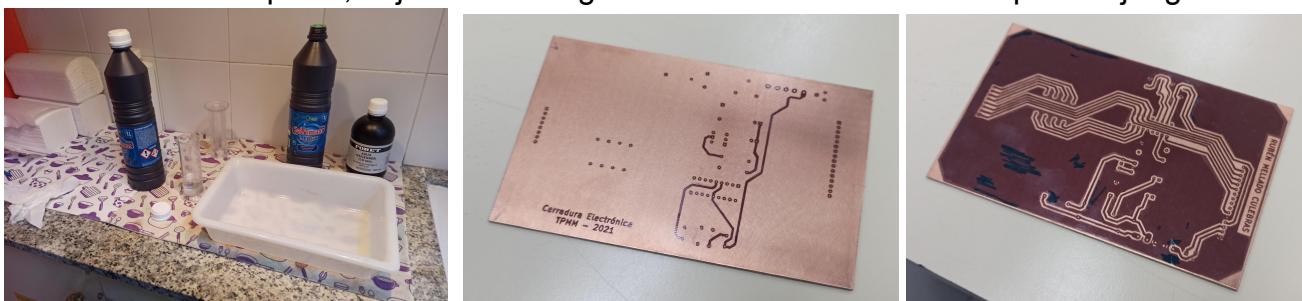


## 4.2 - Revelado del diseño de placa PCB con productos químicos.

Primero hay que diluir en agua la sosa cáustica. Con una proporción de 3/4 de agua ( $H_2O$ ), y 1/4 de sosa ( $NaOH$ ). Esta la agitamos hasta su completa disolución, ya que sino, dejará marcas o rayaduras en la placa de baquelita, en el cobre. Para este paso, prepararemos 2 probetas iguales de sosa, por si acaso una no fuese suficientemente fuerte. **Si hay poca sosa, el ácido no comerá.**



En la bandeja, poner 1 dedo de altura en agua. Vaciar ahí la disolución anterior, en la bandeja, y colocar también la placa PCB para su revelado, habrá que mover durante unos segundos. Retirar inmediatamente la placa para enjuagar bajo el grifo. Si vemos que no se ven cambios en la placa, dejarla unos segundos más. Y volver a retirar para enjuagar.



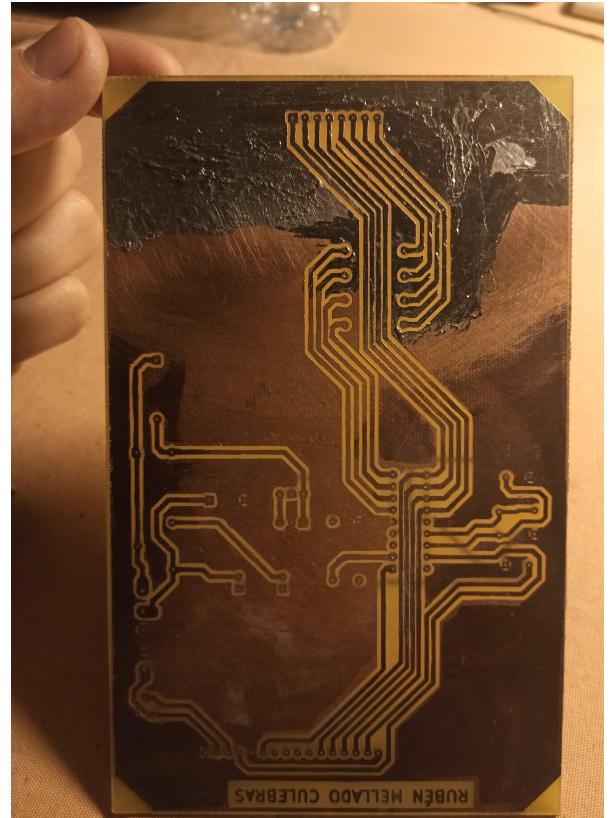
Cuando esté como arriba, se lava bien ,y se reserva. Ahora habrá que hacer la mezcla del ácido con agua (40cc  $H_2O$ ), agua oxigenada (40cc  $H_2O_2$ ), y saltumán (40cc  $HCl$ ), y colocarlo en otra bandeja. También colocar el PCB. En este proceso se “comerá” el cobre que no se haya tapado (al imprimir en la hoja). Por lo que se verá con mucha mayor claridad el circuito impreso final. Al estar con productos químicos, hay que protegerse bien. Tras esto, al ir moviendo la bandeja, cuando consideremos que se vean ya las pistas correctamente, retiramos y enjuagamos bien con agua la placa para que el proceso no siga “comiéndose” el cobre.



#### 4.3 - Eliminar la capa protectora del cobre.

En este paso, se va a rascar con un estropajo de metal, e ir limpiando a cada poco la placa con alcohol y algodón.

A medida que vayamos limpiando y rascando la placa, le tendremos que ir aplicando estaño para proteger la capa de cobre al descubierto.



## 5 - Montaje en la placa PCB.

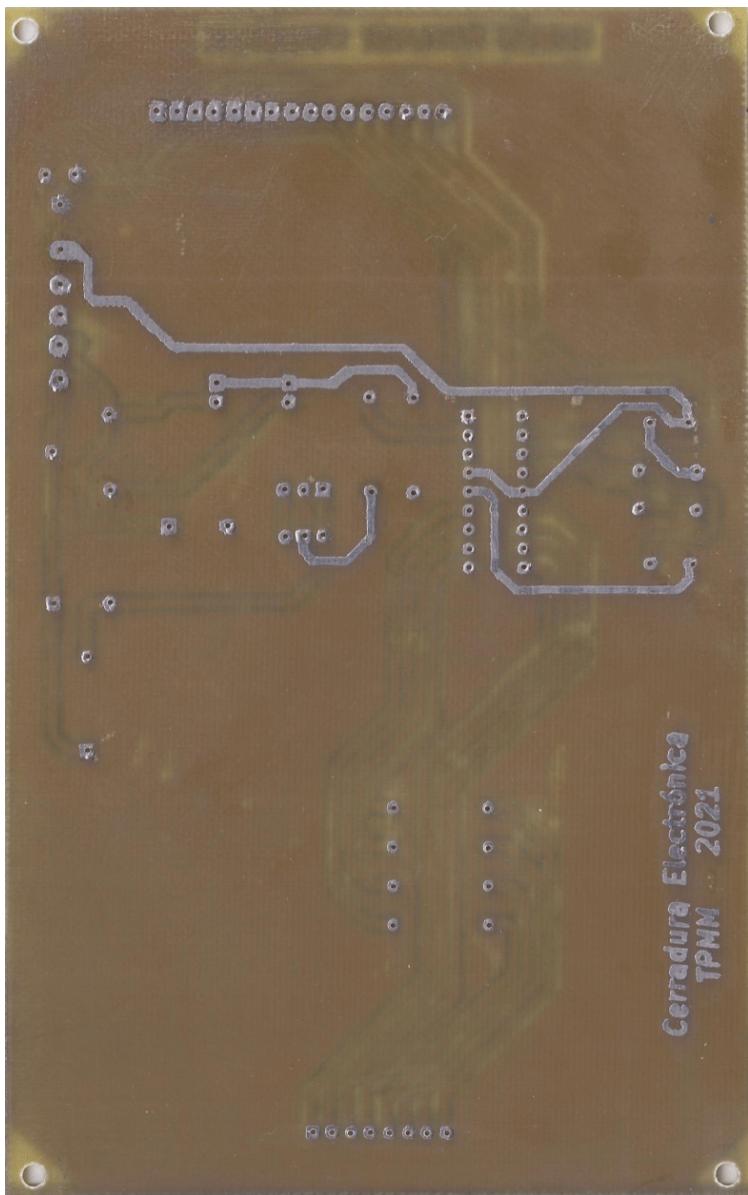
Para esto, vamos a requerir de tener los componentes mencionados anteriormente, taladro y brocas (0'8mm a 3'5mm), soldador, estaño, y pasta de soldadura o flux.

### 5.1 - Estañado.

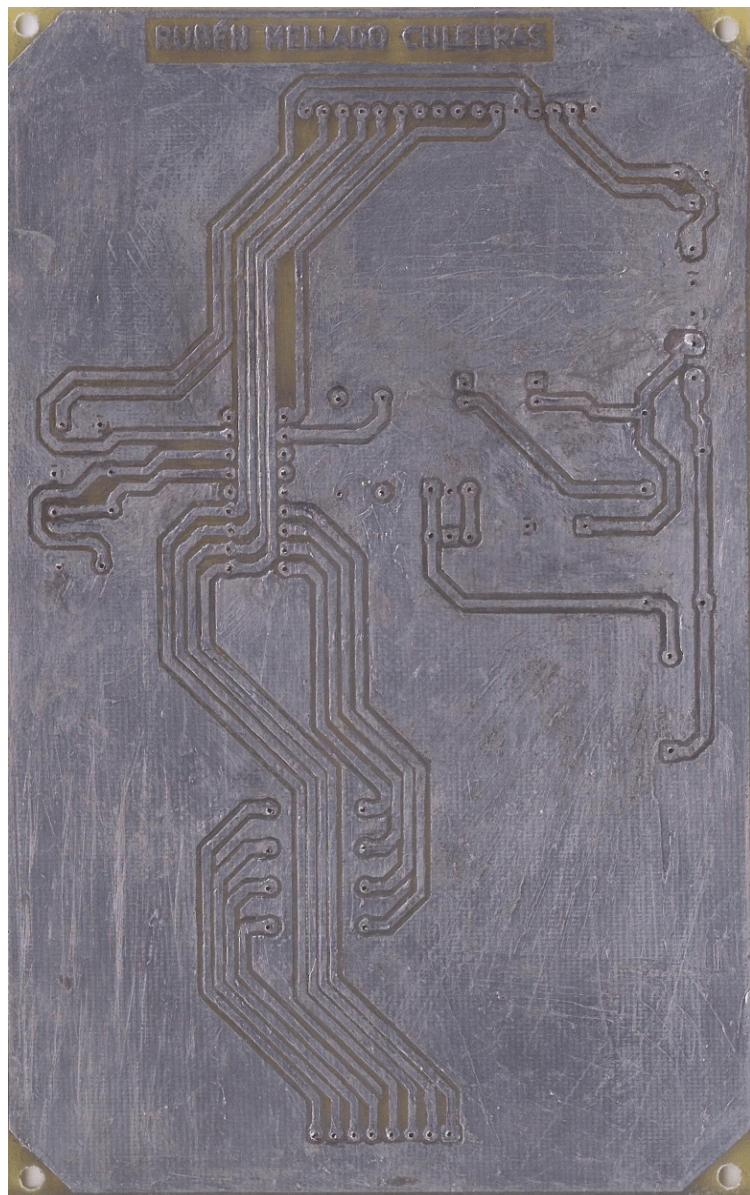
En este paso, vamos a requerir de usar el cautín, estaño, y bastante pasta de soldar o flux. Tras pasar con cuidado y repartiendo homogéneamente el estaño, veremos que no se va a necesitar especialmente mucha cantidad de estaño.

Así es como quedan las 2 caras de la placa PCB de baquelita tras estañarlas.

Parte delantera:

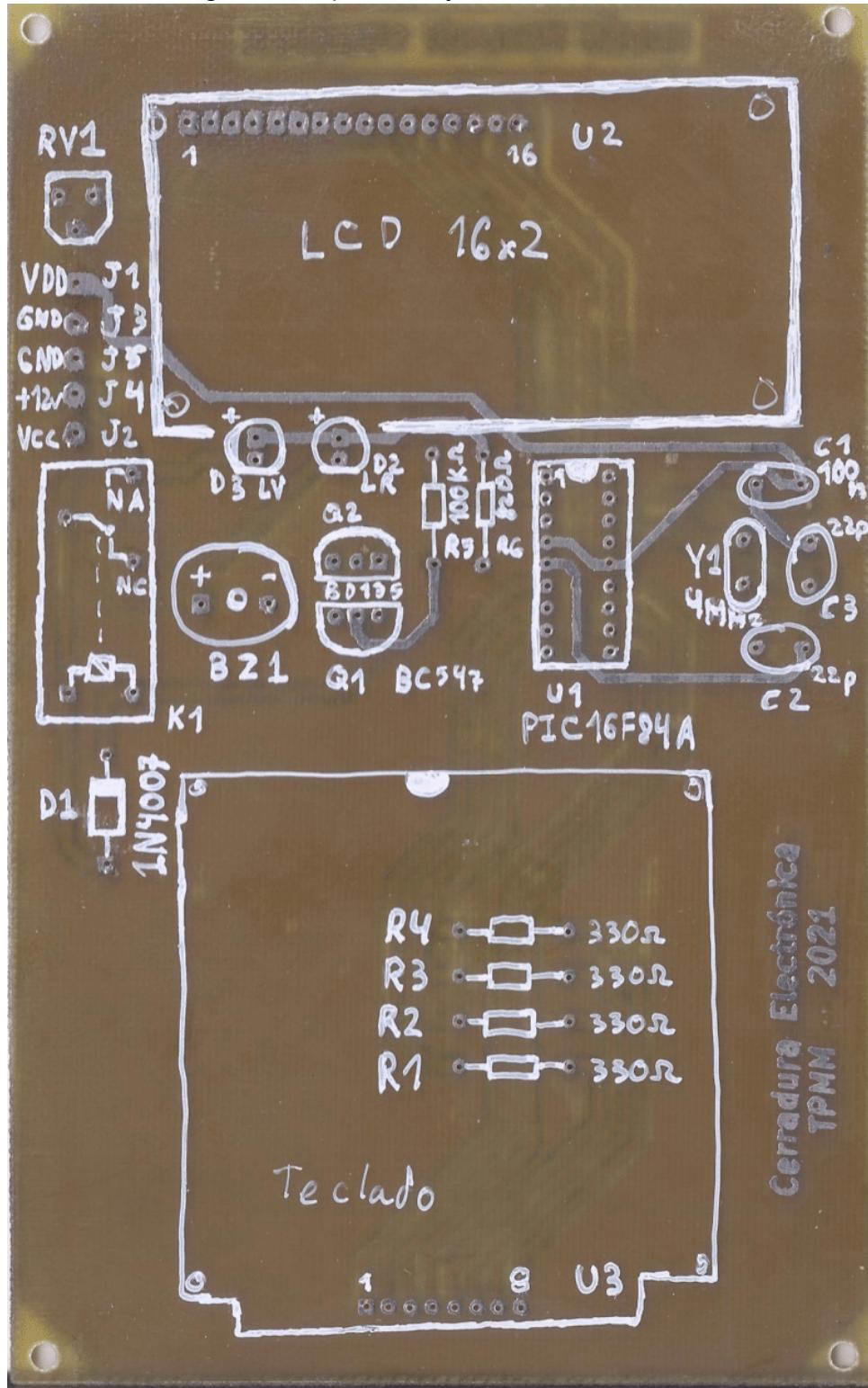


Parte trasera:



## 5.2 - Serigrafía placa PCB.

Para facilitar el montaje y mantenimiento, a futuro, ante posible reemplazo de componentes, vamos a serigrafiar la posición y número de cada uno.

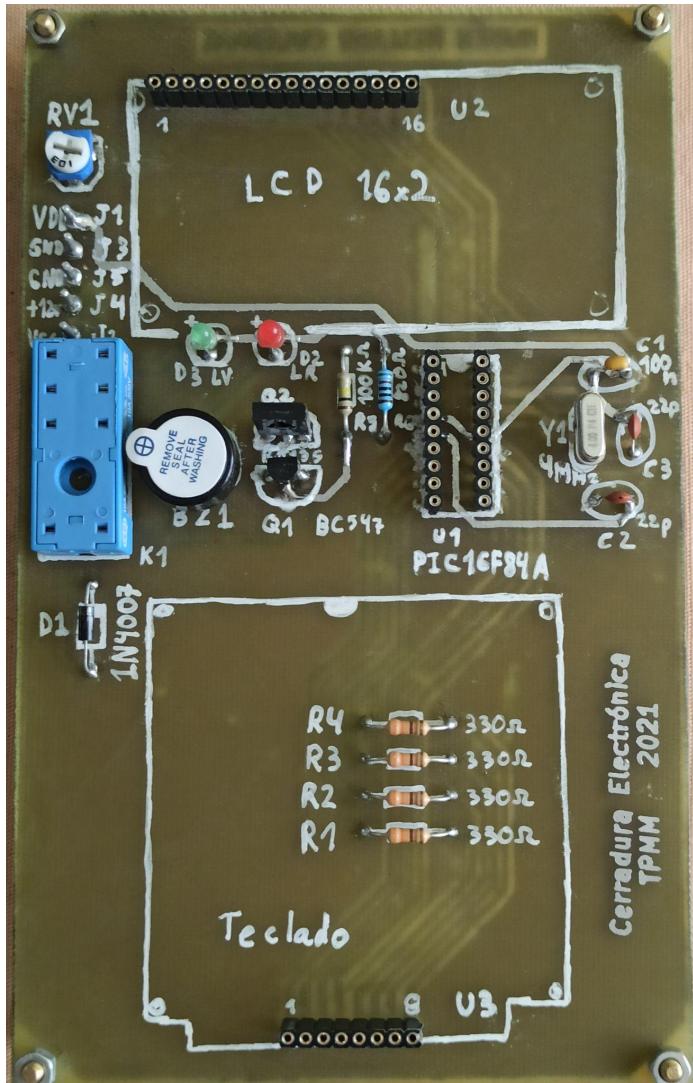


Tras esto, utilizaremos un taladro y un juego de brocas para ir progresivamente taladrando hasta llegar al tamaño adecuado de broca en cada sección de pines a perforar.

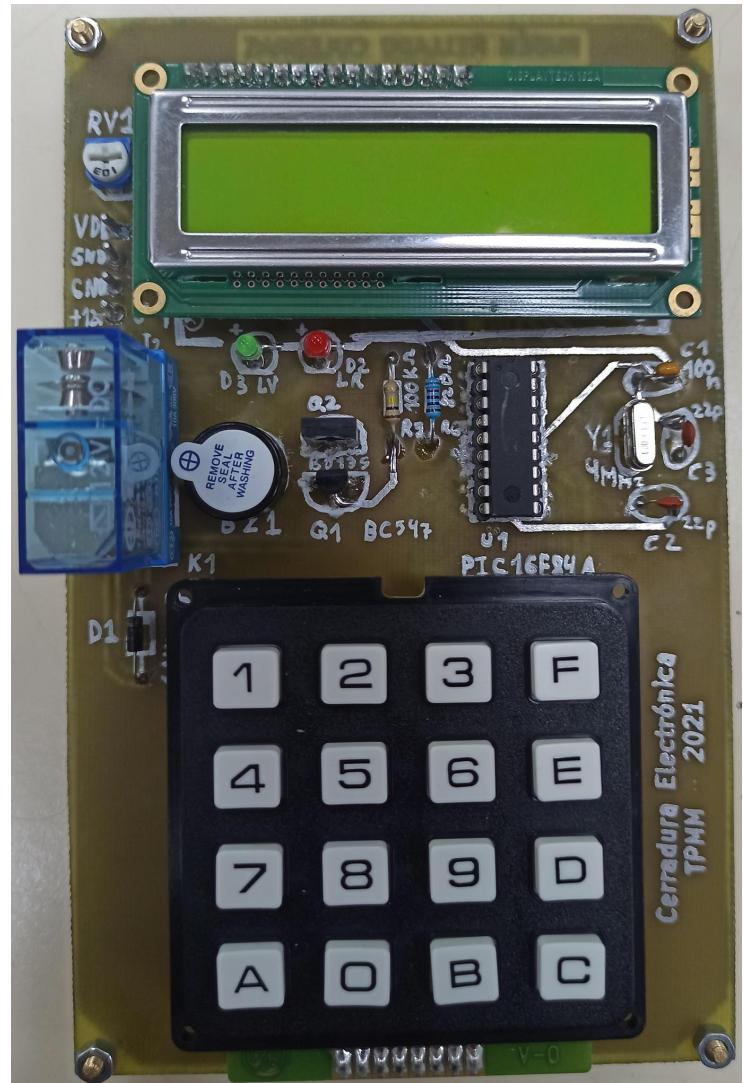
### 5.3 - Soldar componentes.

Toca colocar y soldar los componentes pequeños que en caso de dejarlos para el final, nos dificultan el montaje. Despues, seguiremos con los de mayor tamaño, y así hasta terminar.

Tras soldar los primeros componentes (resistencias, diodos, transistores, etc).



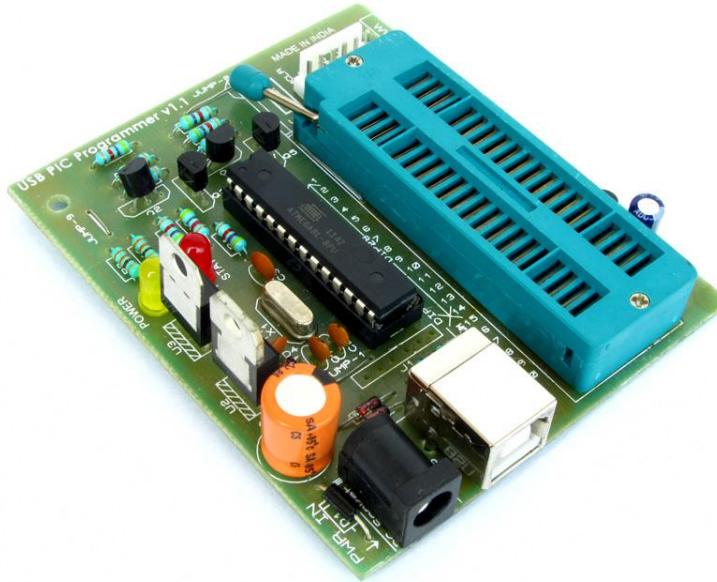
Tras acabar el soldado, y montaje de todos los componentes.



Con esto ya tenemos montada por completo la placa PCB. Actualmente no va a hacer nada, ya que el cerebro está vacío. En el siguiente apartado, vamos a ver el código que se va a utilizar para programarlo y así que funcione la cerradura correctamente al teclear la secuencia preestablecida de teclas.

## 6 - Programar el PIC.

En este caso, lo va a programar el profesor, con un programador para circuitos integrados del tipo PIC, mediante conexión USB.



### 6.1 - Código del programa.

El código que nos han facilitado es el siguiente:

```
.***** Teclado_09.asm *****
;
;
;
!
=====
;! Del libro "MICROCONTROLADOR PIC16F84. DESARROLLO DE PROYECTOS"
;! E. Palacios, F. Remiro y L. LÚpez.
;! Editorial Ra-Ma. www.ra-ma.es
;
;
!
=====
;
; Cerradura ElectrÚnica: la salida se activa cuando una clave de varios dígitos introducida
; por teclado sea correcta. El esquema se describe en la figura 19-7.
;
;
; Tiene una salida "CerraduraSalida" que, cuando se habilita, activa durante unos
; segundos
; el electroim·n de la cerradura permitiendo la apertura de la puerta:
; - Si (CerraduraSalida) = 1, la puerta se puede abrir.
; - Si (CerraduraSalida) = 0, la puerta no se puede abrir.
;
;Funcionamiento:
```

```
; - En pantalla visualiza "Introduzca CLAVE". Segun se va escribiendo, visualiza asteriscos  
**.  
; - Cuando termine de escribir la clave pueden darse dos posibilidades:  
; -Si la clave es incorrecta la cerradura sigue inactivada, en pantalla aparece el  
mensaje  
;! "Clave INCORRECTA" durante unos segundos y tiene que repetir de nuevo el  
proceso.  
; -Si la clave es correcta la cerradura se activa durante unos segundos y la puerta  
! puede ser abierta. En pantalla aparece: "Clave CORRECTA" (primera linea) y "Abra  
;! la puerta" (segunda linea). Pasados unos segundos, se repite el proceso.  
;  
; ZONA DE DATOS *****  
! __CONFIG_C_P_OFF & _WDT_OFF & _PWRTE_ON & _XT_OSC  
! LIST! P=16F84A  
! INCLUDE <P16F84A.INC>  
! CBLOCK 0x0C  
! ENDC  
; La clave puede tener cualquier tamaño y su longitud se calcula:  
#DEFINE LongitudClave! (FinClaveSecreta-ClaveSecreta)  
#DEFINE CerraduraSalida! PORTA,3  
Proyecto Cerradura Electrónica 1º GS - Mantenimiento Electrónico 2012-13 Jorge Celestino! 18  
; ZONA DE C"DIGOS *****  
! ORG!0  
! goto !Inicio  
! ORG!4  
! goto!ServicioInterrupcion  
Mensajes  
! addwf! PCL,F  
MensajeTeclee  
! DT! "Teclee CLAVE:", 0x00  
MensajeClaveCorrecta  
! DT! "Clave CORRECTA", 0x00  
MensajeAbraPuerta  
! DT! "Abra la puerta", 0x00  
MensajeClaveIncorrecta  
! DT! "Clave INCORRECTA", 0x00  
;  
LeeClaveSecreta  
! addwf! PCL,F  
ClaveSecreta  
! DT! 4h,5h,6h,0Eh! ! ; Ejemplo de clave secreta.  
! DT! 7h,8h  
FinClaveSecreta  
Inicio!call! LCD_Inicializa  
! bsf! STATUS,RP0  
! bcf! CerraduraSalida! ! ; Define como salida.  
! bcf! STATUS,RP0  
! call! Teclado_Inicializa! ! ; Configura las líneas del teclado.  
! call! InicializaTodo! ! ; Inicializa el resto de los registros.  
! movlw! b'10001000' ! ! ; Habilita la interrupción RBI y la general.  
! movwf! INTCON  
Principal  
! sleep! ! ! ! ; Espera en modo bajo consumo que pulse alguna tecla.  
! goto! Principal
```

```
; Subrutina "ServicioInterrupcion" -----
;
! CBLOCK
! ContadorCaracteres
! GuardaClaveTecleada
! ENDC
ServicioInterrupcion
! call! Teclado_LeeHex! ! ; Obtiene el valor hexadecimal de la tecla pulsada.
;
; Seg n va introduciendo los d gitos de la clave, estos van siendo almacenados a partir de
; las posiciones RAM "ClaveTecleada" mediante direccionamiento indirecto y utilizando el
; FSR como apuntador. Por cada d gito le do en pantalla se visualiza un asterisco.
Proyecto Cerradura Electr nica 1  GS - Mantenimiento Electr nico 2012-13 Jorge Celestino! 19
;
! movwf! INDF! ! ; Almacena ese d gito en memoria RAM con
!!!! ! ; con direccionamiento indirecto apuntado por FSR.
! movlw! "*! ! ! ; Visualiza asterisco.
! call! LCD_Caracter
! incf! FSR,F! ! ! ; Apunta a la pr xima posici n de RAM.
! incf! ContadorCaracteres,F! ; Cuenta el n mero de teclas pulsadas.
! movlw! LongitudClave! ! ; Comprueba si ha introducido tantos caracteres
! subwf! ContadorCaracteres,W! ; como longitud tiene la clave secreta.
! btfss!STATUS,C! ! ; o Ha terminado de introducir caracteres?
! goto!FinInterrupcion!! ; No, pues lee el siguiente car cter tecleado.
;
; Si ha llegado aqu  es porque ha terminado de introducir el m ximo de d gitos. Ahora
; procede a comprobar si la clave es correcta. Para ello va comparando cada uno de los
; d gitos almacenados en las posiciones RAM a partir de "ClaveTecleada" con el valor
; correcto de la clave almacenado en la posici n ROM "ClaveSecreta".
;
; Para acceder a las posiciones de memoria RAM a partir de "ClaveTecleada" utiliza
; direccionamiento indirecto siendo FSR el apuntador.
;
; Para acceder a memoria ROM "ClaveSecreta" se utiliza direccionamiento indexado con
el
; el registro ContadorCaracteres como apuntador.
;
! call! LCD_Borra! ! ; Borra la pantalla.
! clrf! ContadorCaracteres! ! ; Va a leer el primer car cter almacenado en ROM.
! movlw! ClaveTecleada! ! ; Apunta a la primera posici n de RAM donde se ha
! movwf! FSR!! ! ; guardado la clave tecleada.
CompararClaves
! movf!INDF,W! ! ! ; Lee la clave tecleada y guardada en RAM.
! movwf! GuardaClaveTecleada! ; La guarda para compararla despu s.
! movf!ContadorCaracteres,W! ; Apunta al car cter de ROM a leer.
! call! LeeClaveSecreta! ! ; En (W) el car cter de la clave secreta.
! subwf! GuardaClaveTecleada,W! ; Se comparan.
! btfss!STATUS,Z! ; o Son iguales?, o Z=1?
! goto!ClaveIncorrecta! ; No, pues la clave tecleada es incorrecta.
! incf! FSR,F! ! ! ; Apunta a la pr xima posici n de RAM.
! incf! ContadorCaracteres,F! ; Apunta a la pr xima posici n de ROM.
! movlw! LongitudClave! ! ; Comprueba si ha comparado tantos caracteres
! subwf! ContadorCaracteres,W! ; como longitud tiene la clave secreta.
! btfss!STATUS,C! ! ; o Ha terminado de comparar caracteres?
```

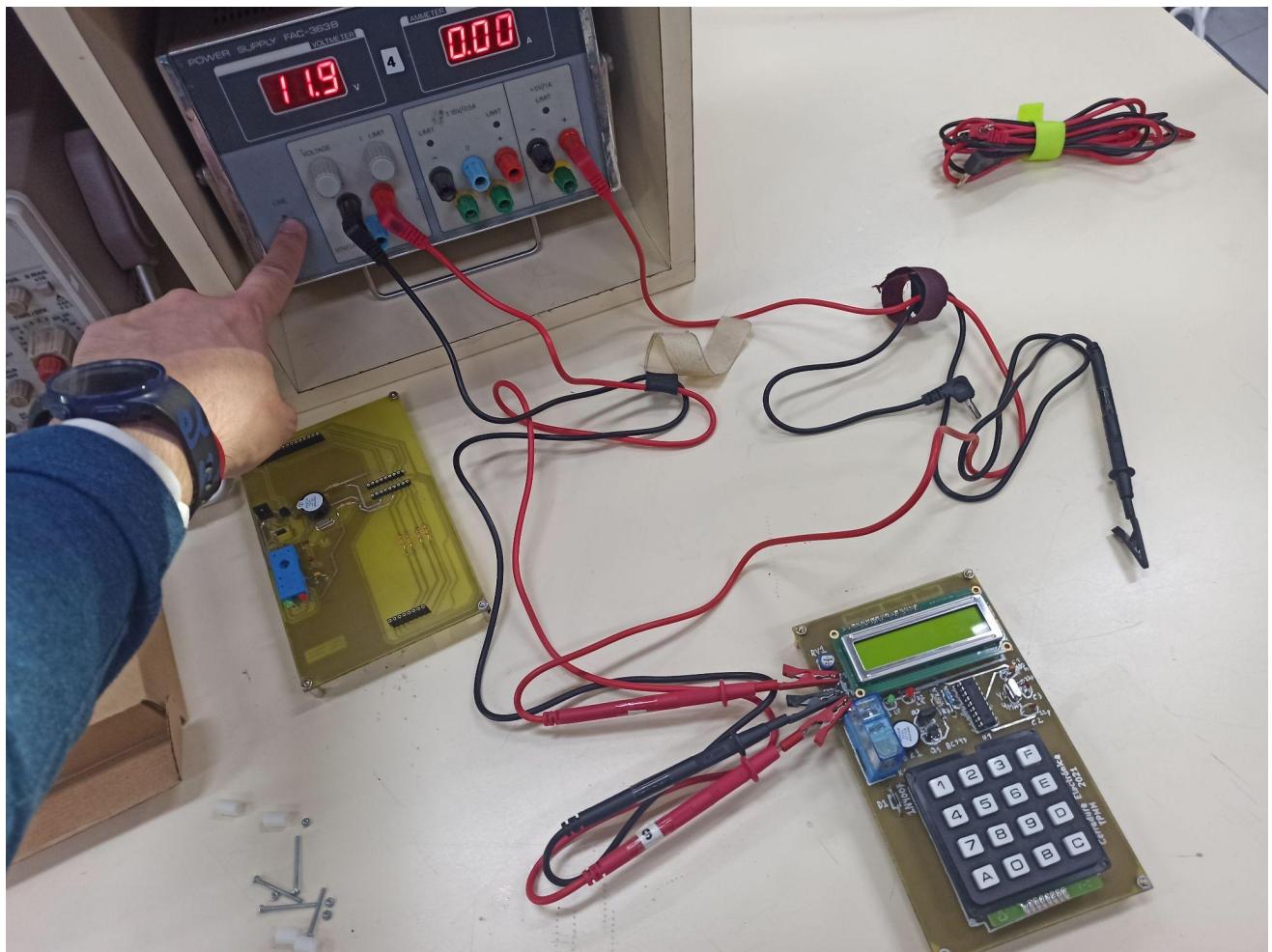
```
! goto!ComparaClaves! ! ; No, pues compara el siguiente carácter.  
ClaveCorrecta! ! ! ; La clave ha sido correcta. Aparecen los mensajes  
! movlw MensajeClaveCorrecta! ; correspondientes y permite la apertura de la  
! call! LCD_Mensaje! ! ; puerta durante unos segundos.  
! call! LCD_Linea2  
! movlw MensajeAbraPuerta  
! call! LCD_Mensaje  
! bsf! CerraduraSalida! ! ; Activa la cerradura durante unos segundos.  
! goto!Retardo  
ClaveIncorrecta  
Proyecto Cerradura Electrónica 1º GS - Mantenimiento Electrónico 2012-13 Jorge Celestino! 20  
! movlw MensajeClaveIncorrecta  
! call! LCD_Mensaje  
Retardo  
! call! Retardo_2s  
! call! Retardo_1s  
InicializaTodo  
! bcf! CerraduraSalida! ! ; Desactiva la cerradura.  
! clrf! ContadorCaracteres! ! ; Inicializa este contador.  
! movlw ClaveTecleada! ! ; FSR apunta a la primera dirección de la RAM  
! movwf! FSR!! ! ; donde se va a almacenar la clave tecleada.  
! call! LCD_Borra! ! ; Borra la pantalla.  
! movlw MensajeTeclee! ! ; Aparece el mensaje para que introduzca la clave.  
! call! LCD_Mensaje  
! call! LCD_Linea2! ! ; Los asteriscos se visualizan en la segunda línea.  
FinInterrupcion  
! call! Teclado_EspereDejePulsar  
! bcf! INTCON, RBIF  
! retfie!  
! INCLUDE <TECLADO.INC>  
! INCLUDE <LCD_4BIT.INC>  
! INCLUDE <LCD_MENS.INC>  
! INCLUDE <RETARDOS.INC>  
; Las posiciones de memoria RAM donde se guardarán la clave leída se definen al final,  
después  
; de los Includes, ya que van a ocupar varias posiciones de memoria mediante el  
; direccionamiento indirecto utilizado.  
! CBLOCK  
! ClaveTecleada  
! ENDC  
! END!!! ; Fin del programa.  
!  
;  
!  
=====  
;! Del libro "MICROCONTROLADOR PIC16F84. DESARROLLO DE PROYECTOS"  
;! E. Palacios, F. Remiro y L. López.  
;! Editorial Ra-Ma. www.ra-ma.es  
;  
!  
=====
```

## 6.2 - Código ensamblador a decimal.

En este paso, vamos a ver el código hexadecimal resultante del código proporcionado en el apartado anterior. Recuerda que hará falta tener las librerías usadas en la misma carpeta.

```
:020000040000FA  
:02000004A288C  
:080008005428820754346534CA  
:1000100063346C3465346534203443344C344134B7  
:10002000563445343A34003443346C3461347634D5  
:100030006534203443344F345234523445344334DD  
:1000400054344134003441346234723461342034E5  
:100050006C346134203470347534653472347434E3  
:100060006134003443346C34613476346534203484  
:1000700049344E3443344F3452345234453443348B  
:1000800054344134003482070434053406340E34C9  
:100090007340834C4208316851183129C207A20EB  
:1000A00088308B0063005228852080002A30082188  
:1000B000840A8C0A06300C02031C822803218C015E  
:1000C0001A30840000088D000C0843200D02031D27  
:1000D0007628840A8C0A06300C02031C622814302D  
:1000E0004821F720233048218515782832304821CF  
:1000F000A521A72185118C011A3084000321063027  
:100100004821F720A1200B100900A920031C8A28F0  
:100110008B200314080082070134023403340F34A7  
:100120000434053406340E340734083409340D34ED  
:100130000A3400340B340C348316F03086008113FB  
:100140008312F03086008D210608F03C031DA328A1  
:1001500008008E01FE308600061EC1288E0A861E0B  
:10016000C1288E0A061FC1288E0A861FC1288E0A42  
:100170000F300E020318BF280314060DAB2803101E  
:10018000C3280E08031408008316051005118510F6  
:1001900083128510051105108D213030DC2091214E  
:1001A0003030DC207A213030DC202030DC2005218A  
:1001B00003210121F3200800F0398F0006080F39D0  
:1001C0008F048316060891000F30860583120F08EE  
:1001D000860005150511051C93217F218316110842  
:1001E0008600831208000630062980300629C030B8  
:1001F000062980380629C0380629083006290E301D  
:1002000006290C30062901300629283005100A2954  
:1002100005140F219000DC20100EDC2008008F0058  
:10022000F13C031D1629EE308F0023290F08D13C25  
:10023000031D1D29EE308F0023290F08BA3C031D32  
:100240002329DF308F000F08080010302C290130DF  
:100250002C2902302C290330920020300821920BE7  
:100260002D2908009300F039031D3A292030082178  
:100270003C299300130E3D2113080F399200093CCD  
:10028000031C45291208303E47291208373E082929  
:1002900094000530940294031408052095009508F5  
:1002A000031955290821940A4C29080094000530A7  
:1002B000940294039601032110301602031D652950  
:1002C000872187210F3094025A29140805209500B0  
:1002D000950803196F290821960A940A5C290800D9  
:1002E000000000000000000000000000000000000006  
:1002F000A43083290000403083291F308329000067  
:100300000E30832905309700970B84290800C830E8  
:1003100096296430962932309629143096290A306D  
:100320009629053096290230962901309800F93037  
:1003300097000000970B9929980B97290800C8305F  
:10034000AA296430AA293230AA291430AA290A30ED  
:10035000AA290530990064309800F9309700000010  
:0E036000970BAF29980BAD29990BAB2908001C  
:02400E00F13F80  
:00000001FF
```

### 6.3 - Conectar para comprobar funcionamiento.



## 7 - Pliego del proyecto.

---

En este apartado se describe como se ha llevado a cabo el proyecto de manera general y particular, y las normativas que se deben de cumplir.

### 7.1 - Listado completo de componentes.

---

Nombre	Tipo	Valor	Fabricante	Cant.
U2	Pantalla LCD 16 x 2	LCD 16X2	POWERTIP	1
U3	Teclado 4x4	Teclado hexadecimal	MULTICOMP	1
K1	Relé	Relé 5 contactos	FINDER	1
K1	Soporte	Porta Relés	FINDER	1
RV1	Resistencia valor variable	10K	BOURNS	1
R1, R2, R3, R4	Resistencia valor fijo 1/4w	330	MULTICOMP PRO	4
R6	Resistencia valor fijo 1/4w	820	MULTICOMP PRO	1
R5	Resistencia valor fijo 1/4w	100K	MULTICOMP PRO	1
D1	Diodo rectificador	Diodo 1N4007	VISHAY	1
D3	Diodo LED	LED Verde 2V	KINGBRIGHT	1
D2	Diodo LED	LED Rojo 1'8V	MULTICOMP PRO	1
BZ1	Zumbador acústico	Buzzer	MURATA	1
RB0, RB1, RB2, RB3, RB4, RB5, RB6, RB7	Conector	Pines para teclado	AMP - TE CONNECTIVITY	1
RB4, RB5, RB6, RB7	Conector	Pines para pantalla	AMP - TE CONNECTIVITY	1
RB0, RB1, RB2, RB3, RB4, RB5, RB6, RB7	Conector	Pines para el PIC	MULTICOMP PRO	1

J1, J2, J3, J4, J5	Conektor	Espadines entrada tensión	WEIDMULLER	1
U1	PIC programable	PIC16F84A20P	Microchip Technology	1
Y1	Oscilador 2 patas	Cristal 4MHz	MULTICOMP PRO	1
C1	Condensador tantalio	100nF	KYOCERA AVX	1
C2, C3	Condensador cerámico	22pF	MULTICOMP	1
Q1	Transistor NPN	BC547B	MULTICOMP PRO	1
Q2	Transistor NPN	BD135	MULTICOMP PRO	1
PCB	Placa de baquelita	PCB 100x160mm	ELECTROSON	1

## 7.2 - Condiciones en general.

---

En este caso no se ha seguido ningún tipo de normativas para realizar el proyecto en sí. Pero sí que se ha seguido las pautas del sentido común, con tal de contaminar y reciclar lo máximo posible, los componentes que han sobrado.

Pese a ello, para esto, hay que tener en cuenta las normativas vigentes. Se debe de especificar y etiquetar con las normas (UNE, DIN, AENOR...) que se han utilizado para realizar el proyecto.

Es importante también cumplir con el Estatuto de los trabajadores referente a la responsabilidad de los empleados en el caso de contratos de obras o servicios. Decir que se debe cumplir con la Ley General de la Seguridad Social y la de satisfacer la cotización a la Seguridad Social en los contratos a nuestros trabajadores. Algo a tener en cuenta es que también hayan realizado algún curso, y sepan la normativa de la ley de prevención de riesgos laborales

Un mínimo de normativas de seguridad, y de salud, respecto al lugar de oficio y sus reglamentos existentes que hagan referencia a la higiene y seguridad en el trabajo.

## 7.3 - Condiciones de los materiales y equipo de trabajo.

---

La cerradura necesita de una toma de red de 230VAC con un sistema de alimentación ininterrumpida, para evitar que la puerta que controla no abra cuando exista un posible corte de suministro.

El lugar de instalación debe estar preservado de agentes externos, de lo contrario debe ser instalada en una caja estanca para evitar su deterioro.

Para su instalación y para cambiar el código de apertura, requiere de personal técnico cualificado con los conocimientos necesarios en electrónica y en programación en lenguaje ensamblador.

## 7.4 - Condiciones para realizarlo.

---

Para crear los diseños en KiCAD, hice uso de mi portátil para trabajar en casa y en clase. En este, diagrama de conexiones, no me llevó mucho tiempo, ya que era seguir los pasos de la hoja facilitada.

El modelado y diseño de componentes, es lo que más tiempo requiere, puesto que es donde me tocó invertir cierto tiempo para diseñar las huellas sin errores de medidas. Aparte de el ruteado, que aunque parece difícil, es relativamente sencillo de hacer, aunque también vas a tener que invertir varias horas si quieras que quede decente, y salga un buen circuito sin errores.

Para hacer un buen trabajo, en este aspecto, tuve que realizar varias veces un cambio de medidas en las huellas creadas en la librería hecha en el KiCAD. Debido a que o salían muy grandes, o demasiado pequeños algunos componentes.

Una vez terminado el diseño, imprimí una prueba en una hoja de papel estándar, para comprobar que todos los componentes fuesen de la medida de las huellas. Al ver que al fin ya había salido bien, ya es momento de imprimir en la hoja de papel vegetal para insolar.

Tras imprimir, toca recortar la hoja, el lado con la cara top y el lado con la cara bottom, con 1 mm de margen, y asegurar las uniones con cinta adhesiva, para que el sobre resultante no se separe.

Los demás pasos, ya los hemos visto en el apartado 3 y 4 de esta memoria. Que es el cómo hacer el diseño en ordenador, imprimirla, la mezcla de productos químicos, etc. Al revelar en la insoladora, hay que tener en cuenta los tiempos, que aunque parezcan poco, puede hacer que luego cueste más trabajo preparar la placa para soldar.

Al estar esperando a que se acabe la insularización, se puede aprovechar para preparar las mezclas químicas para revelar las pistas, y que se coman el cobre. Siempre usando protección para manos, ojos, y vías respiratorias.

A la hora de taladrar, en los taladros utilizamos broca de 0.8mm. Para los componentes un poco más anchos de sus terminales, usamos la de 1mm, y para los taladros de los tornillos 3mm. Como recomendación antes de usar el taladro, es estañar toda la placa, con el mejor amigo del electrónico, el querido flux. Gracias a esto, no tendremos problemas de oxidación del cobre.

Restaría soldar los demás componentes, empezando de menor a mayor tamaño. Así no se entorpecen entre sí al querer ir a soldar el siguiente, haciendo que sea más fácil y cómodo realizarlo.

## **7.5 - Condiciones para realizarlo.**

---

Entre todos los componentes, y la subida de precios actual en el mercado, debido a cierta escasez en el transporte de mercancías, no resulta fácil realizar el proyecto manteniendo un precio asequible para todos los bolsillos, de manera que el cliente no te trate de usurero o, incluso, estafador.

Pese a ello, he usado páginas de internet que compiten por ser las mejores en cuanto a precio de venta, y calidad de sus productos. Lo cual es bastante relevante, en el caso de que queramos llevar a cabo una producción en grandes cantidades de este proyecto.

Ya que tanto estas empresas compiten por tener los mejores precios, para salir a flote, y nosotros también tendríamos que usar esta estrategia, para poder también tener éxito.

Aún así, para conseguir los precios más bajos, por lo general hay que recurrir al mercado asiático, pero teniendo en cuenta los tiempos de entrega, siendo previsores. Con lo que podríamos ahorrarnos en muchas cosas, hasta la mitad de precio, respecto a recurrir a páginas más conocidas, cercanas y de prestigio, como las usadas para el presupuesto.



## 8 - Presupuesto del proyecto.

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Tenemos que tener en cuenta que los precios varían según disponibilidad, fabricante, proveedor, y necesidad del mercado.

### 8.1 - Presupuesto parcial.

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Material	Valor	Tienda	Enlace	Precio	Cant.	Subtotal
Pantalla LCD 16 x 2	PC1602	Farnell	<a href="https://es.farnell.com/powerti/p/pc1602aru-hwb-g-q/lcd-module-16x2-x-tmp/dp/1671498">https://es.farnell.com/powerti/p/pc1602aru-hwb-g-q/lcd-module-16x2-x-tmp/dp/1671498</a>	5.38€	1	5,38 €
Teclado hexadecimal	MCAK16 04NBWB	Farnell	<a href="https://es.farnell.com/multicomp/mcak1604nbwb/keypad-4x4-array-plastic/dp/1182239">https://es.farnell.com/multicomp/mcak1604nbwb/keypad-4x4-array-plastic/dp/1182239</a>	11.76€	1	11,76 €
Relé	40.31.7.0 12.0000	Farnell	<a href="https://es.farnell.com/finder/40-31-7-012-0000/rel-spdt-12vdc-10a/dp/1169158">https://es.farnell.com/finder/40-31-7-012-0000/rel-spdt-12vdc-10a/dp/1169158</a>	4.23€	1	4,23 €
Soporte para Relé	95.13.2S MA	Farnell	<a href="https://es.farnell.com/finder/95-13-2sma/z-caloclip-pcb-3-5-mm-rel-/dp/1169217?MER=sy-me-pd-mi-acce">https://es.farnell.com/finder/95-13-2sma/z-caloclip-pcb-3-5-mm-rel-/dp/1169217?MER=sy-me-pd-mi-acce</a>	2.45€	1	2,45 €
Resistencia valor variable	10K	Farnell	<a href="https://es.farnell.com/bourns/3306p-1-103/trimmer-10k/dp/108239?st=trimmer%2010k">https://es.farnell.com/bourns/3306p-1-103/trimmer-10k/dp/108239?st=trimmer%2010k</a>	0.387€	1	0,39 €
Resistencia valor fijo para teclado	330	Farnell	<a href="https://es.farnell.com/multicomp/mccfr0w8j0331a20/resistor-carbon-film-330-ohm-125mw/dp/1128099">https://es.farnell.com/multicomp/mccfr0w8j0331a20/resistor-carbon-film-330-ohm-125mw/dp/1128099</a>	0.0524€	4	0,21 €
Resistencia valor fijo para LEDs	820	Farnell	<a href="https://es.farnell.com/multicomp/mccfr0w8j0821a20/resistor-carbon-film-820-ohm-125mw/dp/1128126">https://es.farnell.com/multicomp/mccfr0w8j0821a20/resistor-carbon-film-820-ohm-125mw/dp/1128126</a>	0.0524€	1	0,05 €
Resistencia valor fijo para BC547	100K	Farnell	<a href="https://es.farnell.com/multicomp/mcre000061/resistor-carbon-film-100k-0-125w/dp/1700264">https://es.farnell.com/multicomp/mcre000061/resistor-carbon-film-100k-0-125w/dp/1700264</a>	0.0359€	1	0,04 €

Diodo rectificador	1N4007	Farnell	<a href="https://es.farnell.com/vishay/1n4007gp-e3-54/diode-standard-1a-1000v-do-41/dp/9549129?st=1n4007">https://es.farnell.com/vishay/1n4007gp-e3-54/diode-standard-1a-1000v-do-41/dp/9549129?st=1n4007</a>	0.629€	1	0,63 €
Diodo LED verde	Verde 2V	Farnell	<a href="https://es.farnell.com/kingbright/l-934gd/led-3mm-green-20mcd-568nm/dp/1142502">https://es.farnell.com/kingbright/l-934gd/led-3mm-green-20mcd-568nm/dp/1142502</a>	0.201€	1	0,20 €
Diodo LED rojo	Rojo 1'8V	Farnell	<a href="https://es.farnell.com/multicomp/703-0090/led-3mm-red-100mcd-643nm/dp/2112100">https://es.farnell.com/multicomp/703-0090/led-3mm-red-100mcd-643nm/dp/2112100</a>	0.237€	1	0,24 €
Zumbador acústico	PKM13E PYH4000-A0	Farnell	<a href="https://es.farnell.com/murata/pkm13epyh4000-a0/sounder-4khz-12-6mm/dp/1192513">https://es.farnell.com/murata/pkm13epyh4000-a0/sounder-4khz-12-6mm/dp/1192513</a>	0.282€	1	0,28 €
Pines para teclado y pantalla	826629-6	Farnell	<a href="https://es.farnell.com/amp-te-connectivity/826629-6/headers-1row-6way/dp/3418327?st=headers">https://es.farnell.com/amp-te-connectivity/826629-6/headers-1row-6way/dp/3418327?st=headers</a>	0.564€	1	0,56 €
Pines para el PIC	2227MC-16-03-F1	Farnell	<a href="https://es.farnell.com/multicomp/2227mc-16-03-f1/z-calodil-tubo-30-16v-as/dp/1103833">https://es.farnell.com/multicomp/2227mc-16-03-f1/z-calodil-tubo-30-16v-as/dp/1103833</a>	13.54€	1	13,54 €
Espadines entrada tensión	BL 5.08/4	Farnell	<a href="https://es.farnell.com/weidmuller/bl-5-08-4/bloque-terminal-pluggable-4p-26/dp/1131814">https://es.farnell.com/weidmuller/bl-5-08-4/bloque-terminal-pluggable-4p-26/dp/1131814</a>	2.60€	1	2,60 €
PIC16F84A programable	PIC16F84A20P	Electroson	<a href="https://www.electroson.com/producto/circuito-integrado-dip-18-memoria-68byte/PIC16F84A20P">https://www.electroson.com/producto/circuito-integrado-dip-18-memoria-68byte/PIC16F84A20P</a>	12.39€	1	12,39 €
Cristal oscilador de cuarzo	4MHz	Farnell	<a href="https://es.farnell.com/multicomp/mcrs004000f183000rr/crystal-4mhz-18pf-thru-hole/dp/1701127">https://es.farnell.com/multicomp/mcrs004000f183000rr/crystal-4mhz-18pf-thru-hole/dp/1701127</a>	0.362€	1	0,36 €
Condensador tantalio	100nF	Farnell	<a href="https://es.farnell.com/avx/tap104m035ccs/condenser-0-1-f-35v-20/dp/1100483?st=capacitor-100nf">https://es.farnell.com/avx/tap104m035ccs/condenser-0-1-f-35v-20/dp/1100483?st=capacitor-100nf</a>	0.418€	1	0,42 €
Condensador cerámico	22pF	Farnell	<a href="https://es.farnell.com/multicomp/mc0805n220j500a5-08mm/capacitor-ceramic-22pf-50v-c0g/dp/1694230">https://es.farnell.com/multicomp/mc0805n220j500a5-08mm/capacitor-ceramic-22pf-50v-c0g/dp/1694230</a>	0.243€	1	0,24 €

Transistor NPN BC547	BC547B	Farnell	<a href="https://es.farnell.com/multicomp/bc547b/transistor-npn-45-v-100ma-to-92/dp/1574381?st=bc547">https://es.farnell.com/multicomp/bc547b/transistor-npn-45-v-100ma-to-92/dp/1574381?st=bc547</a>	0.363€	1	0,36 €
Transistor NPN BD135	BD135	Farnell	<a href="https://es.farnell.com/multicomp/bd135/transistor-npn-to-126/dp/1574347?st=bd135">https://es.farnell.com/multicomp/bd135/transistor-npn-to-126/dp/1574347?st=bd135</a>	0.56€	1	0,56 €
Placa de baquelita	100x160	Electroson	<a href="https://www.electroson.com/producto/placa-fibra-de-vidrio-100x160/PKP203">https://www.electroson.com/producto/placa-fibra-de-vidrio-100x160/PKP203</a>	7.45€	1	7,45 €
					Subtotal	65,22 €
					IVA 21%	13,70 €
					Total	78,91 €

## 8.2 - Presupuesto total.

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Mano de obra, pruebas, y funcionamiento	Precio la hora	Total
15 horas	12.50€	187.5€

Mano de obra	Materiales	Subtotal	Beneficio	Beneficio bruto	Precio venta, sin iva
187.5€	78.91€	266.41€	40%	106.56€	372.97€

## 9 - Bibliografía.

---

### Ficha técnica del diodo rectificador.

Diodo 1N4007 -

<https://pdf1.alldatasheet.com/datasheet-pdf/view/58825/DIODES/1N4007.html>

### Ficha técnica de las interfaces de entrada - salida.

Pantalla LCD 16x2 -

<https://pdf1.alldatasheet.com/datasheet-pdf/view/431751/LUMEX/LCM-S01602DTR-M.html>

Teclado hexadecimal -

[https://components101.com/sites/default/files/component\\_datasheet/4x4%20Keypad%20Module%20Datasheet.pdf](https://components101.com/sites/default/files/component_datasheet/4x4%20Keypad%20Module%20Datasheet.pdf)

Relé -

<https://cdn.findernet.com/app/uploads/2020/09/25140323/S40ES.pdf>

### Fichas técnicas de transistores.

BC547 (NPN) -

<https://pdf1.alldatasheet.com/datasheet-pdf/view/11551/ONSEMI/BC547.html>

BD135 (NPN) -

<https://pdf1.alldatasheet.com/datasheet-pdf/view/2918/MOTOROLA/BD135.html>

### Fichas técnicas del chip programable.

PIC16F84A -

<https://pdf1.alldatasheet.com/datasheet-pdf/view/77366/MICROCHIP/PIC16F84A.html>

Código para PIC -

PDF de Jorge Celestino, proyecto cerradura electrónica.

## 10 - Anexos y ficha técnica.

### Diodo 1N4007.

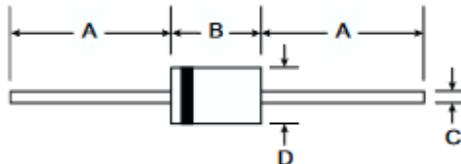


### 1N4001G/L - 1N4007G/L

1.0A GLASS PASSIVATED RECTIFIER

#### Features

- Glass Passivated Die Construction
- Diffused Junction
- High Current Capability and Low Forward Voltage Drop
- Surge Overload Rating to 30A Peak
- Plastic Material - UL Flammability Classification 94V-0



#### Mechanical Data

- Case: Molded Plastic
- Terminals: Plated Leads Solderable per MIL-STD-202, Method 208
- Polarity: Cathode Band
- Weight: DO-41 0.30 grams (approx)  
A-405 0.20 grams (approx)
- Mounting Position: Any
- Marking: Type Number

	DO-41 Plastic		A-405	
Dim	Min	Max	Min	Max
A	25.40	—	25.40	—
B	4.06	5.21	4.10	5.20
C	0.71	0.864	0.53	0.64
D	2.00	2.72	2.00	2.70

All Dimensions in mm

"L" Suffix Designates A-405 Package  
No Suffix Designates DO-41 Package

#### Maximum Ratings and Electrical Characteristics

④ T<sub>A</sub> = 25°C unless otherwise specified

Single phase, half wave, 60Hz, resistive or inductive load.  
For capacitive load, derate current by 20%.

Characteristic	Symbol	1N4001 G/GL	1N4002 G/GL	1N4003 G/GL	1N4004 G/GL	1N4005 G/GL	1N4006 G/GL	1N4007 G/GL	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V <sub>RRM</sub> V <sub>WRM</sub> V <sub>R</sub>	50	100	200	400	600	800	1000	V
RMS Reverse Voltage	V <sub>RRMS</sub>	35	70	140	280	420	560	700	V
Average Rectified Output Current (Note 1) ④ T <sub>A</sub> = 75°C	I <sub>O</sub>				1.0				A
Non-Repetitive Peak Forward Surge Current 8.3ms single half sine-wave superimposed on rated load (JEDEC Method)	I <sub>FSM</sub>				30				A
Forward Voltage ④ I <sub>F</sub> = 1.0A	V <sub>FM</sub>				1.0				V
Peak Reverse Current ④ T <sub>A</sub> = 25°C at Rated DC Blocking Voltage ④ T <sub>A</sub> = 125°C	I <sub>RM</sub>				5.0	50			μA
Reverse Recovery Time (Note 3)	t <sub>rr</sub>				2.0				μs
Typical Junction Capacitance (Note 2)	C <sub>J</sub>				8.0				pF
Typical Thermal Resistance Junction to Ambient	R <sub>θJA</sub>				100				K/W
Operating and Storage Temperature Range	T <sub>j</sub> , T <sub>STG</sub>				-65 to +175				°C

Notes:

1. Leads maintained at ambient temperature at a distance of 9.5mm from the case.
2. Measured at 1.0 MHz and applied reverse voltage of 4.0V DC.
3. Measured with I<sub>F</sub> = 0.5A, I<sub>R</sub> = -1A, I<sub>rr</sub> = 0.25A.

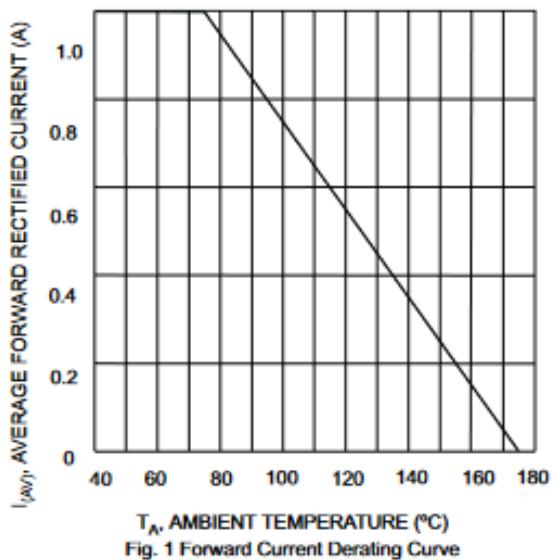


Fig. 1 Forward Current Derating Curve

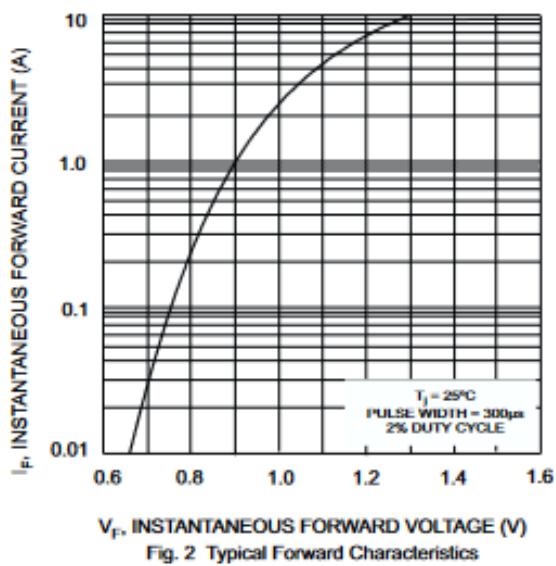


Fig. 2 Typical Forward Characteristics

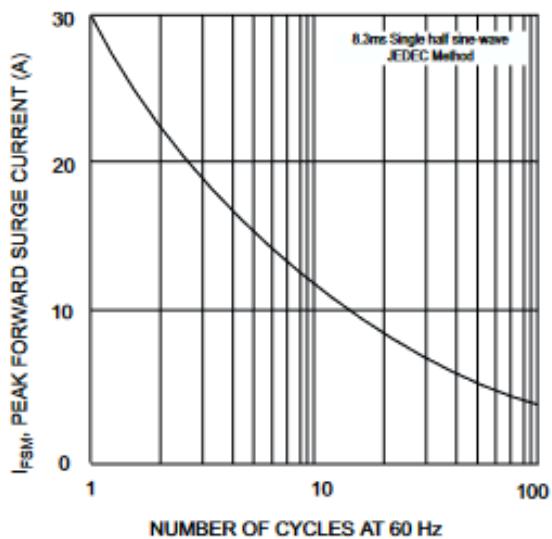


Fig. 3 Max Non-Repetitive Peak Fwd Surge Current

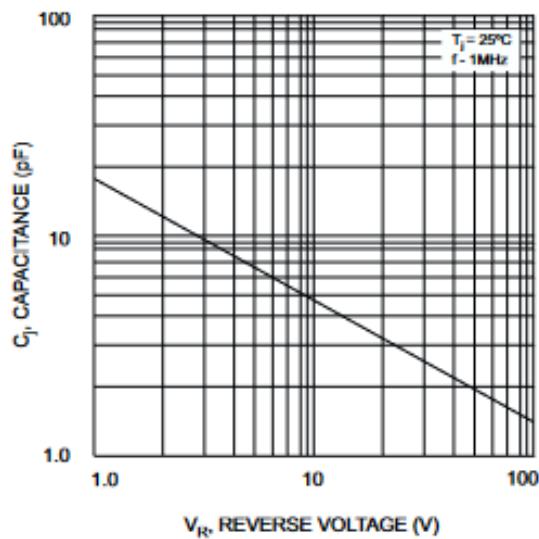


Fig. 4 Typical Junction Capacitance

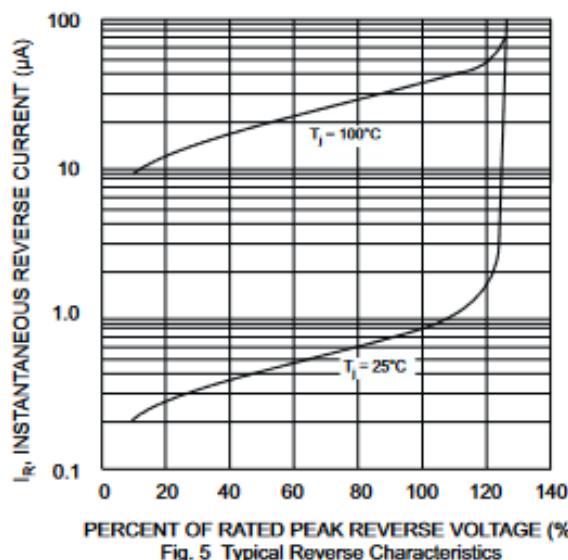
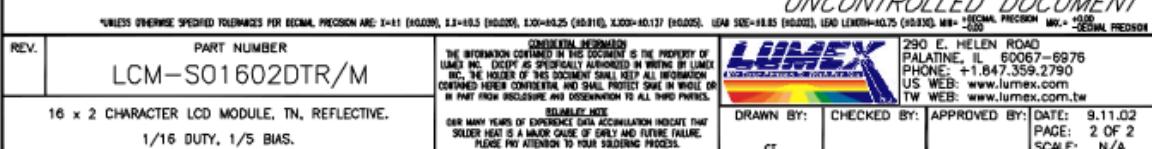
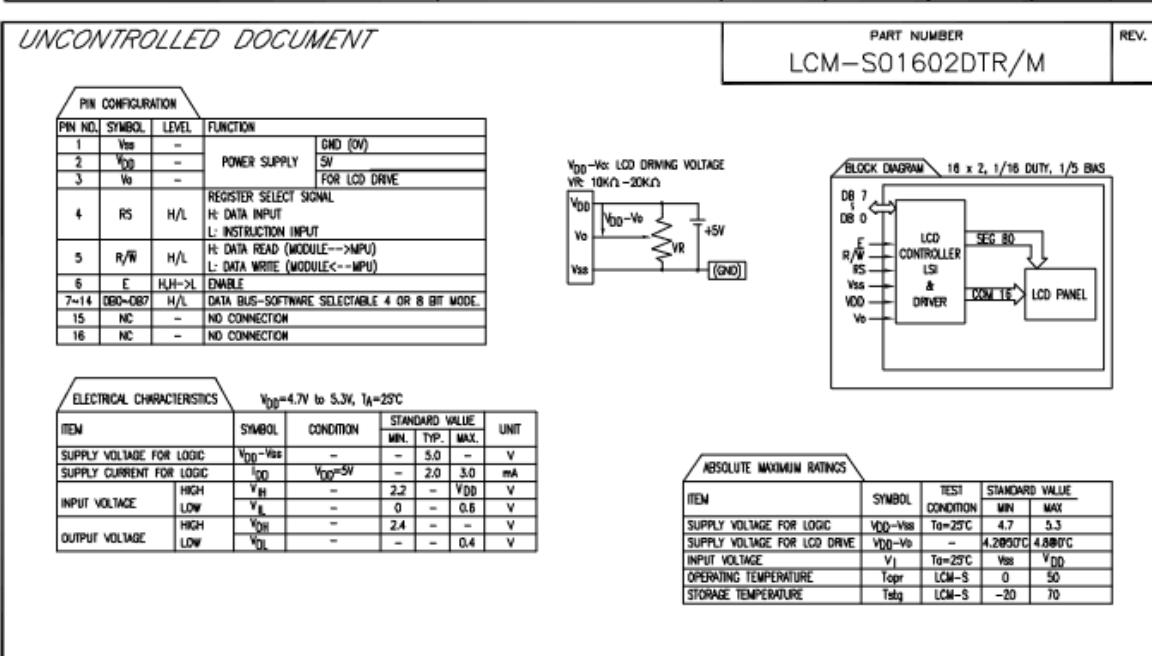
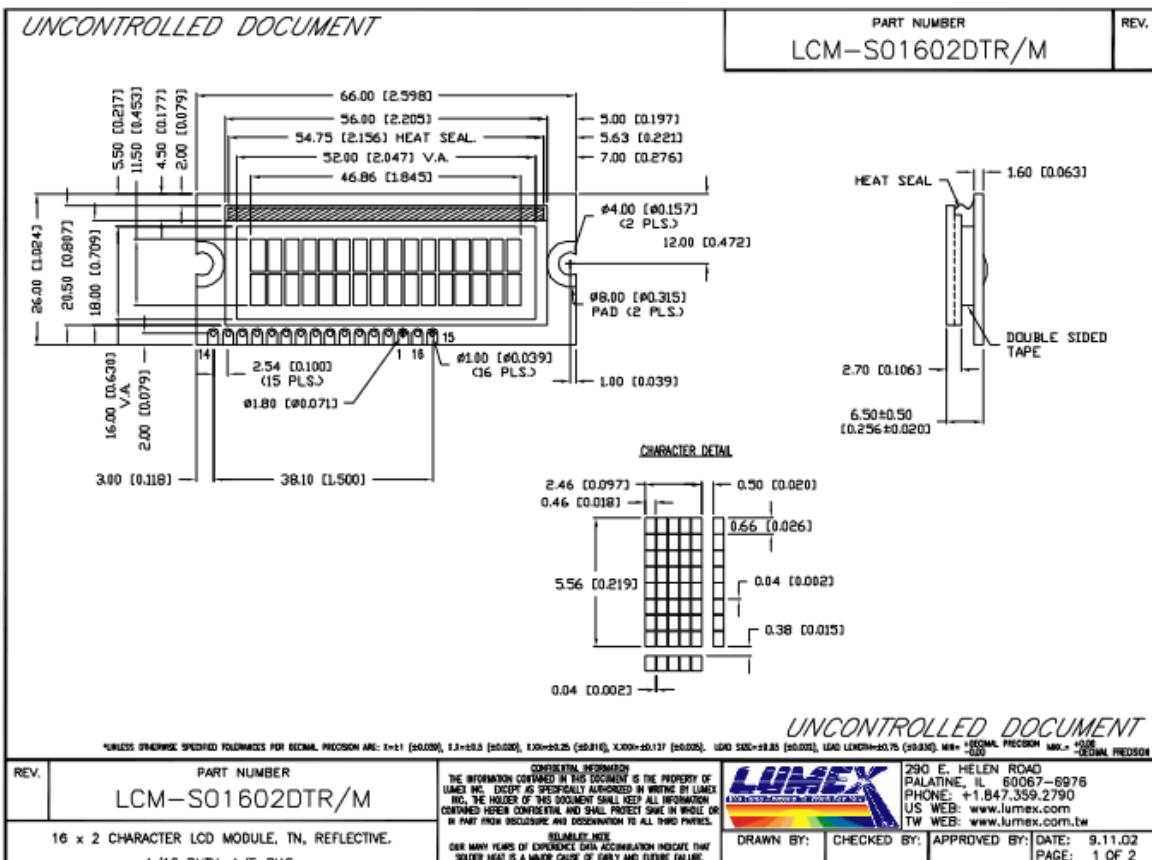


Fig. 5 Typical Reverse Characteristics

## Pantalla LCD 16x2.



## Teclado hexadecimal.



Web Site: [www.parallax.com](http://www.parallax.com)  
Forums: [forums.parallax.com](http://forums.parallax.com)  
Sales: [sales@parallax.com](mailto:sales@parallax.com)  
Technical: [support@parallax.com](mailto:support@parallax.com)

Office: (916) 624-8333  
Fax: (916) 624-8003  
Sales: (888) 512-1024  
Tech Support: (888) 997-8267

## 4x4 Matrix Membrane Keypad (#27899)

This 16-button keypad provides a useful human interface component for microcontroller projects. Convenient adhesive backing provides a simple way to mount the keypad in a variety of applications.

### Features

- Ultra-thin design
- Adhesive backing
- Excellent price/performance ratio
- Easy interface to any microcontroller
- Example programs provided for the BASIC Stamp 2 and Propeller P8X32A microcontrollers

### Key Specifications

- Maximum Rating: 24 VDC, 30 mA
- Interface: 8-pin access to 4x4 matrix
- Operating temperature: 32 to 122 °F (0 to 50°C)
- Dimensions:  
Keypad, 2.7 x 3.0 in (6.9 x 7.6 cm)  
Cable: 0.78 x 3.5 in (2.0 x 8.8 cm)

### Application Ideas

- Security systems
- Menu selection
- Data entry for embedded systems



## How it Works

Matrix keypads use a combination of four rows and four columns to provide button states to the host device, typically a microcontroller. Underneath each key is a pushbutton, with one end connected to one row, and the other end connected to one column. These connections are shown in Figure 1.

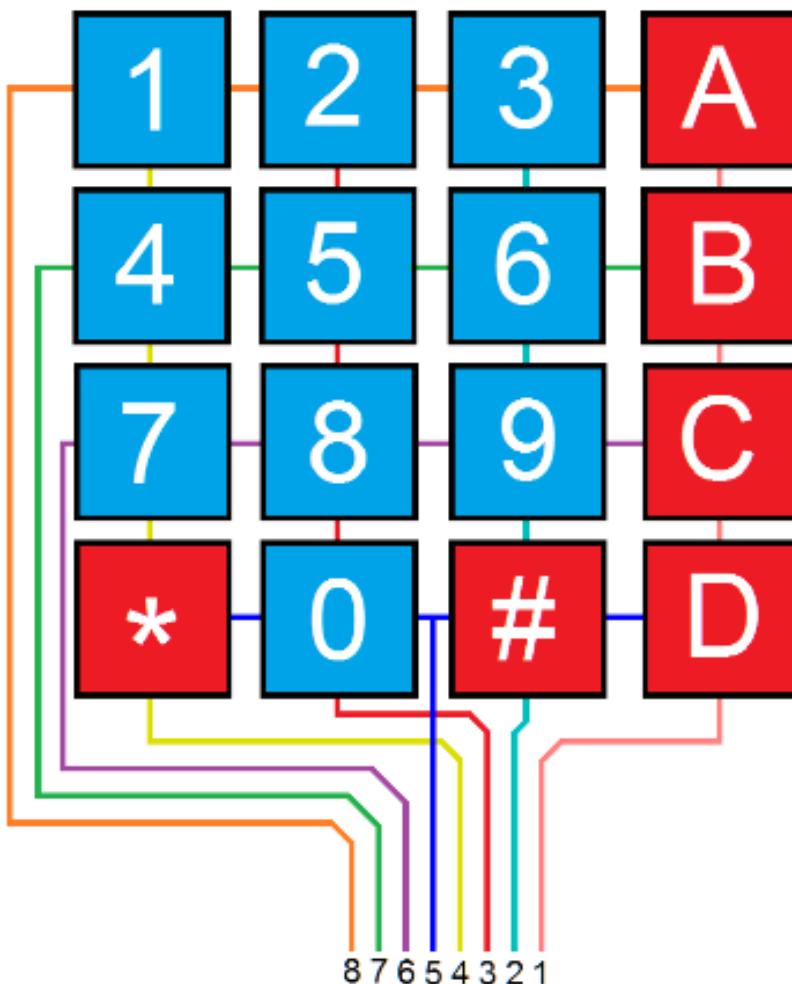


Figure 1: Matrix Keypad Connections

In order for the microcontroller to determine which button is pressed, it first needs to pull each of the four columns (pins 1-4) either low or high one at a time, and then poll the states of the four rows (pins 5-8). Depending on the states of the columns, the microcontroller can tell which button is pressed.

For example, say your program pulls all four columns low and then pulls the first row high. It then reads the input states of each column, and reads pin 1 high. This means that a contact has been made between column 4 and row 1, so button 'A' has been pressed.

## Connection Diagrams

Figure 2

For use with the BASIC Stamp example program listed below.

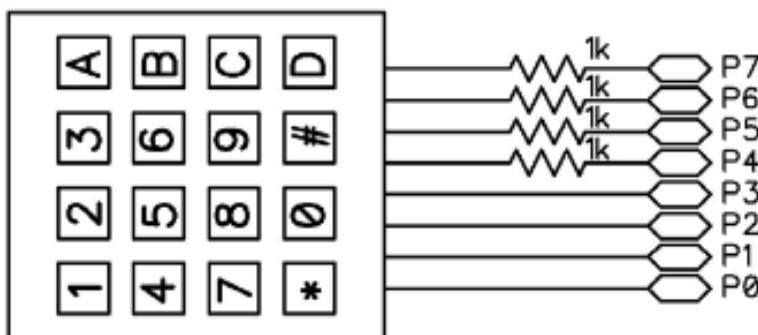
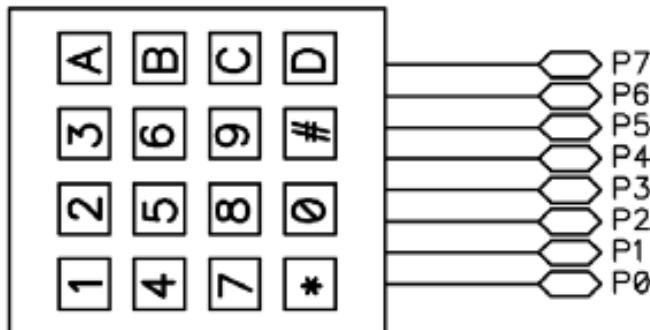


Figure 3

For use with the Propeller P8X32A example program listed below.



## BASIC Stamp® Example Code

The example code below displays the button states of the 4x4 Matrix Membrane Keypad. It uses the Debug Terminal, which is built into the BASIC Stamp Editor software. The software is a free download from [www.parallax.com/basicstampsoftware](http://www.parallax.com/basicstampsoftware).

```
' 4x4MatrixKeypad_Demo.bs2
' Display buttons pressed on the 4x4 Matrix Membrane Keypad
' Author: Parallax HK Engineering

' {$STAMP BS2}
' {$PBASIC 2.5}

row      VAR  Nib          ' Variable space for row counting
column   VAR  Nib          ' Variable space for column counting
keypad   VAR  Word         ' Variable space to store keypad output
keypadOld VAR  Word        ' Variable space to store old keypad output
temp     VAR  Nib          ' Variable space for polling column states

DEBUG CLS           ' Clear Debug Terminal
GOSUB Update       ' Display keypad graphic

DO
    GOSUB ReadKeypad
    DEBUG HOME, BIN16 keypad, CR, CR,
    BIN4 keypad >> 12,CR,
    BIN4 keypad >> 8, CR,
    BIN4 keypad >> 4, CR,
    BIN4 keypad          ' Read keypad button states
                           ' Display 16-bit keypad value
                           ' Display 1st row 4-bit keypad value
                           ' Display 2nd row 4-bit keypad value
                           ' Display 3rd row 4-bit keypad value
                           ' Display 4th row 4-bit keypad value
```

```

IF keypad <> keypadOld THEN                                ' If different button is pressed,
    GOSUB Update                                         ' update the keypad graphic to clear
ENDIF                                                       ' old display

IF keypad THEN                                            ' Display button pressed in graphic
    GOSUB display
ENDIF

keypadOld = keypad                                       ' Store keypad value in variable keypadOld
LOOP

' -----[ Subroutine - ReadKeypad ]-----
' Read keypad button states
ReadKeypad:
    keypad = 0
    OUTL   = $00000000                                     ' Initialize IO
    DIRL   = $00000000

    FOR row = 0 TO 3
        DIRB = $1111                                      ' Set columns (P7-P4) as outputs
        OUTB = $0000                                      ' Pull columns low (act as pull down)
        OUTA = 1 << row                                    ' Set rows high one by one
        DIRA = 1 << row

        temp = 0                                           ' Reset temp variable to 0
        FOR column = 0 TO 3
            INPUT (column + 4)                            ' Set columns as inputs
            temp = temp | (INB & (1 << column))          ' Poll column state and store in temp
        NEXT

        keypad = keypad << 4 | (Temp REV 4)                ' Store keypad value
    NEXT
RETURN

' -----[ Subroutine - Update ]-----
' Graphical depiction of keypad
Update:
    DEBUG CRSRXY,0,7,
    "+---+---+---+",CR,
    "|   |   |   |",CR,
    "+---+---+---+"
RETURN

' -----[ Subroutine - Display ]-----
' Display button pressed in keypad graphic
Display:
    IF KeyPad.BIT15 THEN DEBUG CRSRXY, 02,08,"1"
    IF KeyPad.BIT14 THEN DEBUG CRSRXY, 06,08,"2"
    IF KeyPad.BIT13 THEN DEBUG CRSRXY, 10,08,"3"
    IF KeyPad.BIT12 THEN DEBUG CRSRXY, 14,08,"A"
    IF KeyPad.BIT11 THEN DEBUG CRSRXY, 02,10,"4"
    IF KeyPad.BIT10 THEN DEBUG CRSRXY, 06,10,"5"
    IF KeyPad.BIT9  THEN DEBUG CRSRXY, 10,10,"6"
    IF KeyPad.BIT8  THEN DEBUG CRSRXY, 14,10,"B"
    IF KeyPad.BIT7  THEN DEBUG CRSRXY, 02,12,"7"
    IF KeyPad.BIT6  THEN DEBUG CRSRXY, 06,12,"8"
    IF KeyPad.BIT5  THEN DEBUG CRSRXY, 10,12,"9"

```

```

IF Keypad.BIT4 THEN DEBUG CRSRXY, 14,12,"C"
IF Keypad.BIT3 THEN DEBUG CRSRXY, 02,14,"+"
IF Keypad.BIT2 THEN DEBUG CRSRXY, 06,14,"0"
IF Keypad.BIT1 THEN DEBUG CRSRXY, 10,14,"#"
IF Keypad.BIT0 THEN DEBUG CRSRXY, 14,14,"D"
RETURN

```

## Propeller™ P8X32A Example Code

The example code below displays the button states of the 4x4 Matrix Membrane Keypad, and is a modified version of the 4x4 Keypad Reader DEMO object by Beau Schwabe.

Note: This application uses the 4x4 Keypad Reader.spin object. It also uses the Parallax Serial Terminal to display the device output. Both objects and the Parallax Serial Terminal itself are included with the Propeller Tool v1.2.7 or higher, which is available from the Downloads link at [www.parallax.com/Propeller](http://www.parallax.com/Propeller).

```

{{ 4x4 Keypad Reader PST.spin
Returns the entire 4x4 keypad matrix into a single WORD variable indicating which buttons are
pressed. }}

CON

    _clkmode = xtall + pll16x
    _xinfreq = 5_000_000

OBJ
    text : "Parallax Serial Terminal"
    KP   : "4x4 Keypad Reader"

VAR
    word keypad

PUB start
    'start term
    text.start(115200)
    text.str(string(13, "4x4 Keypad Demo..."))
    text.position(1, 7)
    text.str(string(13, "RAW keypad value 'word'"))

    text.position(1, 13)
    text.str(string(13, "Note: Try pressing multiple keys"))

repeat
    keypad := KP.ReadKeyPad      '--> One line command to read the 4x4 keypad
    text.position(5, 2)           'Display 1st ROW
    text.bin(keypad>>0, 4)
    text.position(5, 3)
    text.bin(keypad>>4, 4)       'Display 2nd ROW
    text.position(5, 4)
    text.bin(keypad>>8, 4)       'Display 3rd ROW
    text.position(5, 5)
    text.bin(keypad>>12, 4)      'Display 4th ROW
    text.position(5, 9)
    text.bin(keypad, 16)          'Display RAW keypad value

```

## Revision History

v1.0: original document

v1.1: Updated Figure 1 on page 2

v1.2: Updated Figure 1 on page 2 (again); updated BS2 comments

## Relé.



SWITCH TO THE FUTURE

SERIE  
40

# Mini-relés para circuito impreso 8 - 10 - 12 - 16 A



Electromedicina,  
odontología



Cuadros de  
control



Cuadros de mando,  
distribución



Juguetes



Automatización  
de toldos, cierra  
metálicos,  
persianas



Abertura de  
puertas y barreras  
automáticas



Tarjetas  
electrónicas



Máquinas de vending



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## SERIE 40

## Mini-relé para circuito impreso enchufable 8 - 10 - 12 - 16 A

SERIE  
40

A

## Relé de potencia con 1 o 2 contactos para montaje en circuito impreso o en zócalo

## Tipo 40.31/51

- 1 contacto comutado 12 A (reticulado 3.5 mm)
- 1 contacto comutado 12 A (reticulado 5.0 mm)

## Tipo 40.52

- 2 contactos comutados 8 A (reticulado 5.0 mm)

## Tipo 40.61

- 1 contacto comutado 16 A (reticulado 5.0 mm)

- Largo de terminal 3.5 mm para montaje en circuito impreso
- Largo de terminal 5.3 mm para relé enchufable
- Bobinas DC (650 mW o 500 mW) y bobinas AC
- Variante con contactos sin Cadmio
- 8 mm distancia por aire/superficial, 6 kV (1.2/50 µs) entre bobina y contactos
- Cumple requisitos de alambre incandescente según EN 60335-1
- Zócalos serie 95 para montaje en circuito impreso o en carril de 35 mm (EN 60715) con bornes a pletina o de conexión rápida o bornes push-in
- Señalización de bobina y supresión CEM
- módulos serie 99 y opciones de Módulos temporizados 86.30
- Protección ambiental: RT II - Estanco al flux (Estándar)  
RT III - lavable (Opción)

\* Montado sobre zócalos ≤ 10 A

\*\* Con material de contactos AgSnO<sub>2</sub>, la máxima corriente instantánea en el contacto NA es 120 A - 5 ms (para 40.61) y 60 A - 5 ms (para 40.52)

PARA UL, VER:  
"Información técnica general" página V

Dimensiones: ver página 10

## Características de los contactos

## Configuración de contactos

## 40.31/51



- 1 contacto comutado 12 A sobre CI, 10 A con zócalo
- Reticulado de 3.5 mm (40.31), reticulado de 5.0 mm (40.51)
- Montaje en circuito impreso o en zócalo serie 95

## 40.52

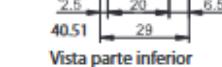
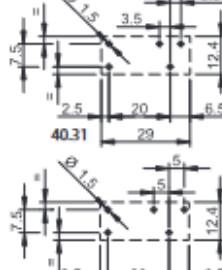
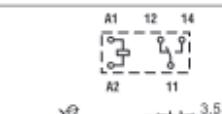


- 2 contactos comutados 8 A
- Reticulado de 5.0 mm
- Montaje en circuito impreso o en zócalo serie 95

## 40.61



- 1 contacto comutado 16 A
- Reticulado de 5.0 mm
- Montaje en circuito impreso o en zócalo serie 95

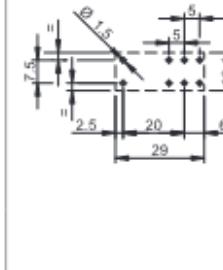
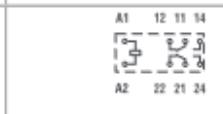


Vista parte inferior

Largo de terminal 3.5 mm solo para CI

Largo de terminal 5.3 mm para CI o zócalos

Ver codificación

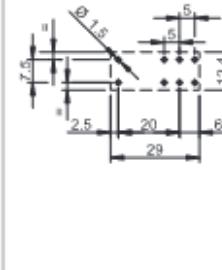
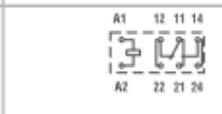


Vista parte inferior

Largo de terminal 3.5 mm solo para CI

Largo de terminal 5.3 mm para CI o zócalos

Ver codificación



Vista parte inferior

Largo de terminal 3.5 mm solo para CI

Largo de terminal 5.3 mm para CI o zócalos

Ver codificación

## Características de la bobina

Tensión nominal de alimentación (U<sub>N</sub>)

## 1 contacto comutado

12\*/20

## 2 contactos comutados

8/15\*\*

## 1 contacto comutado

16/30\*\*

## Tensión nominal/Máx. tensión de conmutación

VAC

250/400

250/400

250/400

## Carga nominal en AC1

VA

3000

2000

4000

## Carga nominal en AC15 (230 V AC)

VA

1000

750

1000

## Motor monofásico (230 V AC)

kW

0.55

0.37

0.55

## Capacidad de ruptura en DC1: 30/110/220 V

A

12/0.6/0.25

8/0.6/0.25

16/0.6/0.25

## Carga mínima comutable

mW (V/mA)

300 (5/5)

300 (5/5)

500 (10/5)

## Material estándar de los contactos

AgNi

AgNi

AgCdO

## Características de la bobina

Tensión nominal de alimentación (U<sub>N</sub>)

VAC (50/60 Hz)

6 - 12 - 24 - 48 - 60 - 110 - 120 - 230 - 240

Tensión nominal de alimentación (U<sub>N</sub>)

VDC

5 - 6 - 7 - 9 - 12 - 14 - 18 - 21 - 24 - 28 - 36 - 48 - 60 - 90 - 110 - 125

## Potencia nominal AC/DC/DC sensible

VA (50 Hz)/W/W

1.2/0.65/0.5

1.2/0.65/0.5

## Campo de funcionamiento

AC

(0.8...1.1)U<sub>N</sub>(0.8...1.1)U<sub>N</sub>(0.8...1.1)U<sub>N</sub>

## DC/DC sensible

(0.73...1.5)U<sub>N</sub>/(0.73...1.5)U<sub>N</sub>(0.73...1.5)U<sub>N</sub>/(0.73...1.5)U<sub>N</sub>(0.73...1.5)U<sub>N</sub>/(0.8...1.5)U<sub>N</sub>

## Tensión de mantenimiento

AC/DC

0.8 U<sub>N</sub>/0.4 U<sub>N</sub>0.8 U<sub>N</sub>/0.4 U<sub>N</sub>0.8 U<sub>N</sub>/0.4 U<sub>N</sub>

## Tensión de desconexión

AC/DC

0.2 U<sub>N</sub>/0.1 U<sub>N</sub>0.2 U<sub>N</sub>/0.1 U<sub>N</sub>0.2 U<sub>N</sub>/0.1 U<sub>N</sub>

## Características generales

## Vida útil mecánica

ciclos

10 - 10<sup>6</sup>10 - 10<sup>6</sup>10 - 10<sup>6</sup>

## Vida útil eléctrica con carga nominal en AC1 ciclos

200 - 10<sup>3</sup>100 - 10<sup>3</sup>100 - 10<sup>3</sup>

## Tiempo de respuesta: ON/OFF

ms

7/3 (10/3 sensible)

7/3 (12/4 sensible)

7/3 (10/3 sensible)

## Aislamiento entre bobina y contactos (1.2/50 µs)

kV

6 (8 mm)

6 (8 mm)

6 (8 mm)

## Rigidez dieléctrica entre contactos abiertos

VAC

1000

1000

1000

## Temperatura ambiente

°C

-40...+85

-40...+85

-40...+85

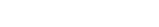
## Categoría de protección

RT II\*\*\*

RT III\*\*\*

RT II\*\*\*

## Homologaciones (según los tipos)



SERIE  
40

## SERIE 40

Mini-relé para circuito impreso enchufable 8 - 10 - 12 - 16 A



**Relé de potencia con 1 o 2 contactos para montaje en circuito impreso o en zócalo**

**Tipo 40.62**

- 2 contactos comutados 10 A (reticulado 5.0 mm)
- Bobinas DC (650 mW o 500 mW) y bobinas AC
- Cumple requisitos de alambre incandescente según EN 60335-1

**Tipo 40.xx.6**

- Versión biestable para relés tipos 40.31, 40.51, 40.52 y 40.61
- Biestable (con un solo bobinado)
- Variante con contactos sin Cadmio
- 8 mm distancia por aire/superficial, 6 kV (1.2/50 µs) entre bobina y contactos
- Zócalos serie 95 para montaje en circuito impreso o en carril de 35 mm (EN 60715) con bornes a pletina o de conexión rápida o bornes push-in
- Protección ambiental:  
RT II - Estanco al flux (Estándar)  
RT III - lavable (Opción)

\* Con material de contactos AgSnO<sub>2</sub>, la máxima corriente instantánea en el contacto NA es 60 A - 5 ms (para 40.62)

PARA UL, VER:  
"Información técnica general" página V

Dimensiones: ver página 10

**Características de los contactos**

Configuración de contactos	2 contactos comutados
----------------------------	-----------------------

Corriente nominal/Max. corriente instantánea A	10/20*
--	--------

Tensión nominal/	
------------------	--

Máx. tensión de conmutación V AC	250/400
----------------------------------	---------

Carga nominal en AC1 VA	2500
-------------------------	------

Carga nominal en AC15 (230 V AC) VA	750
-------------------------------------	-----

Motor monofásico (230 V AC) kW	0.37
--------------------------------	------

Capacidad de ruptura en DC1: 30/110/220 V A	10/0.6/0.25
---	-------------

Carga mínima comutable mW (V/mA)	300 (5/5)
----------------------------------	-----------

Material estándar de los contactos	AgNi
------------------------------------	------

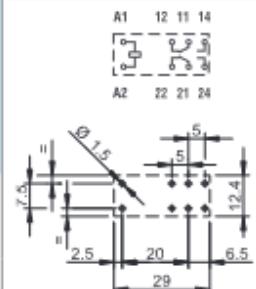
**Características de la bobina**

Tensión nominal de alimentación (U <sub>N</sub> ) V AC (50/60 Hz)	110 - 120 - 230 - 240
---	-----------------------

V DC	5 - 6 - 7 - 9 - 12 - 14 - 18 - 21 - 24 - 28 - 48 - 60 - 110 - 125
------	---

**40.62 NEW**

- 2 contactos comutados 10 A
- Reticulado 5.0 mm
- Montaje en circuito impreso o en zócalo serie 95



Vista parte inferior  
Largo de terminal 5.3 mm para CI o zócalos

**40.xx.6**

- Biestable (con un solo bobinado)
- Reticulado de 3.5 o 5.0 mm
- Montaje en circuito impreso o en zócalo serie 95

Versión biestable (con un solo bobinado) tipos:

- 40.31.6...  
40.51.6...  
40.52.6...  
40.61.6...

Ver esquemas de conexión  
página 10  
Largo de terminal 5.3 mm para  
CI o zócalos

- Ver relés  
40.31  
40.51  
40.52  
40.61  
página 3

**Características generales**

Vida útil mecánica ciclos	10 - 10 <sup>6</sup>
---------------------------	----------------------

Vida útil eléctrica con carga nominal en AC1 ciclos	100 - 10 <sup>3</sup>
---	-----------------------

Tiempo de respuesta: ON/OFF ms	7/3 (12/4 sensible)
--------------------------------	---------------------

Aislamiento entre bobina y contactos (1.2/50 µs) kV	6 (8 mm)
---	----------

Rigidez dieléctrica entre contactos abiertos V AC	1000
---	------

Temperatura ambiente °C	-40...+85
-------------------------	-----------

Categoría de protección	RT II
-------------------------	-------

Homologaciones (según los tipos)	ETL CC GS EAC RINA UL us
----------------------------------	--------------------------

- Ver relés  
40.31

- 40.51

- 40.52

- 40.61

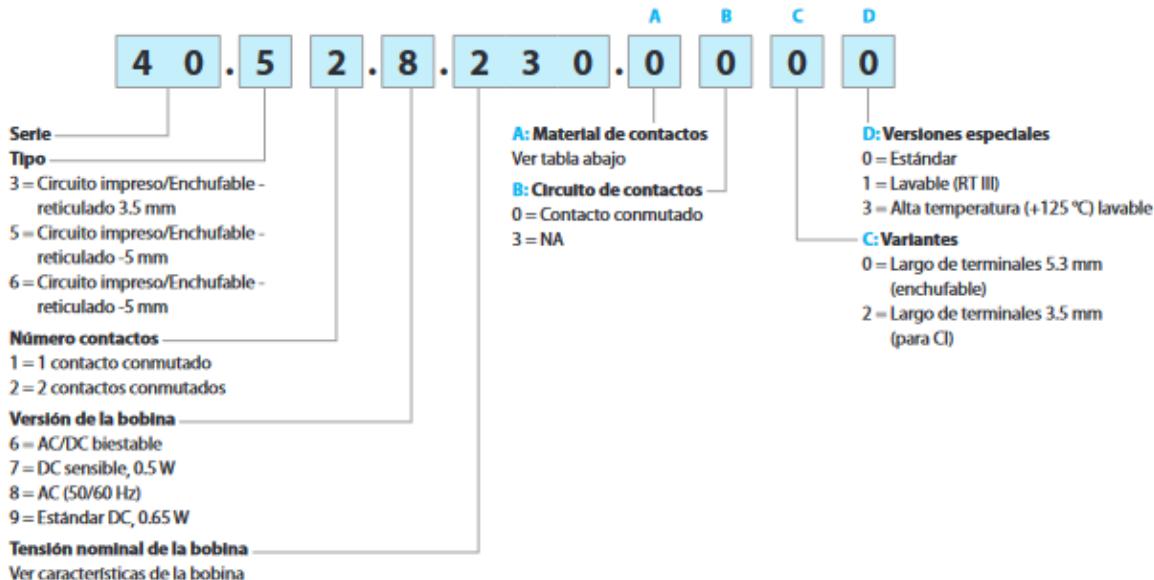
Tiempo mínimo de impulso  
≥ 20 ms

\*\* Ver información técnica "Indicaciones sobre los procedimientos de soldadura automática" página II.

**SERIE 40**  
**Mini-relé para circuito impreso enchufable 8 - 10 - 12 - 16 A**

**SERIE  
40**
**Codificación**

Ejemplo: Serie 40 relé para CI, 2 contactos conmutados, bobina 230 V AC.

**Selección de características y opciones: solo son posibles combinaciones en la misma línea.**

En negrita se muestran las opciones preferentes y con mejor disponibilidad.

Terminal	Tipo	Versión de la bobina	A	B	C	D
Relé para CI, largo de terminales 3.5 mm	40.31/51	Estándar DC/DC sensible	<b>1</b> (AgNi)	<b>0</b> - 3	<b>2</b>	<b>0 - 1</b>
	40.61	Estándar DC/DC sensible	<b>1</b> (AgNi) - 2 (AgCdO)	<b>0</b> - 3	<b>2</b>	<b>0 - 1</b>
Relé para CI/ Enchufar, largo de terminales 5.3 mm	40.31/51	AC/DC sensible	<b>0</b> (AgNi) - 2 (AgCdO) - 5 (AgNi+Au)	<b>0</b> - 3	<b>0</b>	<b>0 - 1</b>
	40.31/51	Estándar DC	<b>0</b> (AgNi) - 2 (AgCdO) - 5 (AgNi+Au)	<b>0</b> - 3	<b>0</b>	<b>0 - 1 - 3</b>
	40.52	AC/DC sensible	<b>0</b> (AgNi) - 4 (AgSnO <sub>2</sub> ) - 5 (AgNi+Au)	<b>0</b> - 3	<b>0</b>	<b>0 - 1</b>
	40.52	Estándar DC	<b>0</b> (AgNi) - 4 (AgSnO <sub>2</sub> ) - 5 (AgNi+Au)	<b>0</b> - 3	<b>0</b>	<b>0 - 1 - 3</b>
	40.61	AC/DC sensible	<b>0</b> (AgCdO) - 4 (AgSnO <sub>2</sub> )	<b>0</b> - 3	<b>0</b>	<b>0 - 1</b>
	40.61	Estándar DC	<b>0</b> (AgCdO) - 4 (AgSnO <sub>2</sub> )	<b>0</b> - 3	<b>0</b>	<b>0 - 1 - 3</b>
	40.62	AC/DC/DC sensible	<b>0</b> (AgNi) - 4 (AgSnO <sub>2</sub> )	<b>0</b>	<b>0</b>	<b>0 - 1</b>
	40.31/51/52	Biestable	<b>0</b> (AgNi)	<b>0</b>	<b>0</b>	<b>0</b>
	40.61	Biestable	<b>0</b> (AgCdO)	<b>0</b>	<b>0</b>	<b>0</b>

SERIE  
40

SERIE 40

Mini-relé para circuito impreso enchufable 8 - 10 - 12 - 16 A

**Características generales****Aislamiento según EN 61810-1**

A		1 contacto		2 contactos	
		V AC	230/400	V AC	230/400
Tensión nominal de alimentación	V AC	250	400	250	400
Tensión nominal de aislamiento	V AC				
Grado de contaminación		3	2	3	2

**Aislamiento entre bobina y contactos**

Tipo de aislamiento	Reforzado (8 mm)	Reforzado (8 mm)
Categoría de sobretensión	III	III
Tensión soportada a los impulsos	kV (1.2/50 µs)	6
Rigidez dieléctrica	V AC	4000

**Aislamiento entre contactos adyacentes (40.52)**

Tipo de aislamiento	—	Principal
Categoría de sobretensión	—	II
Tensión soportada a los impulsos	kV (1.2/50 µs)	—
Rigidez dieléctrica	V AC	—

**Aislamiento entre contactos adyacentes (40.52 + 40.62)**

Tipo de aislamiento	—	Principal
Categoría de sobretensión	—	III
Tensión soportada a los impulsos	kV (1.2/50 µs)	—
Rigidez dieléctrica	V AC	—

**Aislamiento entre contactos abiertos**

Tipo de aislamiento	Microdesconexión	Microdesconexión
Rigidez dieléctrica	V AC/kV (1.2/50µs)	1000/1.5

**Aislamiento entre terminales de bobina**

Tensión soportada a los impulsos (surge) modo diferencial (según EN 61000-4-5)	kV (1.2/50 µs)	2
---	----------------	---

**Otros datos**

Tiempo de rebotes: NA/NC	ms	2/5
Resistencia a la vibración (10...150)Hz: NA/NC	g	20/5 (1 contacto comutado)
Resistencia al choque NA/NC	g	20/13 (1 contacto comutado)
Potencia disipada al ambiente	en vacío	W 0.65
	con carga nominal	W 1.2 (40.31/51)
Distancia de montaje entre relés en un circuito impreso	mm	≥ 5

SERIE 40

Mini-relé para circuito impreso enchufable 8 - 10 - 12 - 16 A

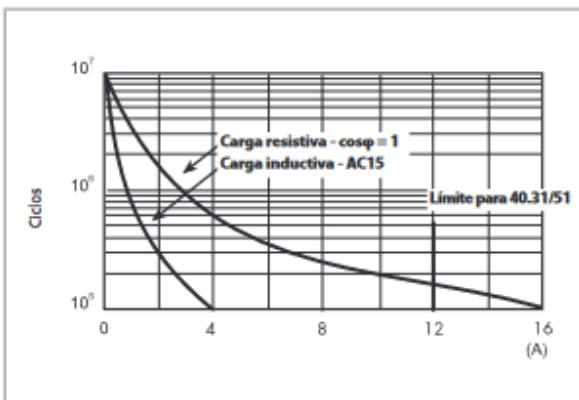


SERIE  
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### Características de los contactos

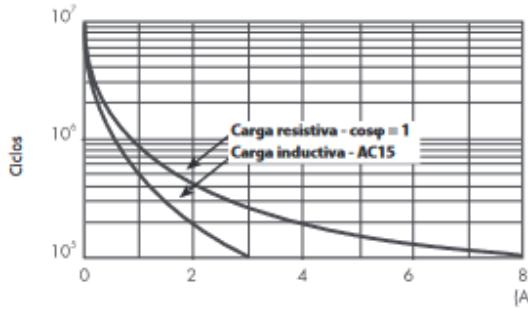
F 40.1 - Vida útil eléctrica (AC) en función de la carga

Tipos 40.31/51/61



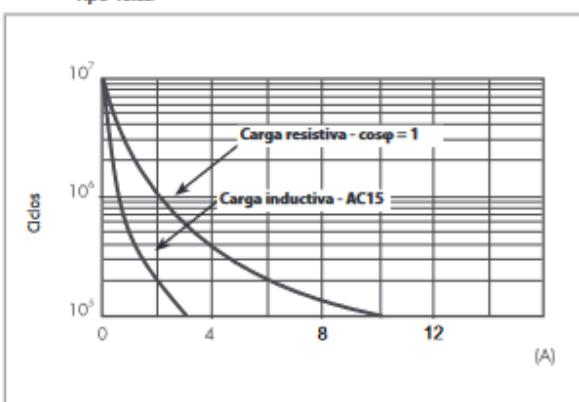
F 40.2 - Vida útil eléctrica (AC) en función de la carga

Tipo 40.52



F 40.6 - Vida útil eléctrica (AC) en función de la carga

Tipo 40.62



A

SERIE  
40

SERIE 40

Mini-relé para circuito impreso enchufable 8 - 10 - 12 - 16 A

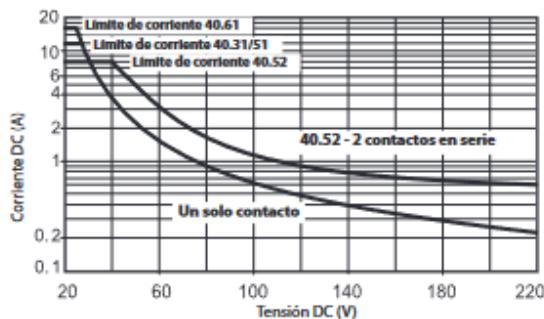


### Características de los contactos

#### H 40.1 - Máximo poder de corte con cargas en DC1

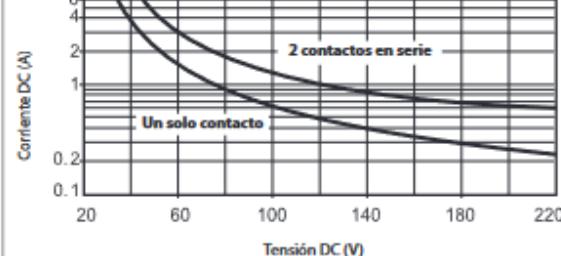
Tipos 40.31/51/52/61

A



#### H 40.6 - Máximo poder de corte con cargas en DC1

Tipo 40.62



- La vida eléctrica para cargas resistivas en (DC1) que tengan valores de tensión y corriente bajo la curva es de  $\geq 100 \cdot 10^3$  ciclos.
  - Para las cargas DC13, la colocación de un diodo con polaridad invertida en paralelo con la carga permite obtener una vida eléctrica idéntica a la que se consigue con una carga en DC1.
- Nota: aumentará el tiempo de desconexión.

SERIE 40

Mini-relé para circuito impreso enchufable 8 - 10 - 12 - 16 A

SERIE  
40**Características de la bobina**

Valores de la versión DC - 0.65 W estándar (Tipos 40.31/51/52/61/62)

Tensión nominal $U_N$	Código bobina V	Campo de funcionamiento		Resistencia R	Nominal absorbida I a $U_N$ mA
		$U_{min}$	$U_{max}$		
5	9.005	3.65	7.5	38	130
6	9.006	4.4	9	55	109
7	9.007	5.1	10.5	75	94
9	9.009	6.6	13.5	125	72
12	9.012	8.8	18	220	55
14	9.014	10.2	21	300	47
18	9.018	13.1	27	500	36
21	9.021	15.3	31.5	700	30
24	9.024	17.5	36	900	27
28	9.028	20.5	42	1200	23
36	9.036	26.3	54	2000	18
48	9.048	35	72	3500	14
60	9.060	43.8	90	5500	11
90	9.090	65.7	135	12500	7.2
110	9.110	80.3	165	18000	6.2
125	9.125	91.2	188	23500	5.3

Valores de la versión DC - 0.5 W sensible (Tipos 40.31/51/52/61/62)

Tensión nominal $U_N$	Código bobina V	Campo de funcionamiento		Resistencia R	Nominal absorbida I a $U_N$ mA
		$U_{min}^*$	$U_{max}$		
5	7.005	3.7	7.5	50	100
6	7.006	4.4	9	75	80
7	7.007	5.1	10.5	100	70
9	7.009	6.6	13.5	160	56
12	7.012	8.8	18	288	42
14	7.014	10.2	21	400	35
18	7.018	13.2	27	650	27.7
21	7.021	15.4	31.5	900	23.4
24	7.024	17.5	36	1150	21
28	7.028	20.5	42	1600	17.5
36	7.036	26.3	54	2600	13.8
48	7.048	35	72	4800	10
60	7.060	43.8	90	7200	8.4
90	7.090	65.7	135	16200	5.6
110	7.110	80.3	165	23500	4.7
125	7.125	91.2	188	32000	3.9

\*  $U_{min} = 0.8 U_N$  para 40.61

Valores de la versión AC (tipos 40.31/51/52/61/62)

Tensión nominal $U_N$	Código bobina V	Campo de funcionamiento		Resistencia R	Nominal absorbida I a $U_N$ (50 Hz) mA
		$U_{min}$	$U_{max}$		
6	8.006	4.8	6.6	21	168
12	8.012	9.6	13.2	80	90
24	8.024	19.2	26.4	320	45
48	8.048	38.4	52.8	1350	21
60	8.060	48	66	2100	16.8
110	8.110	88	121	6900	9.4
120	8.120	96	132	9000	8.4
230	8.230	184	253	28000	5
240	8.240	192	264	31500	4.1

Valores de la versión AC/DC - blestable (tipos 40.31/51/52/61)

Tensión nominal $U_N$	Código bobina V	Campo de funcionamiento		Resistencia R	Nominal absorbida I a $U_N$ mA	Resistencia de desaceleración** $R_{DC}$ $\Omega$
		$U_{min}$	$U_{max}$			
5	6.005	4	5.5	23	215	37
6	6.006	4.8	6.6	33	165	62
12	6.012	9.6	13.2	130	83	220
24	6.024	19.2	26.4	520	40	910
48	6.048	38.4	52.8	2100	21	3,600
110	6.110	88	121	11000	10	16,500

\*\*  $R_{DC}$  - Resistencia en DC,  $R_{AC} = 1.3 \times R_{DC}$  1 W

SERIE  
40

SERIE 40

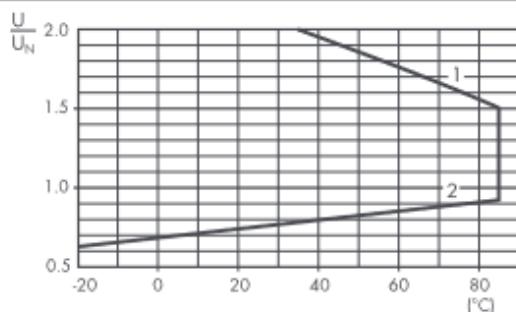
Mini-relé para circuito impreso enchufable 8 - 10 - 12 - 16 A



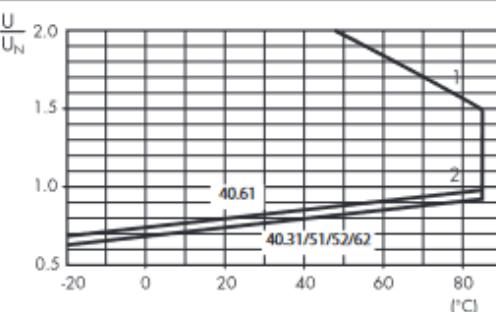
### Características de la bobina

A

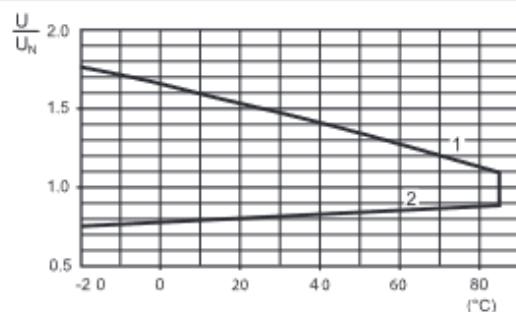
R 40 - Campo de funcionamiento de la bobina DC en función de la temperatura ambiente - Bobina estándar



R 40 - Campo de funcionamiento de la bobina DC en función de la temperatura ambiente - Bobina sensible, tipos 40.31/51/52/61/62



R 40 - Campo de funcionamiento de la bobina AC en función de la temperatura ambiente

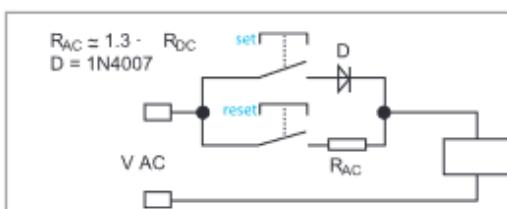


1 - Tensión máx. admisible en la bobina.

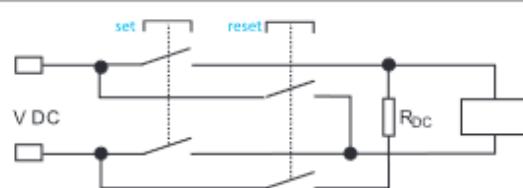
2 - Tensión de conexión mínima con la bobina a temperatura ambiente.

### Esquema de conexionado para serie 40, versión bobina blestable

Funcionamiento en AC



Funcionamiento en DC



Pulsando SET, el relé se magnetiza directamente, los contactos pasan a la posición de trabajo y permanecen en ella.

Pulsando RESET, el relé se desmagnetiza a través de la resistencia (R<sub>AC</sub>) y los contactos retornan a posición de reposo.

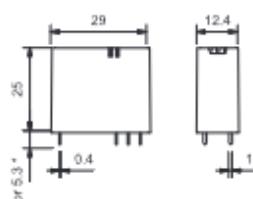
Pulsando SET, el relé se magnetiza a través de un diodo, los contactos pasan a la posición de trabajo y permanecen en ella.

Pulsando RESET, el relé se desmagnetiza a través de la resistencia (R<sub>DC</sub>) y los contactos retornan a posición de reposo.

**Notas:** La duración mínima de los impulsos de SET y RESET es de 20 ms. El impulso puede ser continuo. Hay que asegurarse que los pulsadores de SET y RESET no puedan accionarse al mismo tiempo.

### Dimensiones

Tipos 40.31/51/52/61/62



\* (3.5 o 5.3 mm) ver codificación

## SERIE 95

## Relación de zócalos para relés serie 40

SERIE  
4095.P5  
Ver página 1295.05  
Ver página 1495.85.3  
Ver página 1595.95.3  
Ver página 1695.65  
Ver página 1795.13.2  
Ver página 18

A

Módulo	Zócalos	Relé	Descripción	Montaje	Accesorios
99.02	95.P3	40.31	Zócalos con bornes push-in		
	95.P5	40.51 40.52 40.61 40.62	- Para la conexión rápida de los hilos conductores - Bornes superiores - Contactos - Bornes inferiores - Bobina	Montaje en panel o carril de 35 mm (EN 60715)	- Módulos de señalización y protección CEM - Puente - Módulos temporizados - Palanca de retención y extracción plástica

Módulo	Zócalos	Relé	Descripción	Montaje	Accesorios
99.02	95.03	40.31	Zócalo con bornes de jaula		
	95.05	40.51 40.52 40.61 40.62	- Bornes superiores - Contactos - Bornes inferiores - Bobina	Montaje en panel o carril de 35 mm (EN 60715)	- Módulos de señalización y protección CEM - Puente - Módulos temporizados - Palanca de retención y extracción plástica

Módulo	Zócalos	Relé	Descripción	Montaje	Accesorios
99.80	95.83.3	40.31	Zócalo con bornes de jaula		
	95.85.3	40.51 40.52 40.61 40.62	- Bornes superiores - Contactos NA y COM - Bornes inferiores - Contactos de bobina y NC	Montaje en panel o carril de 35 mm (EN 60715)	- Módulos de señalización y protección CEM - Puente - Palanca de retención y extracción plástica

Módulo	Zócalos	Relé	Descripción	Montaje	Accesorios
99.80	95.93.3	40.31	Zócalo con bornes de jaula		
	95.95.3	40.51 40.52 40.61 40.62	- Bornes superiores - Contactos - Bornes inferiores - Bobina	Montaje en panel o carril de 35 mm (EN 60715)	- Módulos de señalización y protección CEM - Puente - Palanca de retención y extracción plástica

Módulo	Zócalos	Relé	Descripción	Montaje	Accesorios
99.01	95.63	40.31	Zócalo con bornes de jaula		
	95.65	40.51 40.52 40.61 40.62	- Bornes superiores - Contactos - Bornes inferiores - Bobina	Montaje en panel o carril de 35 mm (EN 60715)	- Banda de retención metálica

Módulo	Zócalos	Relé	Descripción	Montaje	Accesorios
—	95.13.2	40.31	Zócalo para circuito Impreso	Montaje en circuito impreso	- Banda de retención metálica - Palanca de retención plástica
—	95.15.2	40.51 40.52 40.61 40.62			

SERIE  
40

SERIE 95

Relación de zócalos para relés serie 40

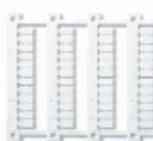


95.P5

Homologaciones  
(según los tipos)



095.91.3



060.48

Zócalo con bornes push-in montaje en panel o carril de 35 mm

95.P3

95.P5

Tipo de relé

40.31

40.51, 40.52, 40.61, 40.62

Accesorios

095.71

Brida de retención metálica

095.91.3

Palanca de retención y extracción plástica  
(suministrada con el zócalo - código de embalaje SPA)

097.58

Puente de 8 terminales

097.52

Puente de 2 terminales (reticulado 12.5 mm)

097.42

Puente de 2 terminales (reticulado 4.6 mm)

097.00

Soporte para etiquetas de identificación (para etiquetas tipo 060.48)

095.00.4

Etiqueta de identificación

99.02

Módulos (ver tabla abajo)

86.30

Módulos temporizados (ver tabla abajo)

Juego de etiquetas de identificación para palanca de retención y extracción plástica 095.91.3 y para soporte de etiquetas de identificación 097.00, 48 etiquetas 6 x 12 mm, para impresora por transferencia térmica CEMBRE

060.48

Características generales

Valor nominal 10 A - 250 V\*

Rigidez dielectrica entre bobina y contactos (1.2/50 µs) 6 kV

Categoría de protección IP 20

Temperatura ambiente °C -40...+70 (ver diagrama L95)

Longitud de pelado del cable mm 10

Capacidad mínima de conexión de los bornes para zócalos 95.P3 y 95.P5

mm² 0.5 hilo rígido 0.5 hilo flexible

AWG 21 21

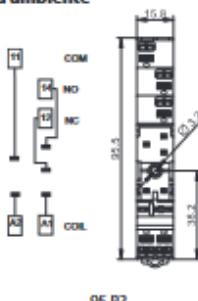
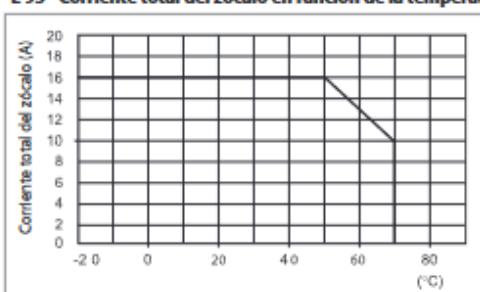
Capacidad máxima de conexión de los bornes para zócalos 95.P3 y 95.P5

mm² 2 x 1.5 / 1 x 2.5 2 x 1.5 / 1 x 2.5

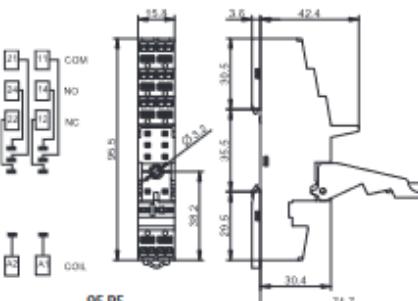
AWG 2 x 16 / 1 x 14 2 x 16 / 1 x 14

\* Con corrientes > 10 A, los bornes de los contactos deben conectarse en paralelo (21 con 11, 24 con 14, 22 con 12).  
Con relés 40.51 utilizar los bornes 21, 12 y 14.

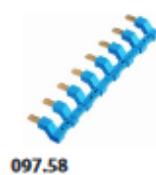
## L 95 - Corriente total del zócalo en función de la temperatura ambiente



95.P3



95.P5



097.58

Puente de 8 terminales para zócalos 95.P3 y 95.P5

097.58

10 A - 250 V



097.52

Puente de 2 terminales para zócalos 95.P3 y 95.P5

097.52

10 A - 250 V



SERIE 95

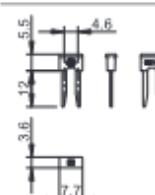
Relación de zócalos para relés serie 40

SERIE  
40

097.42

## Puente de 2 terminales para zócalos 95.P3 y 95.P5

Valor nominal



097.42

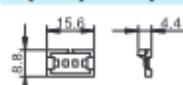
10 A - 250 V

A



097.00

## Soporte para etiquetas de identificación para zócalos 95.P3 y 95.P5



097.00



86.30

## Módulo temporizador serie 86

(12...24)V AC/DC; Bifunción: AI, DI; (0.05 s...100 h)

86.30.0.024.0000

(110...125)V AC; Bifunción: AI, DI; (0.05 s...100 h)

86.30.8.120.0000

(230...240)V AC; Bifunción: AI, DI; (0.05 s...100 h)

86.30.8.240.0000

Homologaciones (según los tipos):

99.02  
Homologaciones  
(según los tipos): Los módulos DC con  
polaridad no estándar  
(+A2) están disponibles  
bajo pedido.

## Módulos de señalización y protección CEM tipo 99.02 para zócalos 95.P3 y 95.P5

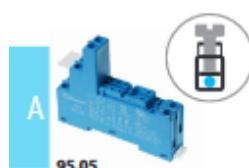
Diodo (+A1, polaridad estándar)	(6...220)V DC	99.02.3.000.00
LED	(6...24)V DC/AC	99.02.0.024.59
LED	(28...60)V DC/AC	99.02.0.060.59
LED	(110...240)V DC/AC	99.02.0.230.59
LED + Diodo (+A1, polaridad estándar)	(6...24)V DC	99.02.9.024.99
LED + Diodo (+A1, polaridad estándar)	(28...60)V DC	99.02.9.060.99
LED + Diodo (+A1, polaridad estándar)	(110...220)V DC	99.02.9.220.99
LED + Varistor	(6...24)V DC/AC	99.02.0.024.98
LED + Varistor	(28...60)V DC/AC	99.02.0.060.98
LED + Varistor	(110...240)V DC/AC	99.02.0.230.98
RC	(6...24)V DC/AC	99.02.0.024.09
RC	(28...60)V DC/AC	99.02.0.060.09
RC	(110...240)V DC/AC	99.02.0.230.09
Antirremanencia*	(110...240)V AC	99.02.8.230.07

\* Potencia adicional de disipación 0.9 W

SERIE  
40

SERIE 95

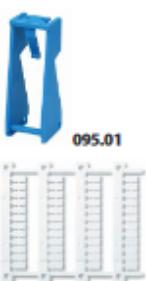
Relación de zócalos para relés serie 40



95.05

Homologaciones  
(según los tipos):

Combinación relé/zócalo

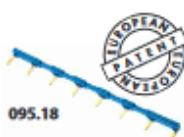
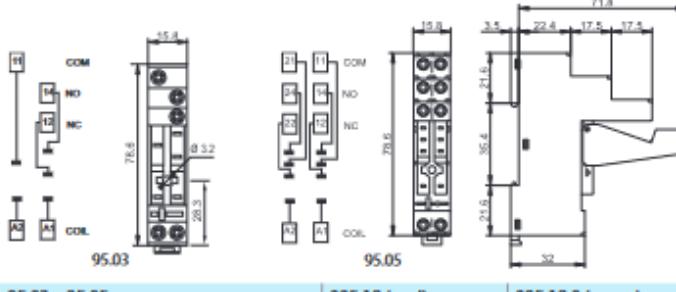
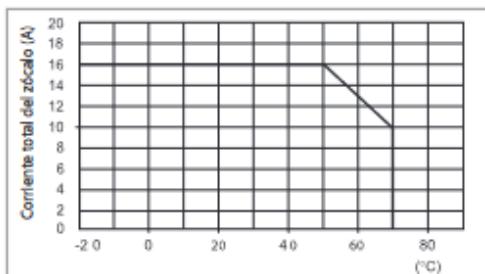


095.01

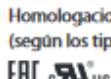
060.48

Zócalo con bornes de jaula montaje en panel o cartón de 35 mm	95.03 (azul)	95.03.0 (negro)	95.05 (azul)	95.05.0 (negro)			
Tipo de relé	40.31		40.51, 40.52, 40.61, 40.62				
<b>Accesorios</b>							
Brida de retención metálica		095.71					
Palanca de retención y extracción plástica (suministrada con el zócalo - código de embalaje SPA)	095.01	095.01.0	095.01	095.01.0			
Puente de 8 terminales	095.18	095.18.0	095.18	095.18.0			
Soporte para etiquetas de identificación (para etiquetas tipo 060.48)			097.00				
Etiqueta de identificación			095.00.4				
Módulos (ver tabla abajo)			99.02				
Módulos temporizados (ver tabla abajo)			86.30				
Juego de etiquetas de identificación para palanca de retención y extracción plástica 095.01 y para soporte de etiquetas de identificación 097.00, 48 etiquetas 6 x 12 mm, para impresora por transferencia térmica CEMBRE				060.48			
<b>Características generales</b>							
Valor nominal	10 A - 250 V*						
Rigidez dielectrica entre bobina y contactos	(1.2/50 µs)	6 kV					
Categoría de protección	IP 20						
Temperatura ambiente	°C -40...+70 (ver diagrama L95)						
Par de apriete	Nm	0.5					
Longitud de pelado del cable	mm	8					
Capacidad de conexión de los bornes para zócalos 95.03 y 95.05	hilo rígido		hilo flexible				
	mm²	1 x 6 / 2 x 2.5		1 x 4 / 2 x 2.5			
	AWG	1 x 10 / 2 x 14		1 x 12 / 2 x 14			

\* Con corrientes > 10 A, los bornes de los contactos deben conectarse en paralelo (21 con 11, 24 con 14, 22 con 12).  
Con relés 40.51 utilizar los bornes 21, 12 y 14.

**L 95 - Corriente total del zócalo en función de la temperatura ambiente**

99.02

Homologaciones  
(según los tipos):

Los módulos DC con polaridad no estándar (+A2) están disponibles bajo pedido.

Mpuente de 8 terminales para zócalos 95.03 y 95.05	095.18 (azul)	095.18.0 (negro)
Valor nominal	10 A - 250 V	

**Módulo temporizador serie 86**

(12...24)V AC/DC; Bifunción: AI, DI; (0.05 s...100 h)	86.30.0.024.0000
(110...125)V AC; Bifunción: AI, DI; (0.05 s...100 h)	86.30.8.120.0000
(230...240)V AC; Bifunción: AI, DI; (0.05 s...100 h)	86.30.8.240.0000

Homologaciones (según los tipos):

**Módulos de señalización y protección CEM tipo 99.02 para zócalos 95.03 y 95.05**

Diodo (+A1, polaridad estándar)	(6...220)V DC	99.02.3.000.00
LED	(6...24)V DC/AC	99.02.0.024.59
LED	(28...60)V DC/AC	99.02.0.060.59
LED	(110...240)V DC/AC	99.02.0.230.59
LED + Diodo (+A1, polaridad estándar)	(6...24)V DC	99.02.9.024.99
LED + Diodo (+A1, polaridad estándar)	(28...60)V DC	99.02.9.060.99
LED + Diodo (+A1, polaridad estándar)	(110...220)V DC	99.02.9.220.99
LED + Varistor	(6...24)V DC/AC	99.02.0.024.98
LED + Varistor	(28...60)V DC/AC	99.02.0.060.98
LED + Varistor	(110...240)V DC/AC	99.02.0.230.98
RC	(6...24)V DC/AC	99.02.0.024.09
RC	(28...60)V DC/AC	99.02.0.060.09
RC	(110...240)V DC/AC	99.02.0.230.09
Antirremanencia*	(110...240)V AC	99.02.8.230.07

\* Potencia adicional de disipación 0.9 W

## SERIE 95

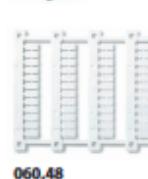
## Relación de zócalos para relés serie 40



## SERIE 40



Homologaciones (según los tipos):  
**CE** **UKCA** **EAC** **cULus**



060.48

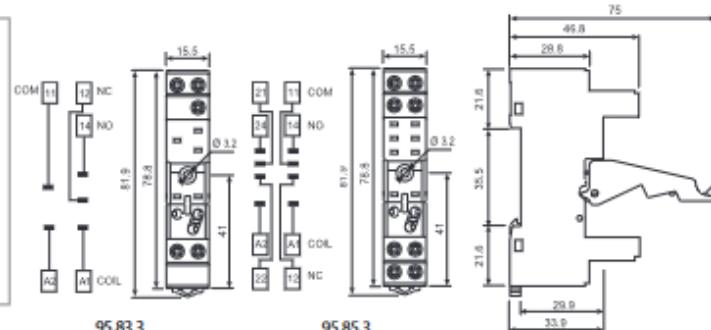
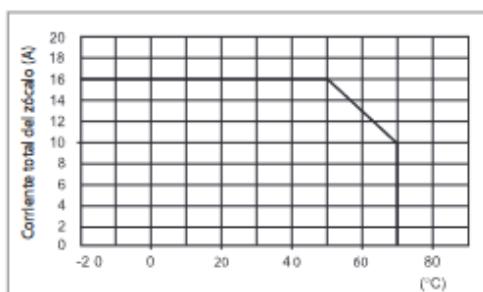
Zócalo con bornes de jaula montaje en panel o carril de 35 mm	95.83.3 (azul)	95.83.30 (negro)	95.85.3 (azul)	95.85.30 (negro)
Tipo de relé	40.31		40.51, 40.52, 40.61, 40.62	

## Accesorios

Brida de retención metálica	095.71			
Palanca de retención y extracción plástica (suministrada con el zócalo - código de embalaje SPA)	095.91.3	095.91.30	095.91.3	095.91.30
Puente de 8 terminales	095.08	095.08.0	095.08	095.08.0
Etiqueta de identificación		095.00.4		
Módulos (ver tabla abajo)		99.80		
Soporte para etiquetas de identificación		097.00		
Juego de etiquetas de identificación para palanca de retención y extracción plástica 095.91.3, 48 etiquetas 6 x 12 mm, para impresoras de transferencia térmica CEMBRE		060.48		
<b>Características generales</b>				
Valor nominal	10 A - 250 V*			
Rigidez dielectrica entre bobina y contactos	(1.2/50 µs)	6 kV	2 kV	
Categoría de protección		IP 20		
Temperatura ambiente	°C	-40...+70 (ver diagrama L95)		
Par de apriete	Nm	0.5		
Longitud de pelado del cable	mm	7		
Capacidad de conexión de los bornes para zócalos 95.83.3 y 95.85.3		hilo rígido	hilo flexible	
mm <sup>2</sup>	1 x 6 / 2 x 2.5	1 x 4 / 2 x 2.5		
AWG	1 x 10 / 2 x 14	1 x 12 / 2 x 14		

\* Con corrientes > 10 A, los bornes de los contactos deben conectarse en paralelo (21 con 11, 24 con 14, 22 con 12).  
 Con relés 40.51 utilizar los bornes 21, 12 y 14.

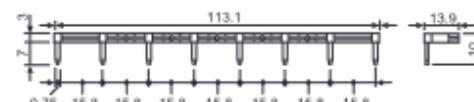
## L 95 - Corriente total del zócalo en función de la temperatura ambiente



Homologaciones (según los tipos):  
**EAC**

\* Los módulos de color negro están disponibles bajo pedido.  
 El LED verde es estándar.  
 El LED rojo está disponible bajo pedido.

Puente de 8 terminales para zócalos 95.83.3 y 95.85.3	095.08 (azul)	095.08.0 (negro)
Valor nominal 10 A - 250 V		



Homologaciones (según los tipos):  
**EAC**

\* Los módulos de color negro están disponibles bajo pedido.  
 El LED verde es estándar.  
 El LED rojo está disponible bajo pedido.

	Azul*
Diodo (+A1, polaridad estándar)	(6...220)V DC 99.80.3.000.00
LED	(6...24)V DC/AC 99.80.0.024.59
LED	(28...60)V DC/AC 99.80.0.060.59
LED	(110...240)V DC/AC 99.80.0.230.59
LED + Diodo (+A1, polaridad estándar)	(6...24)V DC 99.80.9.024.99
LED + Diodo (+A1, polaridad estándar)	(28...60)V DC 99.80.9.060.99
LED + Diodo (+A1, polaridad estándar)	(110...220)V DC 99.80.9.220.99
LED + Varistor	(6...24)V DC/AC 99.80.0.024.98
LED + Varistor	(28...60)V DC/AC 99.80.0.060.98
LED + Varistor	(110...240)V DC/AC 99.80.0.230.98
RC	(6...24)V DC/AC 99.80.0.024.09
RC	(28...60)V DC/AC 99.80.0.060.09
RC	(110...240)V DC/AC 99.80.0.230.09
Antirremanencia*	(110...240)V AC 99.80.8.230.07

\* Potencia adicional de dissipación 0.9 W

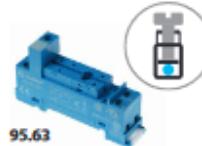


## SERIE 95

## Relación de zócalos para relés serie 40



## SERIE 40



**95.63**  
Homologaciones  
(según los tipos):



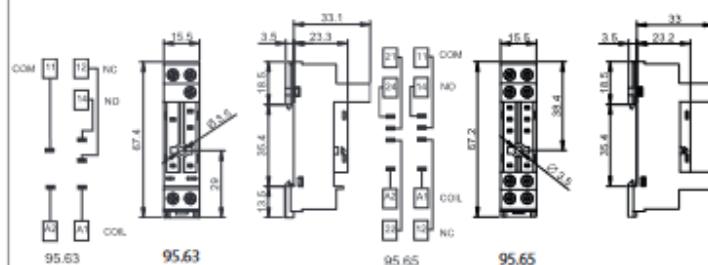
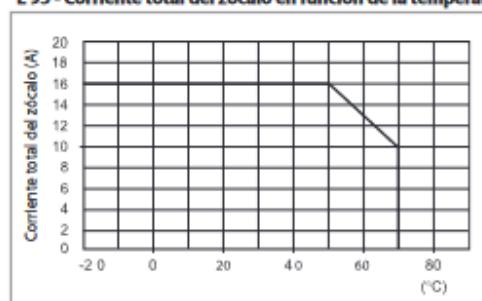
**95.65**  
Homologaciones  
(según los tipos):



Zócalo con bornes de jaula montaje en panel o cartíl de 35 mm	<b>95.63</b>	<b>95.65</b>
Tipo de relé	40.31	40.51, 40.52, 40.61, 40.62
<b>Accesorios</b>		
Brida de retención metálica		095.71
Puente de 8 terminales	095.08	095.08
Módulos (ver tabla abajo)	99.01	—
<b>Características generales</b>		
Valor nominal	10 A - 250 V*	
Rigidez dieléctrica entre bobina y contactos	(1.2/50 µs)	6 kV
Categoría de protección		IP 20
Temperatura ambiente	°C	-40...+70 (ver diagrama L95)
Par de apriete	Nm	0.5
Longitud de pelado del cable	mm	7
Capacidad de conexión de los bornes para zócalos 95.63 y 95.65	mm²	hilo rígido
	1 x 6 / 2 x 2.5	hilo flexible
	AWG 1 x 10 / 2 x 14	1 x 4 / 2 x 2.5
		1 x 12 / 2 x 14

\* Con corrientes > 10 A, los bornes de los contactos deben conectarse en paralelo (21 con 11, 24 con 14, 22 con 12).  
Con relés 40.51 utilizar los bornes 21, 12 y 14.

## L 95 - Corriente total del zócalo en función de la temperatura ambiente

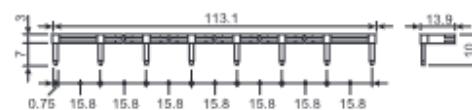


**095.08**  
Puente de 8 terminales para zócalos 95.63 y 95.65

Valor nominal

**095.08 (azul)**

10 A - 250 V



**99.01**  
Homologaciones  
(según los tipos):



\* Los módulos de color negro están disponibles bajo pedido.

El LED verde es estándar.  
El LED rojo está disponible bajo pedido.

## Módulos de señalización y protección CEM tipo 99.01 para zócalo 95.63

	Azul*
Diodo (+A1, polaridad estándar)	(6...220)V DC 99.01.3.000.00
Diodo (+A2, polaridad no estándar)	(6...220)V DC 99.01.2.000.00
LED	(6...24)V DC/AC 99.01.0.024.59
LED	(28...60)V DC/AC 99.01.0.060.59
LED	(110...240)V DC/AC 99.01.0.230.59
LED + Diodo (+A1, polaridad estándar)	(6...24)V DC 99.01.9.024.99
LED + Diodo (+A1, polaridad estándar)	(28...60)V DC 99.01.9.060.99
LED + Diodo (+A1, polaridad estándar)	(110...220)V DC 99.01.9.220.99
LED + Diodo (+A2, polaridad no estándar)	(6...24)V DC 99.01.9.024.79
LED + Diodo (+A2, polaridad no estándar)	(28...60)V DC 99.01.9.060.79
LED + Diodo (+A2, polaridad no estándar)	(110...220)V DC 99.01.9.220.79
LED + Varistor	(6...24)V DC/AC 99.01.0.024.98
LED + Varistor	(28...60)V DC/AC 99.01.0.060.98
LED + Varistor	(110...240)V DC/AC 99.01.0.230.98
RC	(6...24)V DC/AC 99.01.0.024.09
RC	(28...60)V DC/AC 99.01.0.060.09
RC	(110...240)V DC/AC 99.01.0.230.09
Antirremanencia*	(110...240)V AC 99.01.8.230.07

\* Potencia adicional de dissipación 0.9 W

SERIE  
40

SERIE 95

Relación de zócalos para relés serie 40



A 95.13.2

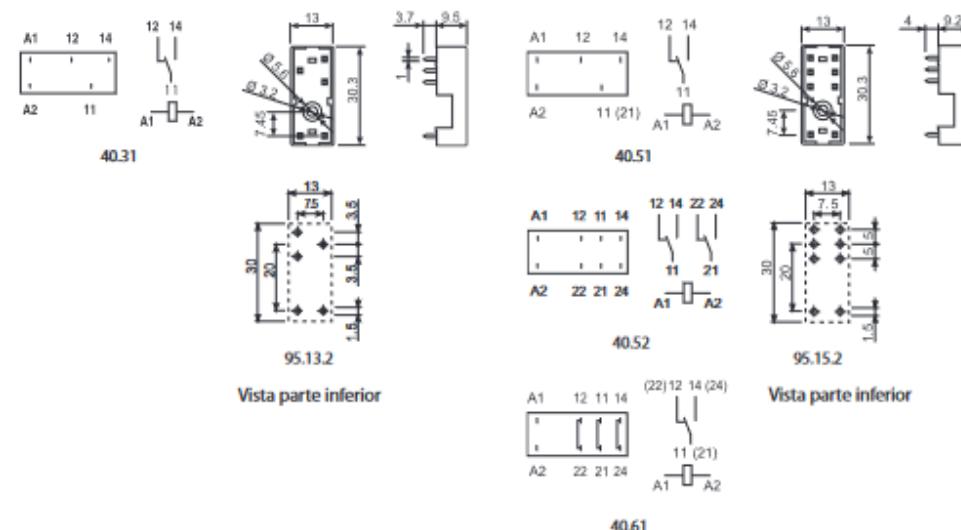


95.15.2

Homologaciones  
(según los tipos):

Zócalo para circuito impreso	95.13.2 (azul)	95.13.20 (negro)	95.15.2 (azul)	95.15.20 (negro)
Tipo de relé	40.31		40.51, 40.52, 40.61, 40.62	
Accesorios				
Palanca de retención metálica (suministrada con el zócalo - código de embalaje SMA)			095.51	
Palanca de retención plástica			095.52	
Características generales				
Valor nominal	12 A - 250 V		10 A - 250 V*	
Rigidez dielectrica entre bobina y contactos (1.2/50 µs)	6 kV			
Categoría de protección	IP 20			
Temperatura ambiente	°C -40...+70			

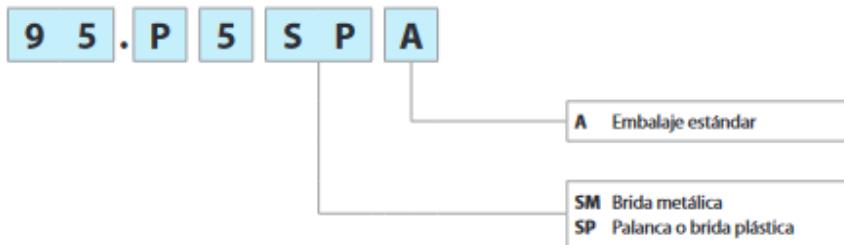
\* Con corrientes > 10 A, los bornes de los contactos deben conectarse en paralelo (21 con 11, 24 con 14, 22 con 12).  
Con relés 40.51 utilizar los bornes 21, 12 y 14.



### Código de embalaje

Identificación de la elaboración y de lasbridas a través de las últimas tres letras.

Ejemplo:



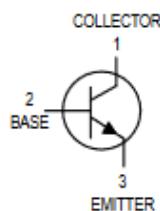
**Transistor BC547 (NPN).**

**MOTOROLA**  
SEMICONDUCTOR TECHNICAL DATA

Order this document  
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**Amplifier Transistors**  
NPN Silicon

**BC546, B  
BC547, A, B, C  
BC548, A, B, C**



CASE 29-04, STYLE 17  
TO-92 (TO-226AA)

**MAXIMUM RATINGS**

Rating	Symbol	BC 546	BC 547	BC 548	Unit
Collector-Emitter Voltage	$V_{CEO}$	65	45	30	Vdc
Collector-Base Voltage	$V_{CBO}$	80	50	30	Vdc
Emitter-Base Voltage	$V_{EBO}$		6.0		Vdc
Collector Current — Continuous	$I_C$		100		mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$		625 5.0		mW mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$		1.5 12		Watt mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{Stg}$	-55 to +150			$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\text{f},JA}$	200	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\text{f},JC}$	83.3	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted)**

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector-Emitter Breakdown Voltage ( $I_C = 1.0 \text{ mA}, I_B = 0$ )	$V_{(BR)CEO}$	65 45 30	— — —	— — —	V
Collector-Base Breakdown Voltage ( $I_C = 100 \mu\text{Adc}$ )	$V_{(BR)CBO}$	80 50 30	— — —	— — —	V
Emitter-Base Breakdown Voltage ( $I_E = 10 \mu\text{A}, I_C = 0$ )	$V_{(BR)EBO}$	6.0 6.0 6.0	— — —	— — —	V
Collector Cutoff Current ( $V_{CE} = 70 \text{ V}, V_{BE} = 0$ ) ( $V_{CE} = 50 \text{ V}, V_{BE} = 0$ ) ( $V_{CE} = 35 \text{ V}, V_{BE} = 0$ ) ( $V_{CE} = 30 \text{ V}, T_A = 125^\circ\text{C}$ )	$I_{CES}$	— — — —	0.2 0.2 0.2 —	15 15 15 4.0	nA $\mu\text{A}$

REV 1

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 **MOTOROLA**

**BC546, B BC547, A, B, C BC548, A, B, C**ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>ON CHARACTERISTICS</b>					
DC Current Gain ( $I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$ )	$h_{FE}$	—	90	—	—
		—	150	—	—
		—	270	—	—
( $I_C = 2.0 \text{ mA}, V_{CE} = 5.0 \text{ V}$ )	BC546	110	—	450	
	BC547	110	—	800	
	BC548	110	—	800	
	BC547A/548A	110	180	220	
	BC546B/547B/548B	200	290	450	
	BC547C/BC548C	420	520	800	
( $I_C = 100 \text{ mA}, V_{CE} = 5.0 \text{ V}$ )	BC547A/548A	—	120	—	
	BC546B/547B/548B	—	180	—	
	BC548C	—	300	—	
Collector-Emitter Saturation Voltage ( $I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$ )	$V_{CE(\text{sat})}$	—	0.09	0.25	V
( $I_C = 100 \text{ mA}, I_B = 5.0 \text{ mA}$ )		—	0.2	0.6	
( $I_C = 10 \text{ mA}, I_B = \text{See Note 1}$ )		—	0.3	0.6	
Base-Emitter Saturation Voltage ( $I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$ )	$V_{BE(\text{sat})}$	—	0.7	—	V
Base-Emitter On Voltage ( $I_C = 2.0 \text{ mA}, V_{CE} = 5.0 \text{ V}$ )	$V_{BE(\text{on})}$	0.55	—	0.7	V
( $I_C = 10 \text{ mA}, V_{CE} = 5.0 \text{ V}$ )		—	—	0.77	
<b>SMALL-SIGNAL CHARACTERISTICS</b>					
Current-Gain — Bandwidth Product ( $I_C = 10 \text{ mA}, V_{CE} = 5.0 \text{ V}, f = 100 \text{ MHz}$ )	$f_T$	150	300	—	MHz
BC546		150	300	—	
BC547		150	300	—	
BC548		150	300	—	
Output Capacitance ( $V_{CB} = 10 \text{ V}, I_C = 0, f = 1.0 \text{ MHz}$ )	$C_{obo}$	—	1.7	4.5	pF
Input Capacitance ( $V_{EB} = 0.5 \text{ V}, I_C = 0, f = 1.0 \text{ MHz}$ )	$C_{ibo}$	—	10	—	pF
Small-Signal Current Gain ( $I_C = 2.0 \text{ mA}, V_{CE} = 5.0 \text{ V}, f = 1.0 \text{ kHz}$ )	$h_{fe}$	125	—	500	—
BC546		125	—	900	
BC547/548		125	—	900	
BC547A/548A		125	220	260	
BC546B/547B/548B		240	330	500	
BC547C/548C		450	600	900	
Noise Figure ( $I_C = 0.2 \text{ mA}, V_{CE} = 5.0 \text{ V}, R_S = 2 \text{ k}\Omega, f = 1.0 \text{ kHz}, \Delta f = 200 \text{ Hz}$ )	NF	—	2.0	10	dB
BC546		—	2.0	10	
BC547		—	2.0	10	
BC548		—	2.0	10	

Note 1:  $I_B$  is value for which  $I_C = 11 \text{ mA}$  at  $V_{CE} = 1.0 \text{ V}$ .

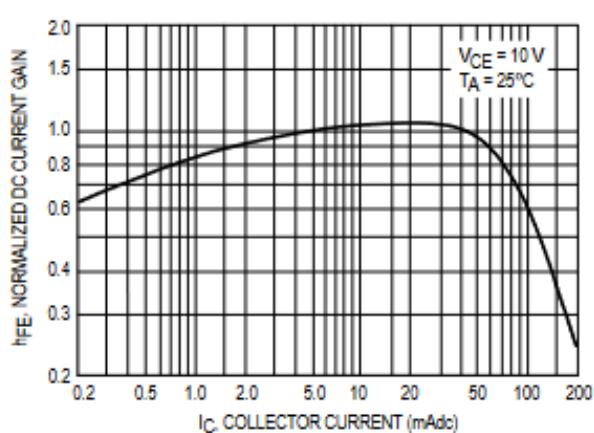


Figure 1. Normalized DC Current Gain

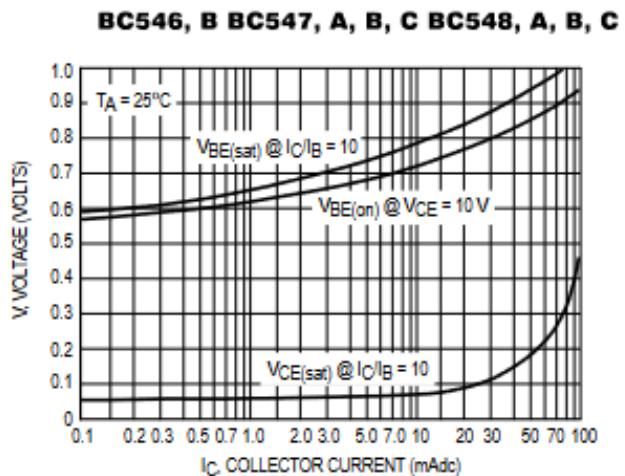


Figure 2. "Saturation" and "On" Voltages

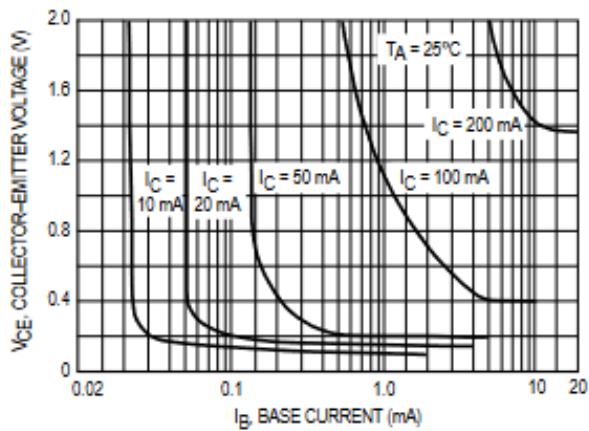


Figure 3. Collector Saturation Region

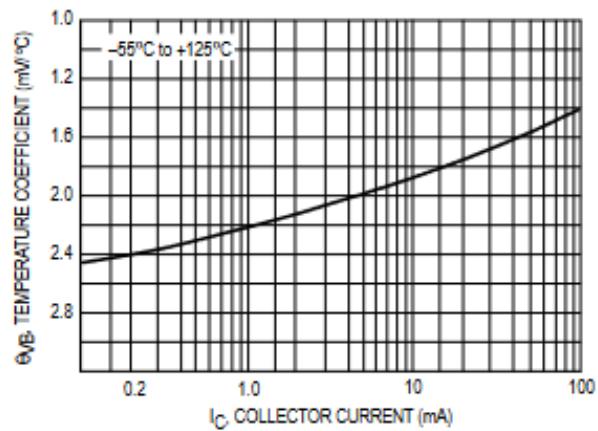


Figure 4. Base-Emitter Temperature Coefficient

### BC547/BC548

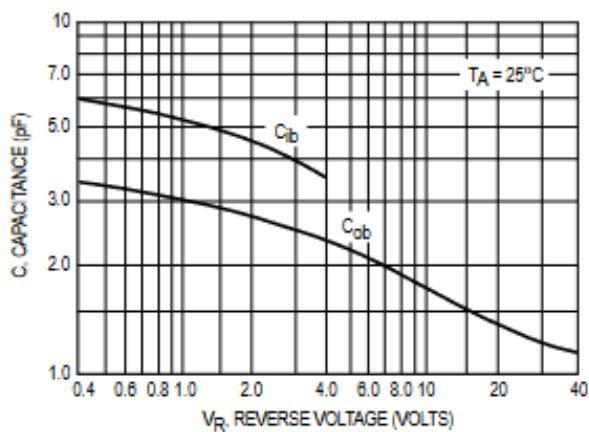


Figure 5. Capacitances

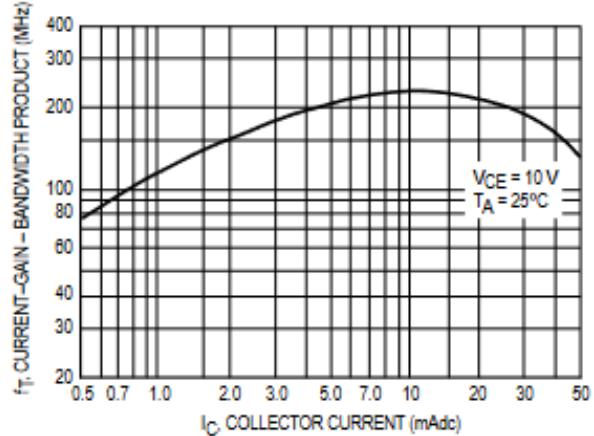
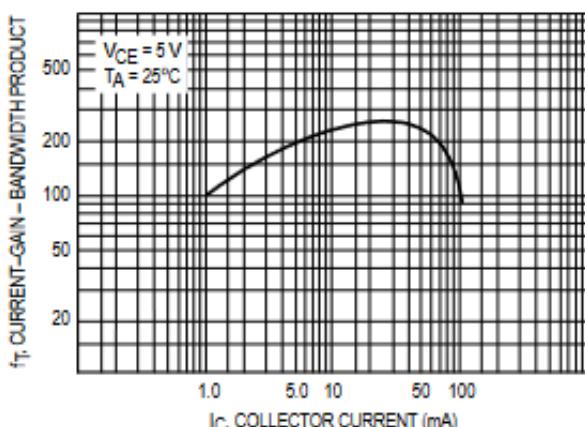
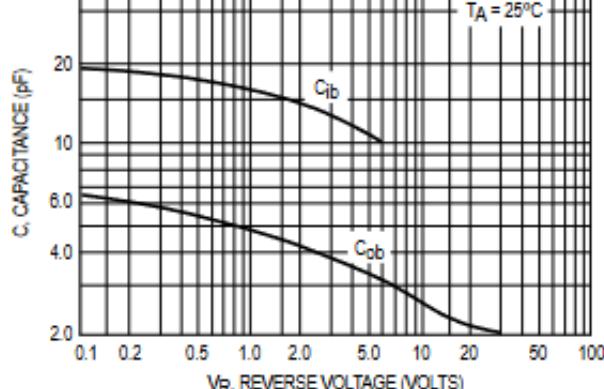
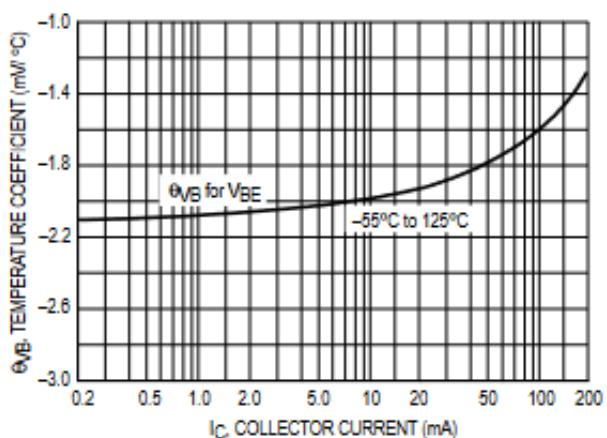
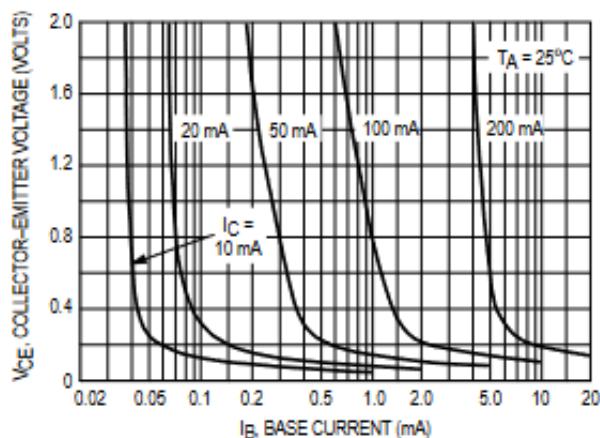
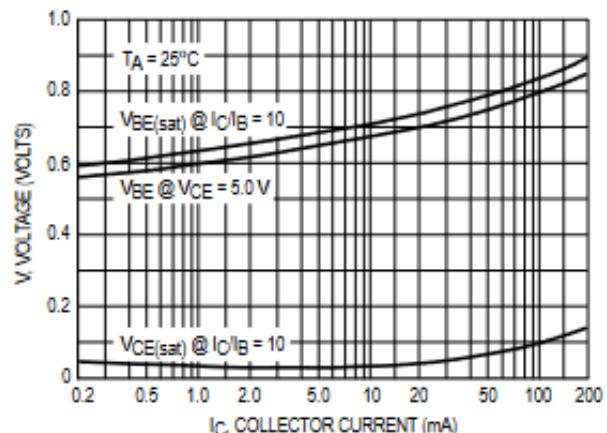
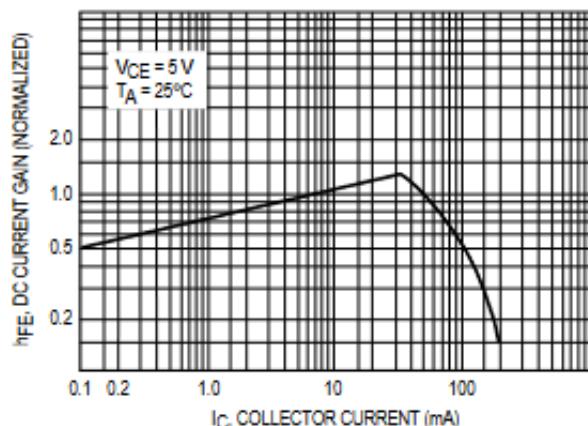


Figure 6. Current-Gain – Bandwidth Product

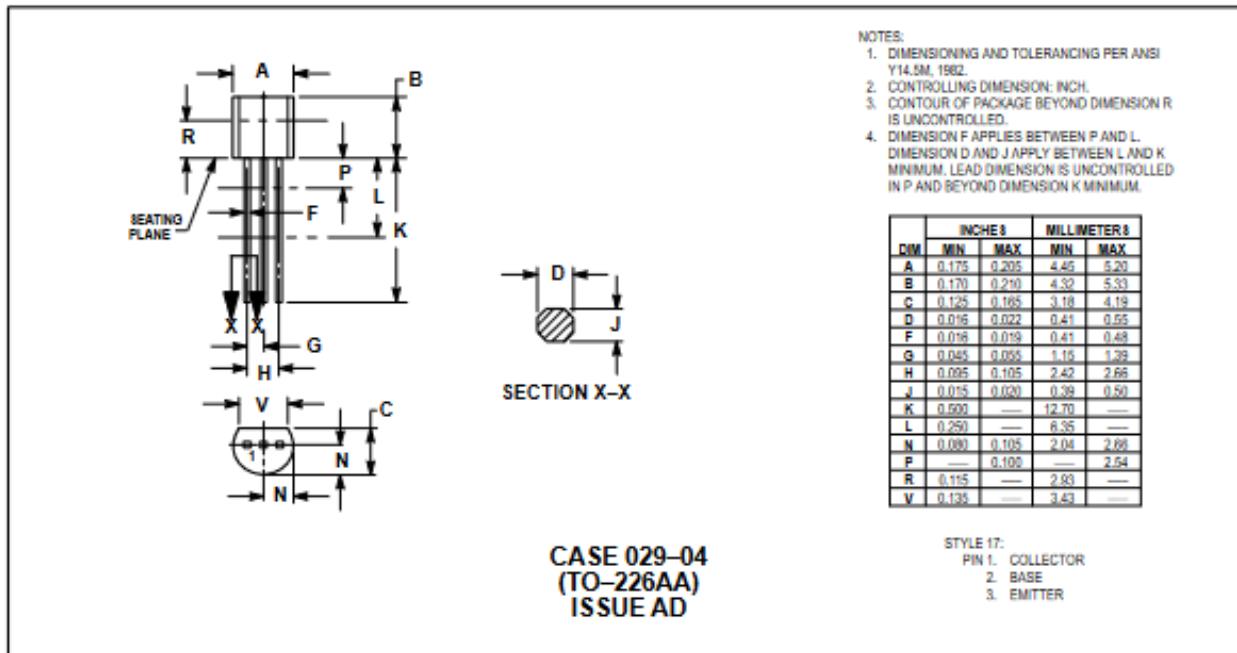
**BC546, B BC547, A, B, C BC548, A, B, C**

**BC547/BC548**



**BC546, B BC547, A, B, C BC548, A, B, C**

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**BC546, B BC547, A, B, C BC548, A, B, C**

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BC546/D



**Transistor BD135 (NPN).**

**MOTOROLA**  
SEMICONDUCTOR TECHNICAL DATA

Order this document  
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## Plastic Medium Power Silicon NPN Transistor

... designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain —  $h_{FE} = 40$  (Min) @  $I_C = 0.15$  Adc
- BD 135, 137, 139 are complementary with BD 136, 138, 140

**BD135  
BD137  
BD139**

1.5 AMPERE  
POWER TRANSISTORS  
NPN SILICON  
45, 60, 80 VOLTS  
10 WATTS



CASE 77-08  
TO-225AA TYPE

### MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	BD 135 BD 137 BD 139	45 60 80	Vdc
Collector-Base Voltage	$V_{CBO}$	BD 135 BD 137 BD 139	45 60 100	Vdc
Emitter-Base Voltage	$V_{EBO}$		5	Vdc
Collector Current	$I_C$		1.5	Adc
Base Current	$I_B$		0.5	Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$		1.25 10	Watts mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$		12.5 100	Watt mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{Stg}$		-55 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	10	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	100	$^\circ\text{C/W}$

**BD135 BD137 BD139**ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector-Emitter Sustaining Voltage* ( $I_C = 0.03 \text{ Adc}$ , $I_B = 0$ )	$BV_{CEO}^*$	BD 135 BD 137 BD 139	45 60 80	— — —	Vdc
Collector Cutoff Current ( $V_{CB} = 30 \text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 30 \text{ Vdc}$ , $I_E = 0$ , $T_C = 125^\circ\text{C}$ )	$I_{CBO}$		— —	0.1 10	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$		—	10	$\mu\text{Adc}$
DC Current Gain ( $I_C = 0.005 \text{ A}$ , $V_{CE} = 2 \text{ V}$ ) ( $I_C = 0.15 \text{ A}$ , $V_{CE} = 2 \text{ V}$ ) ( $I_C = 0.5 \text{ A}$ , $V_{CE} = 2 \text{ V}$ )	$h_{FE}^*$		25 40 25	— 250 —	—
Collector-Emitter Saturation Voltage* ( $I_C = 0.5 \text{ Adc}$ , $I_B = 0.05 \text{ Adc}$ )	$V_{CE(sat)}^*$		—	0.5	Vdc
Base-Emitter On Voltage* ( $I_C = 0.5 \text{ Adc}$ , $V_{CE} = 2.0 \text{ Vdc}$ )	$V_{BE(on)}^*$		—	1	Vdc

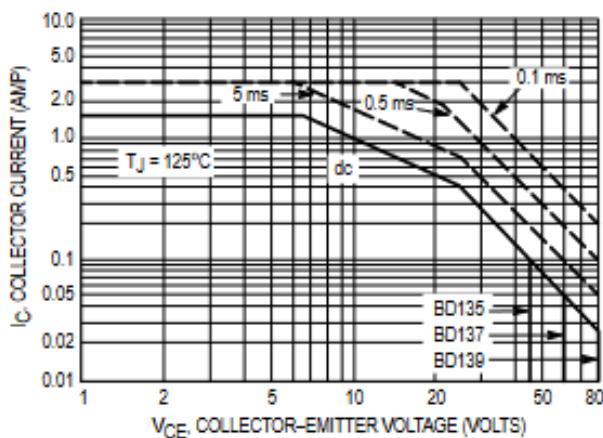
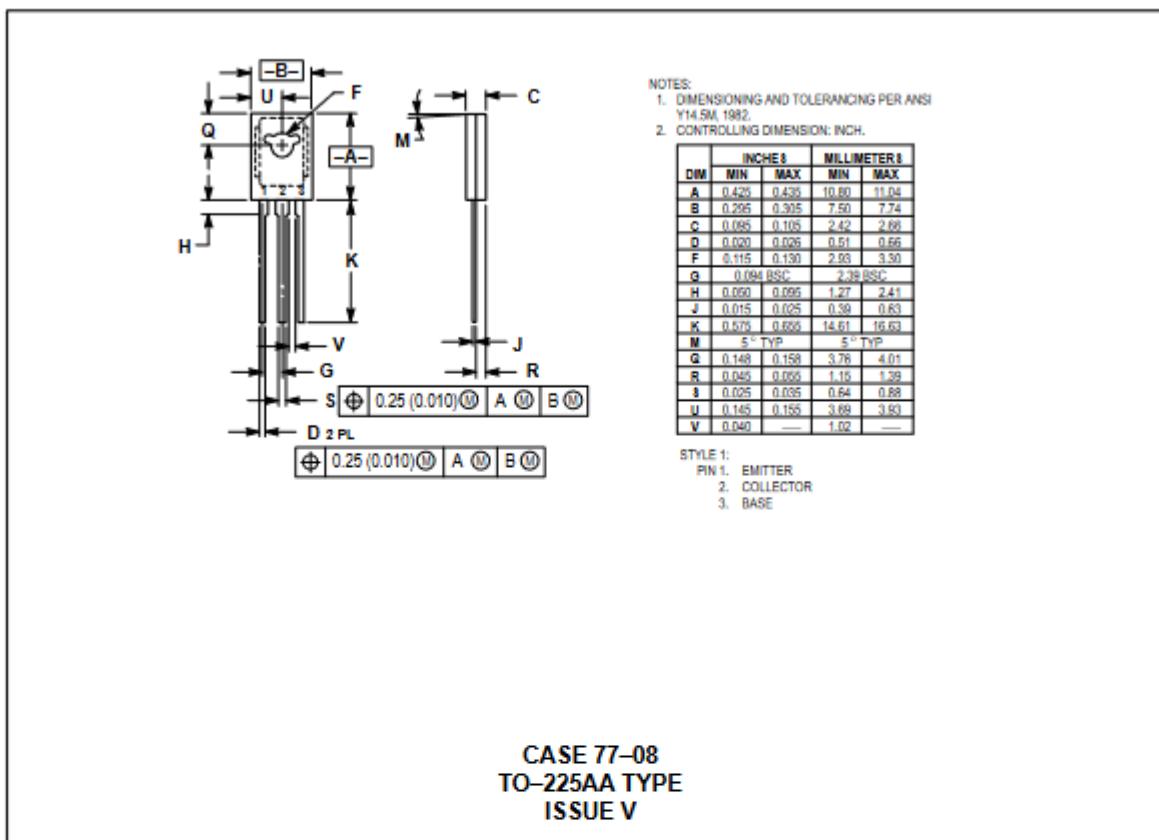
\* Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

Figure 1. Active-Region Safe Operating Area

**BD135 BD137 BD139**

**PACKAGE DIMENSIONS**



**BD135 BD137 BD139**

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◊

BD135/D



## PIC16F84A.



# PIC16F84A

## 18-pin Enhanced Flash/EEPROM 8-Bit Microcontroller

### Devices Included in this Data Sheet:

- PIC16F84A
- Extended voltage range device available (PIC16LF84A)

### High Performance RISC CPU Features:

- Only 35 single word instructions to learn
- All instructions single cycle except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input  
DC - 200 ns instruction cycle
- 1024 words of program memory
- 68 bytes of data RAM
- 64 bytes of data EEPROM
- 14-bit wide instruction words
- 8-bit wide data bytes
- 15 special function hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources:
  - External RB0/INT pin
  - TMR0 timer overflow
  - PORTB<7:4> interrupt on change
  - Data EEPROM write complete

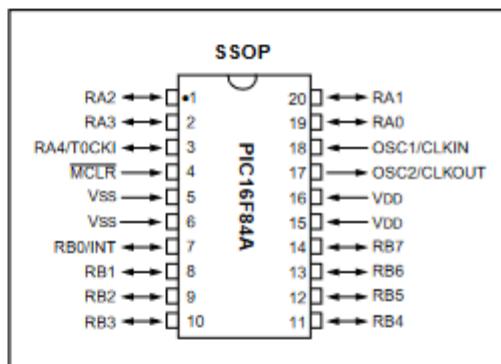
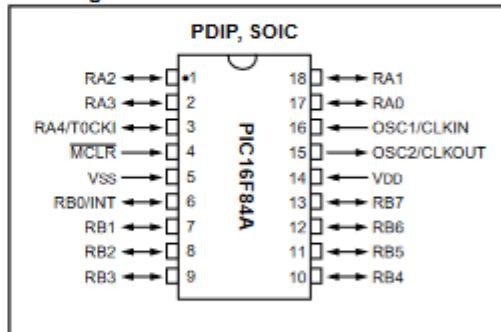
### Peripheral Features:

- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - 25 mA sink max. per pin
  - 25 mA source max. per pin
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler

### Special Microcontroller Features:

- 1000 erase/write cycles Enhanced Flash program memory
- 1,000,000 typical erase/write cycles EEPROM data memory
- EEPROM Data Retention > 40 years
- In-Circuit Serial Programming (ICSP™) - via two pins
- Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Code-protection
- Power saving SLEEP mode
- Selectable oscillator options

### Pin Diagrams



### CMOS Enhanced Flash/EERPOM Technology:

- Low-power, high-speed technology
- Fully static design
- Wide operating voltage range:
  - Commercial: 2.0V to 5.5V
  - Industrial: 2.0V to 5.5V
- Low power consumption:
  - < 2 mA typical @ 5V, 4 MHz
  - 15 µA typical @ 2V, 32 kHz
  - < 0.5 µA typical standby current @ 2V

# PIC16F84A

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We appreciate your assistance in making this a better document.

# PIC16F84A

## 1.0 DEVICE OVERVIEW

This document contains device-specific information for the operation of the PIC16F84A device. Additional information may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023), which may be downloaded from the Microchip website. The Reference Manual should be considered a complementary document to this data sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

The PIC16F84A belongs to the mid-range family of the PICmicro™ microcontroller devices. A block diagram of the device is shown in Figure 1-1.

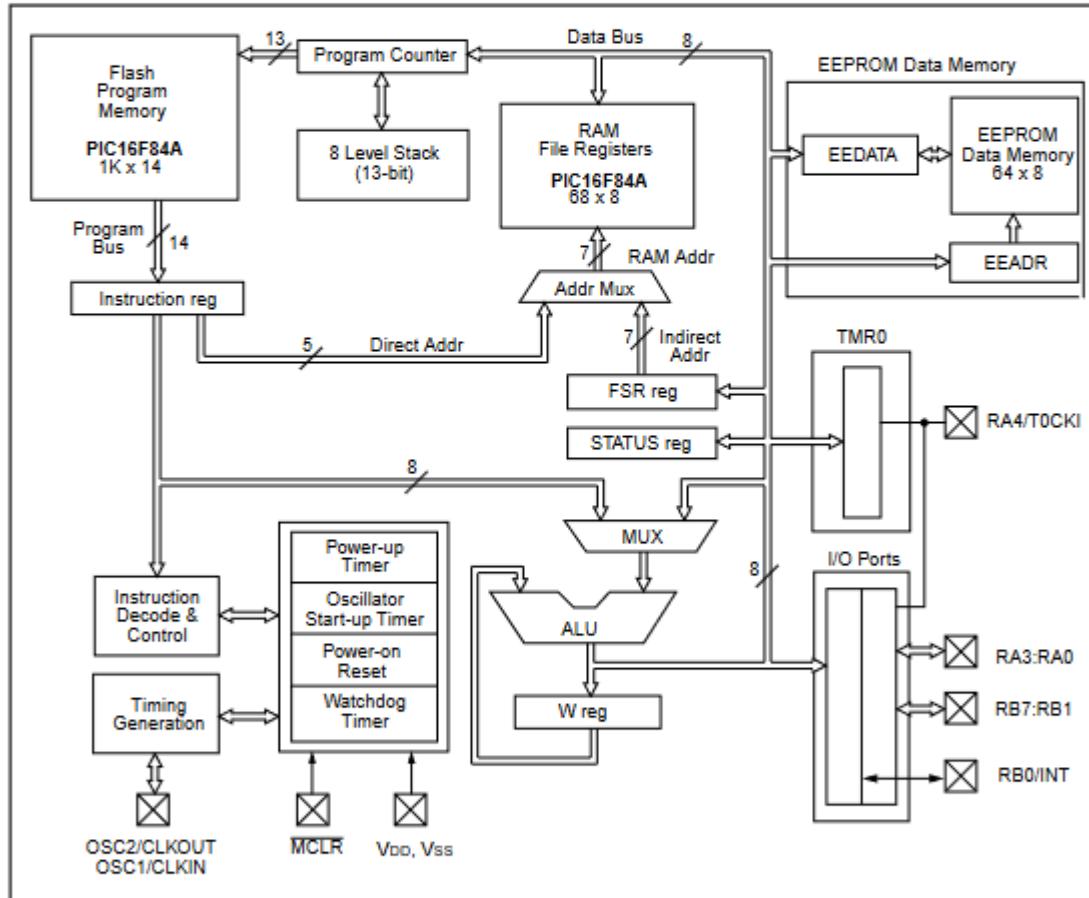
The program memory contains 1K words, which translates to 1024 instructions, since each 14-bit program memory word is the same width as each device instruction. The data memory (RAM) contains 68 bytes. Data EEPROM is 64 bytes.

There are also 13 I/O pins that are user-configured on a pin-to-pin basis. Some pins are multiplexed with other device functions. These functions include:

- External interrupt
- Change on PORTB interrupt
- Timer0 clock input

Table 1-1 details the pinout of the device with descriptions and details for each pin.

FIGURE 1-1: PIC16F84A BLOCK DIAGRAM



# PIC16F84A

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TABLE 1-1 PIC16F84A PINOUT DESCRIPTION

Pin Name	DIP No.	SOIC No.	SSOP No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	16	18	I	ST/CMOS <sup>(3)</sup>	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	19	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR	4	4	4	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0	17	17	19	I/O	TTL	
RA1	18	18	20	I/O	TTL	
RA2	1	1	1	I/O	TTL	
RA3	2	2	2	I/O	TTL	
RA4/T0CKI	3	3	3	I/O	ST	Can also be selected to be the clock input to the TMR0 timer/counter. Output is open drain type.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	7	I/O	TTL/ST <sup>(1)</sup>	RB0/INT can also be selected as an external interrupt pin.
RB1	7	7	8	I/O	TTL	
RB2	8	8	9	I/O	TTL	
RB3	9	9	10	I/O	TTL	
RB4	10	10	11	I/O	TTL	Interrupt on change pin.
RB5	11	11	12	I/O	TTL	Interrupt on change pin.
RB6	12	12	13	I/O	TTL/ST <sup>(2)</sup>	Interrupt on change pin. Serial programming clock.
RB7	13	13	14	I/O	TTL/ST <sup>(2)</sup>	Interrupt on change pin. Serial programming data.
V <sub>ss</sub>	5	5	5,6	P	—	Ground reference for logic and I/O pins.
V <sub>dd</sub>	14	14	15,16	P	—	Positive supply for logic and I/O pins.

Legend: I = input

O = output

I/O = Input/Output

P = power

— = Not used

TTL

= TTL input

ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

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## 2.0 MEMORY ORGANIZATION

There are two memory blocks in the PIC16F84A. These are the program memory and the data memory. Each block has its own bus, so that access to each block can occur during the same oscillator cycle.

The data memory can further be broken down into the general purpose RAM and the Special Function Registers (SFRs). The operation of the SFRs that control the "core" are described here. The SFRs used to control the peripheral modules are described in the section discussing each individual peripheral module.

The data memory area also contains the data EEPROM memory. This memory is not directly mapped into the data memory, but is indirectly mapped. That is, an indirect address pointer specifies the address of the data EEPROM memory to read/write. The 64 bytes of data EEPROM memory have the address range 0h-3Fh. More details on the EEPROM memory can be found in Section 5.0.

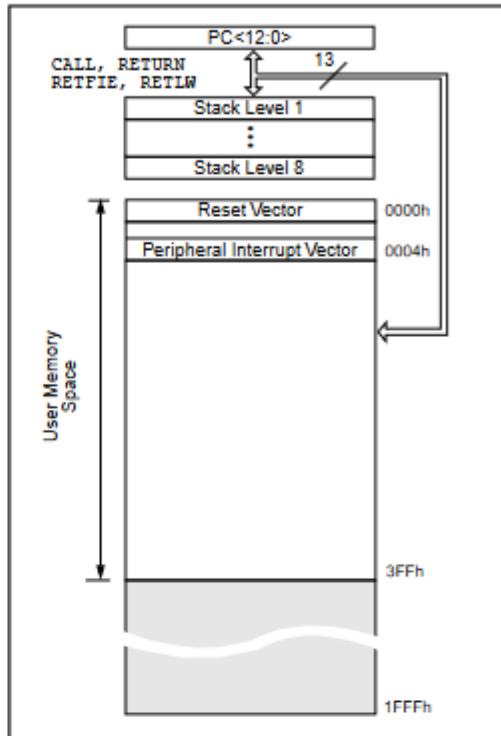
Additional information on device memory may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023).

### 2.1 Program Memory Organization

The PIC16FXX has a 13-bit program counter capable of addressing an 8K x 14 program memory space. For the PIC16F84A, the first 1K x 14 (0000h-03FFh) are physically implemented (Figure 2-1). Accessing a location above the physically implemented address will cause a wraparound. For example, for locations 20h, 420h, 820h, C20h, 1020h, 1420h, 1820h, and 1C20h will be the same instruction.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK - PIC16F84A



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## 2.2 Data Memory Organization

The data memory is partitioned into two areas. The first is the Special Function Registers (SFR) area, while the second is the General Purpose Registers (GPR) area. The SFRs control the operation of the device.

Portions of data memory are banked. This is for both the SFR area and the GPR area. The GPR area is banked to allow greater than 116 bytes of general purpose RAM. The banked areas of the SFR are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the STATUS Register. Figure 2-1 shows the data memory map organization. Instructions `MOVWF` and `MOVE` can move values from the W register to any location in the register file ("F"), and vice-versa.

The entire data memory can be accessed either directly using the absolute address of each register file or indirectly through the File Select Register (FSR) (Section 2.4). Indirect addressing uses the present value of the RP0 bit for access into the banked areas of data memory.

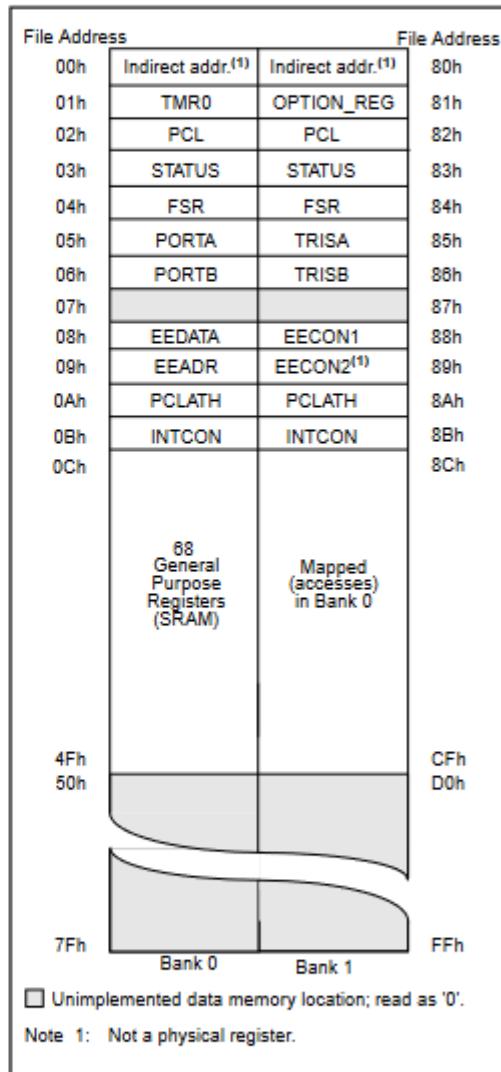
Data memory is partitioned into two banks which contain the general purpose registers and the special function registers. Bank 0 is selected by clearing the RP0 bit (`STATUS<5>`). Setting the RP0 bit selects Bank 1. Each Bank extends up to 7Fh (128 bytes). The first twelve locations of each Bank are reserved for the Special Function Registers. The remainder are General Purpose Registers implemented as static RAM.

### 2.2.1 GENERAL PURPOSE REGISTER FILE

Each General Purpose Register (GPR) is 8 bits wide and is accessed either directly or indirectly through the FSR (Section 2.4).

The GPR addresses in bank 1 are mapped to addresses in bank 0. As an example, addressing location 0Ch or 8Ch will access the same GPR.

**FIGURE 2-1: REGISTER FILE MAP - PIC16F84A**



**PIC16F84A****2.2.2 SPECIAL FUNCTION REGISTERS**

The Special Function Registers (Figure 2-1 and Table 2-1) are used by the CPU and Peripheral functions to control the device operation. These registers are static RAM.

The special function registers can be classified into two sets, core and peripheral. Those associated with the core functions are described in this section. Those related to the operation of the peripheral features are described in the section for that specific feature.

**TABLE 2-1 REGISTER FILE SUMMARY**

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note3)				
<b>Bank 0</b>															
00h	INDF	Uses contents of FSR to address data memory (not a physical register)							----	----	----				
01h	TMR0	8-bit real-time clock/counter							xxxx xxxx	uuuu uuuu	uuuu uuuu				
02h	PCL	Low order 8 bits of the Program Counter (PC)							0000 0000	0000 0000	0000 0000				
03h	STATUS <sup>(2)</sup>	IRP	RP1	RP0	TO	PD	Z	DC	C	0001 1xxx	000q quuu				
04h	FSR	Indirect data memory address pointer 0							xxxx xxxx	uuuu uuuu	uuuu uuuu				
05h	PORTA <sup>(4)</sup>	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	---u uuuu				
06h	PORTB <sup>(5)</sup>	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	uuuu uuuu				
07h		Unimplemented location, read as '0'							----	----	----				
08h	EEDATA	EEPROM data register							xxxx xxxx	uuuu uuuu	uuuu uuuu				
09h	EEADR	EEPROM address register							xxxx xxxx	uuuu uuuu	uuuu uuuu				
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC <sup>(1)</sup>				---0 0000	---0 0000	---0 0000				
0Bh	INTCON	GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u				
<b>Bank 1</b>															
80h	INDF	Uses contents of FSR to address data memory (not a physical register)							----	----	----				
81h	OPTION_REG	RBPU	INTE0G	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111				
82h	PCL	Low order 8 bits of Program Counter (PC)							0000 0000	0000 0000	0000 0000				
83h	STATUS <sup>(2)</sup>	IRP	RP1	RP0	TO	PD	Z	DC	C	0001 1xxx	000q quuu				
84h	FSR	Indirect data memory address pointer 0							xxxx xxxx	uuuu uuuu	uuuu uuuu				
85h	TRISA	—	—	—	PORTA data direction register				---1 1111	---1 1111	---1 1111				
86h	TRISB	PORTB data direction register							1111 1111	1111 1111	1111 1111				
87h		Unimplemented location, read as '0'							----	----	----				
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	---0 q000				
89h	EECON2	EEPROM control register 2 (not a physical register)							----	----	----				
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC <sup>(1)</sup>				---0 0000	---0 0000	---0 0000				
0Bh	INTCON	GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u				

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends on condition.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a slave register for PC<12:8>. The contents of PCLATH can be transferred to the upper byte of the program counter, but the contents of PC<12:8> is never transferred to PCLATH.

2: The TO and PD status bits in the STATUS register are not affected by a MCLR reset.

3: Other (non power-up) resets include: external reset through MCLR and the Watchdog Timer Reset.

4: On any device reset, these pins are configured as inputs.

5: This is the value that will be in the port output latch.

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### 2.2.2.1 STATUS REGISTER

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bit for data memory.

As with any register, the STATUS register can be the destination for any instruction. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CIRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as `000uuuu` (where `u` = unchanged).

Only the BCF, BSE, SWAPF and MOVWF instructions should be used to alter the STATUS register (Table 7-2) because these instructions do not affect any status bit.

**Note 1:** The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16F84A and should be programmed as cleared. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

**Note 2:** The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and SUBWF instructions for examples.

**Note 3:** When the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. The specified bit(s) will be updated according to device logic.

FIGURE 2-1: STATUS REGISTER (ADDRESS 03h, 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	TO	PD	Z	DC	C
bit7							bit0
							R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset

bit 7: **IRP:** Register Bank Select bit (used for indirect addressing)  
The IRP bit is not used by the PIC16F84A. IRP should be maintained clear.

bit 6-5: **RP1:RP0:** Register Bank Select bits (used for direct addressing)  
00 = Bank 0 (00h - 7Fh)  
01 = Bank 1 (80h - FFh)  
Each bank is 128 bytes. Only bit RP0 is used by the PIC16F84A. RP1 should be maintained clear.

bit 4: **TO:** Time-out bit  
1 = After power-up, CLRWDI instruction, or SLEEP instruction  
0 = A WDT time-out occurred

bit 3: **PD:** Power-down bit  
1 = After power-up or by the CLRWDI instruction  
0 = By execution of the SLEEP instruction

bit 2: **Z:** Zero bit  
1 = The result of an arithmetic or logic operation is zero  
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC:** Digit carry/borrow bit (for ADDWF and ADDIW instructions) (For borrow the polarity is reversed)  
1 = A carry-out from the 4th low order bit of the result occurred  
0 = No carry-out from the 4th low order bit of the result

bit 0: **C:** Carry/borrow bit (for ADDWF and ADDIW instructions)  
1 = A carry-out from the most significant bit of the result occurred  
0 = No carry-out from the most significant bit of the result occurred  
**Note:** For borrow the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRE, RLW) instructions, this bit is loaded with either the high or low order bit of the source register.

**PIC16F84A**

## 2.2.2.2 OPTION\_REG REGISTER

The OPTION\_REG register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external INT interrupt, TMR0, and the weak pull-ups on PORTB.

**Note:** When the prescaler is assigned to the WDT (PSA = '1'), TMR0 has a 1:1 prescaler assignment.

FIGURE 2-1: OPTION\_REG REGISTER (ADDRESS 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1																											
RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0																											
bit7							bit0																											
							<div style="border: 1px solid black; padding: 5px;">           R = Readable bit            W = Writable bit            U = Unimplemented bit,            read as '0'            - n = Value at POR reset         </div>																											
bit 7: <b>RBPU</b> : PORTB Pull-up Enable bit 1 = PORTB pull-ups are disabled 0 = PORTB pull-ups are enabled (by individual port latch values)																																		
bit 6: <b>INTEDG</b> : Interrupt Edge Select bit 1 = Interrupt on rising edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin																																		
bit 5: <b>T0CS</b> : TMR0 Clock Source Select bit 1 = Transition on RA4/T0CKI pin 0 = Internal instruction cycle clock (CLKOUT)																																		
bit 4: <b>T0SE</b> : TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on RA4/T0CKI pin 0 = Increment on low-to-high transition on RA4/T0CKI pin																																		
bit 3: <b>PSA</b> : Prescaler Assignment bit 1 = Prescaler assigned to the WDT 0 = Prescaler assigned to TMR0																																		
bit 2-0: <b>PS2:PS0</b> : Prescaler Rate Select bits																																		
<table border="1"> <thead> <tr> <th>Bit Value</th> <th>TMR0 Rate</th> <th>WDT Rate</th> </tr> </thead> <tbody> <tr><td>000</td><td>1:2</td><td>1:1</td></tr> <tr><td>001</td><td>1:4</td><td>1:2</td></tr> <tr><td>010</td><td>1:8</td><td>1:4</td></tr> <tr><td>011</td><td>1:16</td><td>1:8</td></tr> <tr><td>100</td><td>1:32</td><td>1:16</td></tr> <tr><td>101</td><td>1:64</td><td>1:32</td></tr> <tr><td>110</td><td>1:128</td><td>1:64</td></tr> <tr><td>111</td><td>1:256</td><td>1:128</td></tr> </tbody> </table>								Bit Value	TMR0 Rate	WDT Rate	000	1:2	1:1	001	1:4	1:2	010	1:8	1:4	011	1:16	1:8	100	1:32	1:16	101	1:64	1:32	110	1:128	1:64	111	1:256	1:128
Bit Value	TMR0 Rate	WDT Rate																																
000	1:2	1:1																																
001	1:4	1:2																																
010	1:8	1:4																																
011	1:16	1:8																																
100	1:32	1:16																																
101	1:64	1:32																																
110	1:128	1:64																																
111	1:256	1:128																																

## PIC16F84A

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### 2.2.2.3 INTCON REGISTER

The INTCON register is a readable and writable register which contains the various enable bits for all interrupt sources.

**Note:** Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 2-1: INTCON REGISTER (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x	
GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	
bit7							bit0	
							<p>R = Readable bit          W = Writable bit          U = Unimplemented bit,              read as '0'          -n = Value at POR reset</p>	
bit 7:	GIE: Global Interrupt Enable bit 1 = Enables all un-masked interrupts 0 = Disables all interrupts  Note: For the operation of the interrupt structure, please refer to Section 4.							
bit 6:	EEIE: EE Write Complete Interrupt Enable bit 1 = Enables the EE write complete interrupt 0 = Disables the EE write complete interrupt							
bit 5:	T0IE: TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 interrupt 0 = Disables the TMR0 interrupt							
bit 4:	INTE: RB0/INT Interrupt Enable bit 1 = Enables the RB0/INT interrupt 0 = Disables the RB0/INT interrupt							
bit 3:	RBIE: RB Port Change Interrupt Enable bit 1 = Enables the RB port change interrupt 0 = Disables the RB port change interrupt							
bit 2:	T0IF: TMR0 Overflow Interrupt Flag bit 1 = TMR0 has overflowed (must be cleared in software) 0 = TMR0 did not overflow							
bit 1:	INTF: RB0/INT Interrupt Flag bit 1 = The RB0/INT interrupt occurred 0 = The RB0/INT interrupt did not occur							
bit 0:	RBIF: RB Port Change Interrupt Flag bit 1 = When at least one of the RB7:RB4 pins changed state (must be cleared in software) 0 = None of the RB7:RB4 pins have changed state							

# PIC16F84A

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## 2.3 PCL and PCLATH

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 13 bits wide. The low byte is called the PCL register. This register is readable and writable. The high byte is called the PCH register. This register contains the PC<12:8> bits and is not directly readable or writable. All updates to the PCH register go through the PCLATH register.

### 2.3.1 STACK

The stack allows a combination of up to 8 program calls and interrupts to occur. The stack contains the return address from this branch in program execution.

Midrange devices have an 8 level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPped in the event of a RETURN, RETIW or a RETFIE instruction execution. PCLATH is not modified when the stack is PUSHed or POPped.

After the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

## 2.4 Indirect Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a pointer). This is indirect addressing.

### EXAMPLE 2-1: INDIRECT ADDRESSING

- Register file 05 contains the value 10h
- Register file 06 contains the value 0Ah
- Load the value 05 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 06)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 2-2.

### EXAMPLE 2-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```

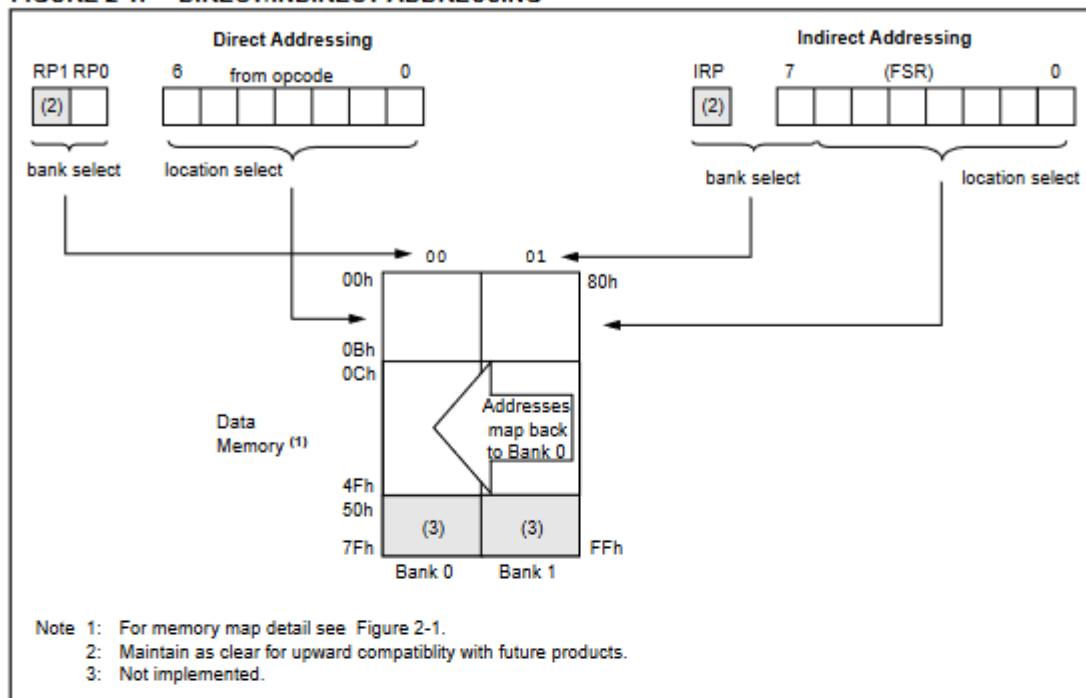
movlw 0x20 :initialize pointer
movwf FSR : to RAM
NEXT    clrf INDF :clear INDF register
        incf FSR :inc pointer
        btfss FSR, 4 :all done?
        goto NEXT :NO, clear next
CONTINUE   :           :YES, continue

```

An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 2-1. However, IRP is not used in the PIC16F84A.

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FIGURE 2-1: DIRECT/INDIRECT ADDRESSING



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## 3.0 I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Additional information on I/O ports may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023).

### 3.1 PORTA and TRISA Registers

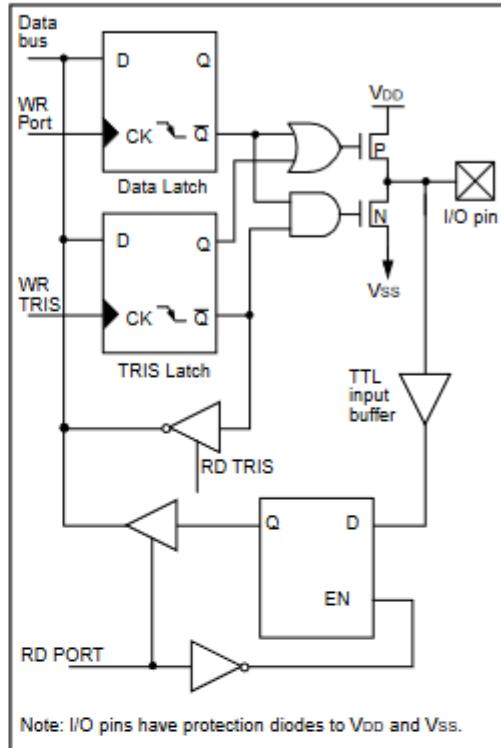
PORATA is a 5-bit wide bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit ( $=1$ ) will make the corresponding PORATA pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISA bit ( $=0$ ) will make the corresponding PORATA pin an output, i.e., put the contents of the output latch on the selected pin.

**Note:** On a Power-on Reset, these pins are configured as inputs and read as '0'.

Reading the PORATA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch.

Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers.

FIGURE 3-1: BLOCK DIAGRAM OF PINS RA3:RA0



### EXAMPLE 3-1: INITIALIZING PORTA

```

BCF STATUS, RP0      ; Initialize PORTA by
CLRF PORTA          ;   clearing output
                     ;   data latches
BSF STATUS, RP0      ; Select Bank 1
MOVLW 0x0F           ; Value used to
                     ; initialize data
                     ; direction
MOUWF TRISA          ; Set RA<3:0> as inputs
                     ; RA4 as output
                     ; TRISA<7:5> are always
                     ; read as '0'.
    
```

## PIC16F84A

---

FIGURE 3-2: BLOCK DIAGRAM OF PIN RA4

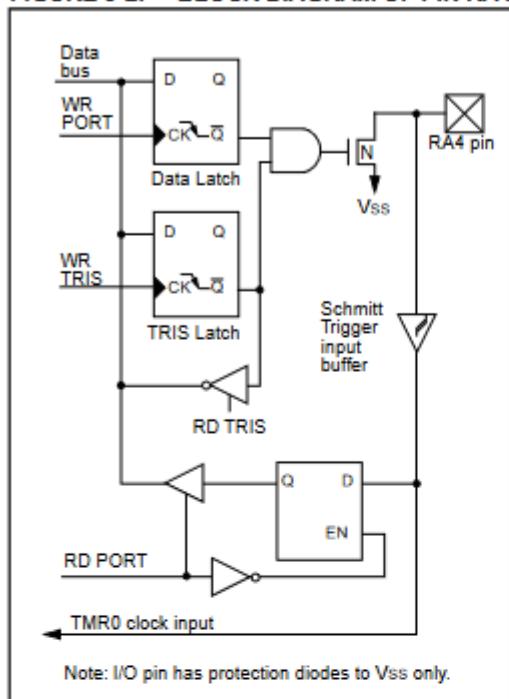


TABLE 3-1 PORTA FUNCTIONS

Name	Bit0	Buffer Type	Function
RA0	bit0	TTL	Input/output
RA1	bit1	TTL	Input/output
RA2	bit2	TTL	Input/output
RA3	bit3	TTL	Input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0. Output is open drain type.

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 3-2 SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
05h	PORTA	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	---u www
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are unimplemented, read as '0'

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### 3.2 PORTB and TRISB Registers

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output, i.e., put the contents of the output latch on the selected pin.

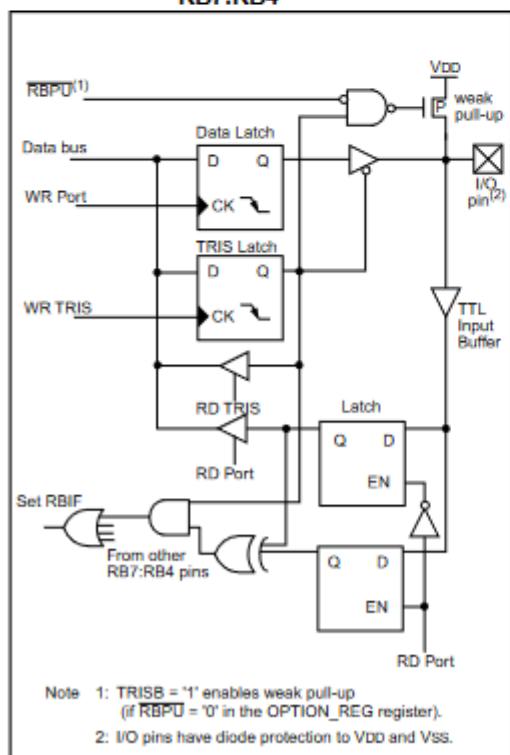
#### EXAMPLE 3-1: INITIALIZING PORTB

```

BCF STATUS, RP0      ; Initialize PORTB by
CLRF PORTB          ;   clearing output
                     ;   data latches
BSF STATUS, RP0      ; Select Bank 1
MOVLW 0xCF           ; Value used to
                     ; initialize data
                     ; direction
MOVWF TRISB          ; Set RB<3:0> as inputs
                     ; RB<5:4> as outputs
                     ; RB<7:6> as inputs
    
```

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

**FIGURE 3-3: BLOCK DIAGRAM OF PINS RB7:RB4**



Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'd together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

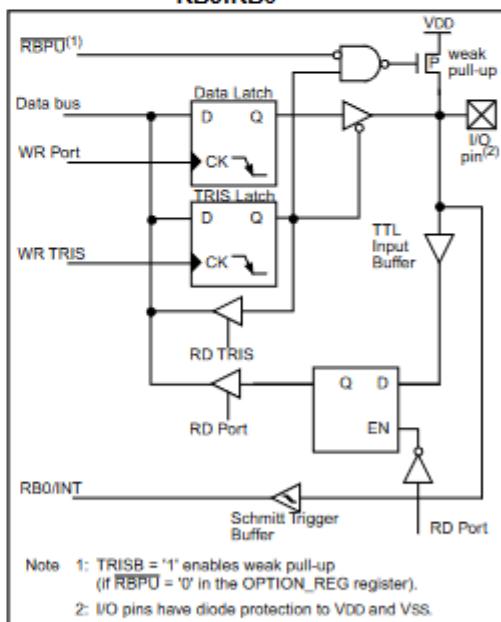
This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

- Any read or write of PORTB. This will end the mismatch condition.
- Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared.

The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

**FIGURE 3-4: BLOCK DIAGRAM OF PINS RB3:RB0**



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**TABLE 3-3 PORTB FUNCTIONS**

Name	Bit	Buffer Type	I/O Consistency Function
RB0/INT	bit0	TTL/ST <sup>(1)</sup>	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger.

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

**TABLE 3-4 SUMMARY OF REGISTERS ASSOCIATED WITH PORTB**

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
08h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	uuuu uuuu
88h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
81h	OPTION_REG	RBU	INTEG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

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## 4.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- Internal or external clock select
- Edge select for external clock
- 8-bit software programmable prescaler
- Interrupt on overflow from FFh to 00h

Figure 4-1 is a simplified block diagram of the Timer0 module.

Additional information on timer modules is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

### 4.1 Timer0 Operation

Timer0 can operate as a timer or as a counter.

Timer mode is selected by clearing bit T0CS (OPTION\_REG<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMRO register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMRO register.

Counter mode is selected by setting bit T0CS (OPTION\_REG<5>). In counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit T0SE (OPTION\_REG<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed below.

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (Tosc). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

Additional information on external clock requirements is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

### 4.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 4-2). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The prescaler is not readable or writable.

The PSA and PS2:PS0 bits (OPTION\_REG<3:0>) determine the prescaler assignment and prescale ratio.

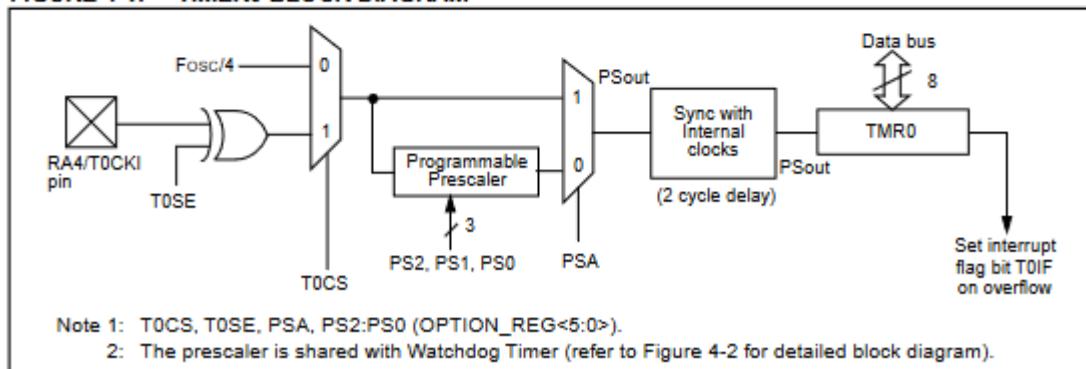
Clearing bit PSA will assign the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable.

Setting bit PSA will assign the prescaler to the Watchdog Timer (WDT). When the prescaler is assigned to the WDT, prescale values of 1:1, 1:2, ..., 1:128 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMRO register (e.g. CLRF 1, MOVWF 1, BSF 1,x,...etc.) will clear the prescaler. When assigned to WDT, a CLRWDI instruction will clear the prescaler along with the WDT.

**Note:** Writing to TMRO when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

FIGURE 4-1: TIMER0 BLOCK DIAGRAM



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## 4.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution.

**Note:** To avoid an unintended device RESET, a specific instruction sequence (shown in the PICmicro™ Mid-Range Reference Manual, DS3023) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

## 4.3 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP since the timer is shut off during SLEEP.

FIGURE 4-2: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

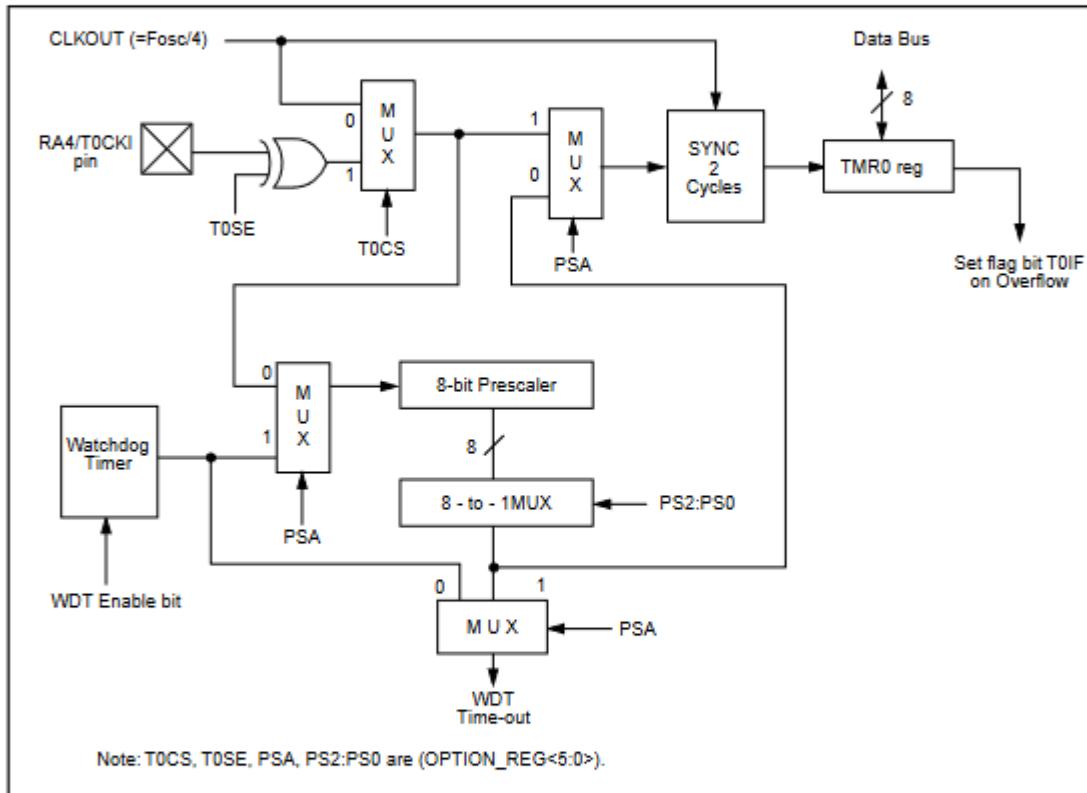


TABLE 4-1 REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
08h,8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

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## 5.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory. These registers are:

- EECON1
- EECON2 (Not a physically implemented register)
- EEDATA
- EEADR

EEDATA holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC16F84A devices have 64 bytes of data EEPROM with an address range from 0h to 3Fh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write-time will vary with voltage and temperature as well as from chip to chip. Please refer to AC specifications for exact limits.

When the device is code protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access this memory.

Additional information on the Data EEPROM is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

FIGURE 5-1: EECON1 REGISTER (ADDRESS 88h)

U	U	U	R/W-0	R/W-x	R/W-0	R/S-0	R/S-x
—	—	—	EEIF	WRERR	WREN	WR	RD
bit7						bit0	

R = Readable bit  
 W = Writable bit  
 S = Settable bit  
 U = Unimplemented bit,  
     read as '0'  
 - n = Value at POR reset

bit 7:5 **Unimplemented:** Read as '0'

bit 4 **EEIF:** EEPROM Write Operation Interrupt Flag bit  
1 = The write operation completed (must be cleared in software)  
0 = The write operation is not complete or has not been started

bit 3 **WRERR:** EEPROM Error Flag bit  
1 = A write operation is prematurely terminated  
    (any MCLR reset or any WDT reset during normal operation)  
0 = The write operation completed

bit 2 **WREN:** EEPROM Write Enable bit  
1 = Allows write cycles  
0 = Inhibits write to the data EEPROM

bit 1 **WR:** Write Control bit  
1 = initiates a write cycle. (The bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.  
0 = Write cycle to the data EEPROM is complete

bit 0 **RD:** Read Control bit  
1 = Initiates an EEPROM read (read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software).  
0 = Does not initiate an EEPROM read

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---

## 5.1 Reading the EEPROM Data Memory

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD (EECON1<0>). The data is available, in the very next cycle, in the EEDATA register; therefore it can be read in the next instruction. EEDATA will hold this value until another read or until it is written to by the user (during a write operation).

### EXAMPLE 5-1: DATA EEPROM READ

```
BCF STATUS, RP0 : Bank 0
MOVLW CONFIG_ADDR :
MOVF EEADR : Address to read
BSF STATUS, RP0 : Bank 1
BSF EECON1, RD : EE Read
BCF STATUS, RP0 : Bank 0
MOVEF EEDATA, W : W = EEDATA
```

## 5.2 Writing to the EEPROM Data Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDATA register. Then the user must follow a specific sequence to initiate the write for each byte.

### EXAMPLE 5-1: DATA EEPROM WRITE

	BSF STATUS, RP0 : Bank 1
	BCF INTCON, GIE : Disable INTs.
	BSF EECON1, WREN : Enable Write
	MOVLW 55h :
Required Sequence	MOVF EECON2 : Write 55h
	MOVLW AAh :
	MOVF EECON2 : Write AAh
	BSF EECON1, WR : Set WR bit
	: begin write
BSF INTCON, GIE : Enable INTs.	

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected)

code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. EEIF must be cleared by software.

## 5.3 Write Verify

Depending on the application, good programming practice may dictate that the value written to the Data EEPROM should be verified (Example 5-1) to the desired value to be written. This should be used in applications where an EEPROM bit will be stressed near the specification limit. The Total Endurance disk will help determine your comfort level.

Generally the EEPROM write failure will be a bit which was written as a '0', but reads back as a '1' (due to leakage off the bit).

### EXAMPLE 5-1: WRITE VERIFY

```
BCF STATUS, RP0 : Bank 0
: : Any code can go here
: :
MOVE EEDATA, W : Must be in Bank 0
BSF STATUS, RP0 : Bank 1
READ
BSF EECON1, RD : YES, Read the
                  : value written
BCF STATUS, RP0 : Bank 0
:
: Is the value written (in W reg) and
: read (in EEDATA) the same?
:
SUBWF EEDATA, W :
BTFSZ STATUS, Z : Is difference 0?
GOTO WRITE_ERR : NO, Write error
: : YES, Good write
: : Continue program
```

TABLE 5-1 REGISTERS/BITS ASSOCIATED WITH DATA EEPROM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
08h	EEDATA	EEPROM data register								xxxx xxxx	uuuu uuuu
09h	EEADR	EEPROM address register								xxxx xxxx	uuuu uuuu
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	---0 q000
89h	EECON2	EEPROM control register 2								-----	-----

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by data EEPROM.

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## 6.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real time applications. The PIC16F84A has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- OSC Selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-circuit serial programming

The PIC16F84A has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep

the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only. This design keeps the device in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode offers a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer time-out or through an interrupt. Several oscillator options are provided to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select the various options.

Additional information on special features is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

### 6.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

Address 2007h is beyond the user program memory space and it belongs to the special test/configuration memory space (2000h - 3FFFh). This space can only be accessed during programming.

FIGURE 6-1: CONFIGURATION WORD - PIC16F84A

| R/P-u |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| CP    | PWRTE | WDTE  | FOSC1 | FOSC0 |       |
| bit13 |       |       |       |       |       |       |       |       |       |       |       |       |       | bit0  |
|       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |

bit 13:4 CP: Code Protection bit  
 1 = Code protection off  
 0 = All memory is code protected

bit 3 PWRTE: Power-up Timer Enable bit  
 1 = Power-up timer is disabled  
 0 = Power-up timer is enabled

bit 2 WDTE: Watchdog Timer Enable bit  
 1 = WDT enabled  
 0 = WDT disabled

bit 1:0 FOSC1:FOSC0: Oscillator Selection bits  
 11 = RC oscillator  
 10 = HS oscillator  
 01 = XT oscillator  
 00 = LP oscillator

R = Readable bit  
 P = Programmable bit  
 -n = Value at POR reset  
 u = unchanged

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### 6.2 Oscillator Configurations

#### 6.2.1 OSCILLATOR TYPES

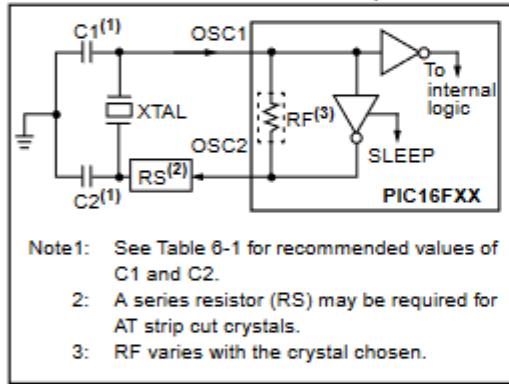
The PIC16F84A can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

#### 6.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

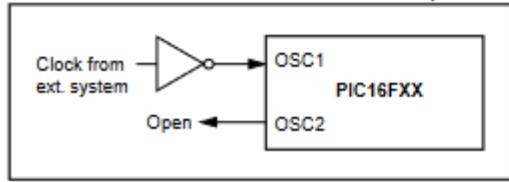
In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 6-2).

**FIGURE 6-2: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)**



The PIC16F84A oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin (Figure 6-3).

**FIGURE 6-3: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)**



**TABLE 6-1 CAPACITOR SELECTION FOR CERAMIC RESONATORS**

Ranges Tested:			
Mode	Freq	OSC1/C1	OSC2/C2
XT	455 kHz	47 - 100 pF	47 - 100 pF
	2.0 MHz	15 - 33 pF	15 - 33 pF
	4.0 MHz	15 - 33 pF	15 - 33 pF
HS	8.0 MHz	15 - 33 pF	15 - 33 pF
	10.0 MHz	15 - 33 pF	15 - 33 pF

Note: Recommended values of C1 and C2 are identical to the ranges tested table.  
Higher capacitance increases the stability of the oscillator but also increases the start-up time.  
These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for the appropriate values of external components.

#### Resonators Tested:

455 kHz	Panasonic EFO-A455K04B	$\pm 0.3\%$
2.0 MHz	Murata Erie CSA2.00MG	$\pm 0.5\%$
4.0 MHz	Murata Erie CSA4.00MG	$\pm 0.5\%$
8.0 MHz	Murata Erie CSA8.00MT	$\pm 0.5\%$
10.0 MHz	Murata Erie CSA10.00MTZ	$\pm 0.5\%$

None of the resonators had built-in capacitors.

**TABLE 6-2 CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR**

Mode	Freq	OSC1/C1	OSC2/C2
LP	32 kHz	68 - 100 pF	68 - 100 pF
	200 kHz	15 - 33 pF	15 - 33 pF
XT	100 kHz	100 - 150 pF	100 - 150 pF
	2 MHz	15 - 33 pF	15 - 33 pF
	4 MHz	15 - 33 pF	15 - 33 pF
HS	4 MHz	15 - 33 pF	15 - 33 pF
	10 MHz	15 - 33 pF	15 - 33 pF

Note: Higher capacitance increases the stability of oscillator but also increases the start-up time.  
These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

For  $V_{DD} > 4.5V$ ,  $C1 = C2 = 30 \text{ pF}$  is recommended.

#### Crystals Tested:

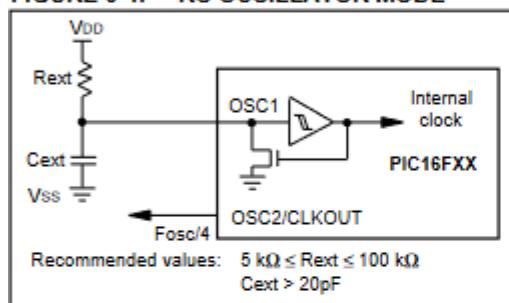
32.768 kHz	Epson C-001R32.768K-A	$\pm 20 \text{ PPM}$
100 kHz	Epson C-2 100.00 KC-P	$\pm 20 \text{ PPM}$
200 kHz	STD XTL 200.000 KHz	$\pm 20 \text{ PPM}$
1.0 MHz	ECS ECS-10-13-2	$\pm 50 \text{ PPM}$
2.0 MHz	ECS ECS-20-S-2	$\pm 50 \text{ PPM}$
4.0 MHz	ECS ECS-40-S-4	$\pm 50 \text{ PPM}$
10.0 MHz	ECS ECS-100-S-4	$\pm 50 \text{ PPM}$

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### 6.2.3 RC OSCILLATOR

For timing insensitive applications the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor ( $R_{ext}$ ) values, capacitor ( $C_{ext}$ ) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types also affects the oscillation frequency, especially for low  $C_{ext}$  values. The user needs to take into account variation due to tolerance of the external R and C components. Figure 6-4 shows how an R/C combination is connected to the PIC16F84A.

**FIGURE 6-4: RC OSCILLATOR MODE**



### 6.3 Reset

The PIC16F84A differentiates between various kinds of reset:

- Power-on Reset (POR)
- MCLR reset during normal operation
- MCLR reset during SLEEP
- WDT Reset (during normal operation)
- WDT Wake-up (during SLEEP)

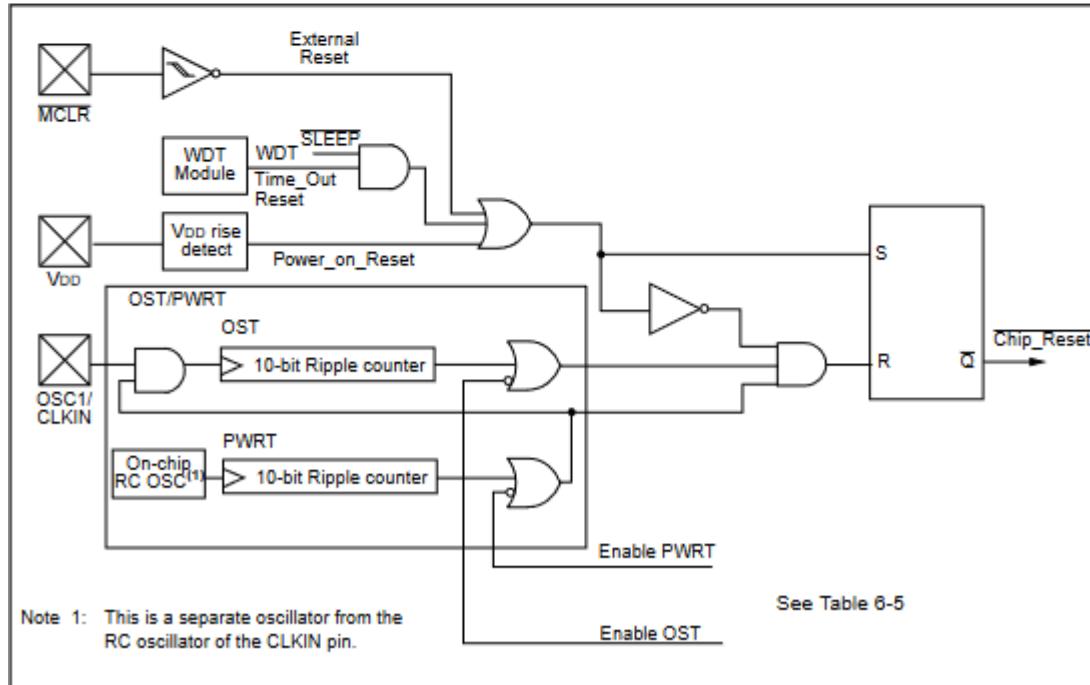
Figure 6-5 shows a simplified block diagram of the on-chip reset circuit. The MCLR reset path has a noise filter to ignore small pulses. The electrical specifications state the pulse width requirements for the MCLR pin.

Some registers are not affected in any reset condition; their status is unknown on a POR reset and unchanged in any other reset. Most other registers are reset to a "reset state" on POR, MCLR or WDT reset during normal operation and on MCLR reset during SLEEP. They are not affected by a WDT reset during SLEEP, since this reset is viewed as the resumption of normal operation.

Table 6-3 gives a description of reset conditions for the program counter (PC) and the STATUS register. Table 6-4 gives a full description of reset states for all registers.

The TO and PD bits are set or cleared differently in different reset situations (Section 6.7). These bits are used in software to determine the nature of the reset.

**FIGURE 6-5: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**



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TABLE 6-3 RESET CONDITION FOR PROGRAM COUNTER AND THE STATUS REGISTER

Condition	Program Counter	STATUS Register
Power-on Reset	000h	0001 1xxxx
MCLR Reset during normal operation	000h	000u uuuu
MCLR Reset during SLEEP	000h	0001 0uuu
WDT Reset (during normal operation)	000h	0000 1uuu
WDT Wake-up	PC + 1	uuu0 0uuu
Interrupt wake-up from SLEEP	PC + 1 <sup>(1)</sup>	uuu1 0uuu

Legend: u = unchanged, x = unknown.

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 6-4 RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-on Reset	MCLR Reset during: – normal operation – SLEEP WDT Reset during normal operation	Wake-up from SLEEP: – through interrupt – through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	---- ----	---- ----	---- ----
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000h	0000h	PC + 1 <sup>(2)</sup>
STATUS	03h	0001 1xxx	000q quuu <sup>(3)</sup>	uuuq quuu <sup>(3)</sup>
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA <sup>(4)</sup>	05h	---x xxxx	---u uuuu	---u uuuu
PORTB <sup>(5)</sup>	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEDATA	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEADR	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu <sup>(1)</sup>
INDF	80h	---- ----	---- ----	---- ----
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
PCL	82h	0000h	0000h	PC + 1
STATUS	83h	0001 1xxx	000q quuu <sup>(3)</sup>	uuuq quuu <sup>(3)</sup>
FSR	84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TRISA	85h	---1 1111	---1 1111	---u uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
EECON1	88h	---0 x000	---0 q000	---0 uuuu
EECON2	89h	---- ----	---- ----	---- ----
PCLATH	8Ah	---0 0000	---0 0000	---u uuuu
INTCON	8Bh	0000 000x	0000 000u	uuuu uuuu <sup>(1)</sup>

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0', q = value depends on condition.

Note 1: One or more bits in INTCON will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: Table 6-3 lists the reset value for each specific condition.

4: On any device reset, these pins are configured as inputs.

5: This is the value that will be in the port output latch.

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## 6.4 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when V<sub>DD</sub> rise is detected (in the range of 1.2V - 1.7V). To take advantage of the POR, just tie the MCLR pin directly (or through a resistor) to V<sub>DD</sub>. This will eliminate external RC components usually needed to create Power-on Reset. A minimum rise time for V<sub>DD</sub> must be met for this to operate properly. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting."

The POR circuit does not produce an internal reset when V<sub>DD</sub> declines.

## 6.5 Power-up Timer (PWRT)

The Power-up Timer (PWRT) provides a fixed 72 ms nominal time-out (TPWRT) from POR (Figure 6-7, Figure 6-8, Figure 6-9 and Figure 6-10). The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT delay allows the V<sub>DD</sub> to rise to an acceptable level (Possible exception shown in Figure 6-10).

A configuration bit, PWRTE, can enable/disable the PWRT. See Figure 6-1 for the operation of the PWRTE bit for a particular device.

The power-up time delay TPWRT will vary from chip to chip due to V<sub>DD</sub>, temperature, and process variation. See DC parameters for details.

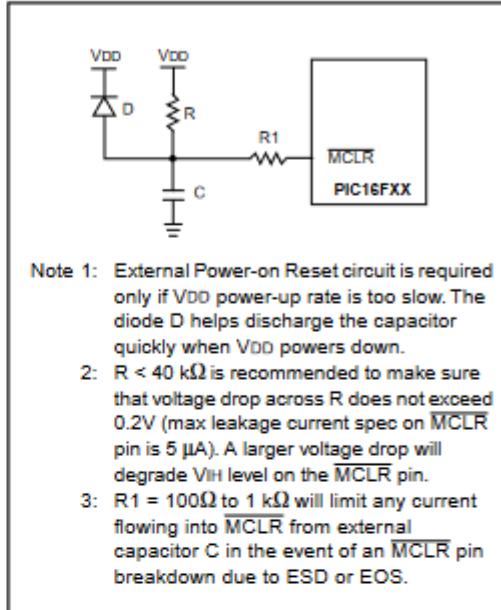
## 6.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle delay (from OSC1 input) after the PWRT delay ends (Figure 6-7, Figure 6-8, Figure 6-9 and Figure 6-10). This ensures the crystal oscillator or resonator has started and stabilized.

The OST time-out (TOST) is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

When V<sub>DD</sub> rises very slowly, it is possible that the TPWRT time-out and TOST time-out will expire before V<sub>DD</sub> has reached its final value. In this case (Figure 6-10), an external power-on reset circuit may be necessary (Figure 6-6).

**FIGURE 6-6: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW V<sub>DD</sub> POWER-UP)**



- Note 1: External Power-on Reset circuit is required only if V<sub>DD</sub> power-up rate is too slow. The diode D helps discharge the capacitor quickly when V<sub>DD</sub> powers down.
- 2: R < 40 kΩ is recommended to make sure that voltage drop across R does not exceed 0.2V (max leakage current spec on MCLR pin is 5 μA). A larger voltage drop will degrade V<sub>IH</sub> level on the MCLR pin.
- 3: R1 = 100Ω to 1 kΩ will limit any current flowing into MCLR from external capacitor C in the event of an MCLR pin breakdown due to ESD or EOS.

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FIGURE 6-7: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO V<sub>DD</sub>): CASE 1

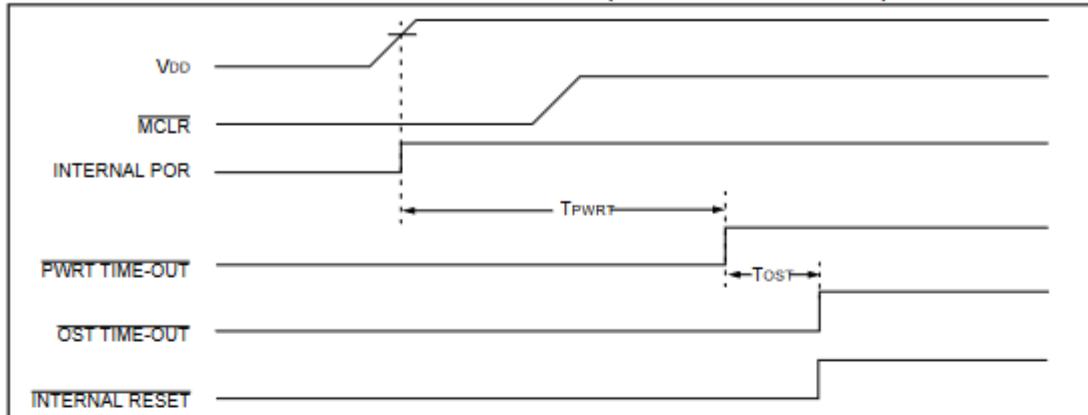
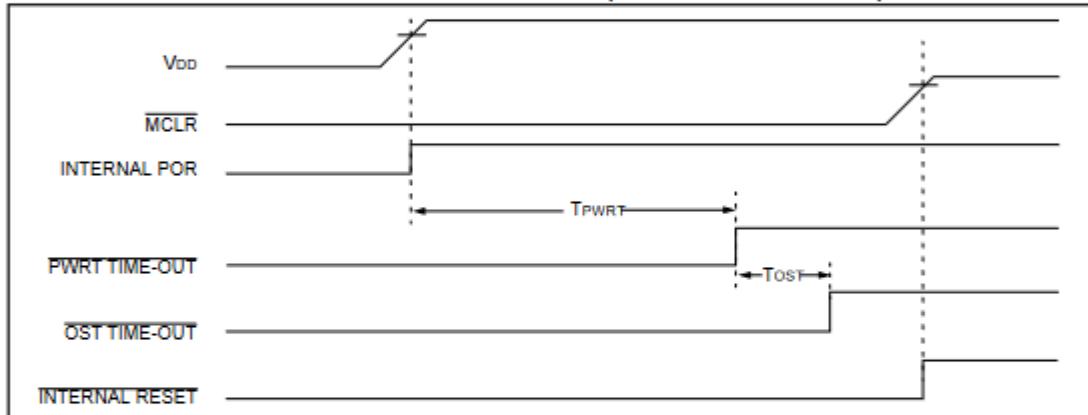


FIGURE 6-8: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO V<sub>DD</sub>): CASE 2



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FIGURE 6-9: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO V<sub>DD</sub>): FAST V<sub>DD</sub> RISE TIME

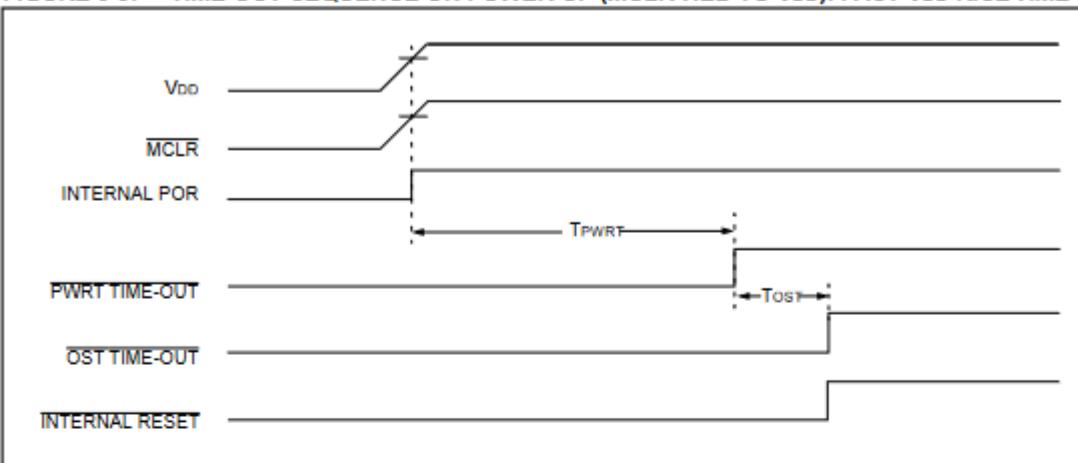
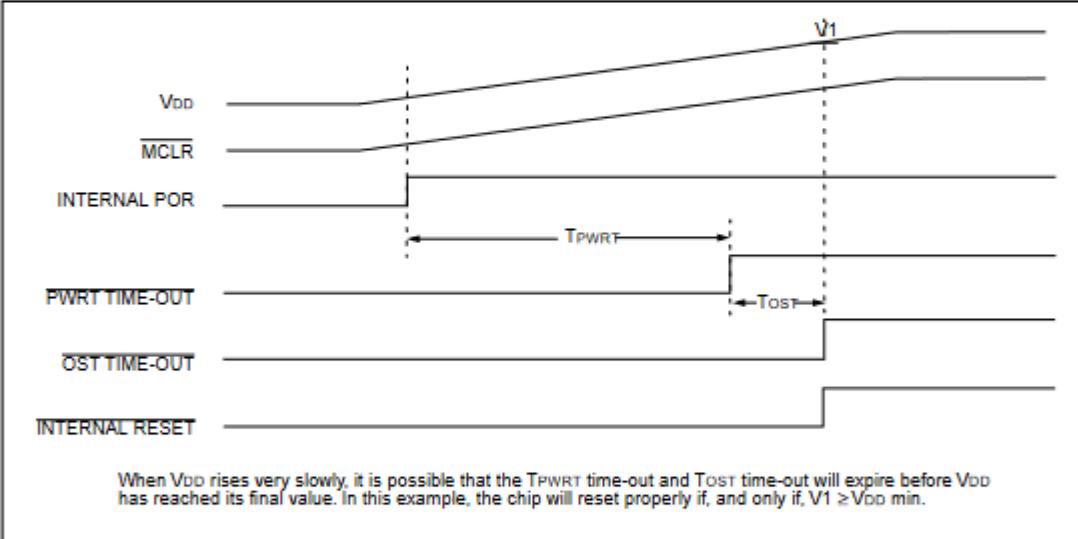


FIGURE 6-10: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO V<sub>DD</sub>): SLOW V<sub>DD</sub> RISE TIME



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### 6.7 Time-out Sequence and Power-down Status Bits (TO/PD)

On power-up (Figure 6-7, Figure 6-8, Figure 6-9 and Figure 6-10) the time-out sequence is as follows: First PWRT time-out is invoked after a POR has expired. Then the OST is activated. The total time-out will vary based on oscillator configuration and PWRTE configuration bit status. For example, in RC mode with the PWRT disabled, there will be no time-out at all.

**TABLE 6-5 TIME-OUT IN VARIOUS SITUATIONS**

Oscillator Configuration	Power-up		Wake-up from SLEEP
	PWRT Enabled	PWRT Disabled	
XT, HS, LP	72 ms + 1024Tosc	1024Tosc	1024Tosc
RC	72 ms	—	—

Since the time-outs occur from the POR reset pulse, if MCLR is kept low long enough, the time-outs will expire. Then bringing MCLR high, execution will begin immediately (Figure 6-7). This is useful for testing purposes or to synchronize more than one PIC16F84A device when operating in parallel.

Table 6-6 shows the significance of the TO and PD bits. Table 6-3 lists the reset conditions for some special registers, while Table 6-4 lists the reset conditions for all the registers.

**TABLE 6-6 STATUS BITS AND THEIR SIGNIFICANCE**

TO	PD	Condition
1	1	Power-on Reset
0	x	Illegal, TO is set on POR
x	0	Illegal, PD is set on POR
0	1	WDT Reset (during normal operation)
0	0	WDT Wake-up
1	1	MCLR Reset during normal operation
1	0	MCLR Reset during SLEEP or interrupt wake-up from SLEEP

### 6.8 Interrupts

The PIC16F84A has 4 sources of interrupt:

- External interrupt RB0/INT pin
- TMR0 overflow interrupt
- PORTB change interrupts (pins RB7:RB4)
- Data EEPROM write complete interrupt

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also contains the individual and global interrupt enable bits.

The global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. Bit GIE is cleared on reset.

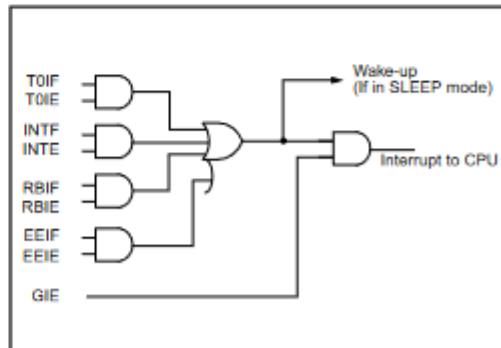
The "return from interrupt" instruction, RETFIE, exits interrupt routine as well as sets the GIE bit, which re-enables interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

When an interrupt is responded to; the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. For external interrupt events, such as the RB0/INT pin or PORTB change interrupt, the interrupt latency will be three to four instruction cycles. The exact latency depends when the interrupt event occurs. The latency is the same for both one and two cycle instructions. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests.

**Note 1:** Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

**FIGURE 6-11: INTERRUPT LOGIC**



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## 6.8.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if INTEDG bit (OPTION\_REG<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing control bit INTE (INTCON<4>). Flag bit INTF must be cleared in software via the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake the processor from SLEEP (Section 6.11) only if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether the processor branches to the interrupt vector following wake-up.

## 6.8.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in TMR0 will set flag bit TOIF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit TOIE (INTCON<5>) (Section 4.0).

## 6.8.3 PORB INTERRUPT

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<3>) (Section 3.2).

**Note 1:** For a change on the I/O pin to be recognized, the pulse width must be at least TCY wide.

## 6.8.4 DATA EEPROM INTERRUPT

At the completion of a data EEPROM write cycle, flag bit EEIF (EECON1<4>) will be set. The interrupt can be enabled/disabled by setting/clearing enable bit EEIE (INTCON<6>) (Section 5.0).

## 6.9 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users wish to save key register values during an interrupt (e.g., W register and STATUS register). This is implemented in software.

Example 6-1 stores and restores the STATUS and W register's values. The User defined registers, W\_TEMP and STATUS\_TEMP are the temporary storage locations for the W and STATUS registers values.

Example 6-1 does the following:

- Stores the W register.
- Stores the STATUS register in STATUS\_TEMP.
- Executes the Interrupt Service Routine code.
- Restores the STATUS (and bank select bit) register.
- Restores the W register.

## EXAMPLE 6-1: SAVING STATUS AND W REGISTERS IN RAM

```

PUSH  MOVWF  W_TEMP          ; Copy W to TEMP register,
      SWAPP  STATUS, W        ; Swap status to be saved into W
      MOVWF  STATUS_TEMP       ; Save status to STATUS_TEMP register
ISR   :                   :
      :                   ; Interrupt Service Routine
      :                   ; should configure Bank as required
      :                   ;
POP   SWAPP  STATUS_TEMP, W ; Swap nibbles in STATUS_TEMP register
      :                   ; and place result into W
      MOVWF  STATUS           ; Move W into STATUS register
      :                   ; (sets bank to original state)
      SWAPP  W_TEMP, F        ; Swap nibbles in W_TEMP and place result in W_TEMP
      SWAPP  W_TEMP, W        ; Swap nibbles in W_TEMP and place result into W

```

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## 6.10 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT Wake-up causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming configuration bit WDTE as a '0' (Section 6.1).

### 6.10.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, V<sub>DD</sub> and process variations from part to

part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION\_REG register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDI and SLEEP instructions clear the WDT and the postscaler (if assigned to the WDT) and prevent it from timing out and generating a device RESET condition.

The TO bit in the STATUS register will be cleared upon a WDT time-out.

### 6.10.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (V<sub>DD</sub> = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

FIGURE 6-12: WATCHDOG TIMER BLOCK DIAGRAM

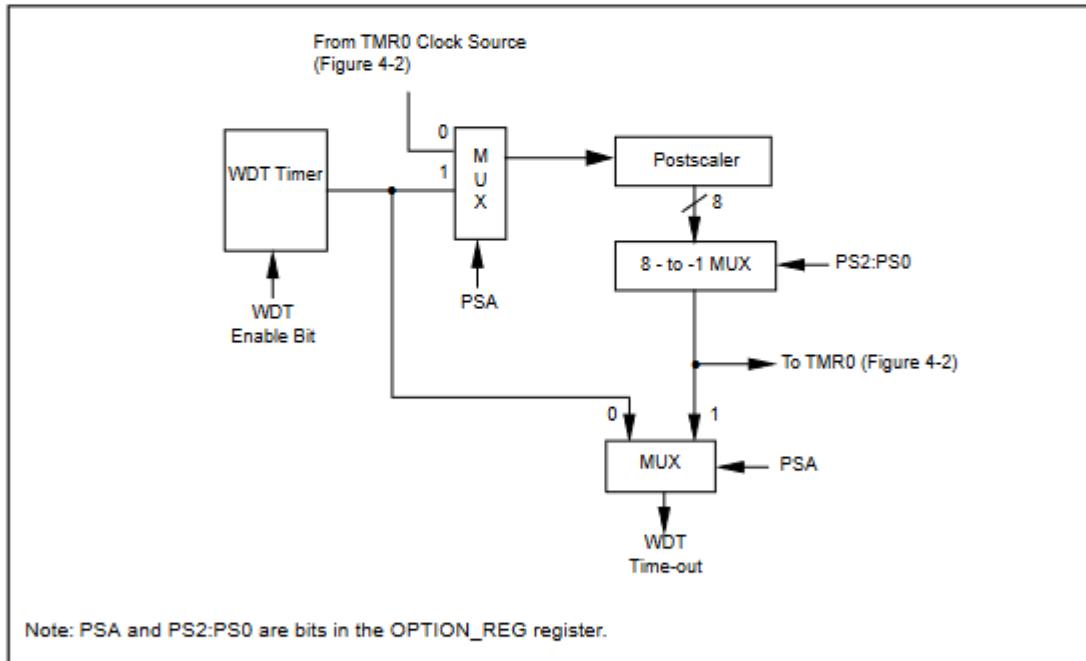


TABLE 6-7 SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
2007h	Config. bits	(2)	(2)	(2)	(2)	PWRTE <sup>(1)</sup>	WDTE	FOSC1	FOSC0	(2)	
81h	OPTION_REG	RBU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown. Shaded cells are not used by the WDT.

Note 1: See Figure 6-1 for operation of the PWRTE bit.

2: See Figure 6-1 and Section 6.12 for operation of the Code and Data protection bits.

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## 6.11 Power-down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

### 6.11.1 SLEEP

The Power-down mode is entered by executing the SLEEP instruction.

If enabled, the Watchdog Timer is cleared (but keeps running), the PD bit (STATUS<3>) is cleared, the TO bit (STATUS<4>) is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For the lowest current consumption in SLEEP mode, place all I/O pins at either at VDD or Vss, with no external circuitry drawing current from the I/O pins, and disable external clocks. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or Vss. The contribution from on-chip pull-ups on PORTB should be considered.

The MCLR pin must be at a logic high level (VIHMC).

It should be noted that a RESET generated by a WDT time-out does not drive the MCLR pin low.

### 6.11.2 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

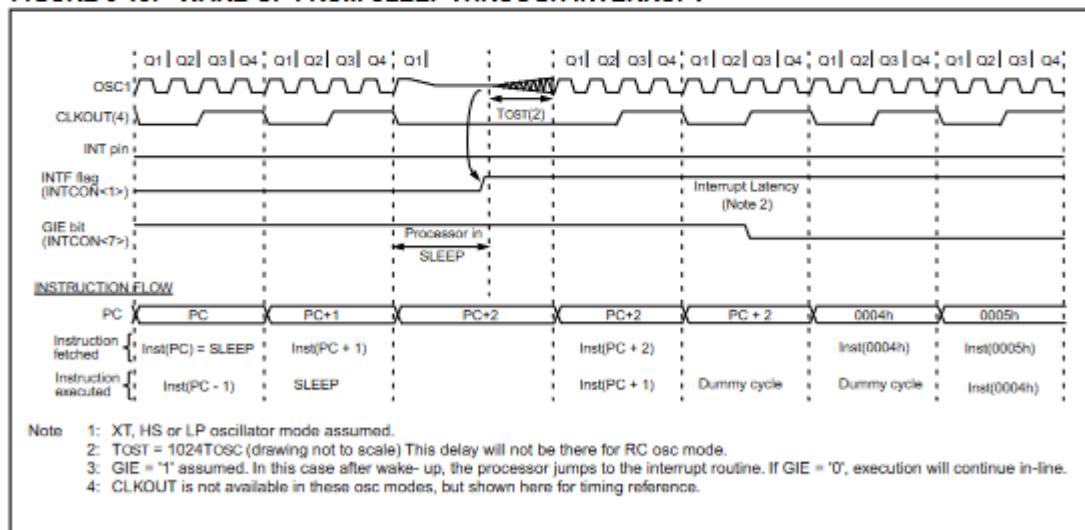
1. External reset input on MCLR pin.
2. WDT Wake-up (if WDT was enabled).
3. Interrupt from RB0/INT pin, RB port change, or data EEPROM write complete.

Peripherals cannot generate interrupts during SLEEP, since no on-chip Q clocks are present.

The first event (MCLR reset) will cause a device reset. The two latter events are considered a continuation of program execution. The TO and PD bits can be used to determine the cause of a device reset. The PD bit, which is set on power-up, is cleared when SLEEP is invoked. The TO bit is cleared if a WDT time-out occurred (and caused wake-up).

While the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

FIGURE 6-13: WAKE-UP FROM SLEEP THROUGH INTERRUPT



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### 6.11.3 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the TO bit will not be set and PD bits will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake up from sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the TO bit will be set and the PD bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the PD bit. If the PD bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

### 6.12 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

**Note:** Microchip does not recommend code protecting windowed devices.

### 6.13 ID Locations

Four memory locations (2000h - 2004h) are designated as ID locations to store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable only during program/verify. Only the four least significant bits of ID location are usable.

### 6.14 In-Circuit Serial Programming

PIC16F84A microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. Customers can manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product, allowing the most recent firmware or custom firmware to be programmed.

For complete details of serial programming, please refer to the In-Circuit Serial Programming (ICSP™) Guide, (DS30277).

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## 7.0 INSTRUCTION SET SUMMARY

Each PIC16CXXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXX instruction set summary in Table 7-2 lists byte-oriented, bit-oriented, and literal and control operations. Table 7-1 shows the opcode field descriptions.

For byte-oriented instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For literal and control operations, 'k' represents an eight or eleven bit constant or literal value.

**TABLE 7-1 OPCODE FIELD DESCRIPTIONS**

Field	Description
<b>F</b>	Register file address (0x00 to 0x7F)
<b>W</b>	Working register (accumulator)
<b>b</b>	Bit address within an 8-bit file register
<b>k</b>	Literal field, constant data or label
<b>x</b>	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
<b>d</b>	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
<b>PC</b>	Program Counter
<b>TO</b>	Time-out bit
<b>PD</b>	Power-down bit

The instruction set is highly orthogonal and is grouped into three basic categories:

- Byte-oriented operations
- Bit-oriented operations
- Literal and control operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1  $\mu$ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2  $\mu$ s.

Table 7-2 lists the instructions recognized by the MPASM assembler.

Figure 7-1 shows the general formats that the instructions can have.

**Note:** To maintain upward compatibility with future PIC16CXXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexadecimal number:

Oxhh

where h signifies a hexadecimal digit.

**FIGURE 7-1: GENERAL FORMAT FOR INSTRUCTIONS**

Byte-oriented file register operations			
13	8	7	6 0
OPCODE	d	f (FILE #)	
<i>d</i> = 0 for destination W <i>d</i> = 1 for destination f <i>f</i> = 7-bit file register address			
Bit-oriented file register operations			
13	10	9	8 6 0
OPCODE	b (BIT #)	f (FILE #)	
<i>b</i> = 3-bit bit address <i>f</i> = 7-bit file register address			
Literal and control operations			
General			
13	8	7	6 0
OPCODE		k (literal)	
<i>k</i> = 8-bit immediate value			
CALL and GOTO instructions only			
13	11	10	6 0
OPCODE		k (literal)	
<i>k</i> = 11-bit immediate value			

A description of each instruction is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

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TABLE 7-2 PIC16CXXX INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	14-Bit Opcode				Status Affected	Notes
			MSb	L Sb				
BYTE-ORIENTED FILE REGISTER OPERATIONS								
ADDWF	f, d	Add W and f	1	00	0111	dfff	eeee	C,DC,Z
ANDWF	f, d	AND W with f	1	00	0101	dfff	eeee	Z
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z
COMF	f, d	Complement f	1	00	1001	dfff	eeee	Z
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	0011	dfff	eeee	Z
INCF	f, d	Increment f	1	00	1010	dfff	eeee	Z
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	eeee	Z
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	eeee	Z
MOVF	f, d	Move f	1	00	1000	dfff	eeee	Z
MOVWF	f	Move W to f	1	00	0000	1fff	ffff	Z
NOP	-	No Operation	1	00	0000	0xxx	0000	
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	eeee	C
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	eeee	C
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	eeee	C,DC,Z
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	eeee	Z
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	eeee	Z
BIT-ORIENTED FILE REGISTER OPERATIONS								
BCF	f, b	Bit Clear f	1	01	00bb	bfff	eeee	Z
BSF	f, b	Bit Set f	1	01	01bb	bfff	eeee	Z
BTFSZ	f, b	Bit Test f, Skip if Clear	1(2)	01	10bb	bfff	eeee	Z
BTFSZ	f, b	Bit Test f, Skip if Set	1(2)	01	11bb	bfff	eeee	Z
LITERAL AND CONTROL OPERATIONS								
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk	
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk	
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk	
RETFIE	-	Return from interrupt	2	00	0000	0000	1001	
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk	
RETURN	-	Return from Subroutine	2	00	0000	0000	1000	
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	TO,PD
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z

Note 1: When an I/O register is modified as a function of itself (e.g., MOVE PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

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### 8.0 DEVELOPMENT SUPPORT

#### 8.1 Development Tools

The PICmicro™ microcontrollers are supported with a full range of hardware and software development tools:

- MPLAB™-ICE Real-Time In-Circuit Emulator
- ICEPIC™ Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE® II Universal Programmer
- PICSTART® Plus Entry-Level Prototype Programmer
- SIMICE
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB™ SIM Software Simulator
- MPLAB-C17 (C Compiler)
- Fuzzy Logic Development System (*fuzzyTECH®-MP*)
- KEELOQ® Evaluation Kits and Programmer

#### 8.2 MPLAB-ICE: High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB-ICE Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers (MCUs). MPLAB-ICE is supplied with the MPLAB Integrated Development Environment (IDE), which allows editing, "make" and download, and source debugging from a single environment.

Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB-ICE allows expansion to support all new Microchip microcontrollers.

The MPLAB-ICE Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows® 3.x or Windows 95 environment were chosen to best make these features available to you, the end user.

MPLAB-ICE is available in two versions. MPLAB-ICE 1000 is a basic, low-cost emulator system with simple trace capabilities. It shares processor modules with the MPLAB-ICE 2000. This is a full-featured emulator system with enhanced trace, trigger, and data monitoring features. Both systems will operate across the entire operating speed range of the PICmicro MCU.

#### 8.3 ICEPIC: Low-Cost PICmicro™ In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC12CXXX, PIC16C5X and PIC16CXXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 386 through Pentium™ based machines under Windows 3.x, Windows 95, or Windows NT environment. ICEPIC features real time, non-intrusive emulation.

#### 8.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode. PRO MATE II is CE compliant.

The PRO MATE II has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode the PRO MATE II can read, verify or program PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices. It can also set configuration and code-protect bits in this mode.

#### 8.5 PICSTART Plus Entry Level Development System

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923, PIC16C924 and PIC17C756 may be supported with an adapter socket. PICSTART Plus is CE compliant.

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### 8.6 SIMICE Entry-Level Hardware Simulator

SIMICE is an entry-level hardware development system designed to operate in a PC-based environment with Microchip's simulator MPLAB™-SIM. Both SIMICE and MPLAB-SIM run under Microchip Technology's MPLAB Integrated Development Environment (IDE) software. Specifically, SIMICE provides hardware simulation for Microchip's PIC12C5XX, PIC12CE5XX, and PIC16C5X families of PICmicro™ 8-bit microcontrollers. SIMICE works in conjunction with MPLAB-SIM to provide non-real-time I/O port emulation. SIMICE enables a developer to run simulator code for driving the target system. In addition, the target system can provide input to the simulator code. This capability allows for simple and interactive debugging without having to manually generate MPLAB-SIM stimulus files. SIMICE is a valuable debugging tool for entry-level system development.

### 8.7 PICDEM-1 Low-Cost PICmicro Demonstration Board

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C81, PIC16C82X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-Plus programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the MPLAB-ICE emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

### 8.8 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I<sup>2</sup>C bus and separate headers for connection to an LCD module and a keypad.

### 8.9 PICDEM-3 Low-Cost PIC16CXXX Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

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### 8.10 MPLAB Integrated Development Environment Software

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- A full featured editor
- Three operating modes
  - editor
  - emulator
  - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information
- Extensive on-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PICmicro tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

### 8.11 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PC-hosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC18C5X, PIC18CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from MPLAB-ICE, Microchip's Universal Emulator System.

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip's emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PICmicro. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

### 8.12 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PICmicro series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C17 and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

### 8.13 MPLAB-C17 Compiler

The MPLAB-C17 Code Development System is a complete ANSI 'C' compiler and integrated development environment for Microchip's PIC17CXXX family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display.

### 8.14 Fuzzy Logic Development System (fuzzyTECH-MP)

fuzzyTECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, fuzzyTECH-MP, Edition for implementing more complex systems.

Both versions include Microchip's fuzzyLAB™ demonstration board for hands-on experience with fuzzy logic systems implementation.

### 8.15 SEEVAL® Evaluation and Programming System

The SEEVAL SEEPEROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPEROM product including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

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### 8.16 KEELOQ® Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

**PIC16F84A****TABLE 8-1: DEVELOPMENT TOOLS FROM MICROCHIP**

Emulator Products	Software Tools	Programmers	Demo Boards	PIC12C5XX	PIC14000	PIC16C5X	PIC16CXXX	PIC16C6X	PIC16C7XX	PIC16C8X	PIC16C9XX	PIC17C4X	PIC17C7XX	24CXX 25CXX 93CXX	HCS200	HCS300	HCS301
MPLAB™-ICE				✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
ICEPIC™ Low-Cost In-Circuit Emulator						✓	✓	✓	✓	✓	✓	✓	✓	✓			
MPLAB™ Integrated Development Environment						✓	✓	✓	✓	✓	✓	✓	✓	✓			
MPLAB™ C17*																	
fuzzyTECH®-MP Compiler																	
Fuzzy Logic Dev. Tool																	
Total Endurance™ Software Model																	
PICSTART™ Plus																	
Low-Cost Universal Dev. Kit																	
PRO MATE® II Universal Programmer																	
KEELOO® Programmer																	
SEEVAL™ Designers Kit																	
SIMICE																	
PICDEM-1A																	
PICDEM-1																	
PICDEM-2																	
PICDEM-3																	
KEELOO® Evaluation Kit																	
KEELOO Transponder Kit																	

## **PIC16F84A**

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### **NOTES:**

**PIC16F84A****9.0 ELECTRICAL CHARACTERISTICS FOR PIC16F84A****Absolute Maximum Ratings †**

Ambient temperature under bias.....	-55°C to +125°C
Storage temperature .....	-65°C to +150°C
Voltage on any pin with respect to VSS (except VDD, MCLR, and RA4).....	-0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss .....	-0.3 to +7.5V
Voltage on MCLR with respect to Vss <sup>(1)</sup> .....	-0.3 to +14V
Voltage on RA4 with respect to Vss .....	-0.3 to +8.5V
Total power dissipation <sup>(2)</sup> .....	800 mW
Maximum current out of VSS pin .....	150 mA
Maximum current into VDD pin .....	100 mA
Input clamp current, I <sub>IK</sub> (VI < 0 or VI > VDD).....	± 20 mA
Output clamp current, I <sub>OK</sub> (VO < 0 or VO > VDD).....	± 20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin .....	20 mA
Maximum current sunk by PORTA .....	80 mA
Maximum current sourced by PORTA .....	50 mA
Maximum current sunk by PORTB.....	150 mA
Maximum current sourced by PORTB.....	100 mA

**Note 1:** Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to Vss.

**Note 2:** Power dissipation is calculated as follows:  $P_{diss} = V_{DD} \times \{I_{DD} + \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$ .

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PREL

## PIC16F84A

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TABLE 9-1 CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16F84A-04	PIC16F84A-20	PIC16LF84A-04
RC	Vdd: 4.0V to 5.5V Idd: 4.5 mA max. at 5.5V Ipd: 14 µA max. at 4V, WDT dis Freq: 4.0 MHz max. at 4V	Vdd: 4.5V to 5.5V Idd: 1.8 mA typ. at 5.5V Ipd: 1.0 µA typ. at 5.5V, WDT dis Freq: 4.0 MHz max. at 4V	Vdd: 2.0V to 5.5V Idd: 4.5 mA max. at 5.5V Ipd: 7.0 µA max. at 2V WDT dis Freq: 2.0 MHz max. at 2V
XT	Vdd: 4.0V to 5.5V Idd: 4.5 mA max. at 5.5V Ipd: 14 µA max. at 4V, WDT dis Freq: 4.0 MHz max. at 4V	Vdd: 4.5V to 5.5V Idd: 1.8 mA typ. at 5.5V Ipd: 1.0 µA typ. at 5.5V, WDT dis Freq: 4.0 MHz max. at 4.5V	Vdd: 2.0V to 5.5V Idd: 4.5 mA max. at 5.5V Ipd: 7.0 µA max. at 2V WDT dis Freq: 2.0 MHz max. at 2V
HS	Vdd: 4.5V to 5.5V Idd: 4.5 mA typ. at 5.5V Ipd: 1.0 µA typ. at 4.5V, WDT dis Freq: 4.0 MHz max. at 4.5V	Vdd: 4.5V to 5.5V Idd: 10 mA max. at 5.5V typ. Ipd: 1.0 µA typ. at 4.5V, WDT dis Freq: 20 MHz max. at 4.5V	Do not use in HS mode
LP	Vdd: 4.0V to 5.5V Idd: 48 µA typ. at 32 kHz, 2.0V Ipd: 0.6 µA typ. at 3.0V, WDT dis Freq: 200 kHz max. at 4V	Do not use in LP mode	Vdd: 2.0V to 5.5V Idd: 45 µA max. at 32 kHz, 2.0V Ipd: 7 µA max. at 2.0V WDT dis Freq: 200 kHz max. at 2V

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

PRELIMINARY

**PIC16F84A**
**9.1 DC CHARACTERISTICS:** PIC16F84A-04 (Commercial, Industrial)  
 PIC16F84A-20 (Commercial, Industrial)

DC Characteristics			Standard Operating Conditions (unless otherwise stated)				
Power Supply Pins			Operating temperature $0^{\circ}\text{C} \leq \text{TA} \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ (industrial)				
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001 D001A	VDD	Supply Voltage	4.0 4.5	— —	5.5 5.5	V	XT, RC and LP osc configuration HS osc configuration
D002*	VDR	RAM Data Retention Voltage (Note 1)	1.5*	—	—	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	—	Vss	—	V	See section on Power-on Reset for details
D004* D004A*	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05* TBD	— —	—	V/ms	PWRT enabled (PWRTB bit clear) PWRT disabled (PWRTB bit set) See section on Power-on Reset for details
D010 D010A	I <sub>DD</sub>	Supply Current (Note 2)	— — —	1.8 3	4.5 10	mA	RC and XT osc configuration (Note 4) $\text{Fosc} = 4.0\text{ MHz}, \text{Vdd} = 5.5\text{V}$ $\text{Fosc} = 4.0\text{ MHz}, \text{Vdd} = 5.5\text{V}$ (During Flash programming) HS osc configuration (PIC16F84A-20) $\text{Fosc} = 20\text{ MHz}, \text{Vdd} = 5.5\text{V}$
D013			—	10	20	mA	
D020 D021 D021A	I <sub>PD</sub>	Power-down Current (Note 3)	— — —	7.0 1.0 1.0	28 14 16	μA	$\text{Vdd} = 4.0\text{V}, \text{WDT enabled, industrial}$ $\text{Vdd} = 4.0\text{V}, \text{WDT disabled, commercial}$ $\text{Vdd} = 4.0\text{V}, \text{WDT disabled, industrial}$
D022*	ΔI <sub>WDT</sub>	Module Differential Current (Note 5) Watchdog Timer	—	6.0 20*	30*	μA	WDTE bit set, $\text{Vdd} = 4.0\text{V}$ , commercial WDTE bit set, $\text{Vdd} = 4.0\text{V}$ , extended

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD,  
MCLR = VDD; WDT enabled/disabled as specified.**3:** The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.**4:** For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula  $IR = \text{Vdd}/2\text{Rext}$  (mA) with Rext in kOhm.**5:** The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD measurement.

## PIC16F84A

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### 9.2 DC CHARACTERISTICS: PIC16LF84A-04 (Commercial, Industrial)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature $0^{\circ}\text{C} \leq \text{TA} \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ (industrial)				
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	2.0	—	5.5	V	XT, RC, and LP osc configuration
D002*	VDR	RAM Data Retention Voltage (Note 1)	1.5*	—	—	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	—	Vss	—	V	See section on Power-on Reset for details
D004* D004A*	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05* TBD	—	—	V/ms	PWRT enabled (PWRTE bit clear) PWRT disabled (PWRTE bit set) See section on Power-on Reset for details
D010 D010A	IDD	Supply Current (Note 2)	—	1 3	4 10	mA	RC and XT osc configuration (Note 4) FOSC = 2.0 MHz, VDD = 5.5V FOSC = 2.0 MHz, VDD = 5.5V (During Flash programming)
D014			—	15	45	μA	LP osc configuration FOSC = 32 kHz, VDD = 2.0V, WDT disabled
D020 D021 D021A	IPD	Power-down Current (Note 3)	—	3.0 0.4 0.4	16 7.0 9.0	μA	VDD = 2.0V, WDT enabled, industrial VDD = 2.0V, WDT disabled, commercial VDD = 2.0V, WDT disabled, industrial
D022*	ΔIwDT	Module Differential Current (Note 5) Watchdog Timer	—	6.0 —	20 25*	μA	WDTE bit set, VDD = 4.0V, commercial WDTE bit set, VDD = 4.0V, industrial

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD,  
MCLR = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula  $IR = VDD/2Rext$  (mA) with Rext in kOhm.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD measurement.

**PIC16F84A**

**9.3 DC CHARACTERISTICS:** PIC16F84A-04 (Commercial, Industrial)  
 PIC16F84A-20 (Commercial, Industrial)  
 PIC16LF84A-04 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise stated)					
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D030 D030A D031 D032 D033 D034	VIL	Input Low Voltage I/O ports with TTL buffer  with Schmitt Trigger buffer MCLR, RA4/T0CKI OSC1 (XT, HS and LP modes) OSC1 (RC mode)	Vss	—	0.8	V	4.5V ≤ VDD ≤ 5.5V (Note 4)
			Vss	—	0.16VDD	V	entire range (Note 4)
			Vss	—	0.2VDD	V	entire range
			Vss	—	0.2VDD	V	(Note 1)
			Vss	—	0.3VDD	V	
			Vss	—	0.1VDD	V	
D040 D040A D041 D042 D043 D043A	VIH	Input High Voltage I/O ports with TTL buffer  with Schmitt Trigger buffer MCLR, RA4/T0CKI OSC1 (XT, HS and LP modes) OSC1 (RC mode)	—	—	VDD	V	4.5V ≤ VDD ≤ 5.5V (Note 4)
			2.0	—	VDD	V	entire range (Note 4)
			0.25VDD	—	VDD	V	
			+0.8	—	VDD	V	
			0.8 VDD	—	VDD	V	entire range
			0.9 VDD	—	VDD	V	(Note 1)
D050	VHYS	Hysteresis of Schmitt Trigger inputs	—	0.1	—	V	
D070	IPURB	PORTB weak pull-up current	50*	250*	400*	µA	VDD = 5.0V, VPIN = Vss
D060 D061 D063	III	Input Leakage Current (Note 2,3) I/O ports MCLR, RA4/T0CKI OSC1	—	—	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
			—	—	±5	µA	Vss ≤ VPIN ≤ VDD
			—	—	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. Do not drive the PIC16F84A with an external clock while the device is in RC mode, or chip damage may result.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: The user may choose the better of the two specs.

## PIC16F84A

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**9.4 DC CHARACTERISTICS:** PIC16F84A-04 (Commercial, Industrial)  
 PIC16F84A-20 (Commercial, Industrial)  
 PIC16LF84A-04 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise stated)					
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D080 D083	VOL	Output Low Voltage I/O ports OSC2/CLKOUT	—	—	0.6 0.6	V V	IOL = 8.5 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, (RC Mode Only)
D090 D092	VOH	Output High Voltage I/O ports (Note 3) OSC2/CLKOUT (Note 3)	VDD-0.7 VDD-0.7	— —	— —	V V	IOP = -3.0 mA, VDD = 4.5V IOP = -1.3 mA, VDD = 4.5V (RC Mode Only)
D150	VOD	Open Drain High Voltage RA4 pin	—	—	8.5	V	
D100	COSC2	Capacitive Loading Specs on Output Pins OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (RC mode)	—	—	50	pF	
D120 D121	ED VDRW	Data EEPROM Memory Endurance VDD for read/write	1M* VMIN	10M	— 5.5	E/W V	25°C at 5V VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	4	8*	ms	
D130 D131	EP VPR	Program Flash Memory Endurance VDD for read	100* VMIN	1000	— 5.5	E/W V	VMIN = Minimum operating voltage
D132 D133	VPEW TPEW	VDD for erasewrite Erase/Write cycle time	4.5	—	5.5 8	V ms	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. Do not drive the PIC16F84A with an external clock while the device is in RC mode, or chip damage may result.

**2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as coming out of the pin.

**4:** The user may choose the better of the two specs.

**PIC16F84A****9.5 AC (Timing) Characteristics****9.5.1 TIMING PARAMETER SYMOLOGY**

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T	F	Frequency	T	Time
---	---	-----------	---	------

Lowercase symbols (pp) and their meanings:

pp	2	to	os,osc	OSC1
	ck	CLKOUT	ost	oscillator start-up timer
	cy	cycle time	pwrt	power-up timer
	io	I/O port	rbt	RBx pins
	inp	INT pin	t0	TOCKI
	mc	MCLR	wdt	watchdog timer

Uppercase symbols and their meanings:

S	F	Fall	P	Period
	H	High	R	Rise
	I	Invalid (Hi-impedance)	V	Valid
	L	Low	Z	High Impedance

## PIC16F84A

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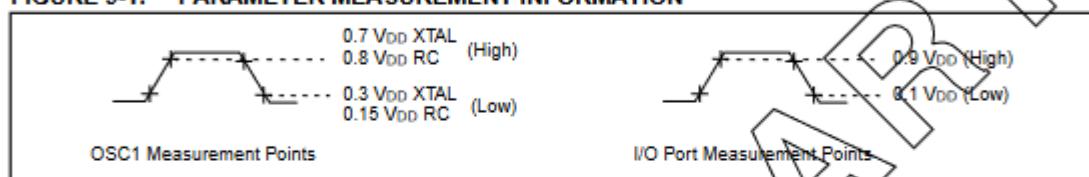
### 9.5.2 TIMING CONDITIONS

The temperature and voltages specified in Table 9-2 apply to all timing specifications unless otherwise noted. All timings are measured between high and low measurement points as indicated in Figure 9-1. Figure 9-2 specifies the load conditions for the timing specifications.

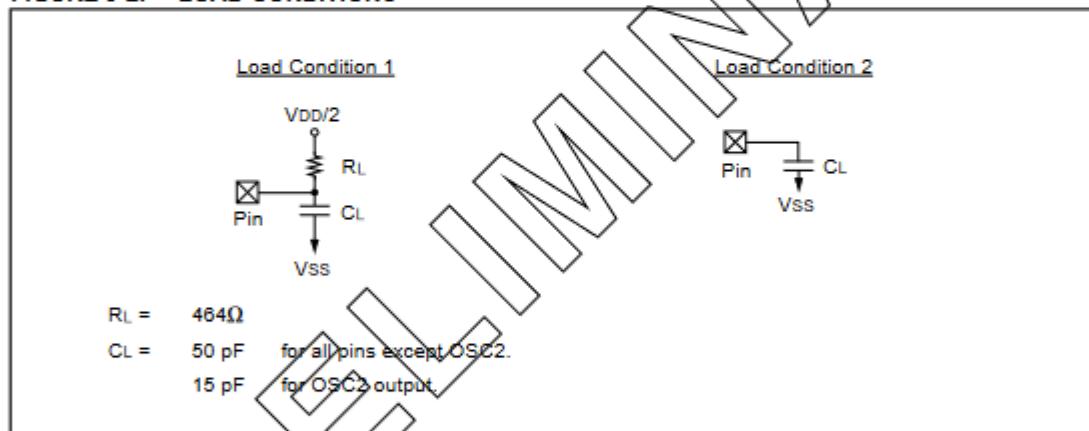
**TABLE 9-2 TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC**

AC CHARACTERISTICS	Standard Operating Conditions (unless otherwise stated)	
	Operating temperature	$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial
	Operating voltage $V_{DD}$ range as described in DC spec Section 9.1 and Section 9.2	

**FIGURE 9-1: PARAMETER MEASUREMENT INFORMATION**



**FIGURE 9-2: LOAD CONDITIONS**



**PIC16F84A**

## 9.5.3 TIMING DIAGRAMS AND SPECIFICATIONS

FIGURE 9-3: EXTERNAL CLOCK TIMING

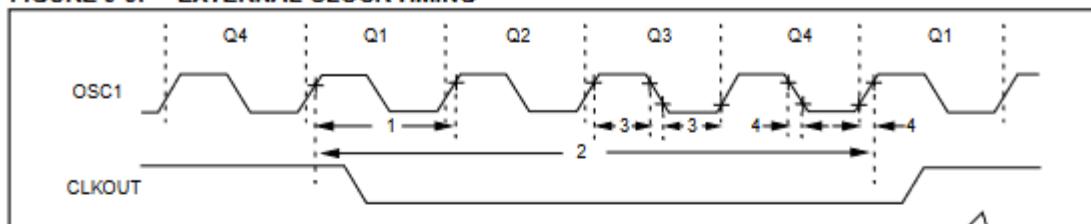


TABLE 9-3 EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Ty†	Max	Units	Conditions
	Fosc	External CLKIN Frequency <sup>(1)</sup>	DC	—	2	MHz	XT, RC osc (-04, LF)
			DC	—	4	MHz	XT, RC osc (-04)
			DC	—	20	MHz	HS osc (-20)
			DC	—	200	kHz	LP osc (-04, LF)
	1	Oscillator Frequency <sup>(1)</sup>	DC	—	2	MHz	RC osc (-04, LF)
			DC	—	4	MHz	RC osc (-04)
			0.1	—	2	MHz	XT osc (-04, LF)
			0.1	—	4	MHz	XT osc (-04)
			1.0	—	20	MHz	HS osc (-20)
			DC	—	200	kHz	LP osc (-04, LF)
	Tosc	External CLKIN Period <sup>(1)</sup>	500	—	—	ns	XT, RC osc (-04, LF)
			250	—	—	ns	XT, RC osc (-04)
			100	—	—	ns	HS osc (-20)
			50	—	—	μs	LP osc (-04, LF)
		Oscillator Period <sup>(1)</sup>	600	—	—	ns	RC osc (-04, LF)
			260	—	—	ns	RC osc (-04)
			600	—	10,000	ns	XT osc (-04, LF)
			250	—	10,000	ns	XT osc (-04)
	2	Instruction Cycle Time <sup>(1)</sup>	100	—	1,000	ns	HS osc (-20)
			5.0	—	—	μs	LP osc (-04, LF)
			—	—	—	—	—
	3	Clock in (OSC1) High or Low Time	60 *	—	—	ns	XT osc (-04, LF)
			50 *	—	—	ns	XT osc (-04)
			2.0 *	—	—	μs	LP osc (-04, LF)
			35 *	—	—	ns	HS osc (-20)
	4	Clock in (OSC1) Rise or Fall Time	25 *	—	—	ns	XT osc (-04)
			50 *	—	—	ns	LP osc (-04, LF)
			15 *	—	—	ns	HS osc (-20)

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period ( $T_{CY}$ ) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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FIGURE 9-4: CLKOUT AND I/O TIMING

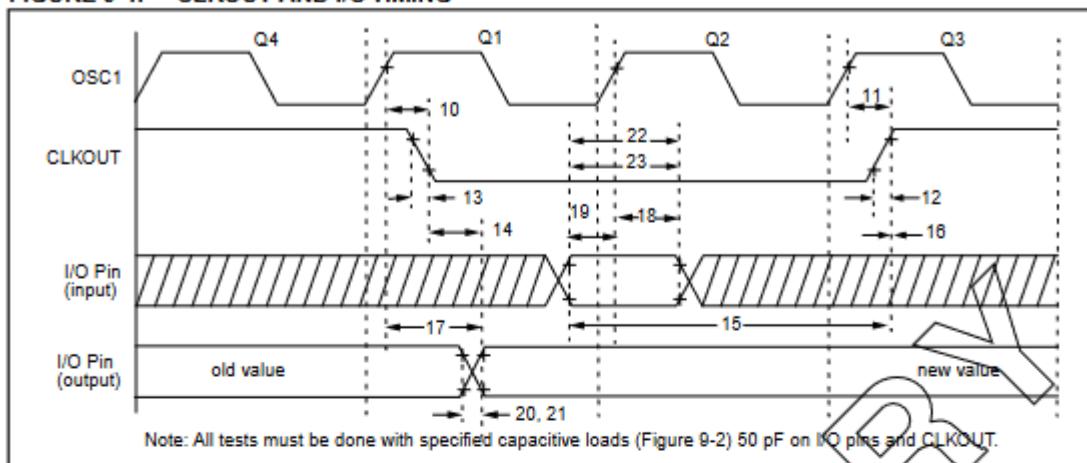


TABLE 9-4 CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓	—	15	30 *	ns	Note 1
10A	10A	Extended (LF)	—	15	120 *	ns	
11	TosH2ckH	OSC1↑ to CLKOUT↑	—	15	30 *	ns	Note 1
11A	11A	Extended (LF)	—	15	120 *	ns	
12	TckR	CLKOUT rise time	—	15	30 *	ns	Note 1
12A	12A	Extended (LF)	—	15	100 *	ns	
13	TckF	CLKOUT fall time	—	15	30 *	ns	Note 1
13A	13A	Extended (LF)	—	15	100 *	ns	
14	TckL2ioV	CLKOUT ↓ to Port out valid	—	—	0.5Tcy +20 *	ns	Note 1
15	TioV2ckH	Port in valid before CLKOUT ↑	Standard	0.30Tcy + 30 *	—	ns	Note 1
15A	15A	Extended (LF)	0.30Tcy + 80 *	—	—	ns	
16	TckH2iol	Port in hold after CLKOUT ↑	0 *	—	—	ns	Note 1
17	TosH2ioV	OSC11 (Q1 cycle) to Port out valid	Standard	—	125 *	ns	
17A	17A	Extended (LF)	—	—	250 *	ns	
18	TosH2iol	OSC11 (Q2 cycle) to Port input invalid (I/O in hold time)	Standard	10 *	—	ns	
18A	18A	Extended (LF)	10 *	—	—	ns	
19	TioV2osH	Port input valid to OSC11 (I/O in setup time)	Standard	-75 *	—	ns	
19A	19A	Extended (LF)	-175 *	—	—	ns	
20	TioR	Port output rise time	Standard	—	10	35 *	ns
20A	20A	Extended (LF)	—	10	70 *	ns	
21	TioF	Port output fall time	Standard	—	10	35 *	ns
21A	21A	Extended (LF)	—	10	70 *	ns	
22	Timp	INT pin high or low time	Standard	20 *	—	ns	
22A	22A	Extended (LF)	55 *	—	—	ns	
23	Trbp	RB7:RB4 change INT high or low time	Standard	Tosc §	—	ns	
23A	23A	Extended (LF)	Tosc §	—	—	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ By design

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

**PIC16F84A**

FIGURE 9-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

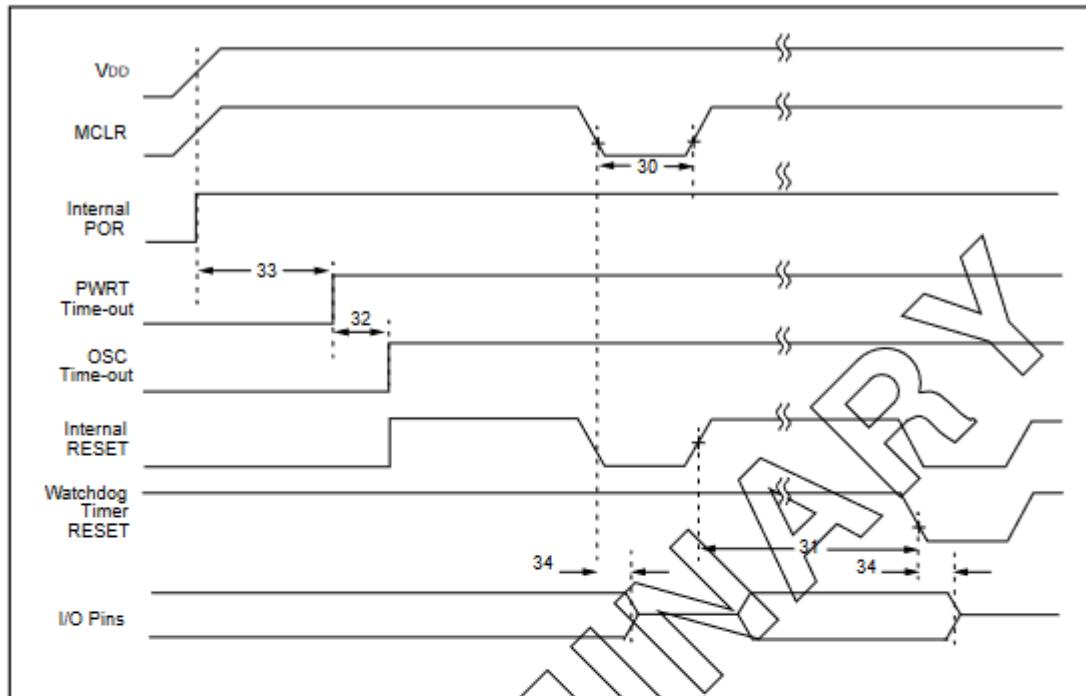


TABLE 9-5 RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmCL	MCLR Pulse Width (low)	2 *	—	—	μs	VDD = 5.0V, extended
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7 *	18	33 *	ms	VDD = 5.0V, extended
32	Tost	Oscillation Start-up Timer Period	—	1024Tosc	—	ms	Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period	28 *	72	132 *	ms	VDD = 5.0V, extended
34	Tioz	I/O Hi-impedance from MCLR Low or reset	—	—	100 *	ns	—

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 9-6: TIMER0 CLOCK TIMINGS

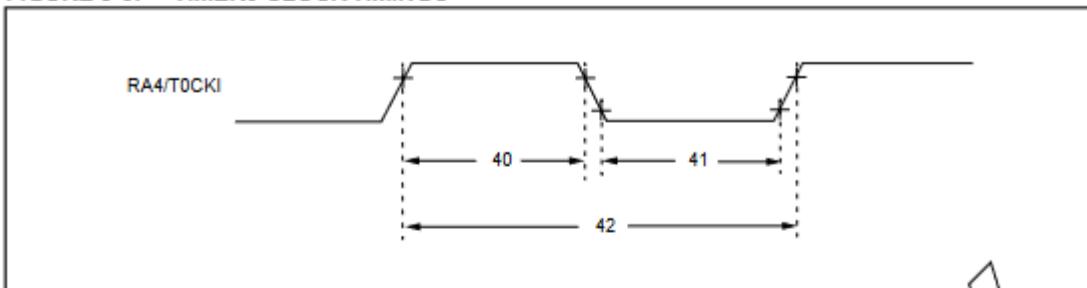


TABLE 9-6 TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	$0.5T_{CY} + 20^*$	—	—	ns
			With Prescaler	50 *	—	ns	$2.0V \leq V_{DD} \leq 3.0V$
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	$0.5T_{CY} + 20^*$	—	—	ns
			With Prescaler	50 *	—	ns	$3.0V \leq V_{DD} \leq 6.0V$
42	Tt0P	T0CKI Period	$T_{CY} + 40^*$		N	ns	N = prescale value (2, 4, ..., 256)

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PRELIMINARY

## PIC16F84A

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### 10.0 DC & AC CHARACTERISTICS GRAPHS/TABLES

No data available at this time.

PRELIMINARY

## PIC16F84A

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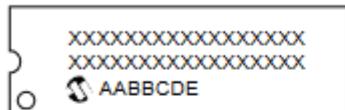
NOTES:

## PIC16F84A

### 11.0 PACKAGING INFORMATION

#### 11.1 Package Marking Information

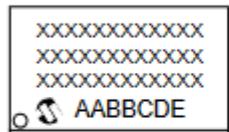
18L PDIP



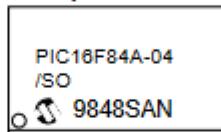
Example



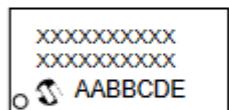
18L SOIC



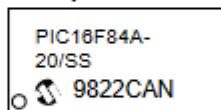
Example



20L SSOP



Example



**Legend:**

MM...M	Microchip part number information
XX...X	Customer specific information*
AA	Year code (last 2 digits of calendar year)
BB	Week code (week of January 1 is week '01')
C	Facility code of the plant at which wafer is manufactured
O	= Outside Vendor
C	= 5" Line
S	= 6" Line
H	= 8" Line
D	Mask revision number
E	Assembly code of the plant or country of origin in which part was assembled

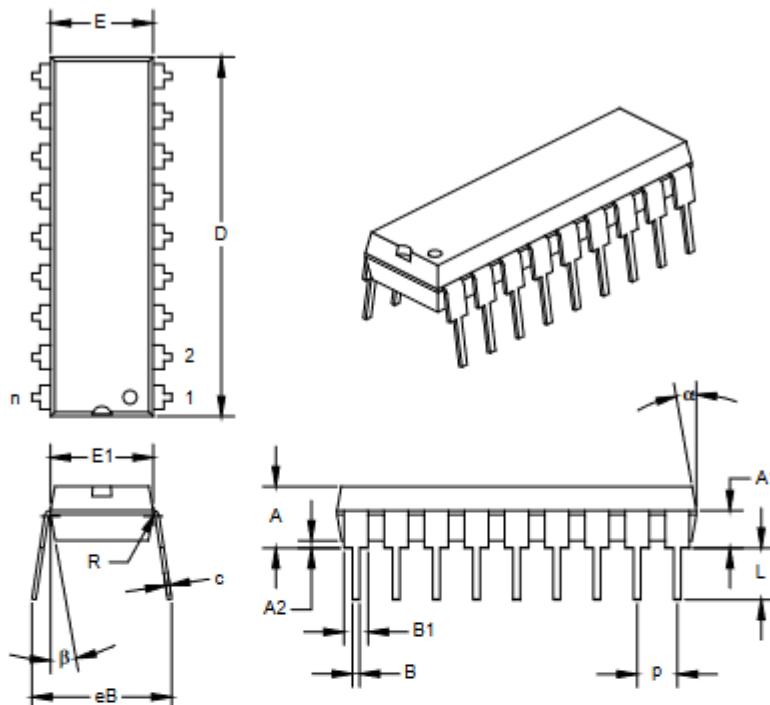
**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

- \* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

## PIC16F84A

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### 11.2 K04-007 18-Lead Plastic Dual In-line (P) – 300 mil

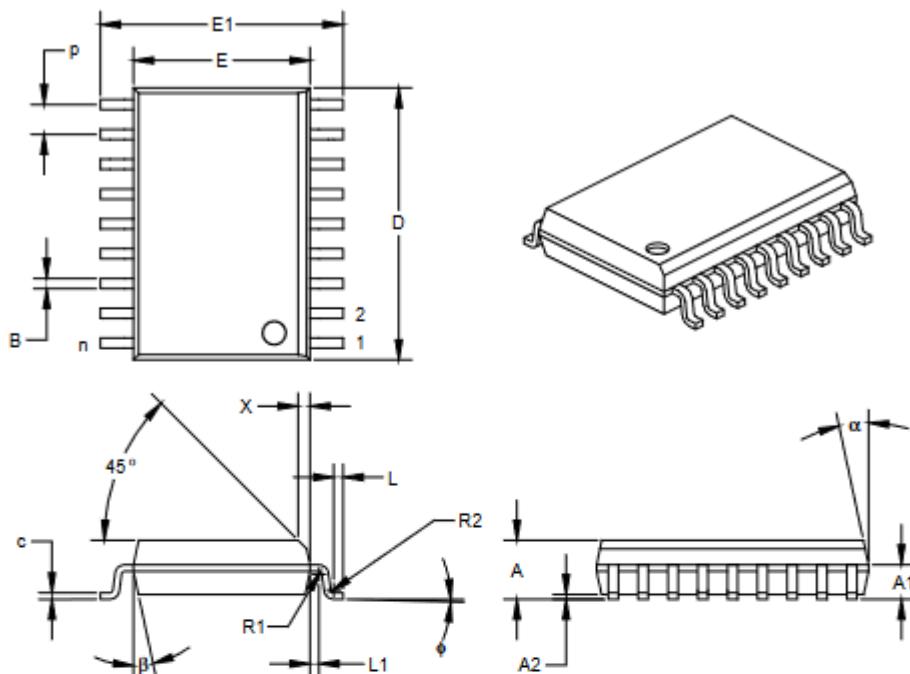


Units	INCHES*			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
Dimension Limits						
PCB Row Spacing		0.300			7.62	
Number of Pins	n	18			18	
Pitch	p	0.100			2.54	
Lower Lead Width	B	0.013	0.018	0.023	0.33	0.46
Upper Lead Width	B1†	0.055	0.060	0.065	1.40	1.52
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13
Lead Thickness	c	0.005	0.010	0.015	0.13	0.25
Top to Seating Plane	A	0.110	0.155	0.155	2.79	3.94
Top of Lead to Seating Plane	A1	0.075	0.095	0.115	1.91	2.41
Base to Seating Plane	A2	0.000	0.020	0.020	0.00	0.51
Tip to Seating Plane	L	0.125	0.130	0.135	3.18	3.30
Package Length	D‡	0.890	0.895	0.900	22.81	22.73
Molded Package Width	E‡	0.245	0.255	0.265	6.22	6.48
Radius to Radius Width	E1	0.230	0.250	0.270	5.84	6.35
Overall Row Spacing	eB	0.310	0.349	0.387	7.87	8.85
Mold Draft Angle Top	α	5	10	15	5	10
Mold Draft Angle Bottom	β	5	10	15	5	10

\* Controlling Parameter.

† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

**PIC16F84A****11.3 K04-051 18-Lead Plastic Small Outline (SO) – Wide, 300 mil**

Units		INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Dimension Limits							
Pitch	p		0.050			1.27	
Number of Pins	n		18			18	
Overall Pack. Height	A	0.093	0.099	0.104	2.36	2.50	2.64
Shoulder Height	A1	0.048	0.058	0.068	1.22	1.47	1.73
Standoff	A2	0.004	0.008	0.011	0.10	0.19	0.28
Molded Package Length	D <sup>†</sup>	0.450	0.456	0.462	11.43	11.58	11.73
Molded Package Width	E <sup>†</sup>	0.292	0.296	0.299	7.42	7.51	7.59
Outside Dimension	E1	0.394	0.407	0.419	10.01	10.33	10.64
Chamfer Distance	X	0.010	0.020	0.029	0.25	0.50	0.74
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	ϕ	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.009	0.011	0.012	0.23	0.27	0.30
Lower Lead Width	B <sup>†</sup>	0.014	0.017	0.019	0.36	0.42	0.48
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

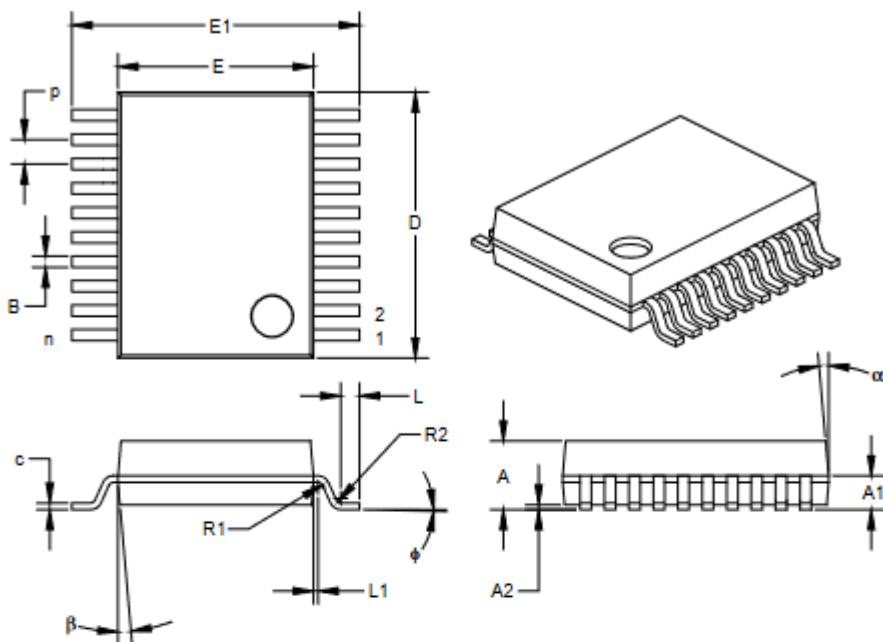
\* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B".

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E".

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### 11.4 K04-072 20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.026			0.65	
Number of Pins	n		20			20	
Overall Pack. Height	A	0.068	0.073	0.078	1.73	1.86	1.99
Shoulder Height	A1	0.026	0.036	0.046	0.66	0.91	1.17
Standoff	A2	0.002	0.005	0.008	0.05	0.13	0.21
Molded Package Length	D <sup>‡</sup>	0.278	0.283	0.289	7.07	7.20	7.33
Molded Package Width	E <sup>†</sup>	0.205	0.208	0.212	5.20	5.29	5.38
Outside Dimension	E1	0.301	0.306	0.311	7.65	7.78	7.90
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.015	0.020	0.025	0.38	0.51	0.64
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.005	0.007	0.009	0.13	0.18	0.22
Lower Lead Width	B <sup>†</sup>	0.010	0.012	0.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B".

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E".

**PIC16F84A****APPENDIX A: REVISION HISTORY**

Version	Date	Revision Description
A	9/14/98	This is a new data sheet. However, the devices described in this data sheet are the upgrades to the devices found in the <i>PIC16F8X Data Sheet</i> , DS30430C.

**APPENDIX B: CONVERSION CONSIDERATIONS**

Considerations for converting from one PIC16X8X device to another are listed in Table B-1.

**TABLE B-1: CONVERSION CONSIDERATIONS - PIC16C84, PIC16F83/F84, PIC16CR83/CR84, PIC16F84A**

Difference	PIC16C84	PIC16F83/F84	PIC16CR83/ CR84	PIC16F84A
Program Memory size	1k x 14	512 x 14 / 1k x 14	512 x 14 / 1k x 14	1k x 14
Data Memory size	36 x 8	36 x 8 / 68 x 8	36 x 8 / 68 x 8	68 x 8
Voltage Range	2.0V - 6.0V (-40°C to +85°C)	2.0V - 6.0V (-40°C to +85°C)	2.0V - 6.0V (-40°C to +85°C)	2.0V - 5.5V (-40°C to +125°C)
Maximum Operating Frequency	10MHz	10MHz	10MHz	20MHz
Supply Current (IDD). See parameter # D014 in the electrical spec's for more detail.	IDD (typ) = 60µA IDD (max) = 400µA (LP osc, FOSC = 32kHz, VDD = 2.0V, WDT disabled)	IDD (typ) = 15µA IDD (max) = 45µA (LP osc, FOSC = 32kHz, VDD = 2.0V, WDT disabled)	IDD (typ) = 15µA IDD (max) = 45µA (LP osc, FOSC = 32kHz, VDD = 2.0V, WDT disabled)	IDD (typ) = 15µA IDD (max) = 45µA (LP osc, FOSC = 32kHz, VDD = 2.0V, WDT disabled)
Power-down Current (IPD). See parameters # D020, D021, and D021A in the electrical spec's for more detail.	IPD (typ) = 26µA IPD (max) = 100µA (VDD = 2.0V, WDT disabled, industrial)	IPD (typ) = 0.4µA IPD (max) = 9µA (VDD = 2.0V, WDT disabled, industrial)	IPD (typ) = 0.4µA IPD (max) = 6µA (VDD = 2.0V, WDT disabled, industrial)	IPD (typ) = 0.4µA IPD (max) = 9µA (VDD = 2.0V, WDT disabled, industrial)
Input Low Voltage (VIL). See parameters # D032 and D034 in the electrical spec's for more detail.	VIL (max) = 0.2VDD (Osc1, RC mode)	VIL (max) = 0.1VDD (Osc1, RC mode)	VIL (max) = 0.1VDD (Osc1, RC mode)	VIL (max) = 0.1VDD (Osc1, RC mode)
Input High Voltage (VIH). See parameter # D040 in the electrical spec's for more detail.	VIH (min) = 0.38VDD (I/O Ports with TTL, 4.5V ≤ VDD ≤ 5.5V)	VIH (min) = 2.4V (I/O Ports with TTL, 4.5V ≤ VDD ≤ 5.5V)	VIH (min) = 2.4V (I/O Ports with TTL, 4.5V ≤ VDD ≤ 5.5V)	VIH (min) = 2.4V (I/O Ports with TTL, 4.5V ≤ VDD ≤ 5.5V)
Data EEPROM Memory Erase/Write cycle time (TDEW). See parameter # D122 in the electrical spec's for more detail.	TDEW (typ) = 10ms TDEW (max) = 20ms	TDEW (typ) = 10ms TDEW (max) = 20ms	TDEW (typ) = 10ms TDEW (max) = 20ms	TDEW (typ) = 4ms TDEW (max) = 10ms

## PIC16F84A

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TABLE B-1: CONVERSION CONSIDERATIONS - PIC16C84, PIC16F83/F84, PIC16CR83/CR84, PIC16F84A

Difference	PIC16C84	PIC16F83/F84	PIC16CR83/CR84	PIC16F84A
Port Output Rise/Fall time (TioR, TioF). See parameters #20, 20A, 21, and 21A in the electrical spec's for more detail.	TioR, TioF (max) = 25ns (C84) TioR, TioF (max) = 60ns (LC84)	TioR, TioF (max) = 35ns (C84) TioR, TioF (max) = 70ns (LC84)	TioR, TioF (max) = 35ns (C84) TioR, TioF (max) = 70ns (LC84)	TioR, TioF (max) = 35ns (C84) TioR, TioF (max) = 70ns (LC84)
MCLR on-chip filter. See parameter #30 in the electrical spec's for more detail.	No	Yes	Yes	Yes
PORTA and crystal oscillator values less than 500kHz	For crystal oscillator configurations operating below 500kHz, the device may generate a spurious internal Q-clock when PORTA<0> switches state.	N/A	N/A	N/A
RBO/INT pin	TTL	TTL/ST* (* Schmitt Trigger)	TTL/ST* (* Schmitt Trigger)	TTL/ST* (* Schmitt Trigger)
EEADR<7:6> and I <sub>DD</sub>	It is recommended that the EEADR<7:6> bits be cleared. When either of these bits is set, the maximum I <sub>DD</sub> for the device is higher than when both are cleared.	N/A	N/A	N/A
The polarity of the PWRTE bit	PWRTE	<u>PWRTE</u>	<u>PWRTE</u>	<u>PWRTE</u>
Recommended value of R <sub>EXT</sub> for RC oscillator circuits	R <sub>EXT</sub> = 3kΩ - 100kΩ	R <sub>EXT</sub> = 5kΩ - 100kΩ	R <sub>EXT</sub> = 5kΩ - 100kΩ	R <sub>EXT</sub> = 3kΩ - 100kΩ
GIE bit unintentional enable	If an interrupt occurs while the Global Interrupt Enable (GIE) bit is being cleared, the GIE bit may unintentionally be re-enabled by the user's Interrupt Service Routine (the RETFIE instruction).	N/A	N/A	N/A
Packages	PDIP, SOIC	PDIP, SOIC	PDIP, SOIC	PDIP, SOIC, SSOP

## **PIC16F84A**

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**NOTES:**

# PIC16F84A

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## APPENDIX C: MIGRATION FROM BASELINE TO MIDRANGE DEVICES

This section discusses how to migrate from a baseline device (i.e., PIC16C5X) to a midrange device (i.e., PIC16CXXX).

The following is the list of feature improvements over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14 bits. This allows larger page sizes both in program memory (2K now as opposed to 512 before) and the register file (128 bytes now versus 32 bytes before).
2. A PC latch register (PCLATH) is added to handle program memory paging. PA2, PA1 and PA0 bits are removed from the status register and placed in the option register.
3. Data memory paging is redefined slightly. The STATUS register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDIW, and SUBIW. Two instructions, TRIS and OPTION, are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers, the Oscillator Start-up Timer (OST) and Power-up Timer (PWRT), are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt on change features.
13. T0CKI pin is also a port pin (RA4/T0CKI).
14. FSR is a full 8-bit register.
15. "In system programming" is made possible. The user can program PIC16CXX devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).

To convert code written for PIC16C5X to PIC16F84A, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables for reallocation.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.

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# PIC16F84A

## PIC16F84A PRODUCT IDENTIFICATION SYSTEM

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PART NO.	-XX	X	/XX	XXX	Examples:
Device	Frequency Range	Temperature Range	Package	Pattern	
Device	PIC16F84A <sup>(1)</sup> , PIC16F84AT <sup>(2)</sup> PIC16LF84A <sup>(1)</sup> , PIC16LF84AT <sup>(2)</sup>				a) PIC16F84A -04/P 301 = Commercial temp., PDIP package, 4 MHz, normal V <sub>DD</sub> limits, QTP pattern #301.
Frequency Range	04 = 4 MHz 20 = 20 MHz				b) PIC16LF84A - 04I/SO = Industrial temp., SOIC package, 200 kHz, Extended V <sub>DD</sub> limits.
Temperature Range	blank = 0°C to +70°C (Commercial) I = -40°C to +85°C (Industrial)				c) PIC16F84A - 20I/P = Industrial temp., PDIP package, 20MHz, normal V <sub>DD</sub> limits.
Package	P = PDIP SO = SOIC (Gull Wing, 300 mil body) SS = SSOP				
Pattern	3-digit Pattern Code for QTP, ROM (blank otherwise)				Note 1: F = Standard V <sub>DD</sub> range LF = Extended V <sub>DD</sub> range 2: T = in tape and reel - SOIC, SSOP packages only.



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## 11 - Conclusión y agradecimientos.

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Ha sido bastante difícil al principio. Debido a que el software de KiCAD (v5.0.0) carece de ciertos componentes y huellas actualizadas que se han usado para este proyecto. Por lo que ha tocado crear desde cero nuestra propia librería, con sus huellas, medidas de componentes, rectificación de medidas (varias veces), diseñar y rutear todo, etc.

Es un buen software, y que está a la altura de cualquier otro gratuito. Lo cual me ha contentado bastante para la iniciación en el mundo del montaje y mantenimiento electrónico. En mi caso particular, es la primera vez que diseño una placa PCB. Y tras los errores cometidos, veo que han sido los típicos de alguien nuevo en el campo.

Agradecer al profesor Rafa Climent Cabanes por enseñarnos el mundo electrónico digital. Y asegurarse que aprendamos todo lo necesario, con tal de valernos por nosotros mismos, allá donde podamos estar en el futuro, sea por trabajo, o por hobby en el hogar.

Animo a cualquiera, a que lleve a cabo este mismo proyecto, siguiendo los pasos que aquí se han mostrado, por la practicidad y utilidad del mismo.

Sin nada más que decir, gracias por su grata atención.