ECEN 5613 Embedded System Design
Fall 2019 Lab #2 Signoff Sheet – Part 1 Elements 9/27/2019

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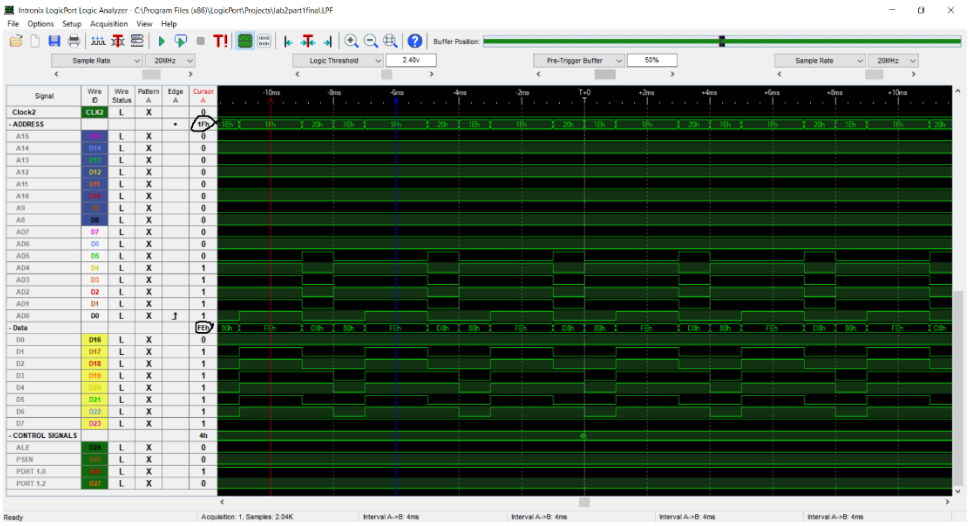
Q1. Using the instruction set summary tables (available in the programmer's guide or instruction set documents), calculate how long the ISR takes to execute once, assuming a clock frequency of 11.0592 MHz. You will likely have some conditional jumps in your ISR code, so make sure to calculate both the longest and shortest time it takes the ISR to execute.
Answer:

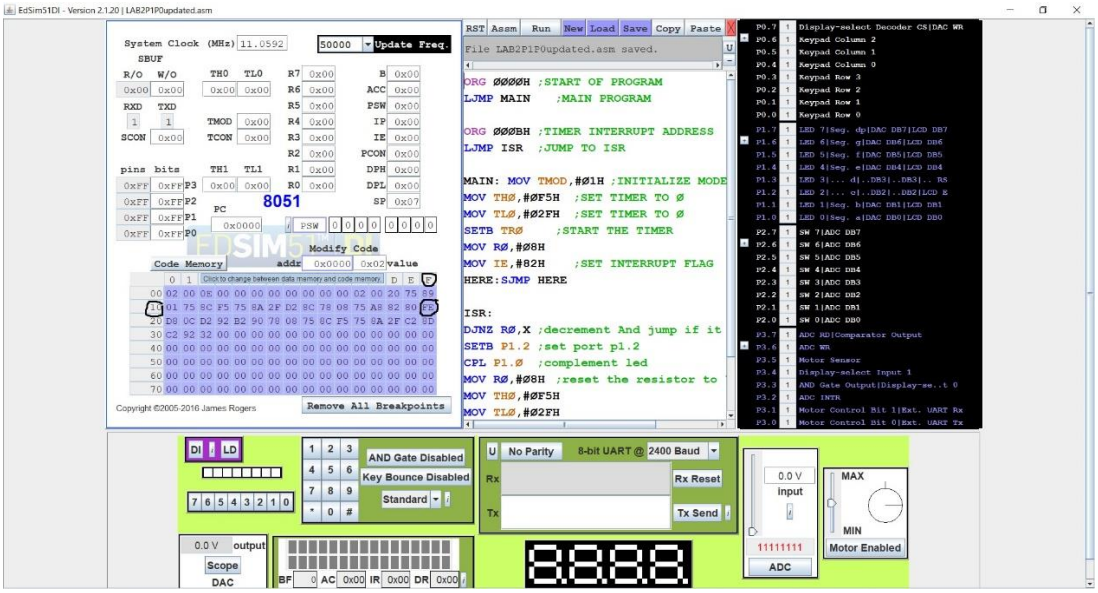
ISR	Machine cycles
DJNZ R0,X	2
CPL P1.0	1
MOV R0,#08H	1
MOV TH0,#0F5H	1
MOV TL0,#02FH	1
X: SETB P1.2	1
CLR TF0	1
CLR P1.2	1
RETI	2
Total	11

Maximum ISR time=11*1.085=11.935 microsec

Minimum ISR time=7*1.085=7.595 microsec

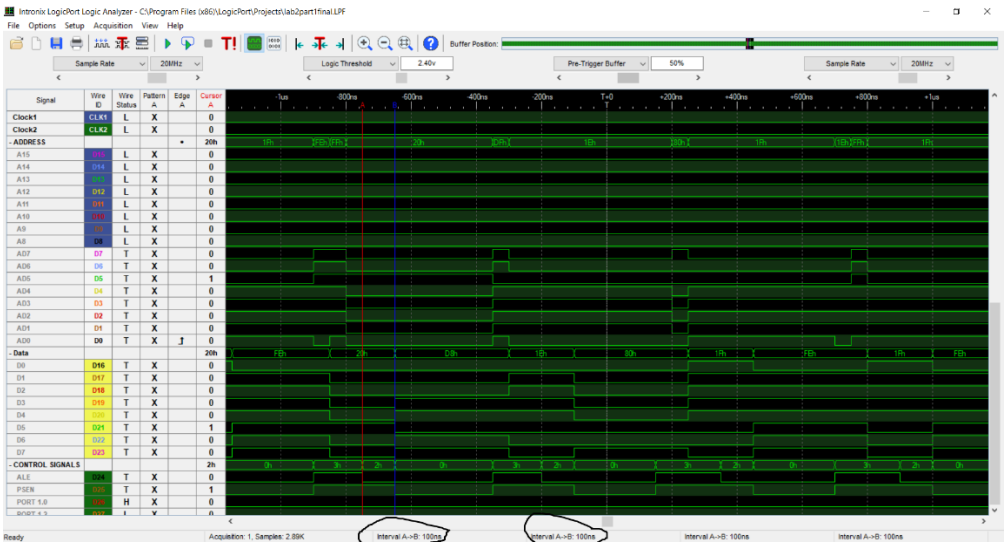
Q2. Using the state mode, capture a sequence of instructions and compare the sequence to the listing file for the code being executed. For the state clock, you can investigate using PSEN , READ , or ALE. Before your demo to the TA, prepare one screen capture of the logic analyzer triggered on a fetch in state mode.





Q3.Using the timing mode, measure the time which elapses from when the 74LS373 latches the address supplied by the 8051 to when the PSEN signal is activated during an instruction fetch. Before your demo to the TA, annotate a screen capture to show the measurement of tLLPL in timing mode and prove that your measured time meets the processor data sheet specification for tLLPL.

Answer:



The Siemens data sheet mentions that minimum value of tllpl=tclcl-25.
Since we are using a 11.0592Mhz frequency we need to calculate tclcl as 1/tclcl=11.0592.Therefore tclcl=90.042nsec.Therefore,tllpl(min)=90-25=65nsec.
Therefore we need to get minimum of 65 nsec and we get an output of 100nsec.