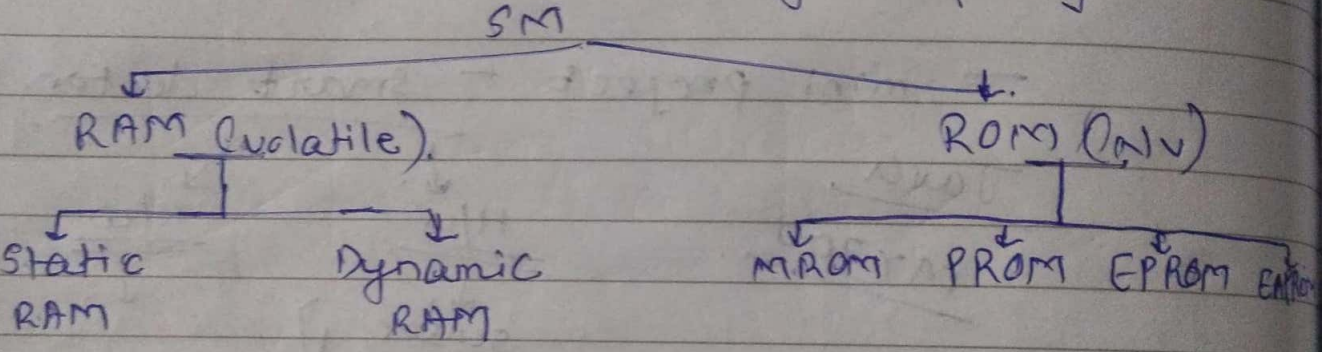
॥ श्री ॥

VLSI

Unit 3: CMOS Subsystem Design.

→ Semiconductor memory :-

- storing digital data
- small size, large capacity.



MROM ⇒ data is permenant.
PROM ⇒ special program and it is programmed memory.
EPROM ⇒ multiple times programable. UV light erasing.
E^2PROM ⇒ electrical erasing.

— memory array Organisation.

- describes how the structural arrangement of memory cells will be
- memory cells
- coord lines and Bit lines.

Types of organisation :-

1D organisation (Linear).
2D organisation (Matrix/Grid).
3D organisation.

— RAM (Random Access Memory).

- volatile
- Fast
- Temorarey
- Read/write.

— SRAM
flip-flop (transistors).
faster,
expensive
CPU cache

— DRAM.
capacitors.
slow
cheap.
periodic refreshing.

— SRAM.

- static RAM
- stores data in flip-flops. (Single bit only).
- these flip-flops are made from transistors.
- 6-transistors collectively create 1 flip-flop.
- volatile
- fast
- CPU cache (L1, L2, L3).

— 6T SRM cell.

- made using 6 transistors
- they create 1 flip-flop.
- holds single-bit value. (0 or 1).
- 2 cross-coupled (4 transistors)
- 2 access transistor total (6 transistors) (NMOS).

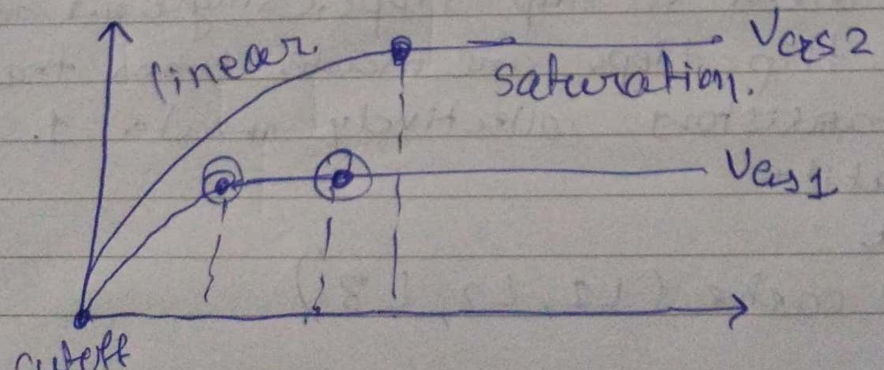
— sense amplifier.

- used to detect and amplify small voltage difference to make a clear logic 1 or 0.
- only during read operation.

— बाकी chat GPT.

— Unit 6

I-V characteristics of MOSFET.



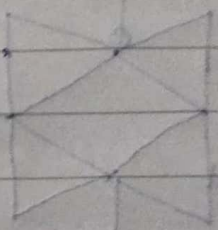
CMOS Inverter.

— combination of NMOS & PMOS Transistor.

DC transfer characteristics.

PMOS	NMOS	Behaviour.
1	0	1.
1	1	Transition zone.
0	1	0.

Max V. == 0 } active low.
Min V == 1. }



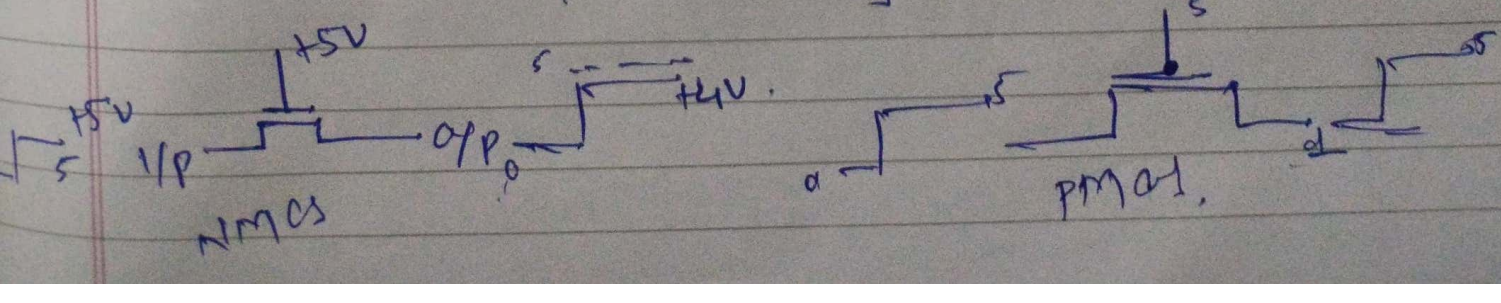
Voltage transfer.

PMOS	NMOS	Behavior.
1	0	1
1	1	Inverter
0	1	0.

— Pass transistor logic (PTL).

— NMOS used as a switch to pass logic signals.

→ NMOS pass strong '0' but week '1'
PMOS pass strong '1' but week '0'.



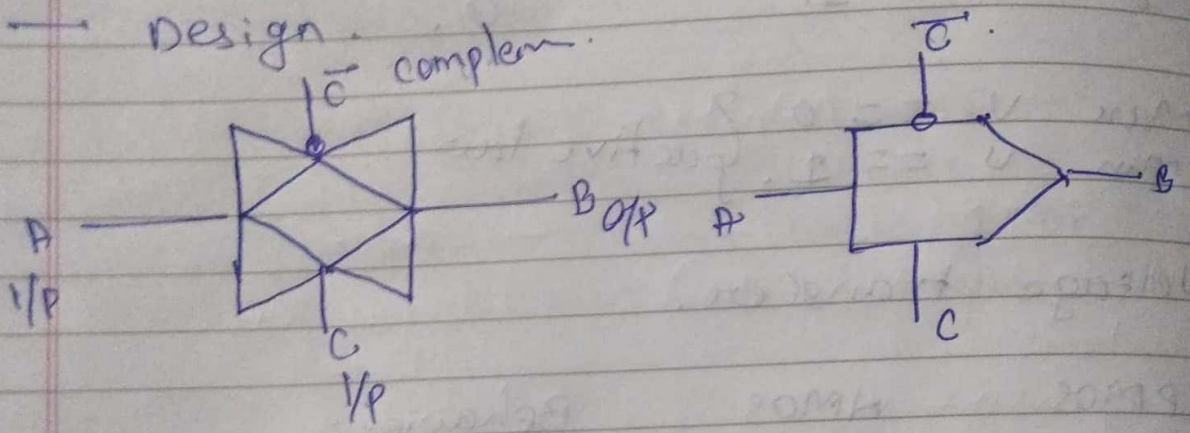
— Transmission Gate.

Combin^ of NMOS & PMOS in parallel

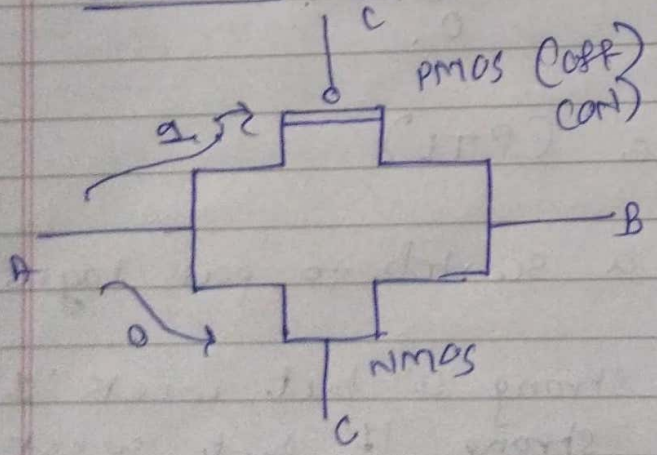
NMOS → 0 (well) } special Sb.
PMOS → 1 (well)

combined together NO LOSS.

— Design.



Circuit



C	A	B
0	0	H.I
0	1	H.I.
1	0	0
1	1	1