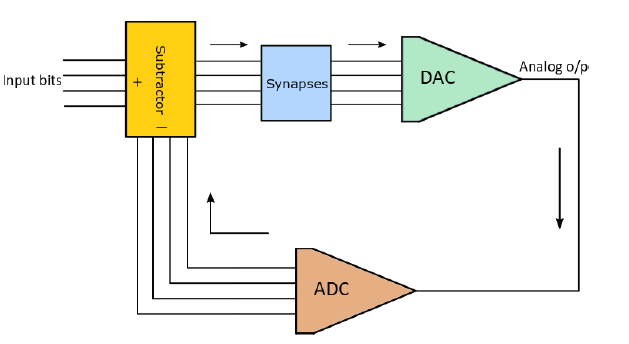
1. Ideal Four bit DAC trained by ADC in feedback:

Stochastic gradient descent is used and the memristors used are y-flash based hence exponential I-V characteristics.



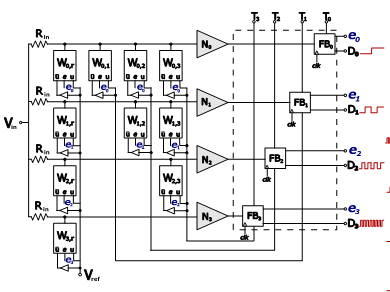
2. Algorithm used:

i) Analog output of the GD algorithm

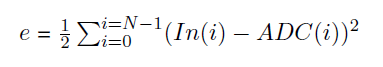
Agd = (Rf\*(Iread\*(exp(D(x,1)/mVT))\*exp(-Vth(1)/mVT)\*(D(x,1)/1.8) + Iread\*(exp(D(x,2)/mVT))\*exp(-Vth(2)/mVT)\*(D(x,2)/1.8) + Iread\*(exp(D(x,3)/mVT))\*exp(-Vth(3)/mVT)\*(D(x,3)/1.8) + Iread\*(exp(D(x,4)/mVT))\*exp(-Vth(4)/mVT)\*(D(x,4)/1.8)));

ii)The DAC used is generic. In the feedback each Agd value is classified in a digital level by comparison to different Vref levels.

NN ADC architecture which can be incorporated to above design:



2. Error Metric:



3. Update Rule:



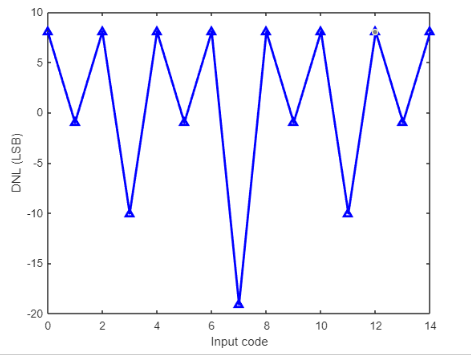
where -

 = Binary-varied update rule

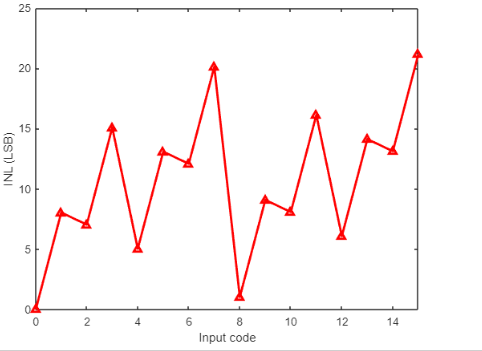
Agd(k) = Analog output from DAC

The update rule is completely digital and allows different type of ADC to be used. No analog labels are used for training.

5. DNL (LSB):

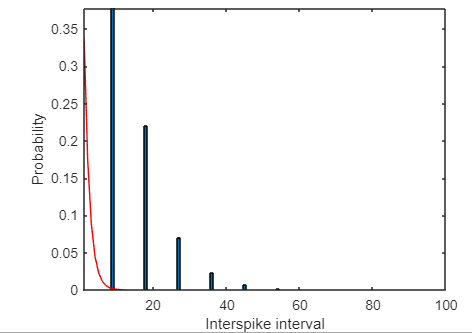


6. INL (LSB):



* Vector Matrix Multiplication: Mathematically implemented in MATLAB.
* Spikes Generation(Preliminary requirement before STDP):

Poisson process is stochastic, each spike train will look different, even though they have the same average number of spikes.



Exponentially distributed interspike intervals can be seen. To see spikes versus time steps raster plot is used.

