module sixteen\_one\_test;

reg [15:0]a;

reg b;

reg clk;

wire [15:0]p;

sixteen\_one PP(a,b,clk,p);

initial begin

a=16'b1111000000000011;b=1'b1;

#1000 a=16'b1111000000001101;b=1'b1;

end

initial

begin

clk=1'b1;

forever #100 clk=~clk;

end

endmodule