module sixteen\_four\_test;

reg [15:0]a;

reg [3:0]b;

reg clk;

wire [19:0]m;

sixteen\_four PP(a,b,clk,m);

initial begin

a=16'b1111000000000011;b=4'b1111;

#1000 a=16'b1111000000001101;b=4'b1100;

end

initial

begin

clk=1'b1;

forever #100 clk=~clk;

end

endmodule