module nzau(A,B,asign,bsign,clk,C,sign);

input [15:0]A;

input [15:0]B;

input asign;

input bsign;

input clk;

output reg [31:0]C;

output sign;

abs a(A,X);

abs b(B,Y);

lzc c(X,C1);

lzc d(Y,C2);

reg D;

wire [31:0]Y;

sixteen\_sign S(A,B,clk,asign,bsign,Y,sign);

always@(A,B)

begin

D=C1+C2;

if(D >> 4'b0110)

C=Y;

else

C=0;

end

endmodule