module nzau\_test;

reg [15:0]A;

reg [15:0]B;

reg asign;

reg bsign;

reg clk;

wire [31:0]C;

wire sign;

nzau ss(A,B,asign,bsign,clk,C,sign);

initial

begin

#10 A=16'b0000101010101010; B=16'b0000101010101010;asign=1'b1; bsign=1'b1;

end

initial

begin

clk=1'b1;

forever #100 clk=~clk;

end

endmodule