module main\_vio(

input clk,

output [7:0]sum);

wire [15:0] a;

wire [15:0] b;

wire [31:0] c;

wire clk,asign,bsign,csign;

wire [32:0] m;

wire sign;

mac g2(a,b,c,clk,asign,bsign,csign,m,sign);

vio\_0 V1(clk,m,sign,a,b,c,asign,bsign,csign);

assign m[7:0]=sum;

endmodule