

# YOUR NAME

yourname@gmail.com | (213) xxx-xxxx | San Diego, CA | [linkedin.com/your-name](https://www.linkedin.com/your-name)

## EDUCATION

**University Name, Location, State**

**Aug 2019 - May 2021**

Master of Science in Electrical & Computer Engineering **GPA: 4.00**

**University Name, Location, State**

**Jul 2014 - Jun 2018**

Bachelor of Science in Electronics & Communications Engineering **GPA: 10/10**

## PROFESSIONAL EXPERIENCE

**Position, Company, San Diego, CA 92121**

**Jul 2022 - Present**

- Each item should be a descriptive point
- Use good set of action verbs
- Communicated and worked with multi-disciplined teams

**Internship - Company, San Jose**

**Month Year - Month Year**

- Working on Design
- Perform coding
- Communicated and worked with multi-disciplined teams

**Internship - Company, San Jose**

**Month Year - Month Year**

- Working on Design
- Perform coding
- Communicated and worked with multi-disciplined teams

**Internship - Company, San Jose**

**Month Year - Month Year**

- Working on Design
- Perform coding
- Communicated and worked with multi-disciplined teams

## SKILLS

- **Programming Languages:** Python, Verilog, C++, Linux, C
- **Software:** QuestaSim, Cadence Virtuoso
- **Coursework:** List it all, don't hold back

## ACADEMIC PROJECTS

**Multiprocessor Design | VS Code | Python | PrimeTime | Verilog**

**Nov 2020 - Dec 2020**

- Designed pipelined processor
- Instantiated 4 processors
- Accomplished full placement
- Carried out power optimization

**Multiprocessor Design | VS Code | Python | PrimeTime | Verilog**

**Nov 2020 - Dec 2020**

- Designed pipelined processor
- Instantiated 4 processors
- Accomplished full placement
- Carried out power optimization

**Multiprocessor Design | VS Code | Python | PrimeTime | Verilog**

**Nov 2020 - Dec 2020**

- Designed pipelined processor
  - Instantiated 4 processors
- Multiprocessor Design | VS Code | Python | PrimeTime | Verilog**
- Designed pipelined processor
  - Instantiated 4 processors

**Nov 2020 - Dec 2020**

**Multiprocessor Design | VS Code | Python | PrimeTime | Verilog**

**Nov 2020 - Dec 2020**

- Designed pipelined processor
- Instantiated 4 processors

## INVOLVEMENT AND LEADERSHIP

- **LinkedIn Learning Student Champion 2020** - It was fun
- **Viterbi Mentor** - It was great too
- **Social Worker** - It was humbling