EE 652: IC Design Lab

Assignment - 3: System Verilog - Pipelined Convolution

(due Midnight Feb 16)

Date: 2nd Feb 2022

General Instructions:

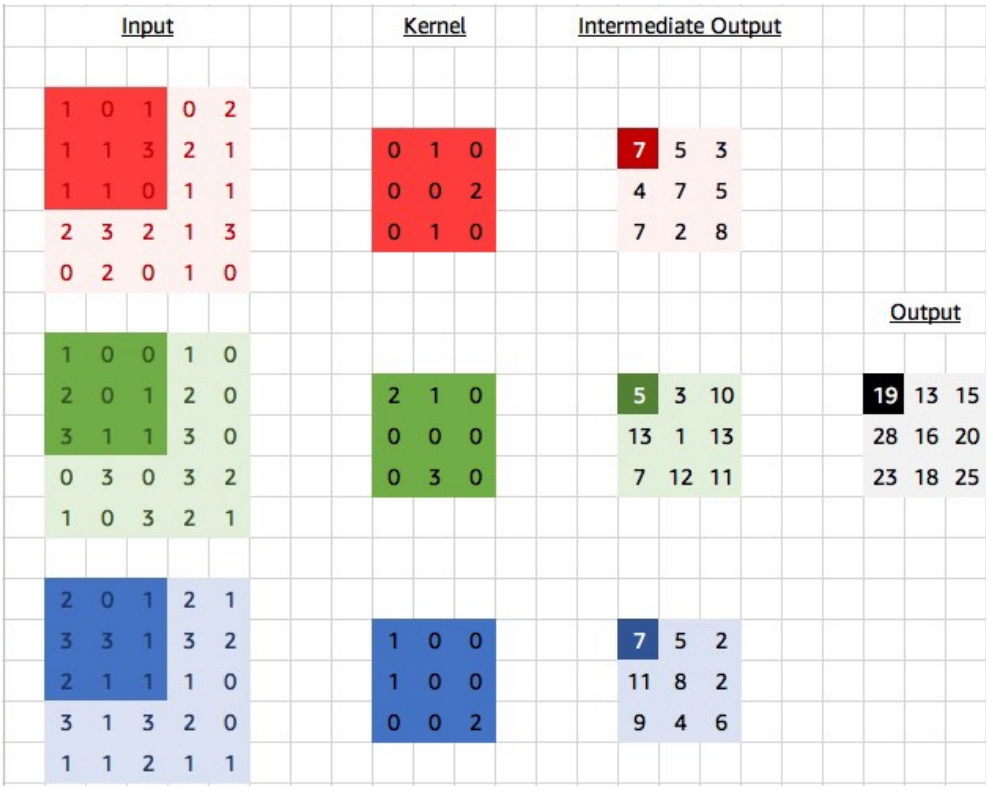
1. Total Marks: 200
2. **Any instances of plagiarism will not be tolerated.**
3. Submissions received 2 days after the due date will not be graded. 20% per day penalty for late submission.

Submission Instruction:

1. Write top_**** as your top Module Name
2. Write ****_tb as your testbench Module Name
3. Module name and Filename should be the same.

Convolution is the basic operation in Neural Networks, Image Processing, and Computer Vision. Design a Pipelined **Five-stage 3 channel** Convolution hardware using System Verilog.

Image Pixels should be provided serially from the testbench.



Link for Image for Convolution:
https://upload.wikimedia.org/wikipedia/commons/c/c0/Wikipedia-sipi-image-db-mandrill-4.2.03-quantize-only-CCC.png

Kernel: Laplacian Edge Detection Kernel

$$\begin{bmatrix} 0 & 1 & 0 \\ 1 & -4 & 1 \\ 0 & 1 & 0 \end{bmatrix}$$

Design a testbench to read the image from a file and store the final output again back in the file. Use Python to Convert image to text and text to Image again.