

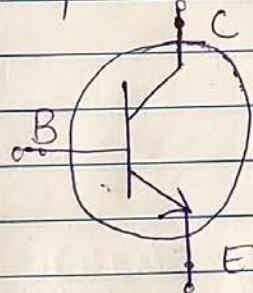
## Unit - 2

### Transistor :-

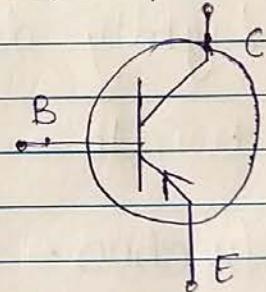
- It is three layer device.
- Transfer + Resistor  $\Rightarrow$  Transistor  
This device transfer the signal from low resistance to high resistance circuit.

### \* Bipolar junction Transistor [BJT]

n-p-n transistor

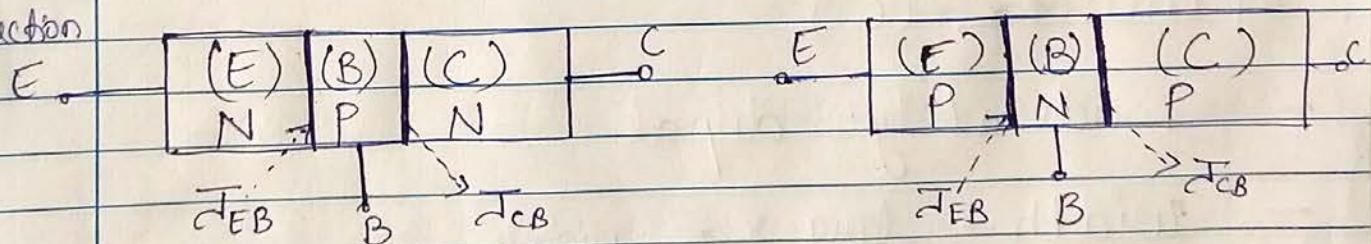


p-n-p transistor

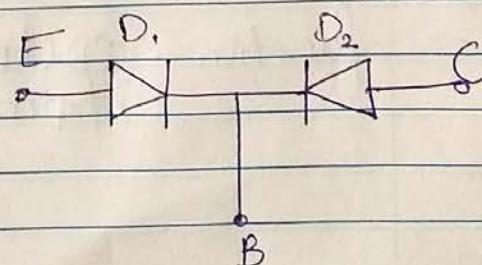
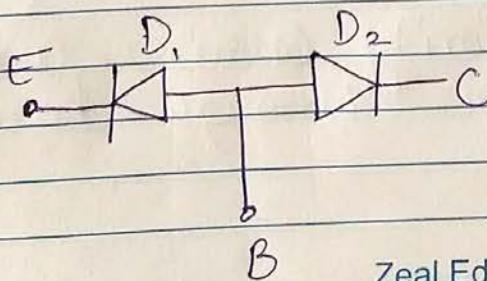


Symbol:-

Construction



Diode  
Analogy



→ Three regions / terminal

1] Emitter (E)  
heavily doped

→ Area width - moderate

→ Function → to supply majority charge carriers [holes & electron]

2] Base (B)

- Lightly doped.

- width - small

- function - carry all majority charge carriers from emitter to collector.

3] Collector - (C)

- moderately doped

- width - larger or wider

- function - collects majority carriers coming from emitter through base.

Doping concentration

Emitter > Collector > Base.

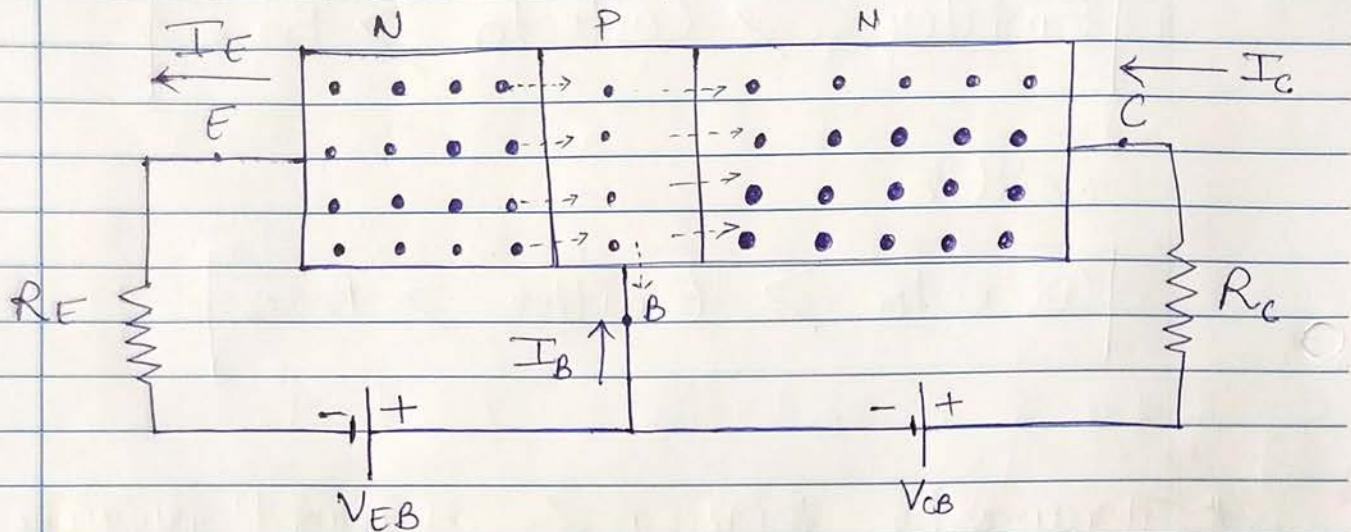
width

Collector > Emitter > Base

\* Transistor Biasing for different regions of operation.

Emitter base junction (TEB)	Collector base junction (TCB)	Region of Operation	Application
Reverse biased	Reverse biased	Cut-off	open / off switch
forward biased	Reverse biased	Active Amplifier	Amplifier
forward biased	forward biased	Saturation	on / closed switch

## \* Working of N-P-N transistor.



- the Emitter base ( $J_{EB}$ ) junction is forward biased & collector base junction is reverse biased.
- As  $J_{EB}$  is forward biased, barrier potential decreases at this junction & electrons from emitter are entered into base region. This will cause emitter current to flow.  $I_E$
- As base is very thin & contains small amount of holes [as lightly doped], few electrons combine with holes & form a base current  $I_B$ .
- The rest of  $e^-$  coming from emitter enters into collector region through reverse bias junction  $J_{CB}$  & constitute a current  $I_C$ .

$$I_E = I_C + I_B$$

Since  $I_C \ggg I_B$

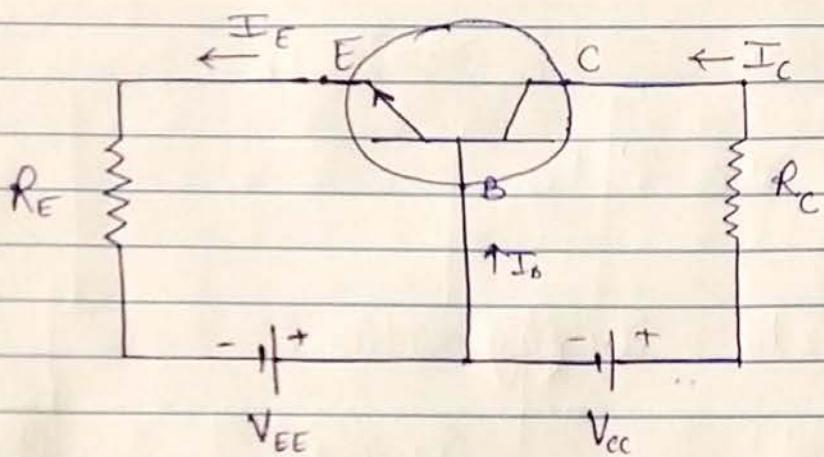
$$\therefore I_E \approx I_C$$

→ Transistor Configuration.



Type of Configuration	Common terminal	Input	Output
1. Common Base [CB]	Base	Emitter	Collector
2. Common Emitter [CE]	Emitter	Base	Collector
3. Common Collector [CE]	Collector	Base	Emitter

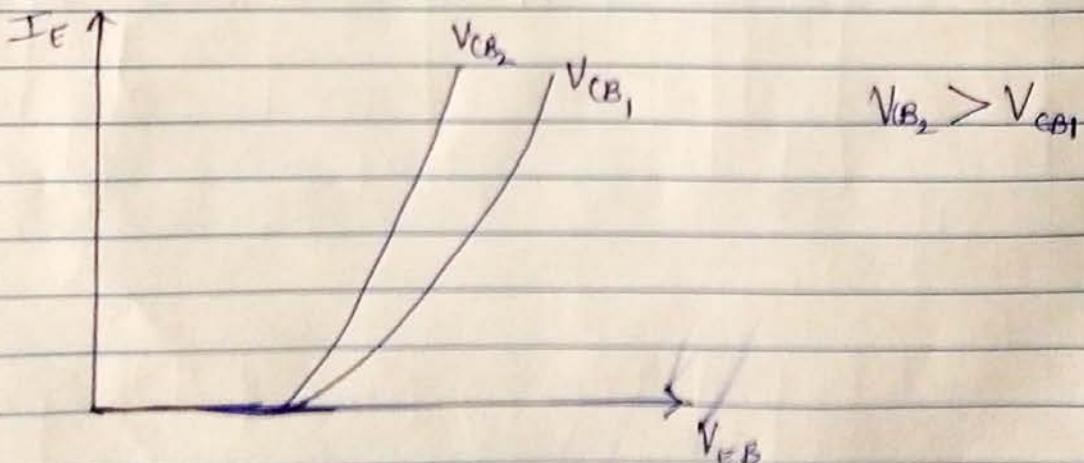
\* Common Base Configuration:-



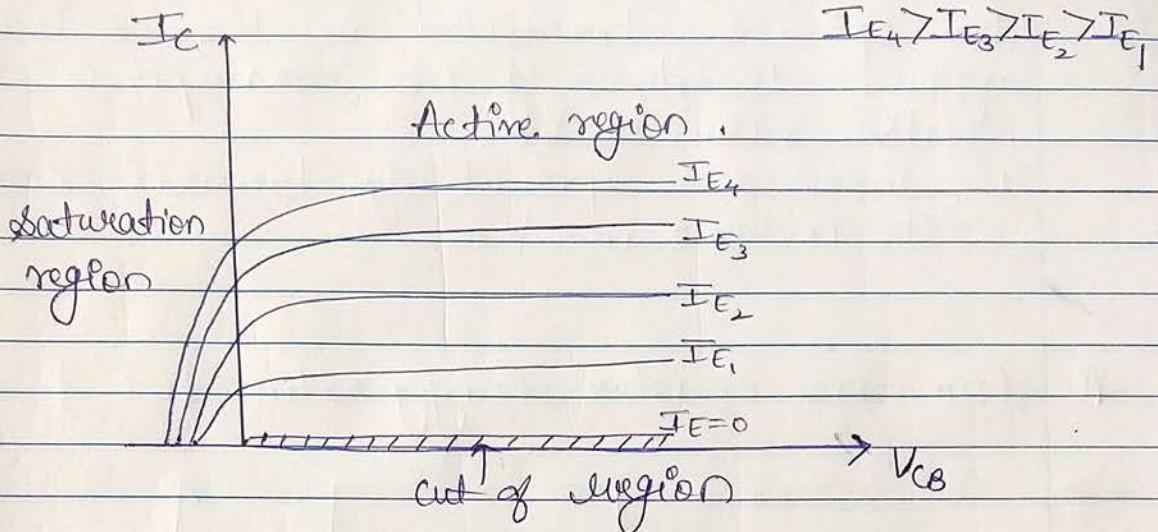
- Current amplification factor:-

$\alpha_{dc} = \frac{I_c}{I_e}$  Current gain or current amplification factor for CB is ratio of collector current to total emitter current.

- i/p char. characteristics of CB.



- O/P characteristics of CB.



→ 1) Cut off region :- (B-E) & (C-B) both junction are reverse biased to operate transistor in cut off region.  
as  $I_E = 0$   $\therefore I_{C\text{ majority}} = 0$

$$I_c = I_{C\text{ majority}} + I_{C\text{ minority}}$$

$$I_c = I_{C\text{ minority}}$$

O/P current  $I_c$  which is very low due to minority charge carriers.

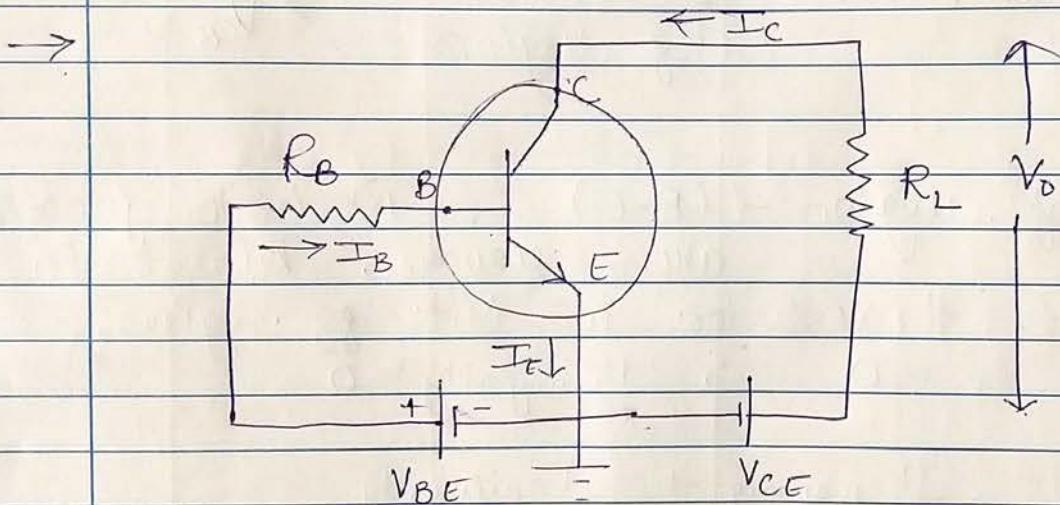
2) Active region :- In this region B-E junction is forward bias & C-B junction is reverse biased.  $I_c \approx I_E$ . Thus if  $I_E$  is constant then  $I_c$  remains constant irrespective of changes in  $V_{CB}$ . In this region transistor acts as amplifier.

3] Active Saturation region.

Both junctions are forward biased to operate transistor in the saturation region. Therefore if it corresponds to negative values of  $V_{CB}$ .

$I_C$  increases exponentially towards zero with increase in  $V_{CB}$ .

4] Common emitter configuration [CE].



$$\beta = \frac{I_C}{I_B} \rightarrow \text{Current gain or current amplification factor.}$$

\* Relation between  $\alpha_{dc}$  &  $\beta_{dc}$ .

$$\alpha_{dc} = \frac{I_c}{I_E}$$

$$I_E = I_C + I_B$$

$$\alpha_{dc} = \frac{I_c}{I_c + I_B}$$

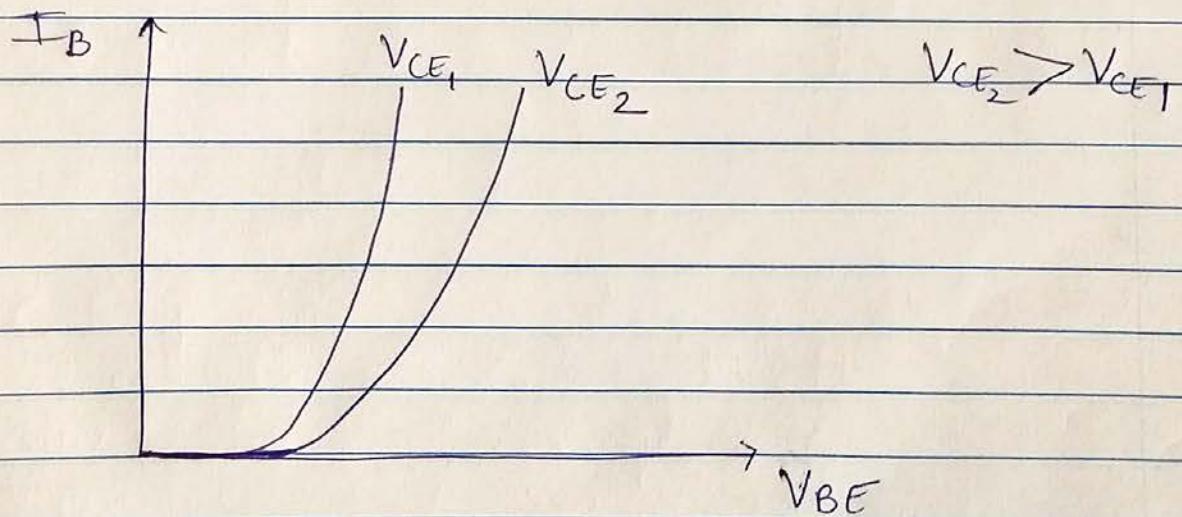
$$\alpha_{dc} = \frac{I_c/I_B}{I_c/I_B + I_B/I_B}$$

}  $\div$  Numerator & Denominator by  $I_B$ .

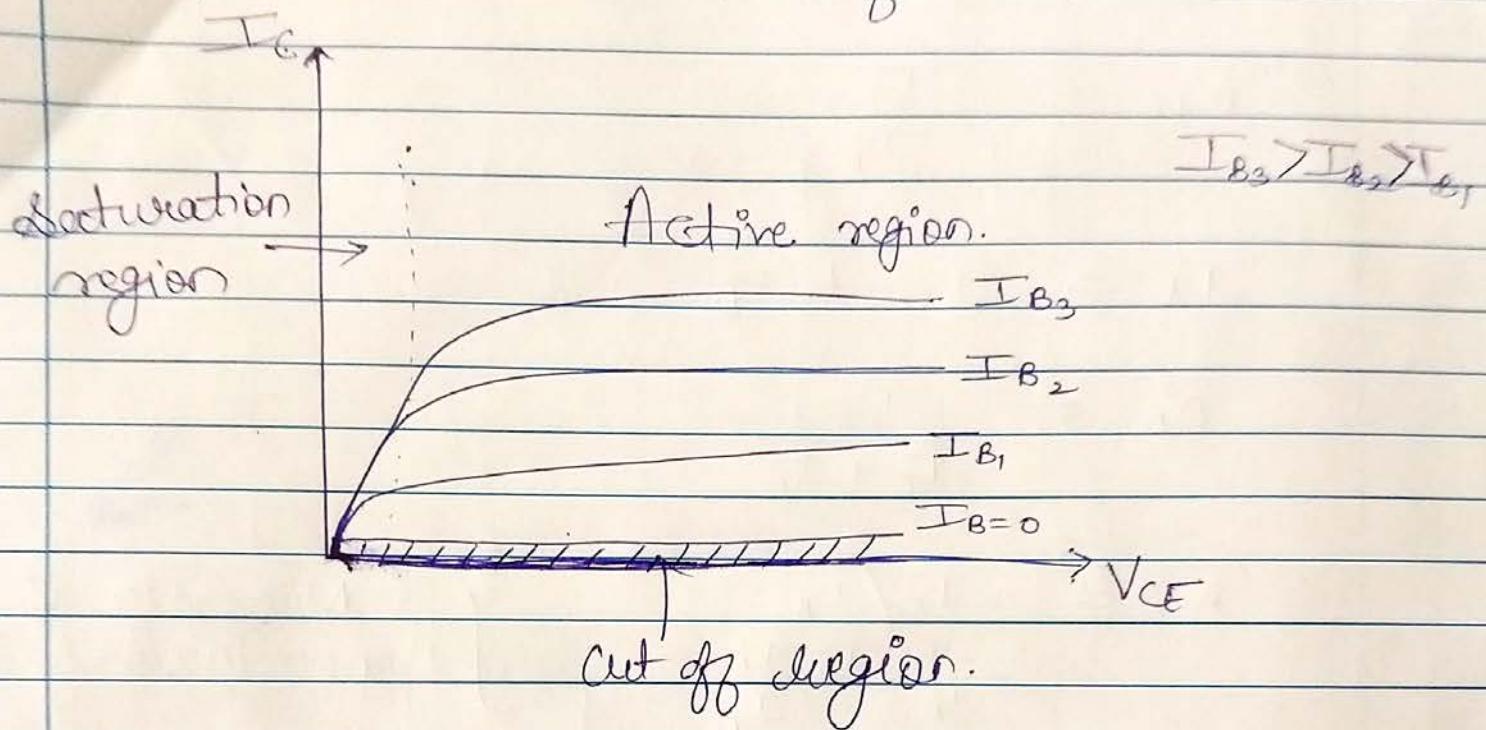
put  $\frac{I_c}{I_B} = \beta$

$\alpha_{dc} = \frac{\beta}{1 + \beta}$
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\* Input characteristics of CE



\* Output characteristics of CE.

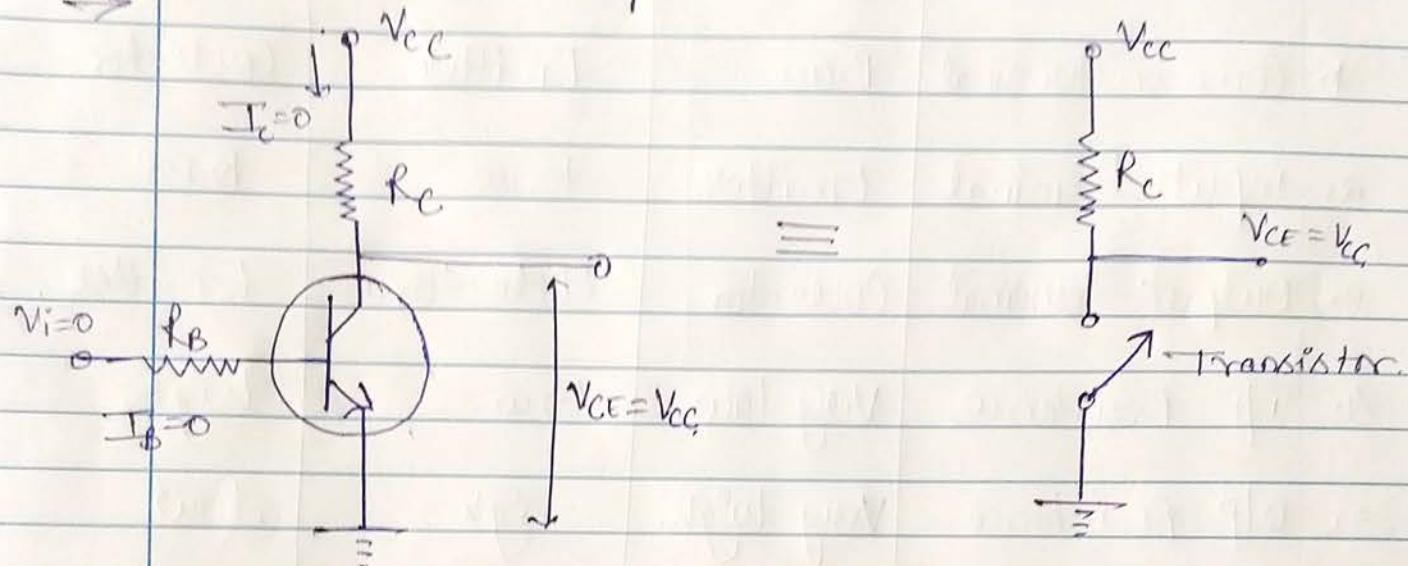


\* Difference b/w CB, CE, CC.

Parameter	Common Base (CB)	Common Emitter (CE)	Common Collector (CC)
1. Common terminal	Base	Emitter	Collector
2. Input terminal	Emitter	Base	Base
3. Output terminal	Collector	Collector	Emitter
4. IP Resistance	Very low	Low	High
5. OP Resistance	Very high	High	Low
6. Voltage gain	Medium	Medium	Less than 1
7. Current gain	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$
8. Application	Non-inverting voltage amplifier	Audio Amplifier	for impedance matching.

- BJT as switch
- To use Transistor as switch it is used in saturation or cut-off region.

→ Transistor as open switch:-



→ As I/P voltage is zero,  $V_i = 0$ .  
 $\therefore I_B = 0$  &  $I_C = 0$ .

→ In cut-off region both junctions of a transistor are reverse biased & very small reverse current flows through the transistor.

→ The voltage drop across transistor [ $V_{CE}$ ] is high. Thus in the cut-off region the transistor is equivalent to an open switch.

Applying KVL to collector circuit.

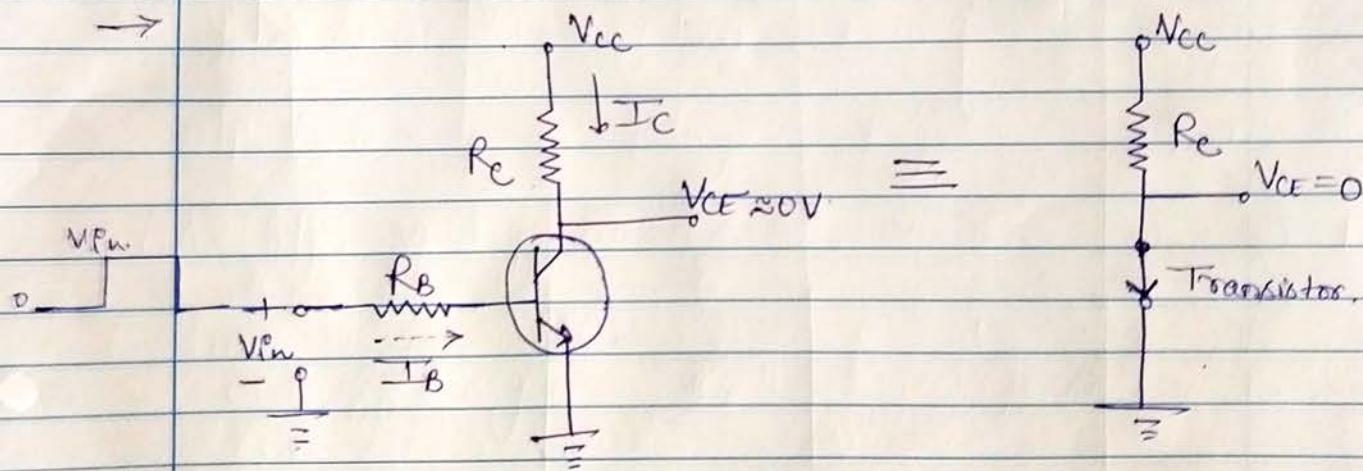
$$V_{CC} = I_C R_C + V_{CE}$$

as  $I_C = 0$ .

$$\therefore V_{CE} = V_{CC}$$

→ This shows that the resistance offered by the transistor is infinite.

2] Transistor in as closed switch.



- Here, transistor is used in saturation region i.e. both junctions are forward biased.
- A high iff voltage  $V_{in}$  is applied at base.
- The value of  $R_b$  is adjusted such that large  $I_B$  flows.

- This will saturate the transistor.  
→ The value of  $I_B$  is such that

$$I_B \geq \frac{I_C(\text{sat})}{\beta}$$

- The voltage drop across transistor is very small and collector current is very large.
- This indicates that the transistor is equivalent to closed switch.

→ Transistor as an Amplifier.

- Properties of an ideal amplifier.

1] Input resistance ( $R_i$ ):-

Ideally  $= \infty$   
Practically  $\Rightarrow$  as high as possible.

2] Output resistance ( $R_o$ ):-

Ideally  $= 0$   
Practically  $\Rightarrow$  as low as possible.

3] Voltage gain ( $A_v$ ):-

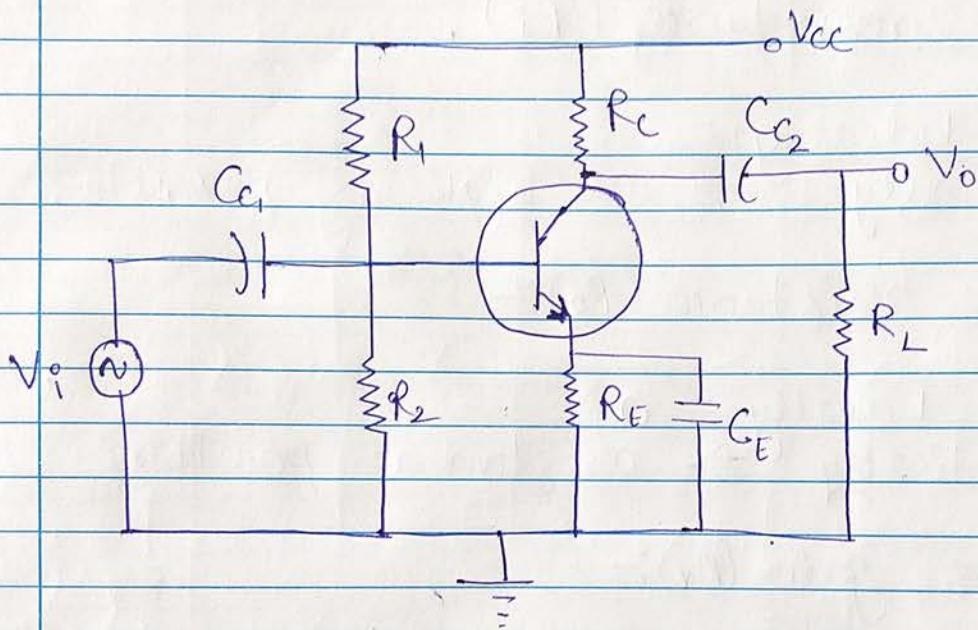
Ideally  $= \infty$   
Practically  $\Rightarrow$  as high as possible.

4] Bandwidth :-

Ideally  $= \infty$   
Practically  $\Rightarrow$  as high as possible

\* C.E Amplifier :-

Single stage, BJT amplifier.



- The input capacitor  $C_1$  is used to block the DC component present in the signal & pass only AC components for amplification.
- The capacitor  $C_E$  used in parallel with  $R_E$  and it is called the emitter bypass capacitor. It provides the low resistance path to amplified AC signal.
- If this capacitor is not used, amplified AC signal passes through  $R_E$  and

will cause voltage drop across it.

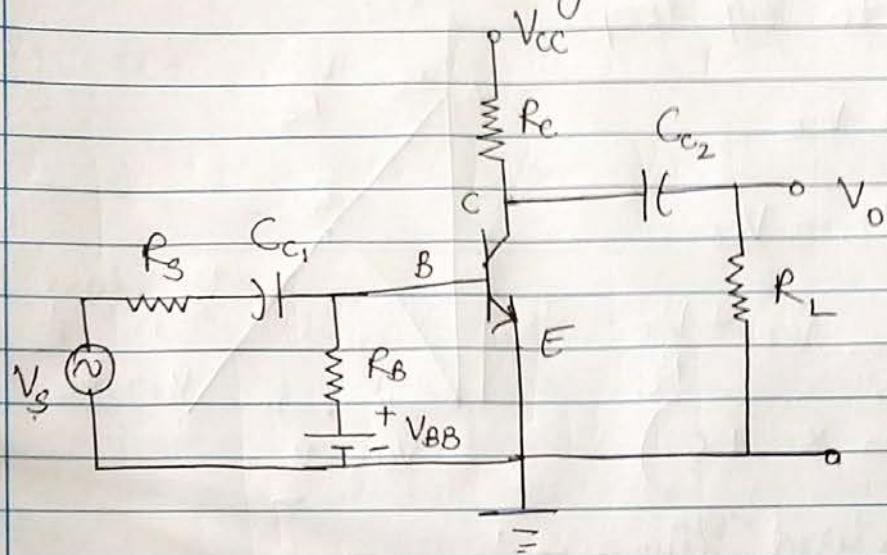
This will reduce the output voltage & also the gain of the amplifier.

- The coupling capacitor  $C_2$  is used to block the DC and couple the A.C. op of the amplifier to the load.
- An imp. point is to be noted here that the i/p voltage & o/p voltage are out of phase ( $180^\circ$  out of phase).
- As we see, during the +ve half cycle due to increasing base current ( $I_B$ ), collector current ( $I_C$ ) also increases, which in turn increases the drop across  $R_C$ .
- Since  $V_C = V_{CC} - I_C R_C$   
the collector voltage decreases with increase in  $I_C$
- Thus, we see that as  $V_{i/p}$  increases, in the +ve direction, the  $V_{o/p}$  also increases but in -ve direction.
- $\therefore$  we say that there is phase shift of  $180^\circ$  between i/p and output.

- \* Why CC & CB Configurations are not used for BJT as switch.
  - To use transistor as switch there must be isolation of both voltage and current.
  - In CB configuration o/p current  $I_C$  & i/p current  $I_E$  are nearly same. Hence there is no current isolation.
  - In CC configuration o/p vgt. ( $V_C$ ) and i/p vgt. ( $V_C$ ) are nearly same, Hence there is no voltage isolation.
  - Due to this reason CC & CB are not preferred for switching application.

- # Why CE is preferred?
  - for CE configuration the o/p current  $I_C$  in mA and i/p current ( $I_B$ ) in  $\mu$ A. Hence current isolation is provided.
  - the o/p vgt. is the amplification of i/p vgt. and it is out of phase or phase shifted version of i/p. Hence voltage isolation is provided.
  - As CE Configuration provides both current & voltage isolation it is preferred for switching application.

\* Load Line Analysis.



1. DC Analysis → to select Q-point.

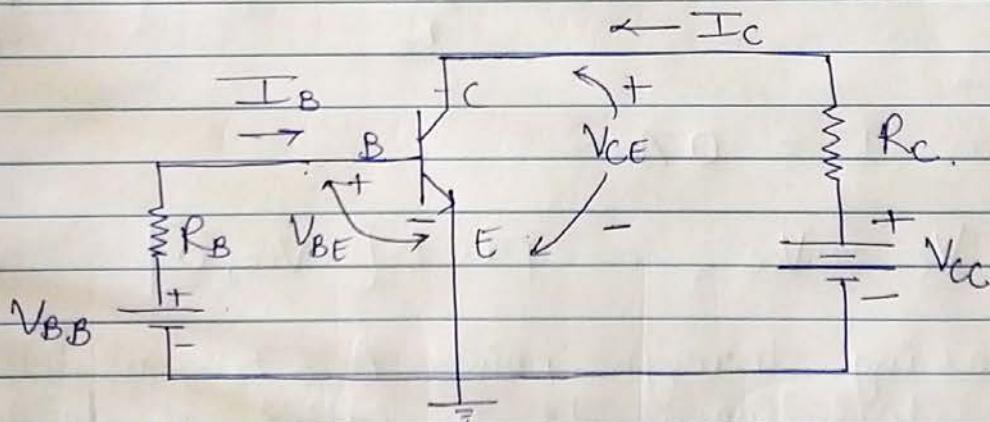


Fig:- DC Equivalent circuit of CE Amp.

→ The DC equivalent circuit can be obtained by opening the capacitors.

$$\therefore X_C = \frac{1}{2\pi f C} = \infty \text{ for DC as } f = 0$$

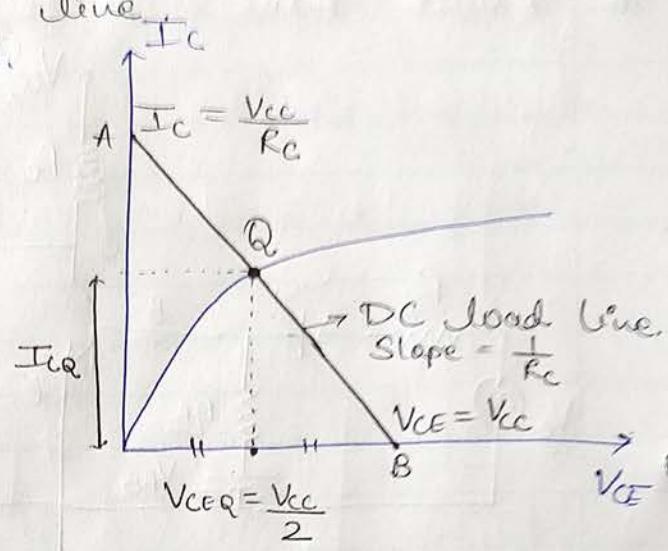
1. To Obtain DC load line  
Apply KVL to O/P loop.

$$V_{CC} = I_C R_C + V_{CE}$$

$$\therefore I_C R_C = V_{CC} - V_{CE}$$

$$I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C}$$

$$(y = m \times + c)$$



$$\therefore \text{Slope of load line} = -\frac{1}{R_C}$$

(i) When  $V_{CE} = 0$  Volt

$$I_C = \frac{V_{CC}}{R_C} \quad \text{pt. A} \left( 0, \frac{V_{CC}}{R_C} \right)$$

(ii) When  $I_C = 0$  Amp

$$V_{CE} = V_{CC}$$

$$\text{pt. B} [ V_{CC}, 0 ]$$

Line passing through points A & B, which is DC load line. It is called as dc load line, because its slope is determined by dc load  $R_C$ .

2. To obtain Q-point

By KVL to input,

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

for this base current, plot output circuit of C.E amplifier passing through centre of DC load line. The intersection with DC load line is 'operating point' or Q-pt.

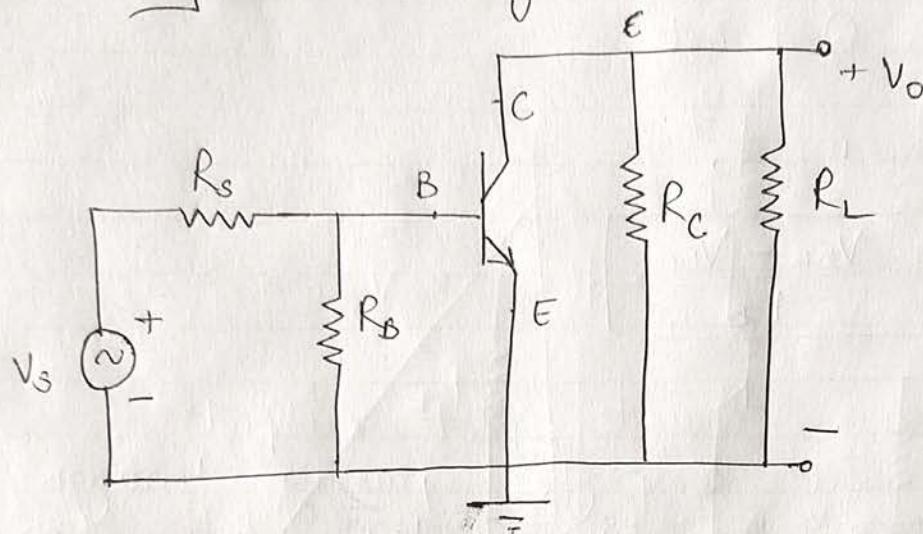
3. Significance of dc load line.

→ DC load line is used to set maximum dc voltage ( $V_{cc}$ ) and maximum dc output current ( $\frac{V_{cc}}{R_L}$ ) for an amplifier, such that ac off voltage & current cannot exceed dc values.

4. Significance of Q-point.

→ the Q-point is selected at the centre of dc load line such that the positive & negative half cycles of the amplified output are identical; it is called faithful amplification.

## Part II.] AC Analysis.



→ The AC equivalent circuit can be obtained by shorting dc battery & capacitors.

→ the dc & AC current Amplification can be defined as.

$$(i) \beta_{dc} = \frac{dc \text{ output current}}{dc \text{ input current}} = \frac{I_C}{I_B}$$

$$(ii) \beta_{ac} = \frac{ac \text{ O/P current}}{ac \text{ i/p current}} = \frac{\dot{I}_C}{\dot{I}_B}$$

→ the AC O/P Voltage is given by.

$$V_{CE} = V_C - \dot{I}_C R_C$$

(i) During 're' half cycle of i/p sig, the forward bias on base increases.

∴  $\dot{I}_B$  &  $\dot{I}_C$  values in positive direction.  
 $\therefore \dot{I}_C R_C$  increases &  $V_{CE}$  decreases.

— Hence, 're' half cycle of O/P is obtained first.

- (ii) During re half cycle of i/p sig, the forward bias on p/p decreases.
- ∴  $i_B$  &  $i_c$  goes to negative direction.
  - $i_c$  &  $i_c$  decreases if  $V_{CE}$  increases.
  - Hence, the amplified ac off voltage is  $180^\circ$  out of phase with respect to i/p.
  - ∴ CE is called as Inverting voltage amplifier

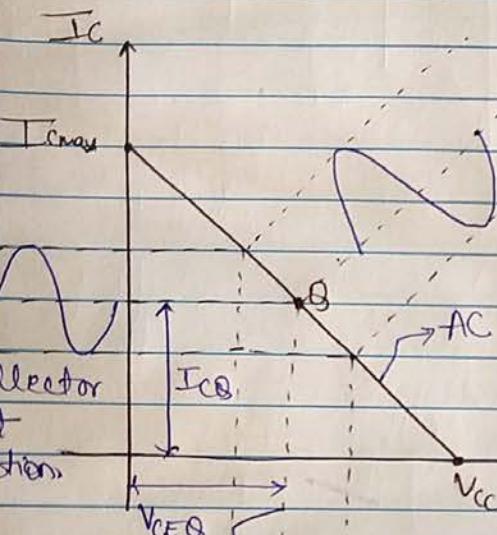


Fig 1: sig variations on load line.

input base current variation.

$$\text{AC load line. slope} = -\frac{1}{R_L}$$

$$R_L' = R_C \parallel R_L$$

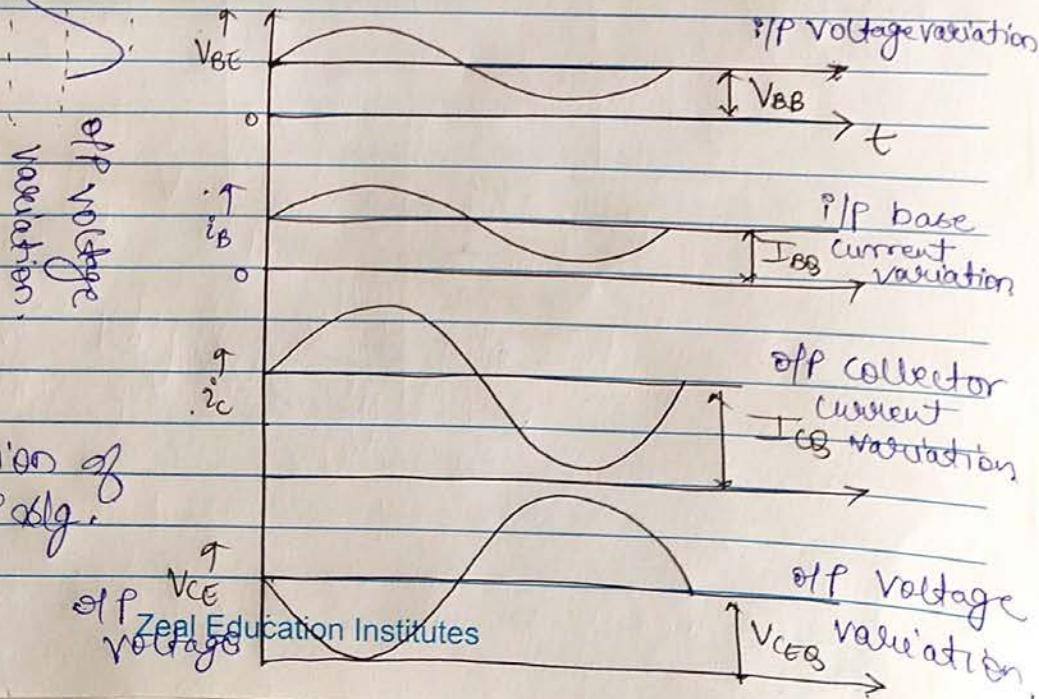
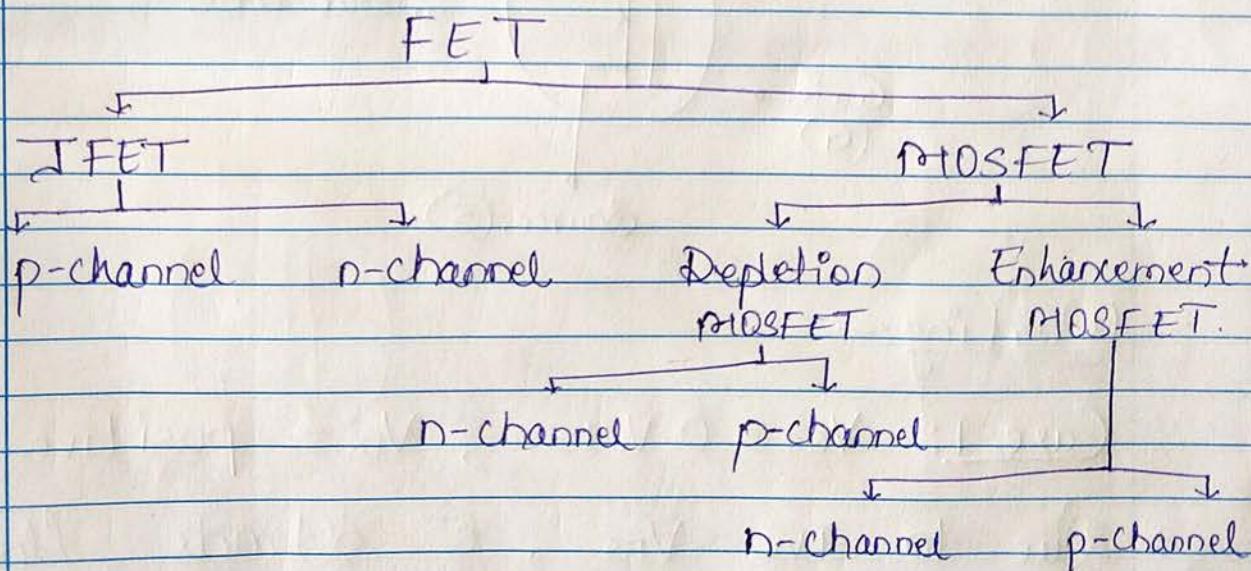


Fig 2: Variation of i/p & off sig.

\* **MOSFET** :- Metal oxide semiconductor field effect transistor

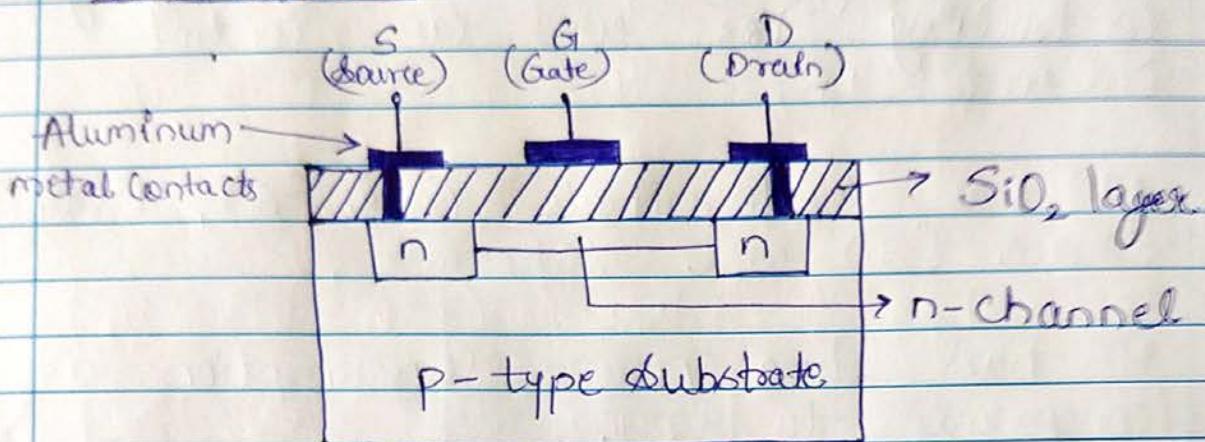
- It is voltage controlled device, by controlling  $V_{GS}$  we can control Current  $I_D$ .
- It has 4 terminals Gate (G), Drain (D), Source (S) and substrate.
- It has low power consumption as compared to BJT.
- high switching speed [ON/OFF speed]
- high i/p impedance.
- more thermal stability as compared to BJT.



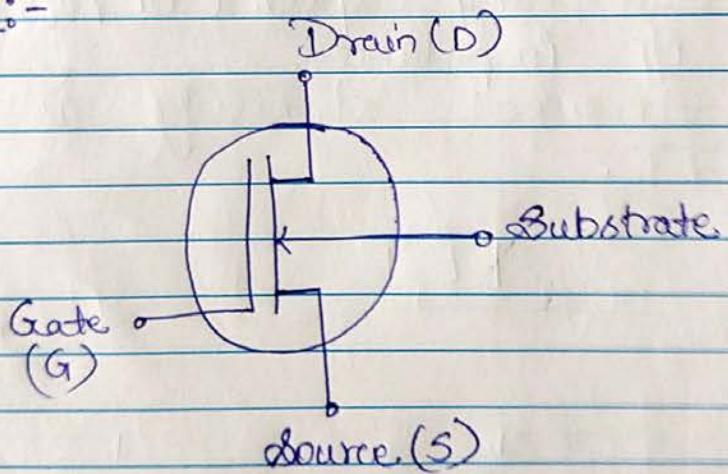
\* Depletion - Type MOSFET

→ N - channel Depletion - Type MOSFET

Construction:-



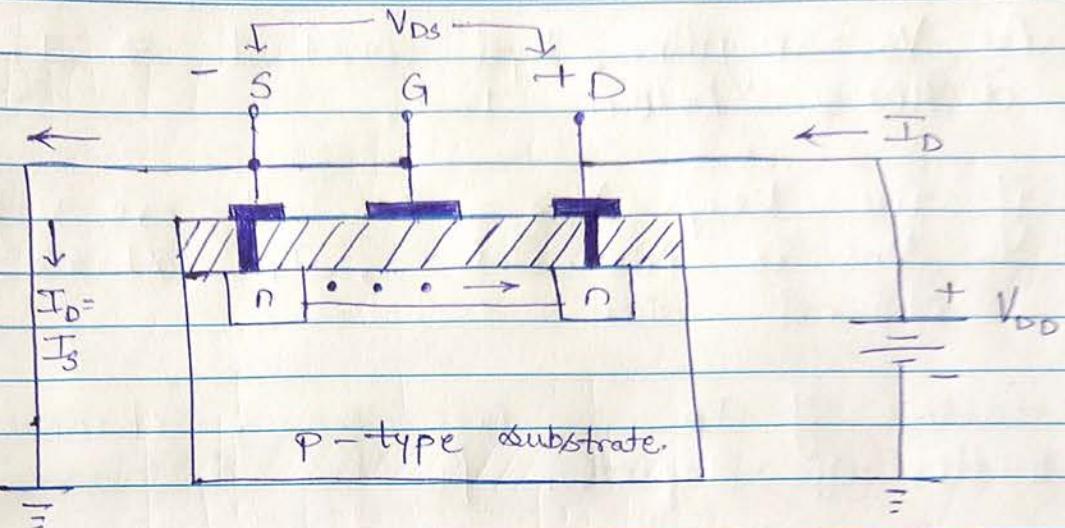
Symbol:-



Working:-

Case 1:  $V_{GS} = 0$  Volt. ;  $V_{DS} = \text{positive}$ .

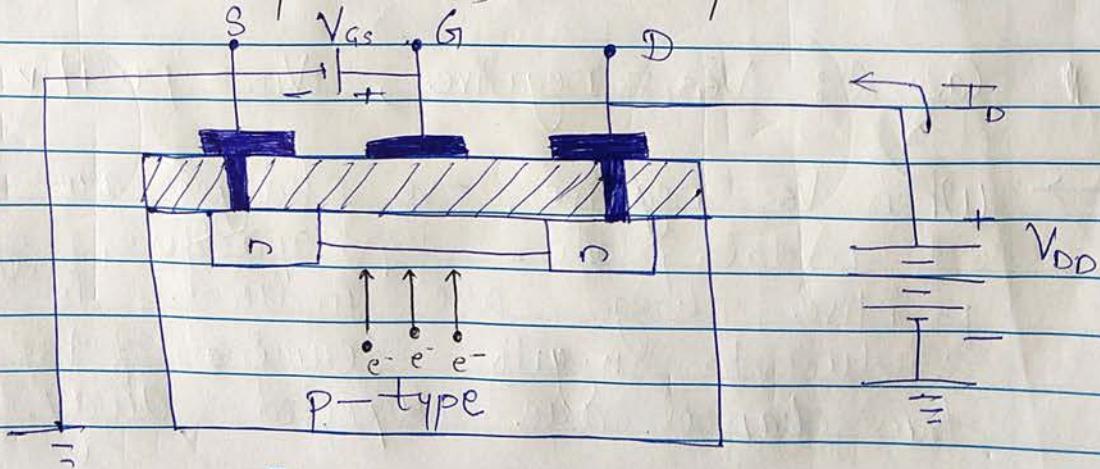
→ Due to +ve  $V_{DS}$ ,  $e^-$  starts flowing from source to drain through channel



- As electrons move from N-channel, +ve ions are generated in the channel.
- As  $V_{DS}$  increases, width of region of +ve ions further increases, width of channel decreases,  $\therefore$  fixed number of  $e^-$  can pass from source to drain  $\therefore I_D$  remains constant.
- Current from drain to source when gate source is shorted [ $V_{GS} = 0V$ ] is called  $I_{DSS}$ . It is maximum current.
- Case 2:  $V_{GS} = \text{negative}$ ,  $V_{DS} = \text{positive}$ .
- When  $V_{GS} = \text{negative}$ , -ve charges are induced on metal plate. By capacitive effect positive charges are induced in the channel.  $\therefore$  due to negative terminal of  $V_{GS}$ ,  $e^-$  from channel are repelled away.

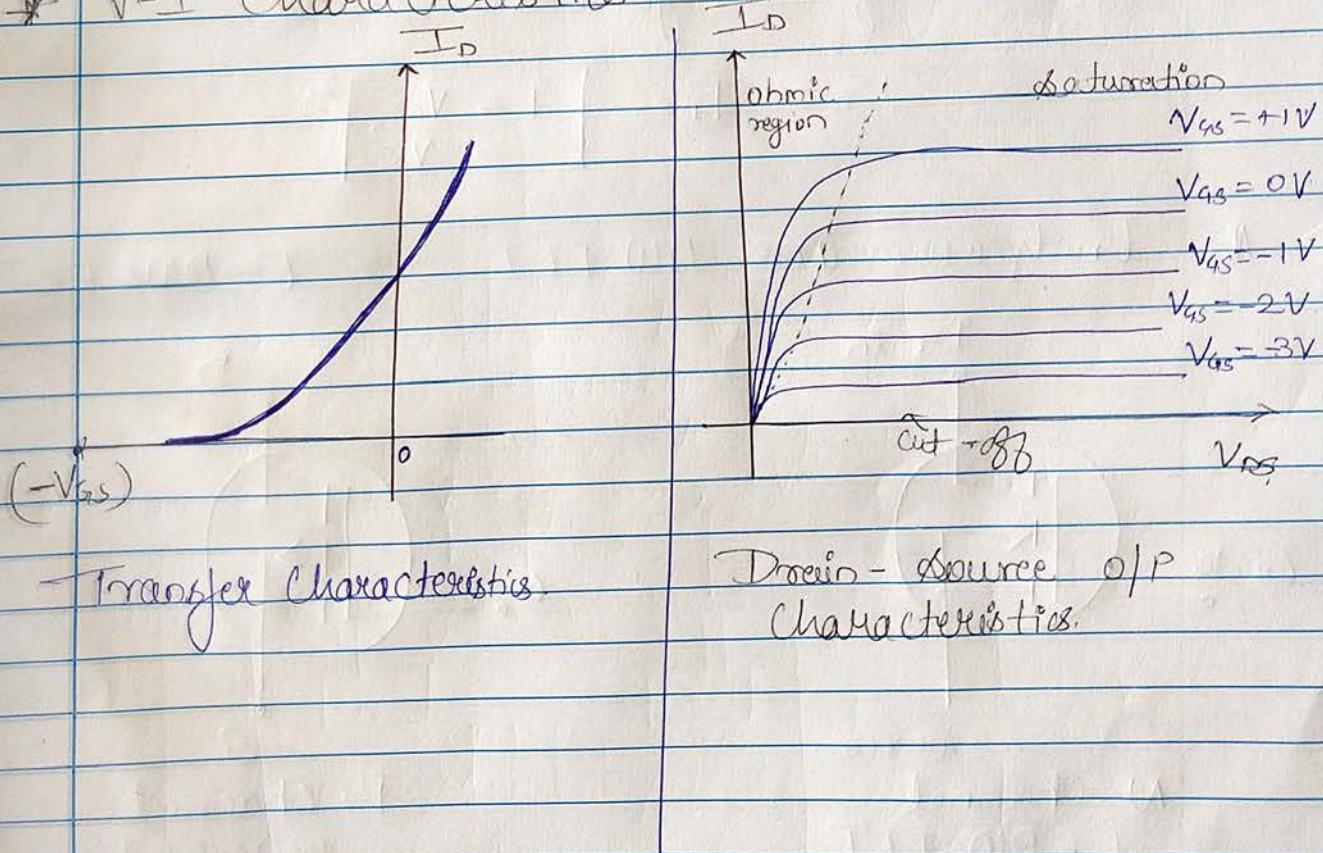
- As  $V_{GS}$  = negative, kept constant  $\&$   $I_D$  decreases below  $I_{DSS}$ .
- if we keep  $V_{GS}$  = constant re value,  $V_{DS}$  is increased,  $I_D$  starts increasing. & channel width decreases.
- further if  $V_{GS}$  is increased, channel width of depletion further decreases.
- finally, channel width becomes very small through which fixed number of  $e^-$  can pass from source to drain &  $I_D$  remains constant. [below  $I_{DSS}$ ]
- if  $V_{GS}$  becomes more negative, width of depletion region in channel goes on increasing. finally, at pinch-off voltage ( $V_P$ ), the depletion region blocks the channel & drain current becomes zero.

\* Case III:  $V_{GS}$  = positive,  $V_{DS}$  = positive.



- When  $V_{GS}$  is positive, the negative charge carrier  $e^-$  present in P-type Substrate (minority) are attracted to Channel by Capacitive effect.
- ∵ No. of  $e^-$  in the channel increases  
Hence, drain current increases above  $I_{DS}$ .  
∴ Conduction is enhanced in D-MOSFET for positive  $V_{GS}$  and work as E-MOSFET.

\* V-I characteristics.

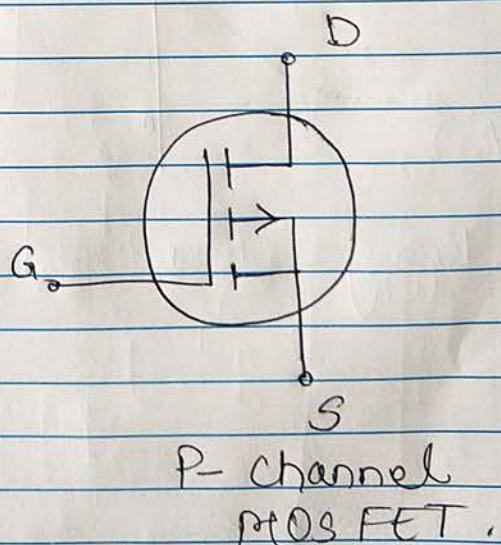
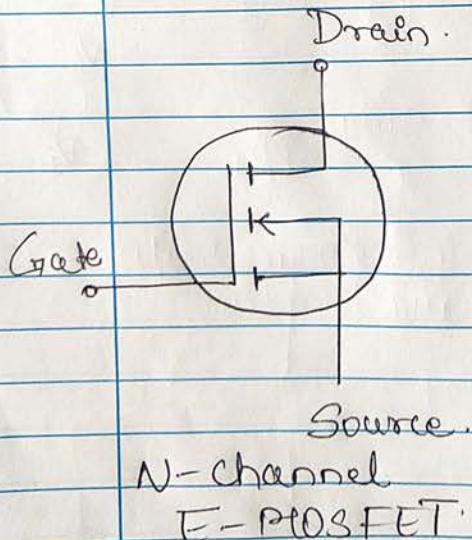


## \* Parameters

- 1] transconductance,  $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$  |  $V_{DS} = \text{constant}$ .  
(from transfer characteristic)
- 2] Dynamic output impedance or internal drain resistance,  $r_d = \frac{\Delta V_{DS}}{\Delta I_D}$  |  $V_{GS} = \text{constant}$ .
- 3] Equation of transfer characteristics

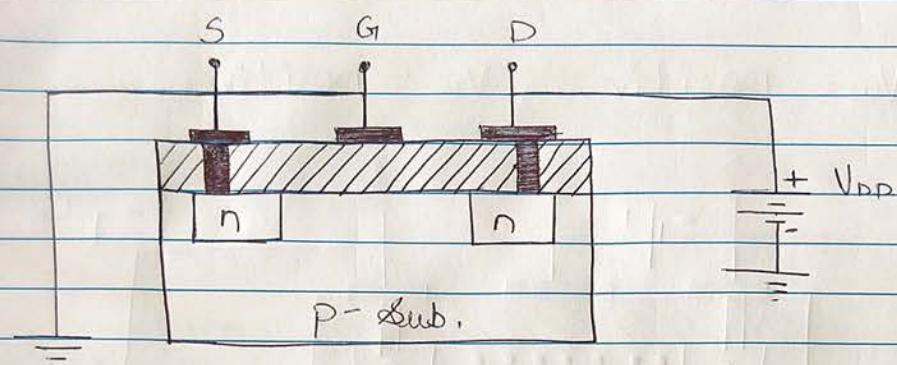
$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$$

## \* Enhancement型 MOSFET $\rightarrow$ E-MOSFET



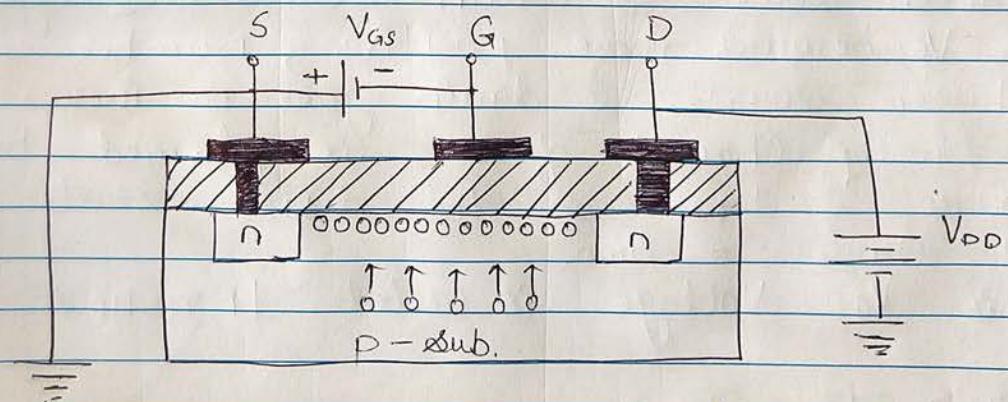
\* E-MOSFET Operation N-Channel.

Case 1:  $V_{GS} = 0V$ ,  $V_{DS} = \text{Positive}$ .



→ As there is no-channel between drain and source, E-MOSFET cannot be operated for  $V_{GS} = 0V$ .

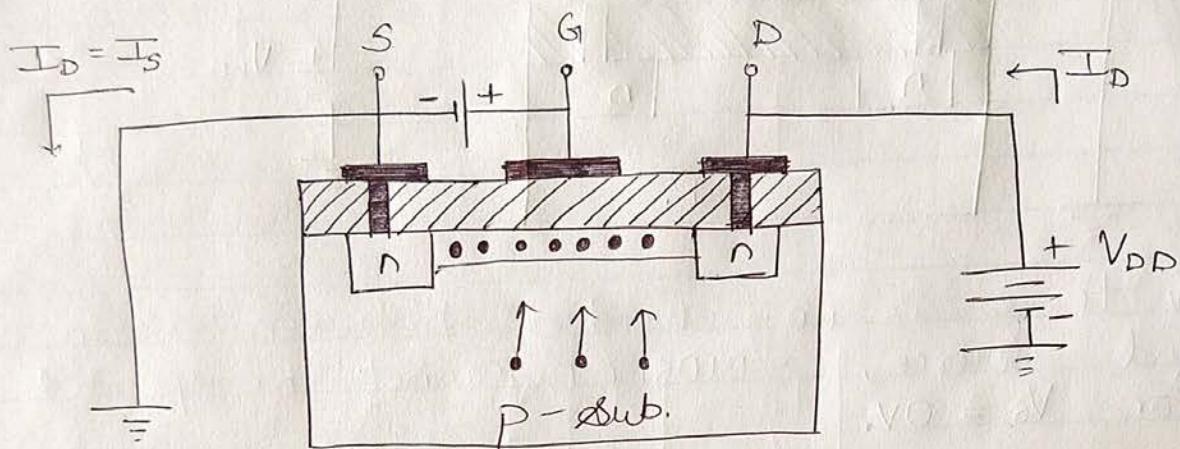
Case 2:  $V_{GS} = \text{negative}$ ,  $V_{DS} = \text{positive}$ .



→ As  $V_{GS}$  is negative, positive charges <sup>(holes)</sup> are induced between drain & source but n-type e-

Cannot travel from source to drain through channel of holes because there will be recombination of holes &  $e^-$ .  
 $\therefore$  E MOSFET cannot be operated for negative  $V_{GS}$ .

Case 3 :-  $V_{GS}$  = positive,  $V_{DS}$  = positive.



- As  $V_{GS}$  = positive, negative charges are attracted between source & drain near  $\text{SiO}_2$  layer.
- As  $V_{GS}$  becomes more positive, number of  $e^-$  between source & drain goes on increasing & finally channel of  $e^-$  is formed between source & drain & the device starts conducting.
- $I_D$  starts to flow.
- This  $V_{GS}$  Voltage is called Threshold Voltage ( $V_T$ )
- Here  $I_D = I_S$
- As  $V_{DS}$  increases,  $I_D$  increases.  $V_{DG} = V_D - V_G$ . When  $V_D > V_G$ , the width of  $e^-$  channel on drain side starts decreasing because

- Current Equation for E-MOSFET

In Saturation Region.

$$I_D = k_n [V_{GS} - V_{TN}]^2$$

$$k_n = \frac{W \cdot \mu_n \cdot C_{ox}}{2L}$$

$k_n \rightarrow$  Conduction Constant in mA/V<sup>2</sup>.

$W \rightarrow$  Channel Width

$L \rightarrow$  Channel length.

$V_{TN} \rightarrow$  Threshold Voltage.

$\mu_n \rightarrow$  Mobility of  $e^-$

$C_{ox} \rightarrow$  Oxide Capacitance.

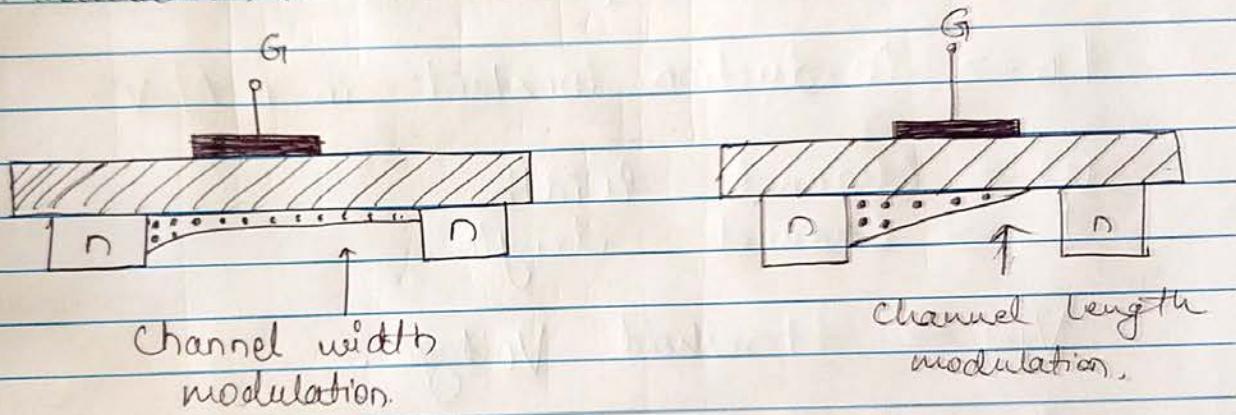
$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$\epsilon_{ox} \rightarrow$  Oxide permittivity.

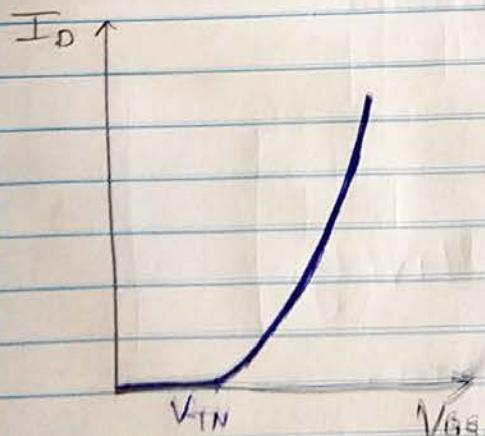
$t_{ox} \rightarrow$  Oxide thickness.

These  $e^-$  are attracted by drain voltage.  $V_{DD}$ . It is called as Channel width modulation.

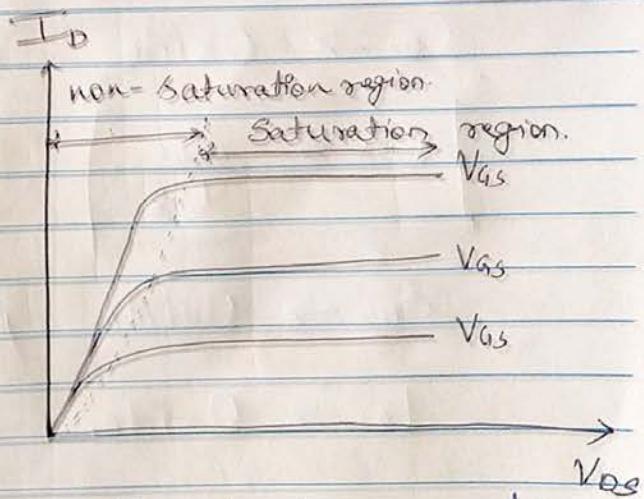
→ As  $V_{GS}$  further increases with  $V_D > V_S$ , the length of channel on drain side starts decreasing because channel  $e^-$  are pulled by  $V_{DD}$ . It is called as Channel length modulation.



\* V-I characteristics.



Transfer characteristics.



Drain source off characteristics.