EXPLORING THE CHARACTERISTICS OF 3-D NANOSHEET FETs IN INVERSION MODE

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EXPLORING THE CHARACTERISTICS OF 3-D NANOSHEET FETs IN INVERSION MODE

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By

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APPROVAL SHEET

This project report entitled **EXPLORING THE CHARACTERISTICS OF 3-D NANOSHEET FETs IN INVERSION MODE by Ms. K Ruchitha** is approved for the award of the Degree Bachelor of Technology in **Electronics and Communication Engineering.**

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I perceive this opportunity as a big milestone in my career development. I will strive to use gained skills and knowledge in the best possible way, and I will continue to work on their improvement, to attain desired career objectives. Hope to continue cooperation with all of you in the future.

ABSTRACT

The characteristics and performance of 3-D nanosheet Field-Effect Transistors (FETs) when operated in Inversion mode. Through a thorough investigation employing experimental analysis and simulation techniques utilizing the TCAD platform and the behaviour of inversion mode FETs is comprehensively examined and compared with junctionless (JL) mode.

The research findings shed light on the behaviour of Inversion mode FETs across various circuit applications, including common source (CS) amplifiers, CMOS inverters, and three-stage ring oscillators (ROs). Key findings include a decrease in ON current ($\boldsymbol{I_{ON}}$) with increasing temperature in Inversion mode, alongside a superior negative temperature coefficient of threshold voltage (dV_{th}/dT) compared to junctionless mode. Mixed-mode circuit simulations reveal a significant gain enhancement for CS amplifiers and heightened CMOS inverter switching current in Inversion mode.

Despite lower energy-delay products in junctionless mode, Inversion mode demonstrates superior performance in terms of gain and current switching. Furthermore, Inversion mode FETs exhibit elevated oscillation frequencies ($\boldsymbol{f_{osc}}$) in three-stage Ring Oscillator designs, attributed to their higher $\boldsymbol{I_{ON}}$. However, a reduction in supply voltage (VDD) leads to decreased $\boldsymbol{f_{osc}}$, with INV mode experiencing a slightly larger reduction compared to Junctionless mode. In summary, these are another work provides valuable insights into the behaviour and advantages of Inversion mode FETs in advanced technology nodes.

Keywords: CMOS inverter, CS amplifier, TCAD, inversion, nanosheet FET.

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LIST OF ABBREVIATIONS

FET - Field-effect transistor

CMOS – Complementary metal oxide semiconductor

FinFET – Fin-shaped field-effect transistor

JL – Junctionless

E_{OT} – Effective oxide thickness

IRDS – International roadmap for devices and circuits

I_{ON} – ON Current

I_{OFF} - OFF Current

f_{osc} - Oscillation Frequency

DIBL – Drain – induced barrier Lowering

SS – Subthreshold swing

T_{GF} – Transconductance generation factor

CHAPTER 1

INTRODUCTION

1.1 Overview of the transition in transistor technology from its inception to the current era of nanosheets:

Invention of Transistors (1947):

In 1947, the transistor was invented at Bell Laboratories, marking a significant milestone in electronics.

The transistor, which offered smaller size, lower power consumption, and improved reliability, replaced the large and unreliable vacuum tubes.

Bipolar Junction Transistors (BJTs) (1950s - 1960s):

Bipolar Junction Transistors (BJTs) emerged as the first type of transistor to gain widespread use.

BJTs consist of three semiconductor regions: the emitter, base, and collector, and were utilized in early electronic devices such as amplifiers and switching circuits.

Integrated Circuits (ICs) (1960s):

The 1960s witnessed the advancement of integrated circuits (ICs), which combine several transistors with additional electronic components on a single silicon chip.

The digital age was ushered in by this breakthrough, which transformed electronics and caused devices to become smaller.

Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) (1960s - Present):

Metal -Oxide-Semiconductor Field-Effect Transistors (MOSFETs) were introduced in the 1960s and quickly became the dominant type of transistor.

When compared to BJTs, MOSFETs have benefits including smaller size, lower power consumption, and higher scalability.

MOSFETs are utilized in various applications, including digital circuits, microprocessors, and memory chips.

Moore's Law and Semiconductor Scaling (1970s - 2010s):

In 1965, Gordon Moore created Moore’s Law, which predicted that the number of transistors in a microchip will typically triple every two years.

Semiconductor manufacturers adhered to Moore's Law by continuously shrinking transistor sizes, leading to increased performance, energy efficiency, and cost reduction in electronic devices.

This period saw the development of various semiconductor technologies, including CMOS (Complementary Metal-Oxide-Semiconductor), which became the dominant technology for manufacturing microchips.

Nanotechnology and Nanosheets (2000s - Present):

As transistor dimensions approached atomic scales, researchers began exploring alternative materials and structures to sustain Moore's Law.

The unusual features of nanosheets, commonly referred to as 2D materials, have made them an attractive candidate for next-generation transistors.

Graphene, transition metal dichalcogenides (TMDs), and other 2D materials demonstrated intriguing properties for transistor applications.

Research into nanosheets and 2D materials continues to advance, with applications in transistors, sensors, energy storage, and biomedical devices.

This comprehensive overview traces the evolution of transistor technology from its inception through the eras of BJTs, MOSFETs, and into the current exploration of nanosheets, showcasing the continuous drive for innovation and advancement in electronics.

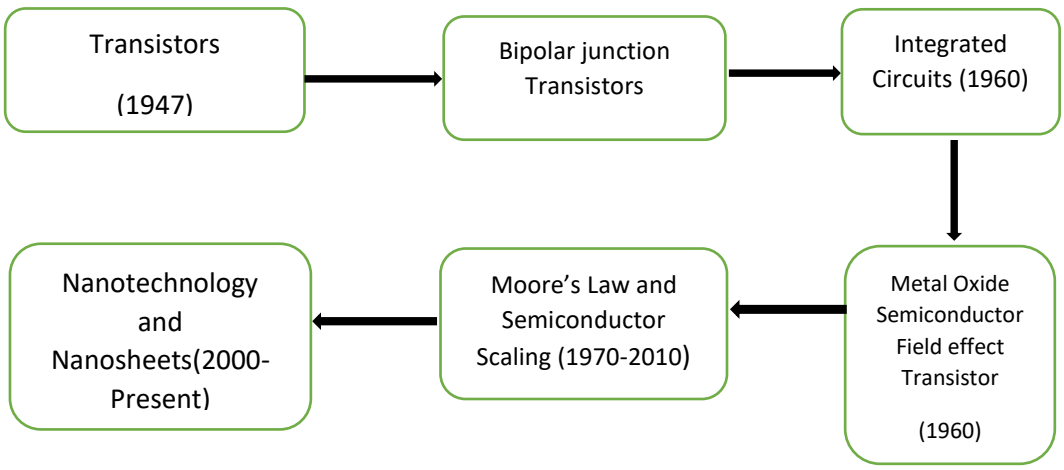

Fig 1.1 Evolution of transistors to Nanosheet FET's

1.2 Introduction of Nanosheet FET:

A nanosheet FET is likely associated with advancements in transistor design that move beyond traditional FinFET (Fin Field-Effect Transistor) structures. FinFETs are commonly used in the manufacture of semiconductors because they regulate the flow of current between the drain and source terminals by use of a fin-like structure. A nanosheet FET could be an evolution of FinFET technology, incorporating nanosheet structures instead of fins. The transition to nanosheets is driven by the need for continued scaling down of transistor dimensions to enhance performance, reduce power consumption, and increasetransistor density.

The provided continuation delves into the complexities of semiconductor scaling and the role ofadvanced transistor structures like gate-all-around (GAA) and junction less (JL) transistors in overcoming scaling challenges. It emphasizes the necessity for thorough analysis of NS-FET performance in different modes and under varying conditions, particularly in circuit-level applications. The paper aims to fill the gap in existing literature by investigating the behavior of NS-FETs in Inversion mode, considering temperature effects and circuit performance.

The format of the project is as follows:

Section I: Physical Models and Parameters

The physical models utilized in simulation are covered in this section as well as the important parameters taken into account for NS-FET design. Device performance is greatly influenced by parameters including doping levels and gate length (LG) scaling. The physical models integrated into simulationsoftware are essential for accurately capturing the behavior of nanoscale devices, including effects like quantum confinement, bandgap narrowing, recombination, mobility reduction, and tunneling phenomena.

Section II: Impact of Scaling and Temperature Variations on NS-FET Performance

The purpose of Section II is to investigate how temperature variations and gate length scaling affect the NS-FETs running in inversion mode's DC figures of merit (FOMs). The performance of devices can be greatly impacted by short-channel effects (SCEs), which are a challenge when scaling beyond conventional bounds. exhibit varying behaviors at different operating temperatures. By analyzing NS-FET performance under

these conditions, the section aims to provide insights into the device's reliability and stability.

Section III: Circuit Performance Analysis

In Section III, the project demonstrates the performance of NS-FETs in Inversion mode in various circuit configurations. Ring oscillators, common-source amplifiers, and complementary metal-oxide-semiconductor (CMOS) inverters are examples of this. These circuit configurations are fundamental building blocks in modern electronic systems, and understanding how NS-FETs behave within them is essential for assessing their suitability for practical applications. The Cadence Virtuoso platform is employed for designing and simulating these circuits, allowing for comprehensive analysis of AC, DC, and mixed-mode operations.

Section IV: Conclusion

The project concludes by summarizing the findings from the investigation and highlighting potential areas for future research. It emphasizes the importance of thorough analysis and simulation in understanding the behavior of emerging transistor technologies like NS-FETs. Thestudy contributes to the ongoing efforts in advancing nanoscale device design and paves the wayfor further exploration and optimization of NS-FETs for future electronic systems.

1.3 Overview of 3-D Nanosheet in Inversion mode:

The study derived into the operational dynamics of 3-D Nanosheet Field-Effect Transistors (FETs) when employed in inversion mode. In this mode, a gate voltage is applied to the semiconductor material's source and drain terminals to produce a conducting channel, which changes the transistor's behaviour. The key objective is to comprehend the nuanced characteristics and performance metrics of these transistors under such operational conditions.

Researchers focus on investigating essential characteristics, notably the ON current ($\boldsymbol{I_{ON}}$), threshold voltage ($\boldsymbol{V_{th}}$)**,** and their temperature dependency. Understanding these traits is pivotal for optimizing transistor performance across diverse circuit applications. To achieve this, a blend of experimental analysis and simulation methodologies is employed, leveraging software platforms like TCAD and Verilog-A models. These approaches facilitate a comprehensive exploration of transistor behaviour under varying conditions and circuit configurations.

A crucial aspect of the study involves contrasting the performance of FETs in inversion mode with their junction less (JL) mode counterparts. Such comparative analysis aids in delineating the relative strengths and limitations of each mode, offering insights into their applicability across different scenarios and technological advancements.

Furthermore, the investigation extends to assessing the transistor's efficacy in various circuit applications, including common source amplifiers, CMOS inverters, and ring oscillators. Analysing transistor behaviour within these circuits provides valuable insights into their practical implications and potential advantages over alternative transistor configurations.

In essence, the study provides an in-depth exploration of the operational intricacies, performance characteristics, and potential applications of 3-D Nanosheet FETs in inversion mode. Such insights contribute to the advancement of semiconductor technology, paving the way for enhanced circuit performance and functionality.

CHAPTER 2

LITERATURE REVIEW

Q. M. Khan [1] has proposed the evaluation of 6T and 9T SRAM integrated circuits side by side, emphasizing their advantages and disadvantages. Designers can use this information to make informed decisions when selecting the appropriate SRAM architecture for their designs, considering factors such as area constraints, power consumption, and reliability requirements. Future research may focus on optimizing hybrid SRAM architectures that combine the advantages of both 6T and 9T cells to achieve a better balance between performance and efficiency.

E. D. Kurniawan[2] has proposed the profound understanding of the junctionless, accumulation, and inversion modes of carrier transport in vertical stacked nanosheet FETs intended for N5 logic technologies. Each operational mode offers unique advantages and challenges, necessitating careful optimization to meet the requirements of next-generation logic applications. Future research directions may focus on further enhancing device performance, reliability, and manufacturability through advanced material engineering and innovative device architectures.

Kumar, S[3] has proposed The thorough investigation emphasizes how important junctionless stacked nanosheet transistors are for applications requiring extremely low power. By leveraging their unique properties, including enhanced electrostatic control and reduced leakage currents, these transistors hold great promise for powering the next generation of energy-efficient electronics. Future research endeavors may focus on further optimizing device performance, exploring novel material architectures, and advancing fabrication techniques to realize the complete potential of ultra-low power applications using junctionless stacked nanosheet transistors.

Chen, X[4] have discussed about The demonstrates the potential of low-power, high-performance inversion-mode stacked nanosheet FETs with channel lengths less than 10 nm. By leveraging their superior electrostatic control and scalability, these transistors offer a compelling solution for addressing the evolving demands of modern semiconductor technology. Future research efforts may focus on further optimizing

device designs, refining fabrication processes, and exploring novel material architectures to unlock the full potential of stacked nanosheet FETs in next-generation integrated circuits.

Wang,Q[5] has proposed the potential of strain engineering techniques in enhancing the performance of inversion-mode stacked nanosheet transistors. By employing controlled mechanical strain, the electrical properties of the transistor channel region can be altered, improving the device's functionality and performance. These findings pave the way for the development of strain-engineered stacked nanosheet transistors for next-generation semiconductor applications, offering new avenues for advancing the field of nanoelectronics. Future research may focus on further optimizing strain engineering strategies, exploring novel materials, and integrating strain-engineered devices into practical semiconductor technologies.

Desai, P[6] have discussed about the design and performance evaluation of NJ-TFTs for beyond-CMOS applications. By leveraging their simplified structure and improved electrostatic control, NJ-TFTs offer a promising alternative to conventional CMOS technology for future semiconductor applications. The research findings offer significant perspectives on the possible uses and enhancement tactics of NJ-TFTs, facilitating their incorporation into next-generation electronic systems. Future research directions may focus on further enhancing device performance, exploring novel materials and fabrication techniques, and expanding the scope of beyond-CMOS applications for NJ-TFTs.

Smith, L[7] has proposed the sheds light on the scaling challenges and design strategies for nanosheet-based junctionless transistors. The performance and scalability of junctionless transistor topologies can be maximized by tackling fundamental problems. The results of this study offer insightful information about the optimization of nanosheet-based junctionless transistors for future semiconductor applications, paving the way for their integration into next-generation electronic devices. Future research directions may focus on further enhancing device performance, exploring novel materials and fabrication techniques, and extending the applicability of junctionless transistor architectures to diverse semiconductor applications.

Chen, H[8] has proposed the provides insights into the subthreshold swing and leakage current characteristics of nanosheet junctionless thin-film transistors. By

understanding the factors influencing these performance metrics, it is possible to optimize the design and fabrication of NJ-TFTs for low-power electronic devices. The findings of this research contribute about the ongoing efforts to develop energy-efficient transistors for future electronic applications. Future research directions may focus on further optimizing device performance, exploring novel materials and fabrication techniques, and extending the applicability of NJ-TFTs to diverse electronic applications.

2.1 EXISTING METHOD

A proposed junction-less thin-film transistor, featuring NS channels stacked on a single layer, demonstrates enhanced electrical properties compared to a JL TFT with only one NS channel. The stacked NS channels show improvements such as increased on-current, reduced drain-induced barrier lowering (DIBL) at 50.8 mV/V, and a more favourable subthreshold swing (SS) at 135 mV/dec. These findings indicate enhanced efficiency and current-carrying capacity performance.

An IM TFT and a JL TFT with a single Ns channel (probably an inversion mode thin-film transistor) are also contrasted with the JL TFT that has Stacked Ns channels.

The findings show that compared to the IM TFT with stacked NS channels, the JL TFT with stacked NS channels offers greater design flexibility. This design flexibility is thought to be helpful in mitigating the short-channel impacts of gate length downscaling, a prevalent semiconductor technological difficulty.

2.2 PROPOSED METHOD

The inversion mode (INV) performance of three-dimensional nanosheet FETs (NS-FETs). We will investigate, comparing their characteristics at device and circuit levels.

2.3 Objectives:

1. Explore the operational characteristics of 3-D Nanosheet Field-Effect Transistors (FETs) when utilized in inversion mode.
2. Investigate essential performance parameters of inversion mode FETs, such as ON current (I_{ON}), threshold voltage (V_{th}), and their dependency on temperature variations.

3. Employ a combination of experimental techniques and simulation methods to comprehensively examine the behavior of inversion mode FETs across a range of circuit applications.
4. Assess the applicability of inversion mode FETs in common circuit configurations, including common source amplifiers, CMOS inverters, and ring oscillators.
5. Evaluate the influence of operating conditions such as temperature and supply voltage on the performance characteristics of inversion mode FETs.
6. Offer insights into the practical implications and potential benefits associated with the adoption of inversion mode FETs in advanced semiconductor technology nodes.
7. Contribute to the advancement of semiconductor technology by enhancing understanding of the operational behavior and performance capabilities of 3-D Nanosheet FETs specifically in inversion mode.

CHAPTER 3

DESCRIPTION OF CONCEPTS AND TECHNICAL DETAILS

3.1 Detail description of 3-D Nanosheet FET's:

The properties and behaviors of 3-D (three-dimensional) Nanosheet Field-Effect Transistors (FETs) operating in Inversion (INV) mode. Here's a breakdown of the key concepts and technical details involved:

Nanosheet FETs (NSFETs):

Three-Dimensional (3-D) Structure: Nanosheet FETs are a type of transistor design that involves stacking multiple nanosheets on top of each other. The three-dimensional structure enhances control over the flow of electric current.

Operating Modes:

Inversion Mode (INV): In traditional FETs, When the transistor is in its inversion mode, a gate voltage causes the semiconductor to form an inversion layer, which either permits or prohibits current flow between the source and drain terminals.

Junctionless Mode (JL): In junction less transistors, the source and drain do not clearly meet at any point. Rather, the conduction process involves the entire channel.

Electrical Characteristics:

Subthreshold Swing (SS): A measure of how effectively the transistor can switch between on andoff states. Lower SS values indicate better performance.

Drain-Induced Barrier Lowering (DIBL): Describes the reduction in the energy barrier betweenthe source and drain as the drain voltage increases.

On-Current: The transistor is turned on, the current that passes through it.

Comparison:

Single vs. Stacked Channels: The study likely compares the performance of Nanosheet FETs with a single nanosheet channel against those with stacked nanosheet channels.

Design Flexibility: The research evaluates the design flexibility of different transistorconfigurations, with a focus on JL TFTs compared to other modes like INV TFTs.

Short-Channel Effects: The investigation explores how well the proposed JL TFT with stackedNS channels can mitigate short-channel effects. Short-channel effects become more pronouncedas transistor dimensions are scaled down.

Potential for Advanced 3D Applications:

The analysis concludes that the JL stacked NS channel structure has potential at future technological nodes and shows promise for use in sophisticated 3D applications.

3.2 BLOCK DIAGRAM:

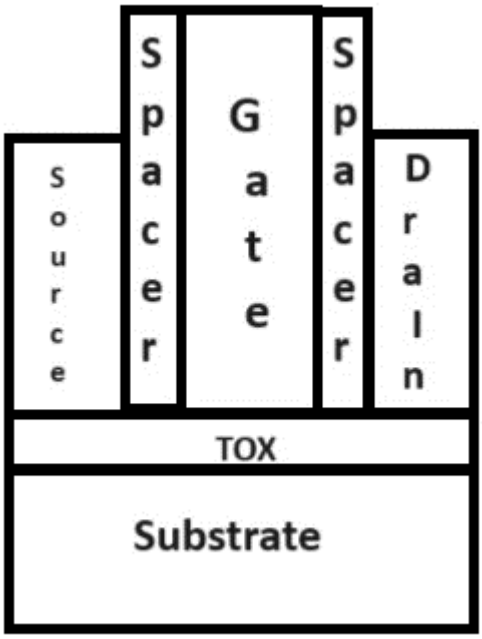

Fig: 3.1 Block diagram of 3-D FETs

3.3 SHORT CHANNEL EFFECTS:

A variety of phenomena that arise in short-channel transistors, especially When the channel length decreases in Field-effect transistors with metal-oxide-semiconductor technology the phenomenon is known as short-channel effects (SCEs). These effects intensify as transistor size decreases, which is a common trend in integrated circuit technology due to the desire for smaller, faster, and more power-efficient devices.

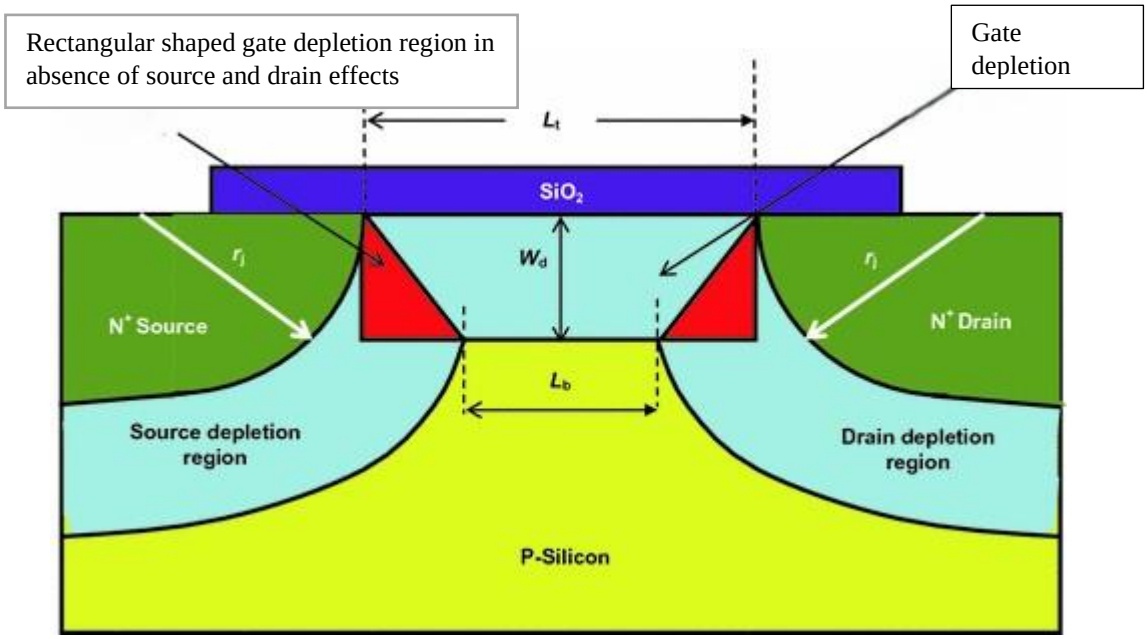

Fig:3.2: Short channel effects of MOSFET

The short-channel effects are believed to be caused by two physical phenomena:

1.Constraints on the electron drift properties in the channel.

2.Alterations in the threshold voltage due to channel shortening.

Eight distinct short-channel effects in particular can be identified.

1. Drain-induced barrier lowering and punch through

2. Surface scattering

3. Velocity saturation

4. Impact ionization

5. Hot electrons

6. Threshold voltage roll-off

7. Channel length modulation

8. “Off-state” leakage current

Drain-induced barrier lowering and punch through:

The electric field vectors, including V_{gs} and V_{ds}, influence obstacles in small MOSFETs. As drain voltage rises, the channel's potential barrier decreases, akin to the negative slope of the pn junction band curve.

Drain-Induced Barrier Lowering (DIBL) is the result. In the case of DIBL, Electrons can move from a source to a drain. even when VGS is less than $\boldsymbol{V_{th}}$.

A decrease in the s and D junction depth x_j might lessen the $\boldsymbol{V_{th}}$ shift when the charge shared by the drain and source lowers due to charge sharing.

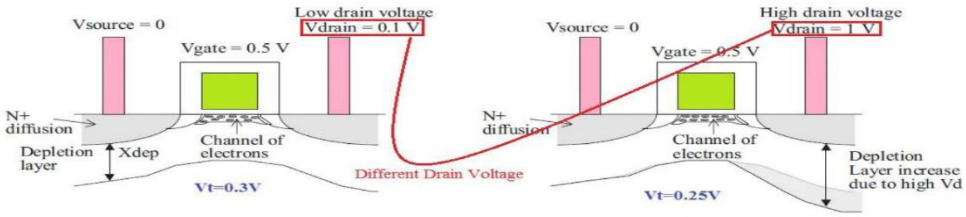

Fig:3.2.1: Drain-induced barrier lowering

As the channel length (L) decreases, the drain voltage's impact extends deeper into the channel area, resulting in a reduction in the effective channel length, known as DIBL.

DIBL arises as the drain voltage generates an electric field, reducing the potential barrier at the drain-channel interface. This enables the drain to influence the channel, even if not directly aligned with the gate.

This phenomenon results in a decrease in threshold voltage (V_{th}) and a rise in subthreshold leakage current, affecting device efficiency and power usage.

Punch through Effect:

Depletion width increases with increasing V_{ds}, and punch through occurs when these source and drain depletion zones come into contact. Higher doping concentrations in the substrate or close to the source and drain can reduce it.

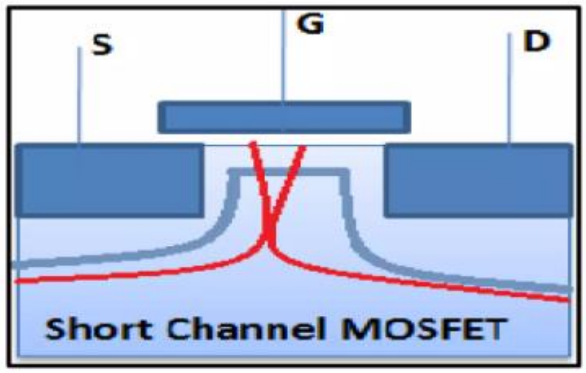

Fig 3.2.2: Punch through effect

Surface scattering:

As the longitudinal electric field component rises, surface mobility ties to the field. The lateral spread of the depletion layer into the channel shortens it. Electrons move slowly along the interface due to the MOSFET's limited carrier transport. Surface scattering, caused by electron collisions accelerated toward the interface, hampers mobility. Consequently, despite low electrons on y axis values, average surface mobility remains roughly half of bulk mobility

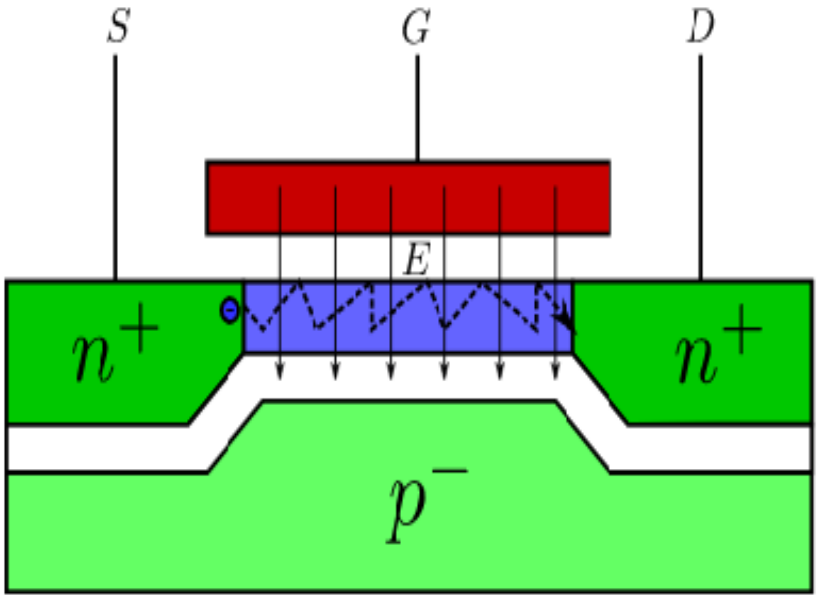

Fig 3.2.3: Surface scattering

Velocity saturation:

Velocity saturation also affects the short-channel devices' efficiency by reducing the transconductance at saturation. The channel's electron drift velocity (v_{de}) changes

linearly in relation to the electric field's strength. at low ey. By reducing the transconductance in the saturation state, velocity saturation also has an impact on the functionality of short-channel devices The channel's electron drift velocity (V_{de}) varies linearly with the electric field's strength. at low electrons on y axis. Note that rather than pinch off, velocity saturation limits the drain current. When dimensions are scaled in short channel devices without reducing the bias voltages, this happens. The highest gain attainable for a MOSFET can be determined using $\boldsymbol{v_{dec(sat)}}$ as

$$\boldsymbol{g_m = WC_{ox}v_{dec(sat)}}$$

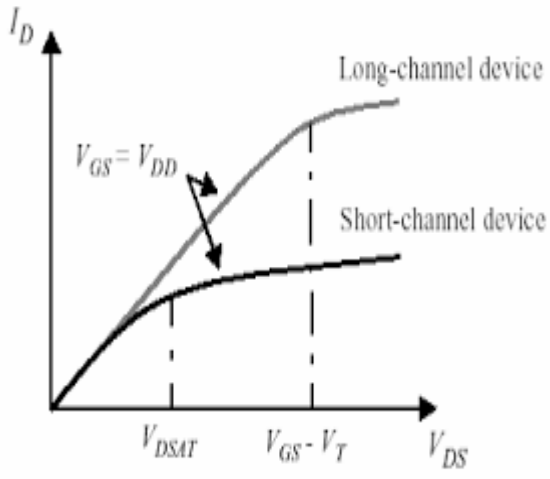

Fig 3.2.4: Velocity saturation

Impact ionization:

An additional undesirable effect, especially in NMOS devices, occurs due to the high electron velocity in strong longitudinal fields. This can generate electron-hole pairs via impact ionization or by ionizing silicon atoms. Holes move into the substrate, contributing to parasitic substrate current, while most electrons are attracted to the drain. Moreover, the region between the source and drain can act like the base of a non-polar nuclear transistor, with the source serving as the emitter and the drain as the collector. When the source gathers the previously indicated holes and the associated hole current results in a voltage drop of approximately.6V in the substrate material, the normally reversed-biased substrate-source pn junction will conduct noticeably Subsequently, an electron injection from the source to the substrate is possible, which is analogous to an electron injection from the emitter to the base. They can make fresh e-h pairings as they go in the direction of the drain by gathering enough energy. If any of the electrons

produced by the high fields manage to escape the drain field and enter the substrate, negatively impacting other devices on the chip, the problem may get worse.

High longitudinal fields have the ability to accelerate electrons that could potentially ionize silicon atoms through impact. It is possible that there is a higher concentration of holes close to the source because the drain normally attracts the majority of e-.

If the concentration of holes on the source can produce a voltage drop of approximately 0.6V at the source-substrate n-p junction, then e- can be injected into the substrate from the source. e- move in the direction of the drain, gaining energy and forming new e-h pairs. e- could seep out of the drain fields and have an impact on other equipment.

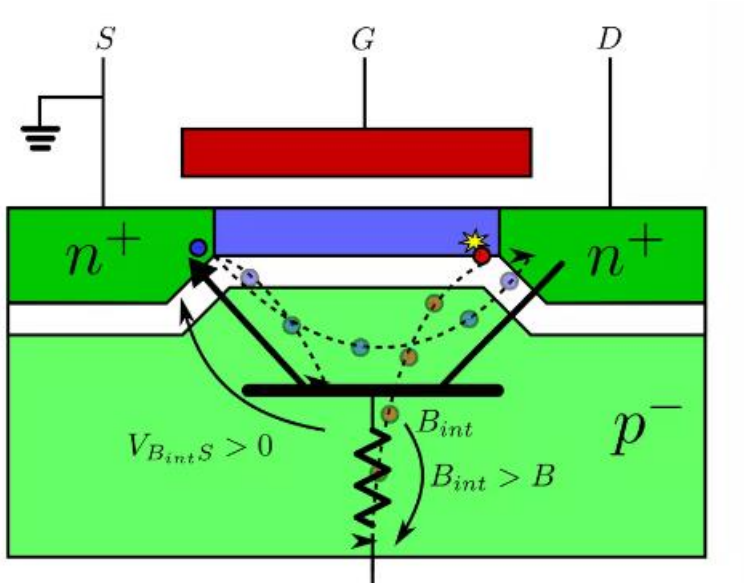

Fig 3.2.5: Impact ionization

Hot Electrons:

"Hot electrons" are the source of another issue with high electric fields. High energy electrons have the potential to enter oxides and become stranded there, resulting in oxide charging. Over time, this oxide charging can build up and impair device performance by raising V_T and negatively affecting the gate's control over the drain current.

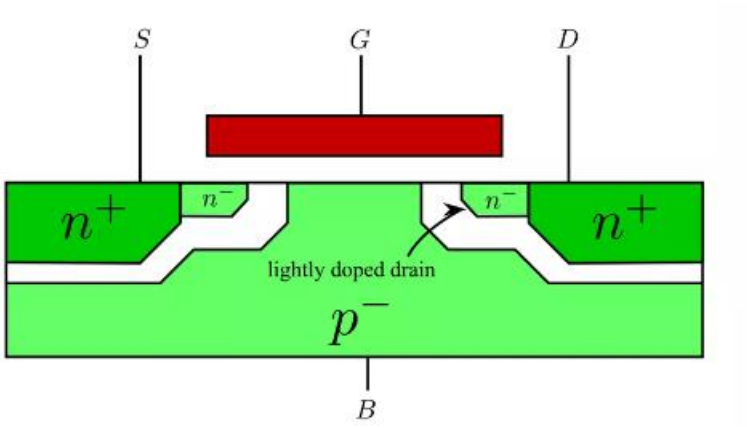

Fig 3.2.6: Hot Electrons

Significant V_{ds} electrons flowing in the channel are the cause of the channel Hot Electrons effect.

Electrons injected into the oxide, reaching the Si-SiO2 contact with sufficient kinetic energy >3.1e.v to overcome the surface potential barrier.

This could result in a permanent degradation of a MOSFET's C-V properties.

Threshold Voltage Roll-off:

A MOSFET's bulk charge terminating on the gate electrode diminishes as its channel length does. The threshold voltage drops as a result of the decrease in charge. In order to clarify this, decrease, let us restate that the depletion of this region down to a depth Wd comes before a layer of inversion is formed beneath the gate dielectric. The source and drain work together with the gate to deplete this area. Source and drain connections also contribute to depletion, even though the gate accounts for a significant portion of it. The charges in the source and drain areas partly offset the charge in the depletion layer. Essentially, a reduced gate charge is required for depletion compared to a scenario where the source and drain don't contribute. This indicates that because to source and drain effects, the threshold voltage is lowered by an amount DV_{Th}. DV_{Th} becomes noticeable in a short-channel device but is negligibly small in a long-channel MOSFET. Additionally, any two transistors with differing channel lengths on the same wafer will have distinct $\boldsymbol{V_{th}}$ values. Even in the same die, this is accurate.

1. The transistor's threshold voltage roll-off is the outcome of threshold voltage decreasing as the channel length does.
2. A number of factors, including velocity saturation and short-channel effects like DIBL, contribute to threshold voltage roll-off.

3. It leads to increased subthreshold leakage currents and degradation in the on-off characteristics of the transistor.

$$V_{th} = 2\emptyset_F - \frac{Q_B}{C_{OX}} = 2\emptyset_F + \frac{qN_AW_T}{C_{OX}}$$

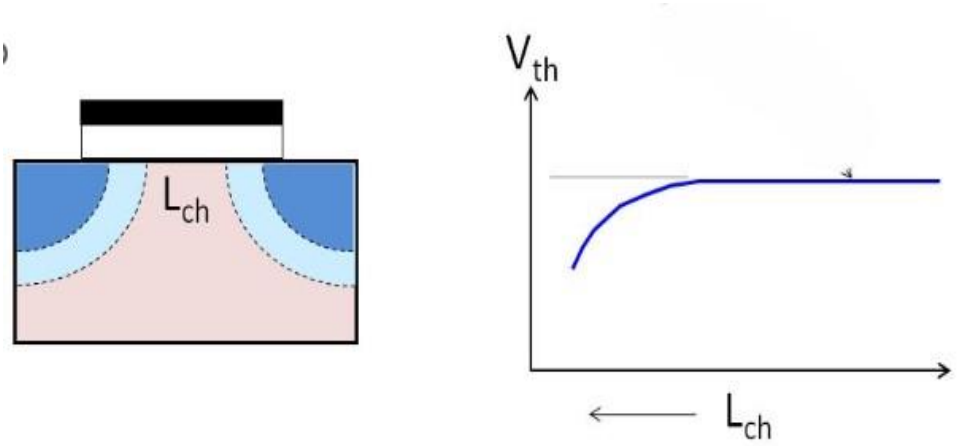

Fig 3.2.7 Threshold velocity roll-off

Channel length modulation:

When the drain voltage rises, the effective channel length decreases due to channel length modulation. This occurs because the drain voltage expansion causes the depletion region around the drain to extend into the channel, thereby shortening its length.

Channel length modulation contributes to DIBL and threshold voltage roll-off, affecting device performance and reliability.

The channel length modulation effect produces in a MOSFET that is operating in the saturation region. a rise in the capacitance of the gate-source. a reduction in the conductivity. a reduction in the cut-off frequency of unity-gain.

In field effect transistors, channel length modulation (CLM) is an effect that causes the length of the inverted channel area to shorten for significant drain biases. CLM causes the output resistance to decrease and the current to increase with drain bias.

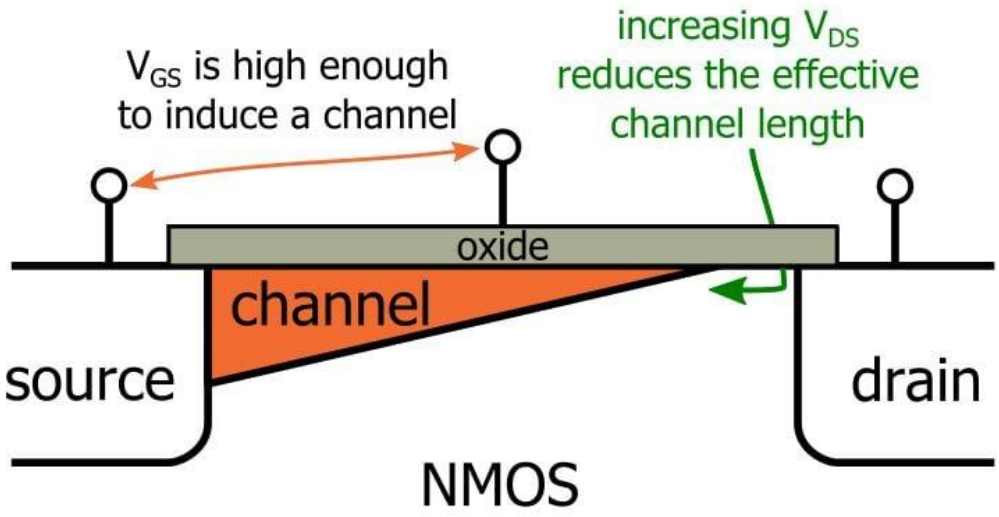

Fig 3.2.8: Channel length Modulation

"Off-state" leakage current:

When a short-channel transistor is meant to be off, with the gate-source voltage below the threshold, it leaks current from drain to source, termed off-state leakage current. As transistors shrink and channel lengths decrease, this leakage becomes more troublesome.

This phenomenon is a significant aspect of short-channel effects (SCEs) and poses challenges for both performance and power consumption in integrated circuits.

The narrowing depletion region due to reduced channel length permits carrier passage across the barrier despite lower gate-source voltage, facilitating hole or electron flow in p-channel or n-channel devices, respectively.

This tunnelling current, known as subthreshold leakage or off-state leakage current, contributes to power consumption and reduces the effectiveness of power-saving techniques.

Off-state leakage current is particularly problematic in standby or idle modes of operation, where the circuit is not actively performing computations but still consumes power.

In modern electronic devices such as smartphones and IoT sensors, minimizing off-state leakage is crucial for prolonging battery life and reducing standby power consumption.

Various techniques are employed to mitigate off-state leakage current in short-channel transistors. This includes optimizing the transistor's structure and materials, reducing the electric field in the channel region, and utilizing advanced transistor architectures such as FinFETs and nanowire transistors, which offer improved control over leakage currents compared to traditional planar transistors.

Additionally, circuit-level optimizations and power management strategies, such as power gating and voltage scaling, are implemented to reduce leakage current during idle states.

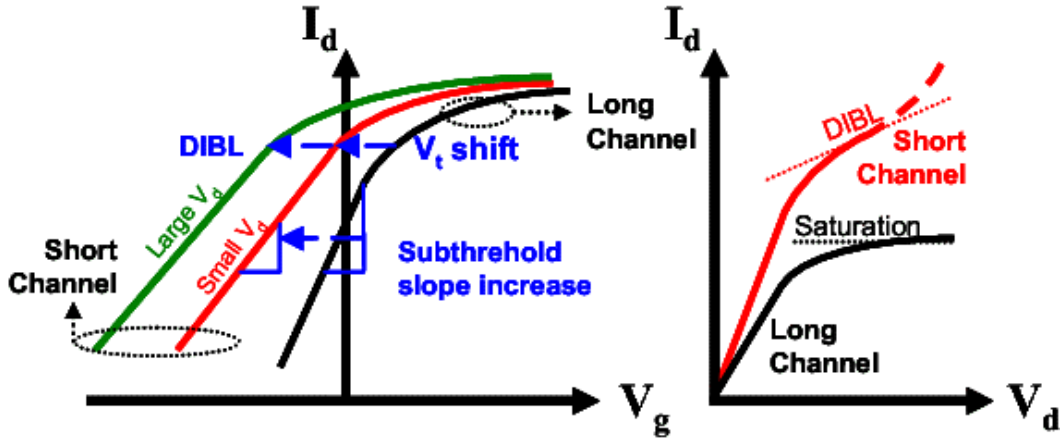

Fig 3.2.9: 'Off – state' leakage current

CHAPTER 4

METHODOLOGY

1. Demonstrate the device structure and schematic of 3-D NS-FET with given all dimension are in micro-meters.
2. Observes the doping concentration.
3. This enables the fine-tuning of NS-FET designs for optimal performance, lower power consumption, and improved reliability in VLSI circuits, ensuring that semiconductor devices meet the desired specifications and adhere to Moore's Law for continued scaling and performance advancements.
4. The provided information gives an overview of the design and simulation setup for a nanoscale field-effect transistor (NS-FET), highlighting its 3-D structure, operational modes, simulation parameters, and technology considerations. Here's a summarized version:
5. NS-FET Structure: The NS-FET incorporates a 3-D structure with a spacer, operating in Inversion(N+-P-N+) mode. INV mode features There is NA doping in the channel and ND doping in the source and drain. Simulation
6. According to IRDS, for the 3-nm technology node, a gate length (LG) of 16 nm is chosen. The aim is to attain an effective oxide thickness (EOT) of 0.78 nm using specific SiO2 and HfO2 layers. Subthreshold characteristics are enhanced with a 5 nm Si3N4 spacer. Ge.
7. Technology Considerations: Channel doping levels are determined from literature for SOI FETs, providing advantages like improved electrostatics, reduced parasitic capacitances, and lower power consumption. SOI technology minimizes threshold voltage (Vth) variations
8. Simulation Tools: Cogenda's Genius 3D TCAD simulator is used. Before simulation, TCAD models undergo calibration using established methodologies involving Poisson, continuity, and self-consistent drift-diffusion equations.
9. Advanced Models: Various models are integrated to accurately capture device behavior. These include density gradient for quantum confinement. For high doping, Schenk's bandgap narrowing and Shockley-Read-Hall for

recombination, Lombardi for mobility reduction, and non-local band-to-band tunneling for lateral tunneling. Additionally, Selberherr's model addresses impact ionization, while Lucent's model captures high-field mobility effects.

By employing these advanced models, the simulation aims to comprehensively understand the NS-FET's performance characteristics. The spacer-equipped 3-D Nanosheet Field-Effect Transistor (NS-FET). The Inversion mode (N+-P-N+) for n-type NS-FETs with certain source, channel, and drain doping profiles is discussed. A description of the 3-D NS-FET with a spacer is given. The NS-FET is shown in cross-section in the X-Y plane. Inversion mode configuration (N+-P-N+). Enhanced electrostatics, subthreshold properties, decreased parasitic capacitances, and suppressed threshold voltage changes are the reasons behind the use of silicon-on-insulator (SOI) technology.

TABLE 1. Parameters used for design the device

Device Parameter	**Inversion Mode**
Gate length	16nm
Source/drain length	12nm
Nanosheet width	10nm
Nanosheet thickness	5nm
EOT	0.78nm
Height of the gate	60nm
Effective width	60nm

CHAPTER 5

SOFTWARE IMPLEMENTATION

STEP-1

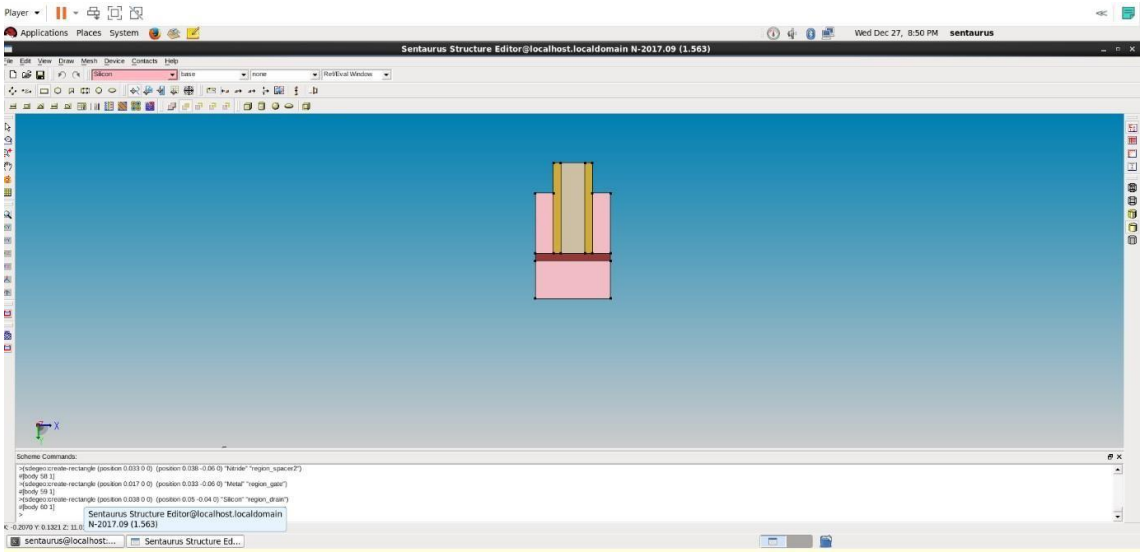

Fig-5.1: Designing the body

STEP-2

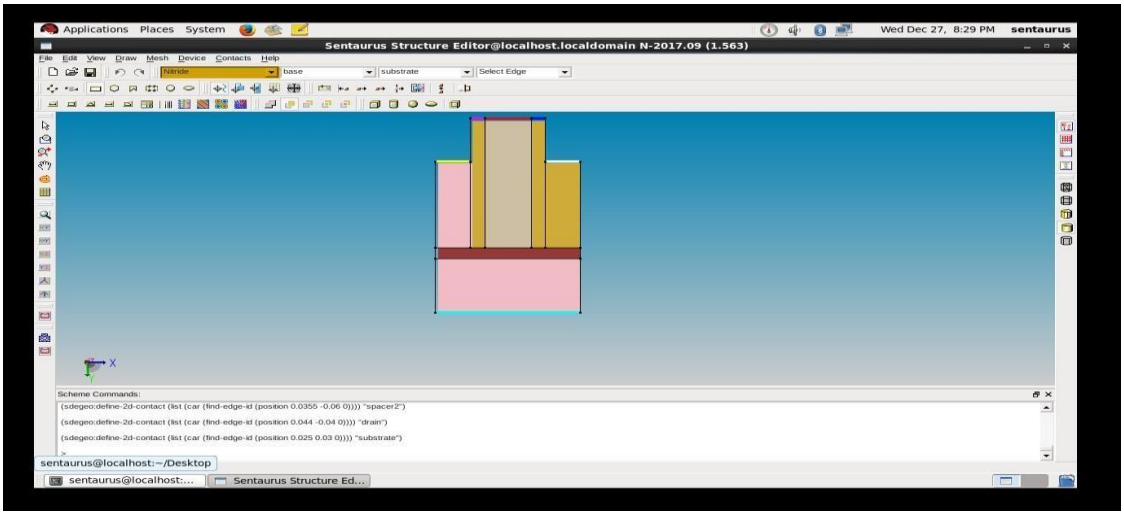

Fig-5.2: Giving the colour code for the structure

STEP-3

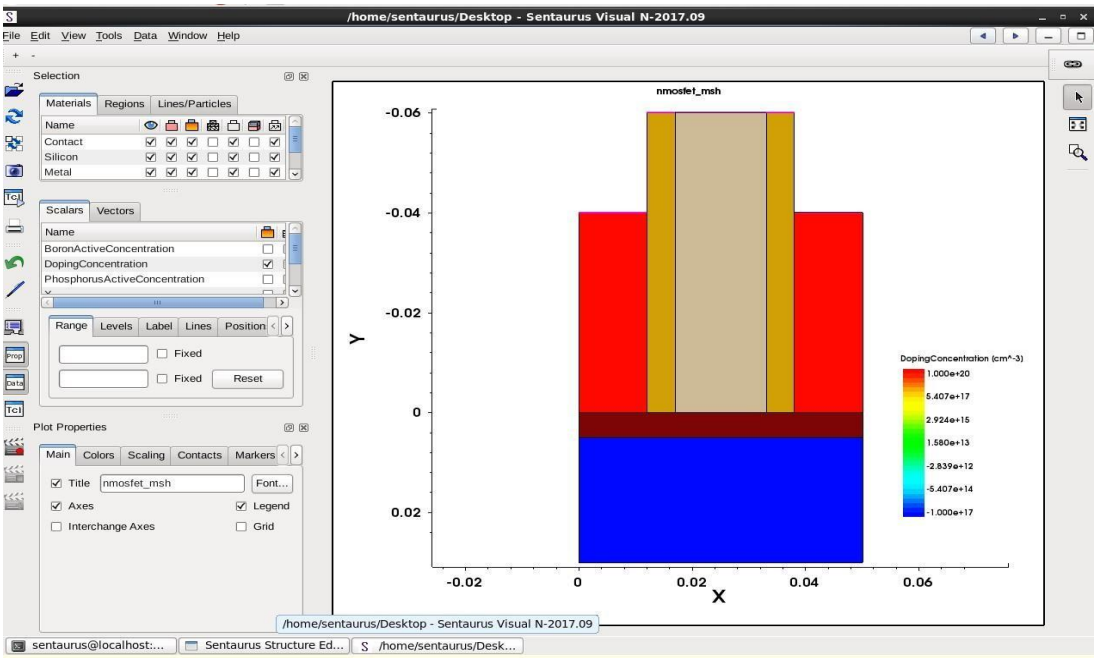

Fig-5.3: Building the mesh

STEP-4

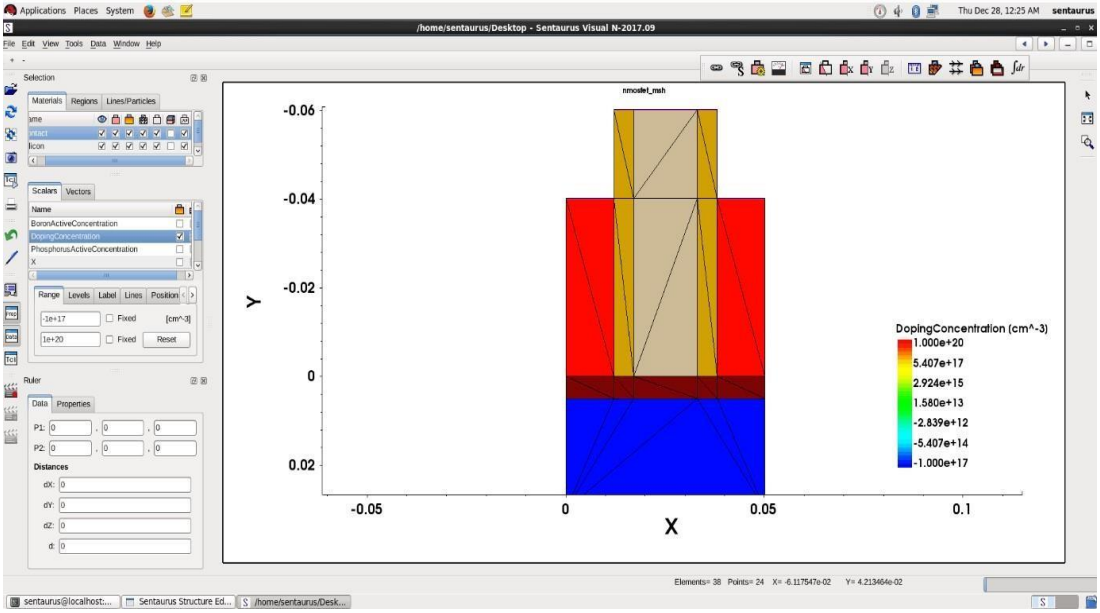

Fig-5.4: Doping concentration

Source Code (Scheme Commands):

```
>

>(set! process-up-direction "+z")

"+z"

#t

>(sdegeo:create-Rectangle (Position 0 0 0)  (position 0.05 0.03 0) "Silicon"
"region_substrate")
```

Explanation: Create the region_substrate with silicon material with rectangle and position1(0,0,0), position2(0.05,0.03,0).

```
#[body 5 1]

>(sdegeo:set-default-boolean "ABA")

"ABA"

>(sdegeo:set-default-boolean "ABA")

"ABA"

>(sdegeo:create-rectangle (position 0 0 0)  (position 0.05 0.005 0) "SiO2" "region_tox")
```

Explanation: Create a region_tox with SiO2 material with rectangle and position1(0,0,0), position2(0.05,0.005,0).

```
#[body 6 1]

>(sdegeo:create-rectangle (position 0 0 0)  (position 0.012 -0.04 0) "Silicon" "region_source")
```

Explanation: Create a region_source with silicon material with rectangle and position1(0,0,0), position2(0.012,-0.04,0).

```
#[body 7 1]

>(sdegeo:create-rectangle (position 0.012 0 0)  (position 0.017 -0.06 0) "Nitride"
"region_spacer1")
```

Explanation: Create a region_spacer1 with Nitride material with rectangle and position1(0.012,0,0), position2(0.017,-0.06,0)

```
#[body 8 1]

>(sdegeo:create-rectangle (position 0.017 0 0)  (position 0.033 -0.06 0) "Metal"
"region_gate")
```

Explanation: Create a region_gate with metal material with rectangle and position1(0.017,0,0), position2(0.033,-0.06,0).

#[body 9 1]

>(sdegeo:create-rectangle (position 0.033 0 0) (position 0.038 -0.06 0) "Nitride" "region_spacer2")

Explanation: Create a region_spacer1 with Nitride material with rectangle and position1(0.033,0,0), position2(0.038,-0.06,0)

#[body 10 1]

>(sdegeo:create-rectangle (position 0.038 0 0) (position 0.05 -0.04 0) "Silicon" "region_drain")

Explanation: Create a region_drain with silicon material with rectangle and position1(0.038,0,0), position2(0.05,-0.04,0)

#[body 12 1]

>(sdedr:define-constant-profile "ConstantProfileDefinition_substrate" "BoronActiveConcentration" 1e+17)

Explanation: Create a Constant ProfileDefinition_substrate with BoronActiveConcentration

#t

>(sdedr:define-constant-profile "ConstantProfileDefinition_source" "PhosphorusActiveConcentration" 1e+20)

Explanation: Create a ConstantProfileDefinition_substrate with PhosphorusActiveConcentration

#t

>(sdedr:define-constant-profile "ConstantProfileDefinition_drain" "PhosphorusActiveConcentration" 1e+20)

Explanation: Create a ConstantProfileDefinition_substrate with PhosphorusActiveConcentration

#t

>(sdegeo:define-contact-set "substrate" 4 (color:rgb 0 1 1) "##")

Explanation: Create a contact-set for substrate with color:rgb(0 1 1)

()

>(sdegeo:define-contact-set "sorce" 4 (color:rgb 1 1 0) "##")

Explanation: Create a contact-set for source with color:rgb(1 1 0)

()

>(sdegeo:define-contact-set "drain" 4 (color:rgb 1 1 1) "##")

Explanation: Create a contact-set for drain with color:rgb(1 1 1)

()

>(sdegeo:define-contact-set "gate" 4 (color:rgb 1 0 0) "##")

Explanation: Create a contact-set for gate with color:rgb(1 0 0)

()

>(sdegeo:define-contact-set "spacer1" 4 (color:rgb 1 0 1) "##")

Explanation: Create a contact-set for spacer1 with color:rgb(1 0 1)

()

>(sdegeo:define-contact-set "spacer2" 4 (color:rgb 0 1 0) "##")

Explanation: Create a contact-set for spacer2 with color:rgb(0 1 0)

()

(sdegeo:define-2d-contact (list (car (find-edge-id (position 0.025 0.03 0)))) "substrate")

Explanation: Create a find-edge-id for substrate with position (0.025 0.03 0)

(sdegeo:define-2d-contact (list (car (find-edge-id (position 0.006 -0.04 0)))) "source")

Explanation: Create a find-edge-id for source with position (0.006 -0.04 0)

(sdegeo:define-2d-contact (list (car (find-edge-id (position 0.0145 -0.06 0)))) "spacer1")

Explanation: Create a find-edge-id for spacer1 with position (0.0145 -0.06 0)

(sdegeo:define-2d-contact (list (car (find-edge-id (position 0.025 -0.06 0)))) "gate")

Explanation: Create a find-edge-id for gate with position (0.025 -0.06 0)

(sdegeo:define-2d-contact (list (car (find-edge-id (position 0.0355 -0.06 0)))) "spacer2")

Explanation: Create a find-edge-id for spacer2 with position (0.0355 -0.06 0)

(sdegeo:define-2d-contact (list (car (find-edge-id (position 0.044 -0.04 0)))) "drain")

Explanation: Create a find-edge-id for drain with position (0.044 -0.04 0)

>(sedr:define-refeval-window "RefEvalWin_all" "Rectangle" (position 0 0 0) (position 0.05 0.03 0))

Explanation: Create a define-refeval-window with Rectangle and position (0.05 0.03 0)

#[body 31 1]

>(sedr:define-refinement-size "Refinement_Definition_all" 0.02 0.02 0.01 0.01)

Explanation: Create a define-refinement-size with position (0.02 0.02 0.01 0.01)

#t

>(sedr:define-refinement-placement "RefinementPlacement_all" "Refinement-Definition_all" (list "window" ,"RefEvalWin_all"))

#t

>(sedr:define-refeval-window "RefEvalWin_channel" "Rectangle" (position 0.15 -0.005 0.0) (position 1.35 0.1 0.0))

Explanation: Create a define-refeval-window for RefEvalWin_channel with Rectangle and positions (0.15 -0.005 0.0) (1.35 0.1 0.0)

#[body 32 1]

>(sedr:define-multibox-size "MultiboxDefinition_channel" 0.01 0.01 0.005 0.005 1 1.35)

Explanation: Create a define-Multibox-size for MultiboxDefinition_channel with positions()

#t

>(sedr:define-multibox-placement "Multibox_Placement_channel" "Multibox_Definition_channel" "RefEvalWin_channel")

#t

>(sde:set-meshing-command "snmesh")

Explanation: Give the set mesh command for the build mesh to structure.

#t

>(sde:build-mesh "" "sdemodel3d")

Expanation: Build Mesh analysis for given above structure.

```
"Meshing successful"
#t
>(system:command "svisual sdemodel3d_msh.tdr &")
0
>
```

CHAPTER 6

RESULTS AND DISCUSSION

6.1 DC CHARACTERISTICS OF INVERSION MODE GRAPH

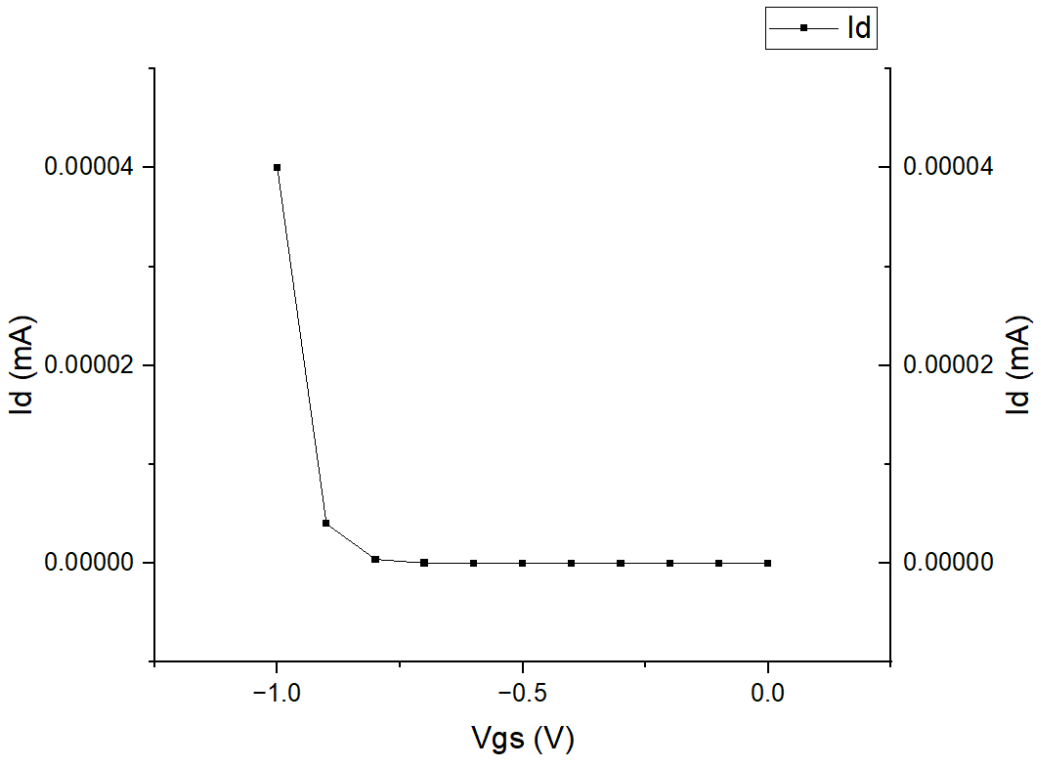

Fig 6.1 Graph of V_{gs} vs I_d

6.2 DC Characteristics

PARAMETER	INV MODES
I_{ON}(A)	4×10^{-5}
I_{OFF}(A)	4×10^{-12}
I_{ON}/I_{OFF}	1×10^{7}
SS (mV/dec) (Subthreshold swing)	60

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

7.1 Conclusion

In device Structure and Schematic, we done with building mesh of the 3D-NS-FET.The doping concentration of metals, silicon dioxide, nitrate, silicon are observed. The characteristics of 3-D Nanosheet FET is observed. The evaluation of device and circuit performance involved assessing different figures of merit (FOMs) of 3D vertically stacked gate-all-around (GAA) nanosheet field-effect transistors (NS-FETs) in inversion (INV) mode. Mixed-mode simulations were used to study circuit applications like CMOS inverters, and common-source (CS) amplifiers. In terms of various device-level metrics like subthreshold swing (SS), drain-induced barrier lowering (DIBL), and on/off-current voltage, Inversion mode proved superior to JL mode. Furthermore, the potential for scaling NS-FETs down to sub-3-nanometer nodes was assessed, demonstrating switching ratios exceeding approximately 10^6 even with a gate length (LG) of 10 nm. The effects of temperature on circuit and device performance were thoroughly examined for both modes. With a lower supply voltage (V_{DD}), it was found that the inversion mode of NS-FETs showed a slight fluctuation in the oscillation frequency ($\boldsymbol{f_{osc}}$). As Inversion mode was applied to digital and analog circuits, propagation time was lowered. Furthermore, Inversion mode demonstrated superior performance in terms of gain and oscillation frequency ($\boldsymbol{f_{osc}}$) for analog applications like CS amplifier. These evaluations offer insightful information about the analog and digital uses of NS-FETs for sub-3-nanometer technological nodes operating in Inversion mode. The findings underscore the potential of Inversion-mode NS-FETs for achieving high-performance and efficient circuit operation, especially in advanced semiconductor technologies.

7.2 Future Scope

The mesh analysis of the structure.
Observe the characteristics of 3D NSFET in both at the circuit and device levels. The performance of 3D NSFET in junction-less (JL) modes.

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