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Grade	**19.75** out of 33.00 (**59.85**%)

Question 1

Correct

Mark 1.00 out of 1.00

Suppose we have a 3 stage pipeline with 3 computation blocks requiring 80ps and 3 registers requiring 20ps. Now we double the number of pipeline stages in the above setup. What is the ratio of throughput improvement? (answer in 2 decimal places, truncate, don't round)

Answer: 1.66 ✔

The correct answer is: 1.66

Question 2

Incorrect

Mark 0.00 out of 2.00

Given the following program executed by the PIPE architecture processor, list out all the exceptions that will be registered at least once in the various stage specific STAT registers (i.e., M_STAT, E_STAT, D_STAT) during the entire execution of the code .

```
0x000: xorl %esp,%esp
  0x002: je dest
  0x007: irmovl $1, %eax
  0x00d: pushl %eax
  0x00f:  halt
  0x010: dest:
  0x010: .byte 0xFF
```

- [ ] a. HLT
- [ ] b. ADR
- [x] c. INS ✔
- [x] d. AOK ✖

Your answer is incorrect.

The correct answers are:
ADR,

INS,

HLT

Question 3

Partially correct

Mark 0.75 out of 1.00

Which of the following are true about early RISC architecture

- a. **Complicated addressing formats**
- b. **Simple addressing formats** ✔
- c. **Developed to reduce semantic gap between high level language and low level language**
- d. **Use of conditional codes**
- e. **Intensive use of registers** ✔
- f. **No use of conditional codes** ✔
- g. **Intensive use of stack**

Your answer is partially correct.

You have correctly selected 3.

The correct answers are:

Simple addressing formats,

No use of conditional codes,

Intensive use of registers ,

Developed to reduce semantic gap between high level language and low level language

Question 4

Correct

Mark 2.00 out of 2.00

You are given the following code having PIPE implementation, with bubbling, forwarding, error handling, etc considered.

xorq %esp, %esp

irmovq $10, %eax

irmovq %2, %ebx

irmovq %3, %ebx

pushq %ebx

What is the value that is stored in M_valE, e_valE, and W_valE in the 6th clock cycle during execution (enter in following format (x,y,z))?

Answer: 2,3,10 ✔

The correct answer is: (2,3,10)

Question 5

Correct

Mark 1.00 out of 1.00

Comparing the time T1 taken for a single instruction on a pipelined CPU with time T2 taken on non-pipelined but identical CPU, we can say that

a. T1 == T2

b. T1 > T2 ✔

c. T1 < T2

d. None

Your answer is correct.

The correct answers are:
T1 > T2,

None

Question 6

Not answered

Marked out of 2.00

For the given code that is being executed in PIPE- implementation:

irmovq $10, %eax

irmovq $50, %edx

Irmovq $0x001a, %esp

pushq %edx

subq %edx, %eax

rrmovq %eax, %ebx

However, while implementing this code, a memory error was encountered. At which clock cycle was the setting of condition codes disabled by the excepting instruction, and at what pipeline stage (F, D, E, M, W) will the excepting instruction stop the program execution? Make sure your answer is comma separated.

Answer: ✖

The correct answer is: 7, W

Question 7

Not answered

Marked out of 2.00

What is the minimum number of stages in pipeline that would lead to maximum throughput in the following sequence of 6 blocks(combinational logic executing micro-instructions) with delays 60, 40, 50, 60, 60, 20 (in picoseconds), assuming blocks cannot be divided into sub-blocks? Also give the throughput up to 2 decimal places(truncate, don't round) in GIPS. (give comma separated answers, eg:12, 34.56)

Answer:

The correct answer is: 6, 16.66

Question 8

Correct

Mark 1.00 out of 1.00

If the W stage was before the M stage, which instructions would fail?

- a. mrmovl ✔
- b. pushl
- c. popl ✔
- d. rmmovl

Your answer is correct.

The correct answers are:
mrmovl,

popl

Question 9

Correct

Mark 1.00 out of 1.00

Which of the following correctly describes the ret function in Y86:

a. Read 1 byte > Read stack pointer > Decrement stack pointer by 4 > Read return address from old stack pointer > Update stack pointer > Set PC to return address

b. Read 1 byte > Read stack pointer > Increment stack pointer by 4 > Update stack pointer > Read return address from old stack pointer > Set PC to return address

c. Read 1 byte > Read stack pointer > Decrement stack pointer by 4 > Update stack pointer > Read return address from old stack pointer > Set PC to return address

d. Read 1 byte > Read stack pointer > Increment stack pointer by 4 > Read return address from old stack pointer > Update stack pointer > Set PC to return address ✔

Your answer is correct.

The correct answer is:
Read 1 byte > Read stack pointer > Increment stack pointer by 4 > Read return address from old stack pointer > Update stack pointer > Set PC to return address

Question 10

Correct

Mark 1.00 out of 1.00

Branch and Call destinations are given as PC-relative addresses in Y86-64, rather than using the absolute addressing seen in x86-64.

Select one:

True

False ✔

The correct answer is 'False'.

Question 11

Partially correct

Mark 1.00 out of 2.00

Which of the following require an explicit control over their sequencing in piped architecture? Mark all that apply.

- a. Instruction memory
- b. Condition code register ✔
- c. Program counter
- d. Combinational logic
- e. Data memory ✔
- f. Register File

Your answer is partially correct.

You have correctly selected 2.

The correct answers are:

Register File,

Condition code register,

Data memory,

Program counter

Question 12

Correct

Mark 2.00 out of 2.00

Determine the number of instructions the following Y 86-64 instruction sequence encodes (only write the integer, for example if the number of instructions are 2 then write 2 in text box provided for answer)

a0af30f30e0040ac109061ed00

Answer: 3 ✔

The correct answer is: 3

Question 13

Not answered

Marked out of 2.00

Consider a 3GHz (gigahertz) processor with a 3 stage pipeline and stage latencies T1, T2 and T3 such that

T1 = 3*T2/4 = 2*T3

If the longest pipeline stage is split into 2 pipeline stages of equal latency, the new frequency is ✖ **GHz, ignoring delays in the pipeline registers.**

The correct answer is: 4

Question 14

Incorrect

Mark 0.00 out of 1.00

A 3-stage pipeline has stage delays as 10, 120, 10 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 instructions on this pipeline will be (in ns)

Answer: 125000 ✖

The correct answer is: 125250

Question 15

Correct

Mark 2.00 out of 2.00

What is the value for A+B+C (eg: if answer for A is 1, for B is 2 and for C is 3, then mark 6)?

In the Y86 architecture,

1. **How many program registers are written by the “pushq rA” instruction?**
2. **What is the increment in the program counter for “mrmovl D(rB), rA” instruction?**
3. **What is the increment in the program counter for “addl rA, rB” instruction?**

Answer: 9 ✔

The correct answer is: 9

Question 16

Incorrect

Mark 0.00 out of 2.00

Given the following program executed by the PIPE architecture processor, what will be the value of W_STAT when the processor stops execution

0x000: xorl %esp,%esp

0x002: jne dest

0x007: irmovl $1, %eax

0x00d: pushl %eax

0x00f: halt

0x010: dest:

0x010: .byte 0xFF

a. ADR

b. INS

c. AOK

d. HLT ✖

Your answer is incorrect.

The correct answer is:
ADR

Question 17

Correct

Mark 2.00 out of 2.00

```
1  .start 0x200 # Start code is at the address 0x200
2      irmovq $7,%r11
3      rrmovq %r11,%r12
4  .loop:
5      rmmovq %r12,-7(%r11)
6      addq %r11,%r12
7      jmp .loop
8  .exit
```

Assuming that the start address is 0x200, if the address of line8 is addr, what do we get when we write bytes of addr in reverse order.

a. 22 20 00 00 00 00 00 00

b. 21 02 00 00 00 00 00 00 ✔

c. 12 20 00 00 00 00 00 00

d. 22 02 00 00 00 00 00 00

Your answer is correct.

The correct answer is:
21 02 00 00 00 00 00 00

Question 18

Correct

Mark 2.00 out of 2.00

addl %eax, %ebx
subl %ebx, %ecx
addl %ecx, %edx

What is the total number of clock cycles required for this snippet to fully run? (in number of cycles, only write the integer ex. 13)

Answer: 7 ✔

The correct answer is: 11

Question 19

Correct

Mark 3.00 out of 3.00

The following set of instructions are being executed on a Y86 SEQ hardware:

Cycle 1) 0x000: irmovl $0x100, %ebx

Cycle 2) 0x006: irmovl $0x050, %edx

Cycle 3) 0x00c: irmovl $0x200, %ecx

Cycle 4) 0x013: subl %edx, %ebx

Cycle 5) 0x015: addl %ecx, %ebx

Answer the following questions:

1. What is the value of the Program counter at the end of Cycle 2?
2. What is the value of the Program counter at the beginning of Cycle 4?
3. What is the value stored at %ebx at the beginning of Cycle 4?
4. What is the value stored at %ebx at the end of Cycle 5?

a. 0x00c, 0x013, 0x100, 0x250

b. 0x00c, 0x013, 0x100, 0x050

c. 0x006, 0x013, 0x100, 0x050 ✔

d. 0x006, 0x013, 0x050, 0x250

Your answer is correct.

The correct answers are:
0x006, 0x013, 0x100, 0x050,

0x00c, 0x013, 0x100, 0x250,

0x006, 0x013, 0x050, 0x250,

0x00c, 0x013, 0x100, 0x050

Question 20

Not answered

Marked out of 1.00

Assuming a perfect scenario (no bubbling, forwarding or error handling and each instruction stays in each stage for exactly 1 clock cycle) and an infinite number of instructions, how many times faster is the pipeline as compared to the sequential architecture? (only put the number)

Answer:

The correct answer is: 5