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Grade	**18.00** out of 30.00 (**60**%)

Question 1

Correct

Mark 3.00 out of 3.00

Consider a Hard Disk with 50 cylinders. The request to access the cylinder occurs in the following sequence of 4 cylinder accesses. The Access sequence is [4, 34, 10, 7]. Assuming that the head is currently at cylinder 10, what is the time taken to satisfy all 4 requests if it takes 2 ms to move from one cylinder to the next left or right adjacent cylinder, and you always move to the nearest cylinder in the next move.

- a. 144 ms ✔
- b. 140 ms
- c. 134 ms
- d. 130 ms

Your answer is correct.

The correct answer is:
144 ms

Question 2

Correct

Mark 1.00 out of 1.00

Consider a 256 block cache that is 4 way set associative. Calculate number of cache misses for accessing the following memory block in order. Sequence of blocks is [1,2,3,4,4,3,2,1]. Assume Least Recently Used policy is used to evict a block from a filled set.

- a. 4 misses ✔
- b. 7 misses
- c. 6 misses
- d. 5 misses

Your answer is correct.

The correct answer is:
4 misses

Question 3

Incorrect

Mark 0.00 out of 3.00

1. **Consider a 4-stage pipeline where different instruction require different no of cycles at different stages :**

	S1	S2	S3	S4
I1	1	3	1	1
I2	1	1	3	1
I3	1	2	1	1
I4	1	1	1	2

How many cycles are required to complete the execution of all 4 instructions?

a. 12 cycles

b. 13 cycles ✖

c. 14 cycles

d. 11 cycles

Your answer is incorrect.

The correct answer is:
12 cycles

Question 4

Correct

Mark 3.00 out of 3.00

A cache has a 0.95 hit rate. The size of each cache block is 1024 bits. The cache hit latency is 5ns. The main memory takes 200 ns to return the first word (32 bits) of a line, and 10ns to return each subsequent word. What is the Cache miss penalty of this system? (Assume that the cache miss is detected by first probing the cache once. Upon a miss the line is fetched and the read operation is re-executed with the data in the cache)

a. 520 ns ✔

b. 530 ns

c. 540 ns

d. 550 ns

Your answer is correct.

The correct answer is:
520 ns

Question 5

Incorrect

Mark 0.00 out of 2.00

Consider a R x C bit DRAM chip. Where R = 16K and C=4. A single refresh operation takes 150 ns.. The refresh operation happens after every 4 milliseconds. The memory read has to happen between two refresh operations. What is the fraction of time in percentage available to the CPU to perform a memory read/write operation on the DRAM ?

- a. 42% ✖
- b. 38 %
- c. 36 %
- d. 32 %

Your answer is incorrect.

The correct answer is:
38 %

Question 6

Incorrect

Mark 0.00 out of 2.00

Consider a 32 KB 2-way set associative with 32-byte block size. The main memory size is 4GB. The CPU hardware takes k/10 nanoseconds to perform a k bit comparison. What is the hit latency of the cache corrected upto 1 decimal place? Assume the time to access a set inside the cache is 0.6 ns and the TAG match happens in parallel.

- a. 1.2 ns ✖
- b. 3.4 ns
- c. 3.2 ns
- d. 2.4 ns

Your answer is incorrect.

The correct answer is:
2.4 ns

Question 7

Incorrect

Mark 0.00 out of 1.00

Which of the following is/are false?

S1: The main advantage of direct mapping is that the cache hit ratio increases drastically if two or more frequently used blocks map onto the same region.

S2: For two level memory hierarchy cache and main memory, WRITE THROUGH results in more write cycles to main memory then WRITE BACK.

a. Only S1

b. Neither ✖

c. Only S2

d. Both S1 and S2

Your answer is incorrect.

The correct answer is:
Only S1

Question 8

Correct

Mark 2.00 out of 2.00

An assembly program has 60% arithmetic instructions and 40% memory read instruction. The arithmetic operations have a single cycle latency. The cache hit rate is 75%. The hit latency is 2 cycles and the cache miss latency is 8 cycles. What is the CPI value of the processor for this program. CPI is clock cycles per instruction.

a. 2 ✔

b. 5

c. 4

d. 3

Your answer is correct.

The correct answer is:
2

Question 9

Correct

Mark 1.00 out of 1.00

Consider a 3 level memory hierarchy L1->L2->L3. L1 is the fastest and L3 is the slowest. The cycle times of L1, L2 and L3 are 400 MHz, 100 MHz and 50 MHz respectively. What is the number of wait states that L1 needs to correctly synchronize its data accessed with L3.

- a. 8 ✔
- b. 7
- c. 6
- d. 4

Your answer is correct.

The correct answers are:
7,

8

Question 10

Correct

Mark 3.00 out of 3.00

Out of 100 memory read requests, 95 are satisfied by the cache with a hit latency of 48 ns. The rest 5 are satisfied by main memory with a miss latency of 120 ns. Main memory access time is 60 ns. CPU generates 80% of the read requests to read the data and the remaining for write operation. What is the average access time (in ns) of the memory when considering both read and write operations?

- a. 52.4 ns
- b. 54.3 ns
- c. 53.2 ns ✔
- d. 55.6 ns

Your answer is correct.

The correct answer is:
53.2 ns

Question 11

Correct

Mark 1.00 out of 1.00

Given a 5 stage pipeline with stages taking 2,4,1,3,6 nano-seconds. The buffer latency of each stage is equal to that of the stage latency. What is the clock period of the pipeline?

a. 13 ns

b. 2 ns

c. 4 ns

d. 12 ns ✔

Your answer is correct.

The correct answer is:
12 ns

Question 12

Incorrect

Mark 0.00 out of 3.00

A distinction is made between physical records and logical records. A logical record is a collection of related data elements treated as a conceptual unit, independent of how or where the information is stored. A physical record is a contiguous area of storage space that is defined by the characteristics of the storage device and operating system. Assume a disk system in which each physical record contains thirty 120-byte logical records. Calculate how much disk space (surfaces) will be required to store 200,000 logical records if the disk is fixed-sector with 512 bytes/sector, with 96 sectors/track, 210 tracks per surface, and 8 usable surfaces. Assume that records cannot span two sectors. A surface is considered taken even if it is partially filled.

a. 5 surfaces ✖

b. 3 surfaces

c. 4 surfaces

d. 2 surfaces

Your answer is incorrect.

The correct answer is:
3 surfaces

Question 13

Correct

Mark 2.00 out of 2.00

Consider a byte addressable machine with 1 GB physical memory. The width of the tag field in a 512 KB 8-way set associative cache is ? Assume the block size is 2^Y bytes and the number of sets is 2^X

- a. 14 ✔
- b. 17
- c. 15
- d. 16

Your answer is correct.

The correct answer is:
14

Question 14

Incorrect

Mark 0.00 out of 1.00

Consider a cache organization C1 with size S and block size B. C1 is m way set associative. Consider another cache organization C2 with size S and block size B. C2 is n way set associative. If n = 2m. Then which of these is true.

- a. C2 has twice the number of TAG bits compared to C1 ✖
- b. C2 has half the number of set bits than C1
- c. C2 has twice the block selection logic within a set than C1.
- d. All of them

Your answer is incorrect.

The correct answer is: C2 has twice the block selection logic within a set than C1.

Question 15

Correct

Mark 2.00 out of 2.00

The average time to move the read/write head of a disk is 8 ms, it rotates at 1200 rpm and has a data transfer rate of 5 MB/sec. What is the average time for accessing a file of 8 kB? (in milliseconds).

- a. 30.8
- b. 50.5
- c. 27.8
- d. 34.5 ✔

Your answer is correct.

The correct answer is:
34.5