Started on	Monday, 2 August 2021, 10:01 AM
State	Finished
Completed on	Monday, 2 August 2021, 11:30 AM
Time taken	1 hour 28 mins
Grade	**46.50** out of 70.00 (**66.43**%)

Question 1

Correct

Mark 1.00 out of 1.00

A CPU generally handles an interrupt by executing an interrupt service routine.

a. **By checking the interrupt register after finishing the execution of the current instruction.** ✔

b. **As soon as the interrupt is raised.**

c. **By checking the interrupt register at fixed time intervals.**

d. **By checking the interrupt register at the end of the cycle.**

Your answer is correct.

The correct answer is:
By checking the interrupt register after finishing the execution of the current instruction.

Question 2

Correct

Mark 2.00 out of 2.00

Find the valid y86 instruction sequence?

1. **30f3fcffffffffffffff4063000800000000000000**
2. **a06f800c0200000000000000**
3. **505407000000000006113f01090**
4. **611310106462**

a. 3 and 4

b. 1 and 2 ✔

c. 1, 2 and 3

d. 2 and 3

Your answer is correct.

The correct answer is:
1 and 2

Question 3

Not answered

Marked out of 4.00

Explain how the system call printf is executed through the exception mechanism. Write the assembly for a program that executes printf(" hello world “). You must only write the assembly code that does the printf part.

Question 4

Correct

Mark 2.00 out of 2.00

```
main(){
printf("PROCESS");
fflush();
fork();
fork();
}
```

a. 6

b. 4 ✔

c. 8

d. 2

Your answer is correct.

The correct answer is:
4

Question 5

Correct

Mark 2.00 out of 2.00

Consider the following code fragment, which of the assembly snippets will it compile to?

```
int woohoo(int a, int r)
{
 int ret = 0;
 switch(a)
 {
   case 11:
    ret = 4;
    break;
   case 22:
   case 55:
    ret = 7;
    break;
   case 33:
   case 44:
    ret = 11;
    break;

   default:
    ret = 1;
 }
 return ret;
}
```

Fragment 1

```
woohoo:
        pushl   %ebp
        movl    %esp, %ebp
        movl    8(%ebp), %edx
        movl    $0, %ecx
        cmpl    $11, %edx
        jne     .L2
        movl    $4, %ecx
        jmp     .L3
.L2:
        cmpl    $22, %edx
        jne     .L3
        movl    $7, %ecx
.L3:
        cmpl    $55, %edx
        jne     .L5
        movl    $7, %ecx
.L5:
        cmpl    $33, %edx
        sete    %al
        cmpl    $44, %edx
        sete    %dl
        orl     %edx, %eax
        testb   $1, %al
        je      .L6
        movl    $11, %ecx
.L6:
        movl    %ecx, %eax
        popl    %ebp
        ret
```

Fragment 2

```
woohoo:
        pushl   %ebp
        movl    $1, %eax
        movl    %esp, %ebp
        movl    8(%ebp), %edx
        decl    %edx
        cmpl    $4, %edx
        ja      .L2
        jmp     *.L9(,%edx,4)
        .section        .rodata
        .align 4
        .align 4
.L9:
        .long   .L3
        .long   .L5
        .long   .L7
        .long   .L7
        .long   .L5
        .text
.L3:
        movl    $4, %eax
        jmp     .L2
.L5:
        movl    $7, %eax
        jmp     .L2
.L7:
        movl    $11, %eax
.L2:
        popl    %ebp
        ret
```

Fragment 3

```
woohoo:
        pushl   %ebp
        movl    %esp,%ebp
        movl    8(%ebp),%eax
        subl    $11,%eax
        je      .L6
        subl    $11,%eax
        je      .L7
        subl    $11,%eax
        je      .L8
        subl    $11,%eax
        je      .L8
        subl    $11,%eax
        je      .L7
        jmp     .L9
.L6:
        movl    $4,%eax
        jmp     .L4
.L7:
        movl    $7,%eax
        jmp     .L4
.L8:
        movl    $11,%eax
        jmp     .L4
.L9:
        movl    $1,%eax
.L4:
        ret
```

a. None

b. Fragment 2

c. Fragment 1

d. Fragment 3 ✔

Your answer is correct.

The correct answer is:
Fragment 3

Question 6

Incorrect

Mark 0.00 out of 2.00

Consider the following code(C code calling assembly function):

```c
#include<stdio.h>
int func(int N);
int main(){
    int n;
    scanf("%d",&n);
    printf("%d\n",func(n));
}

```

```
.text
.global func
func:
    pushq %rbx
    movq %rdi,%rbx
    movq $1 ,%rax
    cmpq $1 ,%rdi
    jle .base
    dec %rdi
    call func
    imul %rbx,%rax
.base:
    popq %rbx
    ret

```

This code computes the factorial of a number(n), which of the following statements are true about it?

1. **If we change line number 7 to cmpq $0, %rdi, code will output the factorial n as output.**
2. **If we change the number 7 to cmpq $0, %rdi, code will not output the factorial of n as output**
3. **If we interchange line 9 and line 11, code will output some random number.**
4. **If we interchange line 9 and line 11, code will throw a segmentation fault.**
5. **If we interchange line 10 and line 11, code will throw a segmentation fault.**

a. 2, 3 and 5

b. 1 and 4

c. 2 and 4 ✖

d. 1, 4 and 5

Your answer is incorrect.

The correct answer is:
1 and 4

Question 7

Correct

Mark 3.00 out of 3.00

Consider a paging system with 48 bit virtual address space. Each address deferes to a byte in memory. Suppose the size of a page is 16 KB and the main memory size is 16 GB. Each page table entry contains frame number and 2 protection bits, 1 valid bit and 1 dirty bit. The minimum size of the page table (in GB) is ?

a. 50

b. 48 ✔

c. 52

d. 42

Your answer is correct.

The correct answer is:
48

Question 8

Correct

Mark 3.00 out of 3.00

Consider a system such that the number of clocks for continuously checking whether an interrupt has arrived from the mouse is 400 cycles. The processor executes at 500 MHz. Determine the fraction of CPU time consumed, in checking for the interrupt, when the mouse has to be probed 30 times per second.

a. 0.01

b. 0.0002 ✔

c. 0.002

d. 0.03

Your answer is correct.

The correct answers are:
0.0002,

0.002

Question 9

Incorrect

Mark 0.00 out of 1.00

In order to go from Kernel mode to User mode during program execution ?

- a. A function call has to happen
- b. A hardware interrupt is required
- c. A system call has to happen ✖
- d. A software interrupt is required

Your answer is incorrect.

The correct answer is:
A software interrupt is required

Question 10

Correct

Mark 1.00 out of 1.00

After the interrupt has occurred, the stack is filled with ?

- a. **Return address**
- b. None
- c. Both ✔
- d. **Status register**

Your answer is correct.

The correct answer is:
Both

Question 11

Correct

Mark 2.00 out of 2.00

If each address space represents one byte of storage space, how many address lines are needed to access DRAM chips arranged in 4 x 6 array, where each chip is 8K x 4 bits in size ?

- a. 13
- b. 16
- c. 17 ✔
- d. 15

Your answer is correct.

The correct answer is:
17

Question 12

Incorrect

Mark 0.00 out of 3.00

A processor has 64 registers and uses 16-bit instruction format. It has two types of instructions: I-type and R-type. Each I-type instruction contains an opcode, a register name, and a 4-bit immediate value. Each R-type instruction contains an opcode and two register names. If there are 16 distinct I-type opcodes, then the maximum number of distinct R-type opcodes is

a. 14

b. 16 ✖

c. 12

d. None of these

Your answer is incorrect.

The correct answer is:
12

Question 13

Correct

Mark 3.00 out of 3.00

Consider a main memory with 5 page frames and the following sequence of page references. [9,8,7,9,3,0,2,9,8,3,9,2,0,9]. Which of the following is true with respect to the page eviction policies First In First Out (FIFO) and Least Recently Used (LRU) ?

a. FIFO incurs 2 more page faults than LRU

b. Both incur the same number of page faults

c. FIFO incurs 1 more page fault than LRU ✔

d. FIFO incurs 1 less page fault than LRU

Your answer is correct.

The correct answer is: FIFO incurs 1 more page fault than LRU

Question 14

Correct

Mark 1.00 out of 1.00

Suppose after analyzing a new cache design, you discover that the cache has far too many conflict misses and this needs to be resolved. You know that you must increase associativity in order to decrease the number of cache misses. What are the implications of increasing the associativity ?

a. **Slower cache access time** ✔

b. **Increased block size**

c. **Increased index bits**

d. **All of these**

Your answer is correct.

The correct answer is:
Slower cache access time

Question 15

Correct

Mark 3.00 out of 3.00

Consider a machine with a byte addressable main memory of 2^24 bytes. The block size is 32 bytes and the cache is 4-way set associative having 2^15 cache blocks. What are the set bits in binary and tag address of memory address (E4201F) in hexadecimal ?

a. **0100, 39** ✔

b. **0100, 27**

c. **0010, 1F**

d. **0110, 37**

Your answer is correct.

The correct answer is:
0100, 39

Question 16

Incorrect

Mark 0.00 out of 2.00

Consider a 2-way set-associative cache of size 5KB. Each cache block is of size 256 Bytes. If the memory blocks are requested in order: 1, 32, 12, 48, 31, 44, 2, 13, 10, 30, 12, 8 ,15. How many conflict misses will occur.

a. 2 ✖

b. 1

c. 5

d. 4

Your answer is incorrect.

The correct answer is:
1

Question 17

Correct

Mark 3.00 out of 3.00

Consider a system employing interrupts for data transfers. The device transfers data at an average rate of 8KB per second. The interrupt handler takes 100 micro-seconds to process the interrupt. Determine what fraction of processor time is consumed by this device if it interrupts for every byte transferred. HINT: calculate the time required by the device to transfer 1 byte. The fraction has to be taken with respect to this value.

a. **0.71**

b. **0.82** ✔

c. **0.56**

d. **0.43**

Your answer is correct.

The correct answer is:
0.82

Question 18

Correct

Mark 3.00 out of 3.00

Suppose we create a 3 stage pipeline from the 5 stage pipeline in the following way:

Stage 1: Combine the fetch and decode stage

Stage 2: Execute

Stage 3: Combine the memory and writeback stage

Suppose the three-stage pipelined processor did not implement forwarding, how many cycles are required of stalling will be required to execute the following code?

```
irmovq $0x4000, %rbx
irmovq $0x50, %rdx
mrmovq 0x3(%rbx), %rcx
subq %rcx, %rbx
addq %rdx, %rbx
```

- a. 5 cycles ✔
- b. 6 cycles
- c. 3 cycles
- d. 8 cycles

Your answer is correct.

The correct answer is:
5 cycles

Question 19

Correct

Mark 1.00 out of 1.00

When (-89) is represented in 2's complement form. The sum of bits will be ?

- a. 6
- b. 5 ✔
- c. 8
- d. 2

Your answer is correct.

The correct answer is:
5

Question 20

Correct

Mark 3.00 out of 3.00

A 4-stage pipeline has stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be:

a. None of these

b. 590.0 microseconds

c. 169.5 microseconds

d. 165.5 microseconds ✔

Your answer is correct.

The correct answer is:
165.5 microseconds

Question 21

Correct

Mark 3.00 out of 3.00

A HDD has 1024 sectors per track, 5 platters, each with 2 recording surfaces and 500 cylinders. The address of the sector is given as (c,h,s), where c=cylinder number, h = surface number and s = sector number. First sector address is (0,0,0) then the address of the last sector in (c,s,h) format is ?

a. **(1023,9,499)**

b. **(1023,499,9)**

c. **(499,9,1023)** ✔

d. **(500,10,1024)**

Your answer is correct.

The correct answers are:
(499,9,1023),

(1023,499,9)

Question 22

Not answered

Marked out of 4.00

A computer system is an accumulation of various parameters and numbers. For example, CPU Frequency, RAM size etc. Each of these numbers affects the properties of the system. A higher CPU frequency means more instructions are executed every cycle. For each of the memory related parameters mentioned below describe one change in the overall system (it can be good or a bad change). Also clearly explain the reason for the change.

1. **Bigger Cache Block size.**
2. **High Cache Associativity.**
3. **Small Swap Area.**
4. **Smaller Virtual Page Table size.**
5. **Higher number of Physical pages.**

Question 23

Correct

Mark 2.00 out of 2.00

If a system has 5 processors and 6 processes, then what will be the maximum and minimum processes in the running state.

a. 36, 6

b. 5, 0 ✔

c. 5, 6

d. 25, 6

Your answer is correct.

The correct answer is:
5, 0

Question 24

Complete

Mark 0.00 out of 4.00

What does data hazard mean, explain with an example and explain briefly about the techniques used to avoid them?

Comment:

Question 25

Correct

Mark 1.00 out of 1.00

An interrupt in relation to the system clock is which type of interrupt?

a. Both

b. **Synchronous** ✔

c. None

d. **Asynchronous**

Your answer is correct.

The correct answer is:
Synchronous

Question 26

Complete

Mark 0.50 out of 4.00

```
1    0x000:  30f209000000 |        irmovl $9, %edx
2    0x006:  30f315000000 |        irmovl $21, %ebx
3    0x00c:  6123         |        subl %edx, %ebx
4    0x00e:  30f480000000 |        irmovl $128,%esp
5    0x014:  404364000000 |        rmmovl %esp, 100(%ebx)
6    0x01a:  a02f         |        pushl %edx
7    0x01c:  b00f         |        popl %eax
8    0x01e:  7328000000   |        je done
9    0x023:  8029000000   |        call proc
10   0x028:               | done:
11   0x028:  0            |        halt
12   0x029:               | proc:
13   0x029:  90           |        ret
```

Consider the irmovl instruction on line 4 of the attached code. For this instruction you have to create the Fetch,Decode, Execute, Memory, Write Back, PC Update Table.. This is similar to the Assignment 2 task 4.

fetch: icode:ifun <- M1[pc]

valP<-PC+1

decode: valA <- imm

execute: valE<-valA+0

Comment:

Question 27

Correct

Mark 1.00 out of 1.00

The result of the subtraction FD (base 16) - 88 (base 16) is in base 16 ?

- a. 10
- b. 75 ✔
- c. 65
- d. 5E

Your answer is correct.

The correct answer is:
75

Question 28

Correct

Mark 2.00 out of 2.00

A 2-level memory system has levels with access time T1 = 15 ns and T2 = 200 ns. The hit ratio for this system is 0.9. If the hit ratio is made to 1 what will be the new value of T1 ?

- a. 15 ns ✔
- b. 20 ns
- c. 25 ns
- d. 10 ns

Your answer is correct.

The correct answer is:
15 ns

Question 29

Correct

Mark 2.00 out of 2.00

Which function compiles into the given assembly code?

```
int fun1(int i, int j)
{
  if(i+3 != j)
   return i+3;
  else
   return j*16;
}

int fun2(int i, int j)
{
  if(i+3 != (unsigned)j)
   return i;
  else
   return j*4;
}

int fun3(int i, int j)
{
  if(i+3 <= (unsigned)j)
   return i;
  else
   return j>>2;
}
```

```
        pushl   %ebp
        movl    %esp, %ebp
        movl    8(%ebp), %eax
        movl    12(%ebp), %ecx
        leal    3(%eax), %edx
        cmpl    %ecx, %edx
        jne     .L4
        leal    0(,%ecx,4), %eax
.L4:
        popl    %ebp
        ret
```

- a. None
- b. fun3
- c. fun1
- d. fun2 ✔

Your answer is correct.

The correct answers are:
fun2,

fun3

Question 30

Correct

Mark 2.00 out of 2.00

What is the value of the condition code (CC) after the execution of line (1) and (2).

irmovq $10, %eax

xorq %esp, %esp (1)

pushq %eax

subq %eax, %eax (2)

a. **100, 101** ✔

b. **101, 101**

c. **101, 000**

d. **100, 000**

Your answer is correct.

The correct answers are:
100, 000,

100, 101