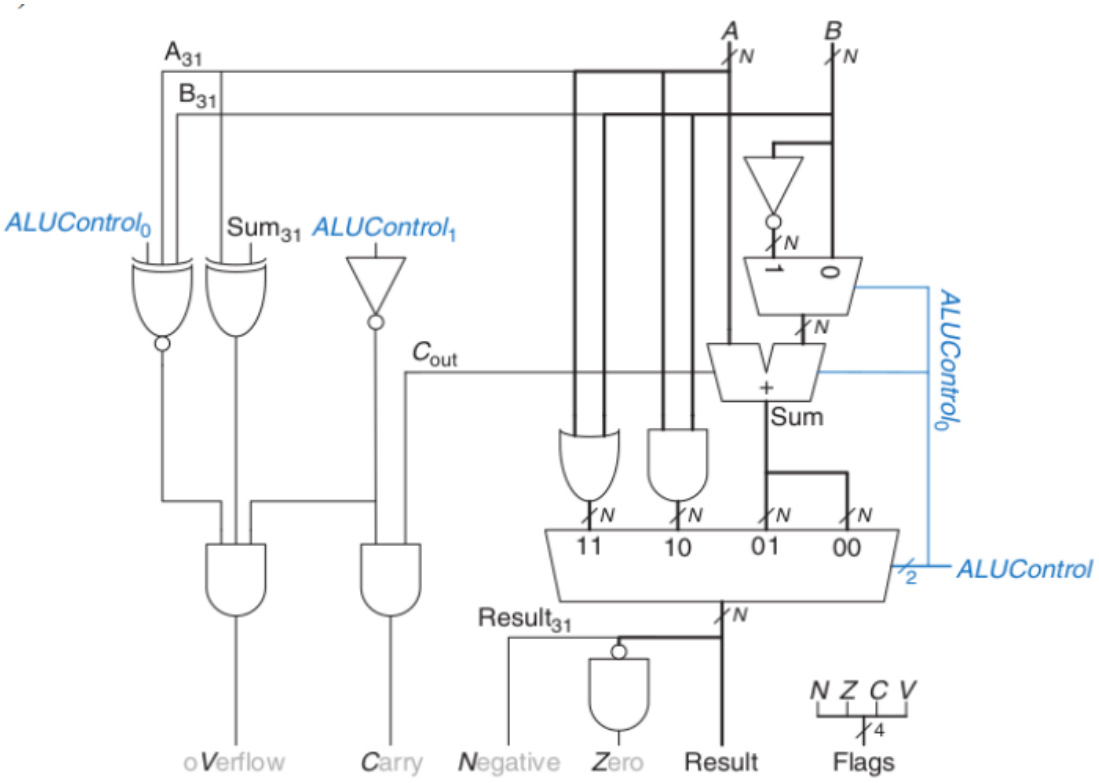
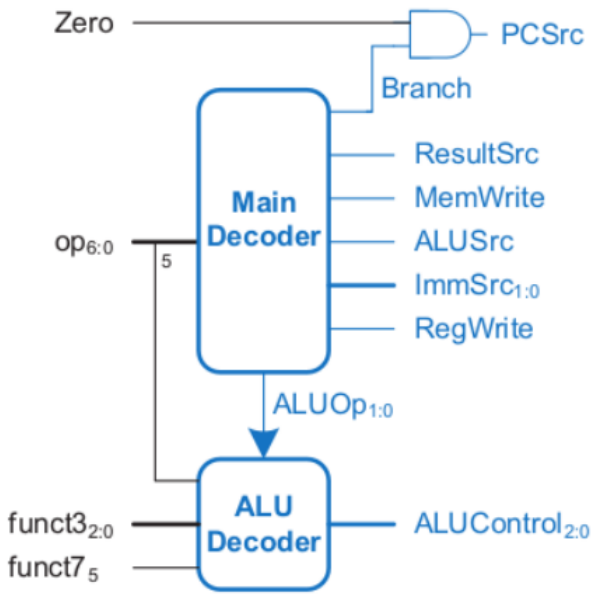
Architecture and other information regarding the model



ALU Design



Control Unit Block Diagram

Main Decoder

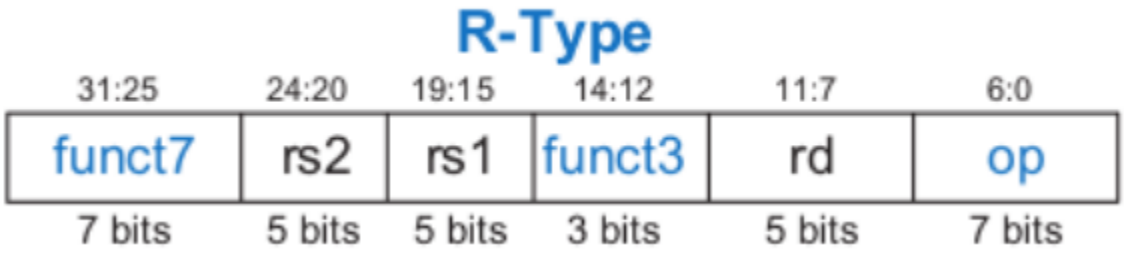
Instruction	Op	RegWrite	ImmSrc	ALUSrc	MemWrite	ResultSrc	Branch	ALUOp
lw	0000011	1	00	1	0	1	0	00
sw	0100011	0	01	1	1	x	0	00
R-type	0110011	1	xx	0	0	0	0	10
beq	1100011	0	10	0	0	x	1	01

ALU Decoder

ALUOp	funct3	{op[5],funct7[5]}	ALUControl	Instruction
00	x	x	000(add)	lw,sw
01	x	x	001(subtract)	beq
10	000	00,01,10	000(add)	add
	000	11	001(subtract)	sub

	010	x	101(set less than)	slt
	110	x	011(or)	or
	111	x	010(and)	and

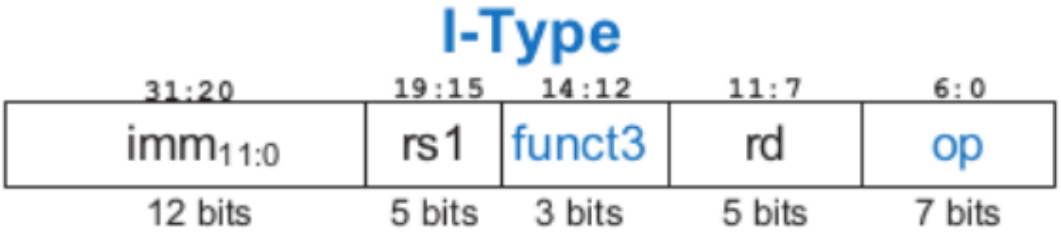
Instruction format of R type instructions



Example

Address	Instruction	Type	Fields						Machine Language	
			funct7	rs2	rs1	f3	rd	op		
0x1008	or x4, x5, x6	R	0000000	00110	00101	110	00100	0110011		0062E233

Instruction format of I type instructions



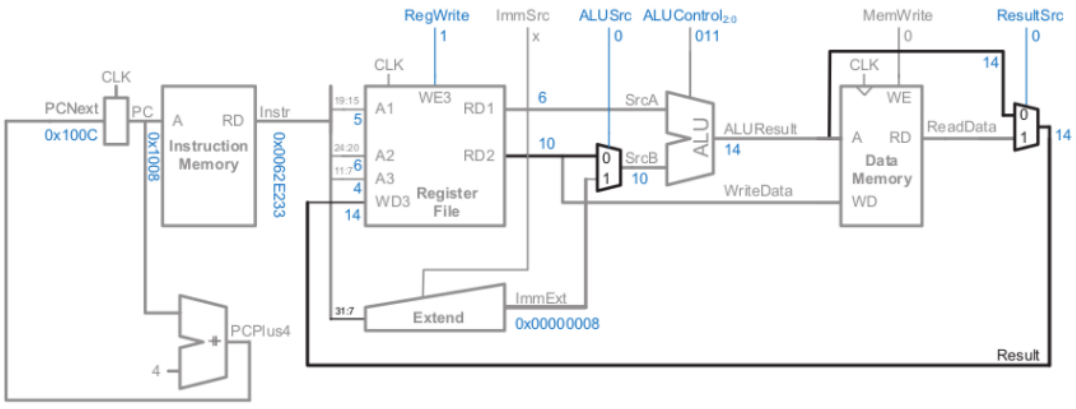
Example

Address	Instruction	Type	Fields					Machine Language
			$imm_{11:0}$	rs1	f3	rd	op	
0x1000	L7: lw x6, -4(x9)	I	111111111100	01001	010	00110	0000011	FFC4A303

Instruction format of S type instructions

Example

Address	Instruction	Type	Fields					Machine Language
			$imm_{11:5}$	rs2	rs1	f3	$imm_{4:0}$ op	
0x1004	sw x6, 8(x9)	S	0000000	00110	01001	010	01000 0100011	0064A423



Complete Architecture of RISC V Processor