ECE 3030: Physical Foundations of Computer Engineering
Fall 2021
Homework 6—Total points 100
Due on Thursday 11/11/2021 at 11.59am. In case of a late submission, you will be penalized by 50 points for each day after the submission deadline has passed. You will receive no score if you submit after the solution has been posted.

Q1 **MOSFET Structure:** What are the dimensions A and B called (see figure 1)? Circle the correct answer. [20 pts]

A= Channel/Gate length (L_G) or Channel Width (W)

B= Channel/Gate length (L_G) or Channel Width (W)

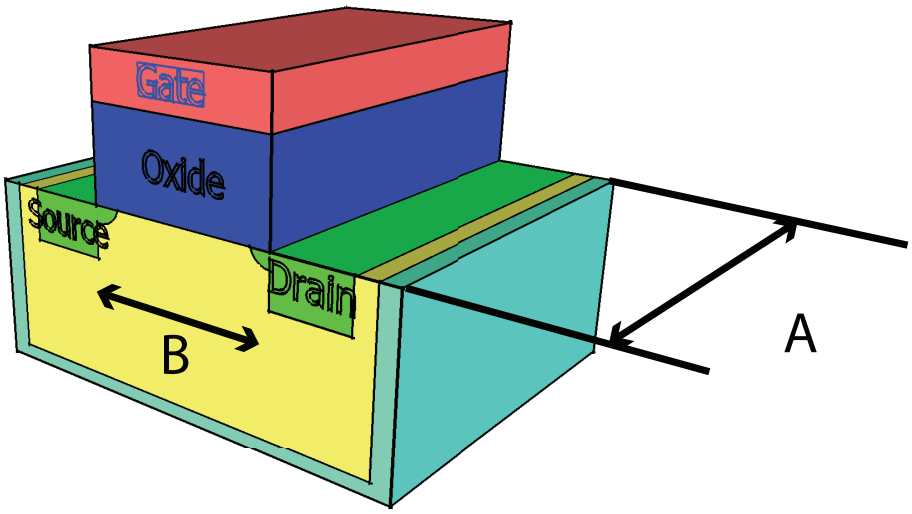

Figure 1: MOSFET structure.

Solution to Q1:

A= Channel Width (W)

B= Channel/Gate length (L_G)

Q2 Power in a microprocessor: Consider a microprocessor logic block that can operate at a maximum clock frequency (f) of 2 GHz and 2.5 GHz when

the power supply voltage (V_{DD}) is 1.2 V and 1.5 V, respectively.

Based on simplest possible assumptions, at which clock frequency will the block consume more power: 2 GHz or 2.5 GHz? Briefly explain your answer. [30 pts]

Solution to Q2:

$P = C_L V_{DD}^2 f_{clk}$

i.e $P \propto V_{DD}^2$ & $P \propto f_{clk}$

1st MOSFET : $V_{DD} = 1.2V$, $f = 2Hz$

2nd " : $V_{DD} = 1.5V$, $f = 2.5Hz$

$\frac{P_2}{P_1} = \frac{1.5^2 \times 2.5}{1.2^2 \times 2} \approx 1.05$

$\therefore P_2 > P_1$

$\therefore$ MOSFET with $V_{DD} = 1.5V$, $f = 2.5Hz$ consumes more power.

Q3 Consider an inverter operating a power supply voltage V_{DD}. Assume that $\mu_n/\mu_p = 3$ and $(W_p/L_p)/(W_n/L_n) = 3$. Make the necessary assumptions to get to an answer for the following questions. [50 pts]

[Q3.1] How will the delay and active power per device change as you increase V_{DD}? Explain with equations.

[Q3.2] How will the delay and active power per device change as you increase the doping density of both the N- and the P-MOSFET? Explain with equations.

Solution to Q2:

Delay $\tau = \frac{C_L V_{DD}}{I_{ON}}$. Active power per device $P_{active} = C_L V_{DD}^2 f$.

Q3.1: Frequency f is constant; $V_{DD} \uparrow$.
$I_{ON} \propto (V_{DD} - V_t)^2$
$V_{DD} \uparrow \Rightarrow \tau \propto \frac{V_{DD}}{(V_D D - V_t)^2} \downarrow$
$V_{DD} \uparrow \Rightarrow P_{active} = C_L V_{DD}^2 f \uparrow$

Q3.2: Frequency f is constant; Doping density$\uparrow$.
Doping density$\uparrow \Rightarrow V_t \uparrow \Rightarrow I_{ON} \propto (V_{DD} - V_t)^2 \downarrow \Rightarrow \tau \downarrow$
Doping density$\uparrow \Rightarrow P_{active} = C_L V_{DD}^2 f$ remains constant.

Q4: They should discuss the trade-off between channel length and MOSFET performance in some way. For example, they could mention a decrease in channel length leads to higher drain current so the MOSFET has higher conductivity.