ECE 3150

Final Exam
Total: 100 points

Name: _____

GTID: _____

1. Books and Class notes are not allowed. You can use 3 double-sided sheets of your own notes.
2. Use of calculators is allowed.
3. Cellphones and all other electronics should be put away.
4. Collaborating with classmates for the exam is NOT allowed.
5. Question 7 is for extra credit. You can receive a maximum score of 110.
6. All the work must be shown to receive credit. If you only write down the answer for any problem, you will not receive FULL credit.

Question Number	Maximum no. of points	Points Earned
1	20	
2	20	
3	15	
4	15	
5	15	
6	15	
7 (Extra Credit Question)	10	
TOTAL	100	

1. (20 points) An n-channel enhancement-mode MOSFET is used in the following circuit:
    - V_{DD}=8V
    - The drain is connected to V_{DD} through a 2kΩ resistor.
    - The source is grounded.
    - The gate is connected to a fixed voltage, V_G=4V.

    The MOSFET has the following parameters:

    - Threshold voltage V_{th}=2 V
    - μC_{OX}=100 μA/V^2
    - W/L=10

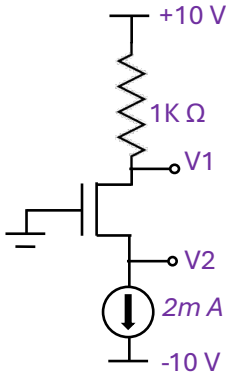
    (a) (5 points) Write the general expressions for I_D in both the saturation and triode regions for this NMOS.

    (b) (5 points) Calculate the drain current I_D assuming the MOSFET is in saturation.

    (c) (5 points) Compute V_{DS} using the circuit values.

    (d) (5 points) Verify if the MOSFET is actually in saturation or if it's in the linear region. If it's not in saturation, compute I_D again.

2. (a) In the circuit shown below, NMOS transistor has the following parameters: $b_n = \mu_n C_{OX}(W/L) = 1mA/V^2$; $V_{TN} = 2V$.

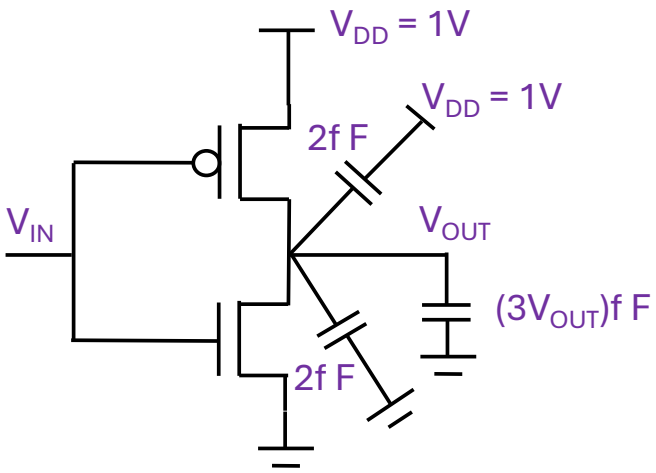


I. (8 points) Assuming that the transistor is in saturation determine V1 and V2.
II. (2 points) Now verify if the transistor is indeed in saturation.

(b) (10 points) Draw the stick diagram using the Euler path method for the following Boolean expression:

$$OUT = (a + b).c + d$$

3. (a) (10 points) Consider an inverter whose load capacitance is shown in the diagram below. Determine the (a) energy drawn from the supply (V_{DD} = 1V) as the input transitions from 1 to 0, (b) the stored energy on the capacitor and (c) the dissipated energy during charging.



(b) (3 points) Determine the dissipated energy by the inverter when the input transitions from 0 to 1.

(c) (2 points) What role do the resistances of the transistors play in the total switching energy?

4. Consider an inverter where the width of the NMOS and PMOS are W and αW respectively.

(a) (7 points) An engineer is analytically studying the relationship between the delay of the inverter and the parametric value, W. Express the delay in the following form.

$$T_{INV} = \frac{T_1}{W}$$

Write down an expression for T_1.

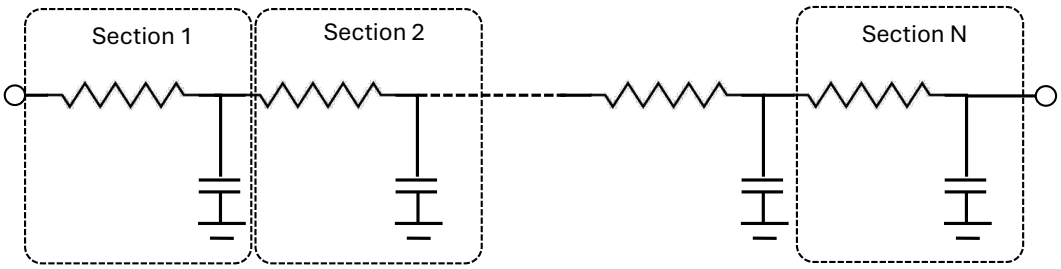
(b) (8 points) The area of the inverter also increases as W increases. However, there is a constant area overhead that arises from the metallic routing and the contacts. Assume that the area of the inverter can be expressed in the form:

$$A_{INV} = A_1.W + A_0$$

An important design criterion is the product of the delay and the area. Show, how you would choose the width of the NMOS, W to have the optimal Area X Delay.

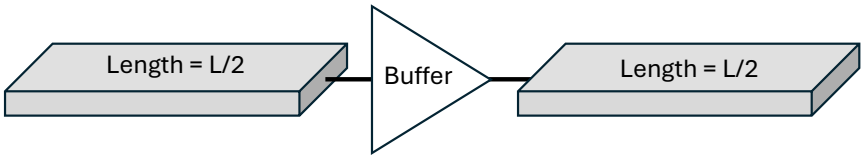
5. Consider a metallic interconnect of length, L where the resistance per unit length is R_S and the capacitance per unit length is C_S.

   (a) (5 points) Determine the total delay of the interconnect by dividing it into N smaller parts as shown in the picture below.



   (b) (5 points) Find an expression for the delay as N approached infinity.

   (c) (5 points) You have inserted a buffer at the center of the interconnect to minimize the total delay. Determine the maximum delay of the buffer that will enable you to have a lower delay compared to part (b).



6. A bit-slice of a 16b ripple carry adder has the following delay parameters: T_{carry} = 1.2ns and T_{sum} = 1.5ns where T_{carry} and T_{sum} are the delays to generate the output carry and the sum, respectively. The two operands are A and B. Consider the two scenarios:
   Scenario (1): A = 0x3333 and B=0xBBBB
   Scenario (2): A = 0xBBBB and B=0x00AA
   (7 points) Determine the delay of the adder in scenario (1).
   (8 points) Determine the delay of the adder in scenario (2).

   Hint: You can check the number of full-adder stages through which the carry propagates. As an example, the binary representation of the HEX number:
   0x4ACF is 0100 1010 1100 1111

7. (Extra Credit Question - 10points) Perform 9x11 using the shift-and-add method in the 4bit unsigned format. Fill up the following table.

Step (i)	Bi	A	Product Register State	Results