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Lab 03 Report
ECE 2031 L10
15 September 2024

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

-- Describes the device from the outside
entity RPS_VHDL is
-- Defines the signals coming into and out of the device
    port(
        R1, P1, S1  : in  std_logic;
        R2, P2, S2  : in  std_logic;
        W1, W2      : out std_logic;
             E1, E2      : out std_logic
    );
end RPS_VHDL;
-- Define the internal architecture of the device
architecture Internals of RPS_VHDL is
     -- Create a 6-bit vector -> gives us easy access to inputs
     signal all_inputs : std_logic_vector(5 downto 0);
begin
     -- "&" is CONCATENATION, not logical AND.
     all_inputs <= R1 & P1 & S1 & R2 & P2 & S2;
     -- Using a "selected signal assignment", aka "with/select"
     with all_inputs select W1 <=
          '1' when "100001",
          '1' when "010100",
          '1' when "001010",
          '0' when others;
     -- Using a "conditional signal assignment", aka "when/else"
     W2 <=
          '1' when all_inputs = "100010" else
          '1' when all_inputs = "001100" else
          '1' when all_inputs = "010001" else
          '0';
     -- Using when/else in a different way
     E1 <=
          '1' when (R1 = '1') and (S1 = '1') else
          '1' when (R1 = '1') and (P1 = '1') else
          '1' when (S1 = '1') and (P1 = '1') else
          '0';

     -- Using Boolean expression
     E2 <= (R2 and S2) or (R2 and P2) or (S2 and P2);
end Internals;
```

Figure 1. VHDL code to model a Rock-Paper-Scissor game between two players. “R1”, “S1”, “P1”, “R2”, “S2”, “P2” are inputs corresponding to rock, paper, and scissors for players one and two, respectively. Outputs “W1” & “W2” indicate which player wins. Outputs “E1” & “E2” indicate an invalid input combination for players one and two, respectively.

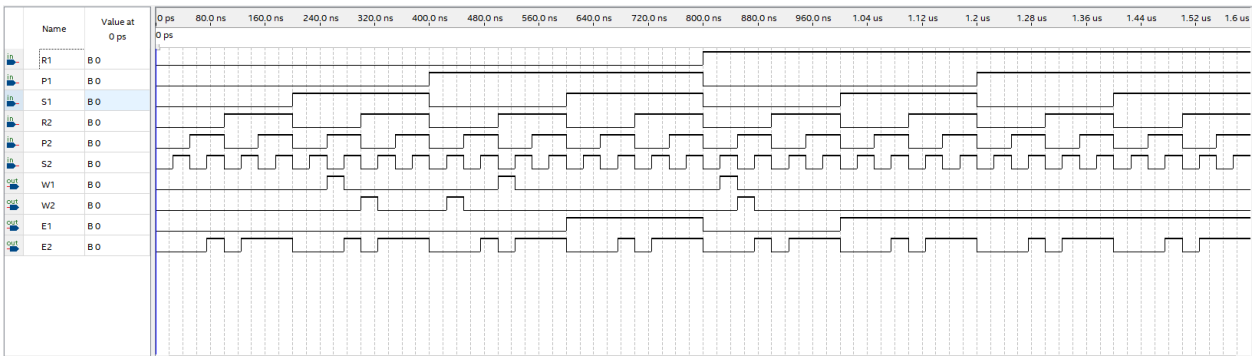

Figure 2. Waveform simulating all possible inputs for Rock-Paper-Scissor game between two players. “W1” goes high when player 1 wins & “W2” goes high when player 2 wins. “E1” and “E2” go high when players one or two put more than one of their dedicated inputs high.

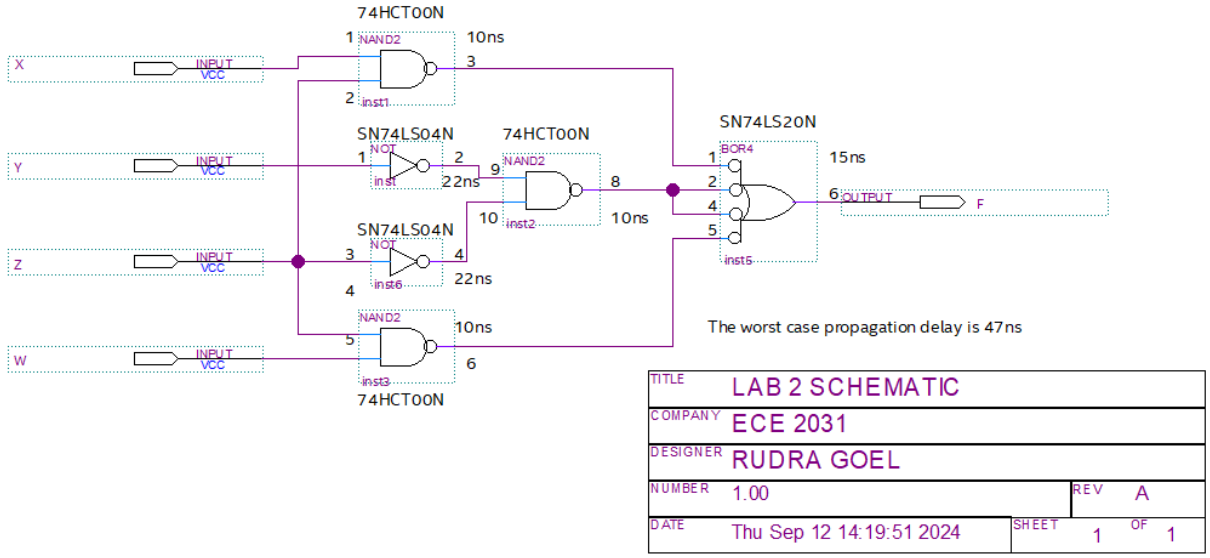

Figure 3. Schematic implementing $F = \overline{\overline{(\bar{Z} \cdot \bar{Y})} \cdot \overline{(X \cdot Z)} \cdot \overline{(W \cdot Z)}}$ with propagation delays for each gate. The greatest propagation delay is 47ns from input “Y” to output “F”.

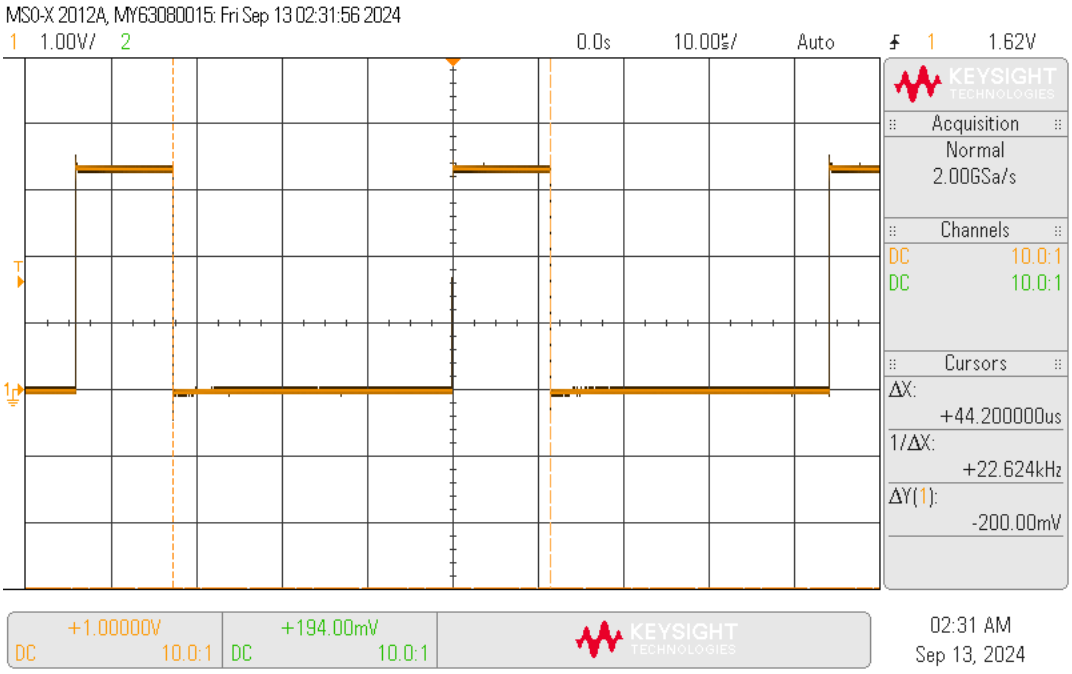

Figure 4. Square waveform of signal with period depending on equation: $\frac{mod(N,16)\cdot 4+455}{575\div 53}$ where $N = 6$. Vertical cursors at each falling edge to measure period of $44.2\mu s$.

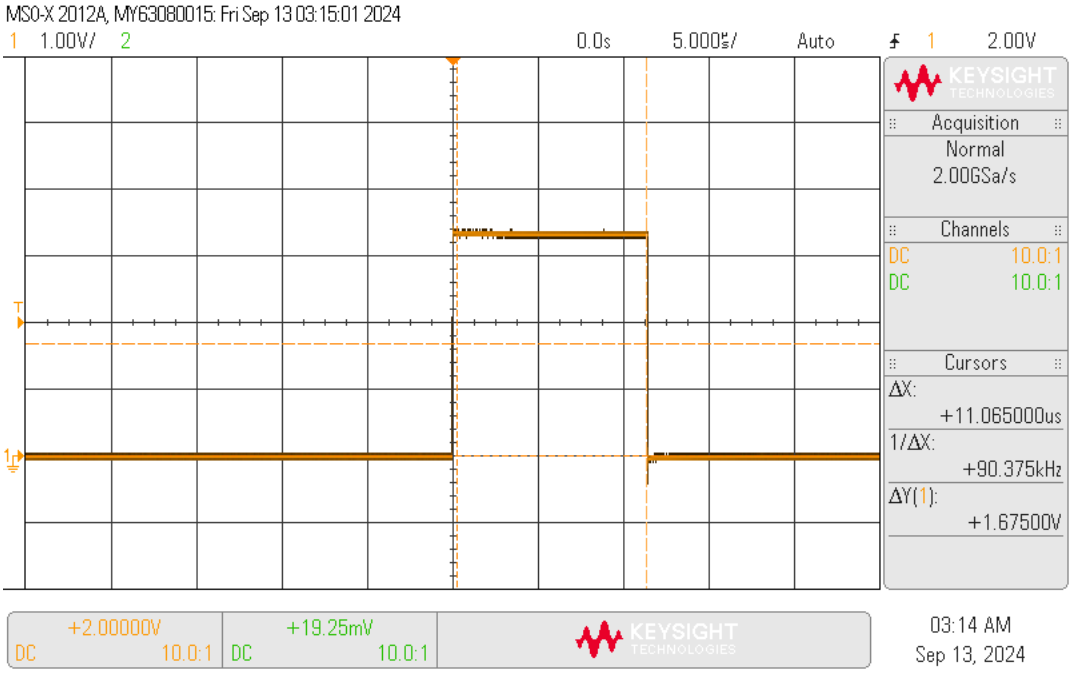

Figure 5. Oscilloscope capture of high time for square wave in Figure 2 meant to determine duty cycle. Vertical cursors measure high time to be $11.065\mu s$ thus indicating a 25% duty cycle.

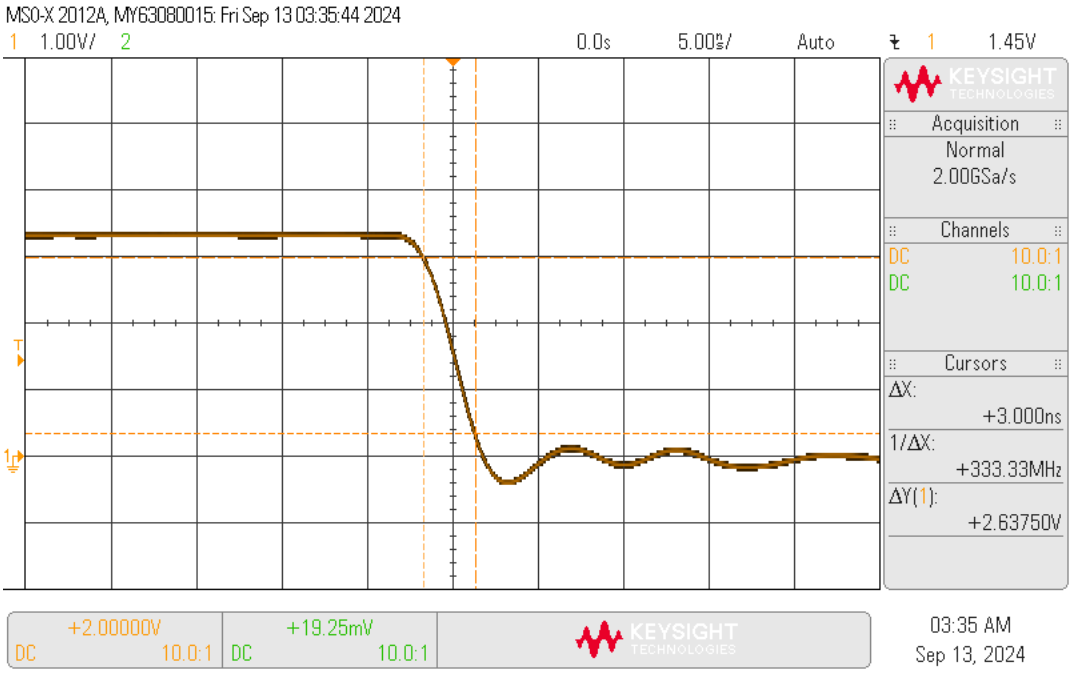

Figure 6. Capture of falling edge of signal to determine fall time. Vertical cursors at intersections of 90% of high voltage and 10% high voltage to measure 3ns fall time.

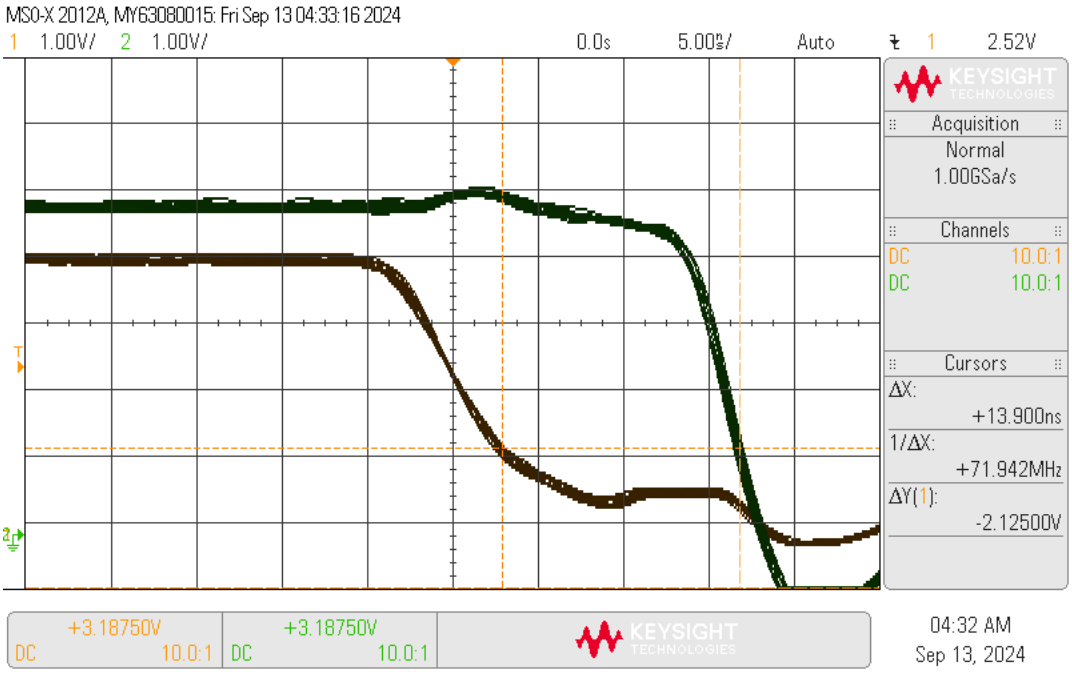

Figure 7. High-to-Low propagation delay for input signal (brown) to output signal (green) for two in-series inverters. Vertical cursor at signal intersecting 1.3V measuring 13.9ns high-to-low delay.

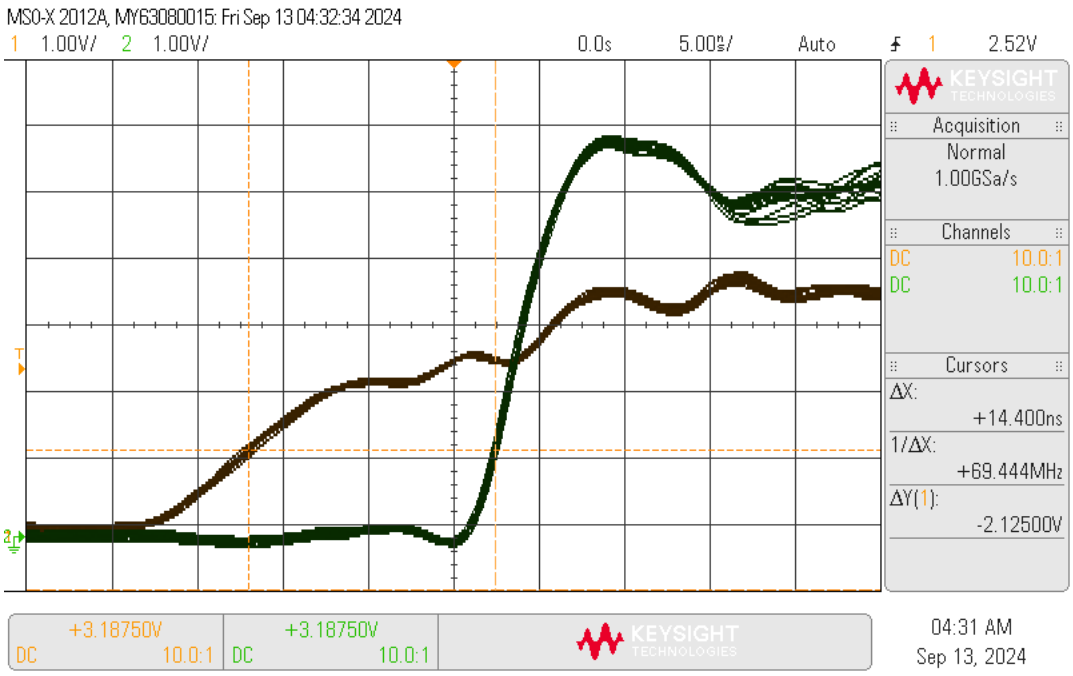

Figure 8. Low-to-High propagation delay for input signal (brown) to output signal (green) for two in-series inverters. Vertical cursor at signal intersecting 1.3V measuring 14.4ns low-to-high delay.