ECE 3150 Syllabus and Course Outline

ECE 3150: VLSI and Advanced Digital Design | Section A | Spring 2025

Class Times: Mondays and Wednesdays from 2:00 pm to 3:15 pm (VL E283)

Instructor:

Nivedita Bhattacharya nbhattacharya6@gatech.edu

Online OFFICE HOURS:

Thursdays from 1:30 PM to 2:30 PM (via Zoom)

Zoom Link: https://gatech.zoom.us/my/nivedita.b

[Other times can be arranged by email]

In-Person OFFICE HOURS:

Room: Van Leer 331W

Please schedule via email nbhattacharya6@gatech.edu

Graduate TAs: TBD

Undergraduate TAs: TBD

Course Description: ECE 3150 introduces advanced digital design issues in the context of VLSI systems. This will include an introduction to a design methodology that encompasses the range from architectural models to circuit simulation.

Course Objectives and Outcomes:

[1] Demonstrate a clear understanding of important concepts in CMOS technology and fabrication that affect design.
[2] Design a gate of any given arbitrary logic function at the transistor-level.
[3] Layout a gate in CMOS VLSI technology.
[4] Size the gates of the given VLSI layout to minimize the delay.

[5] Design a network of complex gates with the ideal number of stages that computes the function with minimum delay.
[6] Simulate a VLSI design in SPICE to obtain delay and power performance measures.
[7] Find a test vector to test given faults in a logic network.
[8] Design and characterize synchronized circuits for asynchronous external inputs.
[9] Design and layout a variety of adders and multipliers.
[10] Analyze and simulate interconnect delay.
[11] Design and layout a datapath that consists of various functional, memory, communication, and interface units.
[12] Understand system issues such as floorplanning and power/ground distribution

Prerequisites: ECE 2031 [min C] and ECE 2040 [min C]

Detailed Course Description and Topics: At the end of this file.

Textbooks:

[1] Wolf, Modern VLSI Design: IP-Based Design (4th edition), Prentice Hall, 2008. ISBN 0137145004, ISBN 978-0137145003 (required)
[2] Sutherland, Sproull & Harris, Logical Effort: Designing Fast CMOS Circuits, Morgan Kaufmann, 1999. ISBN 1558605576, ISBN 978-1558605572 (required)

Lectures: The course is scheduled to meet on Mondays and Wednesdays from 2:00 pm to 3:15 pm in VL E283. Attendance for the class is expected but not mandatory. However, students are encouraged to attend the class to be able to ask questions and participate in the discussions during the lectures. The Class videos will be posted on Canvas so that the students can review the lectures later.

Projects: The course will include projects that will require access to ECE's computing infrastructure using ECE's Lab or remotely using VPN or Virtual Labs. More instructions will be sent out via Canvas.

Class Organization:

1. The classes will meet at the given time in our assigned classroom.
2. The classes will be recorded and posted on Canvas.
3. All the exams will be in-person and in the class.

4. The class material is divided into **eight modules (Module 1 to Module 8)**. Module 9 is an extra reading Module that will not be covered in any of the exams. The modules are summarized in the "Detailed Course Syllabus" at the end of this document.
5. I will not record attendance in class. However, I expect that you will attend every class.
6. The withdrawal deadline is **March 13th, 2025**. We will have completed several homeworks and one midterm by that time, so you should have a good understanding of where you stand in the class. If you have any further questions, feel free to contact me via email.

Grading Policy:

1. Distribution of grades:
    a. Homeworks: 15%
    b. Projects: 25%
    c. Midterm 1: 20%
    d. Midterm 2: 20%
    e. Final Exam: 20%
2. The final grade will be curved. I will treat the highest grade as 100% and the other grades will be adjusted accordingly. The letter-grades will be as follows:
    a. A≥90.0% of the highest total score
    b. B≥80.0% of the highest total score
    c. C≥70.0% of the highest total score
    d. D≥60.0% of the highest total score
3. There will be partial credit in homeworks as well as in all exams. You will be penalized only once per mistake.
4. Grades will be recorded using Canvas. Contact me if anything on Canvas is incorrect.

Homework:

Homework is meant to both assess basic knowledge of the course material and to encourage deeper understanding, so it is likely that some additional research beyond coming to the class will be required. Homework is graded partially on completion and partially on correctness. There will be approximately **eight homeworks (one per module).**

Homework due dates will be announced on Canvas. No plagiarism and late submission will be tolerated.

All homeworks must be submitted via Canvas as a single PDF file.

Examinations:

1. All exams will be in-person and in the class.
2. There will be two midterm exams and a Final exam. Please see the course Canvas for the dates of the midterm exams.
3. Midterm 1 will be a problem-based exam with a format similar to the homeworks. **Please bring your laptops to the class.**
4. Midterm 2 will be a multiple-choice exam which you will need to complete on Canvas in the class. **Please bring your laptops to the class.**
5. The Final exam will also be a problem-based exam. You will have 2hr 50mins to complete it. **Please bring your laptops to the class.**
6. No collaboration or discussions will be allowed during the exams.
7. There will be review sessions before each exam.
8. There will be mock exams posted before the **MIDTERM EXAMS ONLY.**

Late Submission Policy:

Homework: If unexcused, no late submission will be allowed. Email me with excused delays to work out submission details, before the homework is due.

Examinations: If unexcused, no late submission will be allowed.

If you miss:

1. **Exam:** You will receive a score of 0 if you miss an exam without a valid excuse.
2. **Class:** Go through the class notes and videos provided and send me an email if you do not understand the material. You should try to come to one of the scheduled office hours. You can also schedule a separate time to meet me or the TA to clarify any doubts.

Accommodations for Students with Disabilities:

If you are a student with learning needs that require special accommodation, contact the Office of Disability Services at (404)894-2563 or http://disabilityservices.gatech.edu/, as soon as possible, to make an appointment to discuss your special needs and to obtain an accommodations letter. Please also e-mail me as soon as possible to set up a time to discuss your learning needs.

Academic Honesty:

At Georgia Tech we believe that it is important to strive for an atmosphere of mutual respect, acknowledgement, and responsibility between faculty members and the student body. See http://www.catalog.gatech.edu/rules/22/ for an articulation of some basic expectation that you can have of me and that I have of you. In the end, simple respect for knowledge, hard work, and cordial interactions will

help build the environment we seek. Therefore, I encourage you to remain committed to the ideals of Georgia Tech while in this class.

You may not:

- Collaborate at all during midterms and exams.
- Share solutions to any homework assignment before its due date.
- Discuss tests until they have been returned, in case someone has not taken it yet.
- Use or reference lab work from previous semesters.

You may:

- Work with instructors, tutors, TAs, and other students to discuss course material, including current homework and lab problems, as long as the solutions are not shared.

Communication

1. Announcements will be sent through Canvas. You are responsible for information sent in those announcements, so I recommend configuring Canvas for notifications.
2. If you need to contact me, I prefer that you send me an email (nbhattacharya6@gatech.edu) but it is also possible to message me through Canvas. The subject of the email needs to have ECE3150 in it.
3. If I need to contact you personally, I will use your GT email address.
4. We will use Ed discussion for this class. This is the preferred place to ask questions so that everyone in the class can see the answer (or answer themselves) and ask follow-up questions.

Important Dates: Important dates will be announced later via Canvas. Please see the announcement section on Canvas for details.

Detailed Course Modules:

1. **Basic CMOS Logic**
   a. Design of CMOS combinational logic
   b. Design of CMOS sequential logic
2. **Electrical Characteristics of MOSFETs**
   a. MOS I-V Characteristics and Regions of operation
   b. Capacitance of MOS devices
3. **DC Characteristics of CMOS gates**
   a. Voltage Transfer Characteristics (VTC) of inverter
   b. Regions of operation of CMOS inverter
4. **Layouts and Physical Design**
   a. Standard Cell Digital Design principles
   b. Euler paths and Euler Diagrams
5. **Delay of CMOS**
   a. Models of CMOS gate delay
   b. Dependence of gate delay on operating conditions
6. **Power Consumption of CMOS gates**
   a. Dynamic Power
   b. Short Circuit Power
   c. Leakage Power
   d. Total Power Model of CMOS logic
7. **Digital Arithmetic Circuits**
   a. Adders
   b. Multipliers
8. **Timing considerations in CMOS circuits**