

ECE 3150

Final Exam Total: 100 points

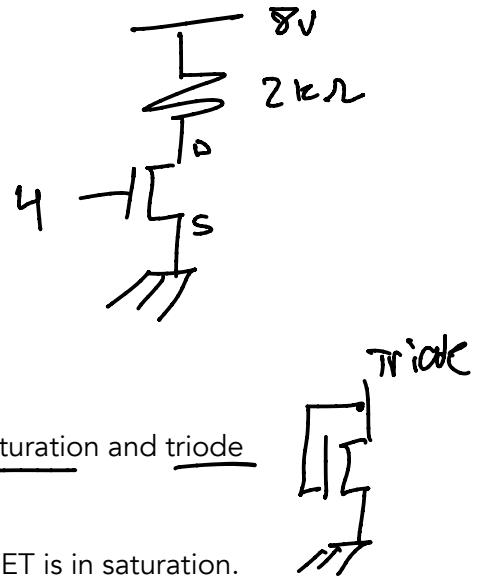
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1. Books and Class notes are not allowed. You can use 3 double-sided sheets of your own notes.
2. Use of calculators is allowed.
3. Cellphones and all other electronics should be put away.
4. Collaborating with classmates for the exam is NOT allowed.
5. Question 7 is for extra credit. You can receive a maximum score of 110.
6. **All the work must be shown to receive credit. If you only write down the answer for any problem, you will not receive FULL credit.**

Question Number	Maximum no. of points	Points Earned
1	20	
2	20	
3	15	
4	15	
5	15	
6	15	
7 (Extra Credit Question)	10	
TOTAL	100	

1. (20 points) An n-channel enhancement-mode MOSFET is used in the following circuit:

- $V_{DD}=8V$
- The drain is connected to V_{DD} through a $2k\Omega$ resistor.
- The source is grounded.
- The gate is connected to a fixed voltage, $V_G=4V$.



The MOSFET has the following parameters:

- Threshold voltage $V_{th}=2 V$ $v_t = 2 V$
- $\mu C_{ox}=100 \mu A/V^2$
- $W/L=10$ $B = \frac{\mu C_{ox}}{t_{ox}} V \frac{W}{2}$

(a) (5 points) Write the general expressions for I_D in both the saturation and triode regions for this NMOS.

(b) (5 points) Calculate the drain current I_D assuming the MOSFET is in saturation.

(c) (5 points) Compute V_{DS} using the circuit values.

(d) (5 points) Verify if the MOSFET is actually in saturation or if it's in the linear region. If it's not in saturation, compute I_D again.

$$I_D = \frac{B}{2} (V_{GS} - V_t)^2 \quad \text{where } B = \mu C_{ox} \frac{W}{2}$$

a) I_D in Saturation in triode $V_{GS} = V_{DS}$

$$I_D = \frac{B}{2} (V_{DS} - V_t)^2$$

b) $I_D = \frac{(100 \times 10)(10)}{2} (4 - 2)^2 = 100 \text{ mA}$

c) I_D on MOS $\Rightarrow I$ over $2k\Omega$ resistor

$$\frac{8 - V_D}{2k\Omega} = (2 \times 10) \quad 8 - V_D = 4 \quad \Rightarrow V_{DS} = 4 - 0$$

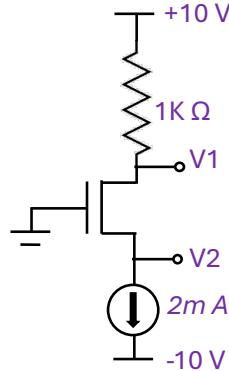
$$V_D = 4 V \quad \boxed{V_{DS} = 4 V}$$

D) Sat when $V_{DS} > V_{GS} - V_t$

$$4 >? 4 - 2 \quad 4 > 2$$

MOS tri Sat. Region

2. (a) In the circuit shown below, NMOS transistor has the following parameters: $b_n = \mu_n C_{OX}(W/L) = 1 \text{ mA/V}^2$; $V_{TN} = 2 \text{ V}$.



$$V_{G2} = 0$$

$$V_{GS} = V_2 - V_S = 0 - V_2 = -V_2$$

$$I_D = \frac{\beta}{2} (V_{GS} - V_T)^2$$

- I. (8 points) Assuming that the transistor is in saturation determine V_1 and V_2 .
 II. (2 points) Now verify if the transistor is indeed in saturation.

i) in Satn. $\Rightarrow I_D = \frac{\beta}{2} (V_{GS} - V_T)^2$, also $I_D = 2 \text{ mA}$ Same node

$$2e-3 = \frac{(1e-3)}{2} (-V_2 - 2)^2$$

$$\frac{4e-3}{1e-3} = \frac{(-V_2 - 2)^2}{2} \Rightarrow 2 = -V_2 - 2 \Rightarrow V_2 = -4 \text{ V}$$

$$(0 - V_1) = I_D R \Rightarrow 10 - V_1 = (2e-3)(1e-3) \Rightarrow 10 - V_1 \approx 2$$

$$V_1 = 8$$

ii) $V_{DS} \Rightarrow V_1 - V_2 = 8 - (-4) = 12 \text{ V}$

$$V_{DS} > ? \quad V_{GS} - V_{TN}$$

$$12 > ? - V_2 - 2$$

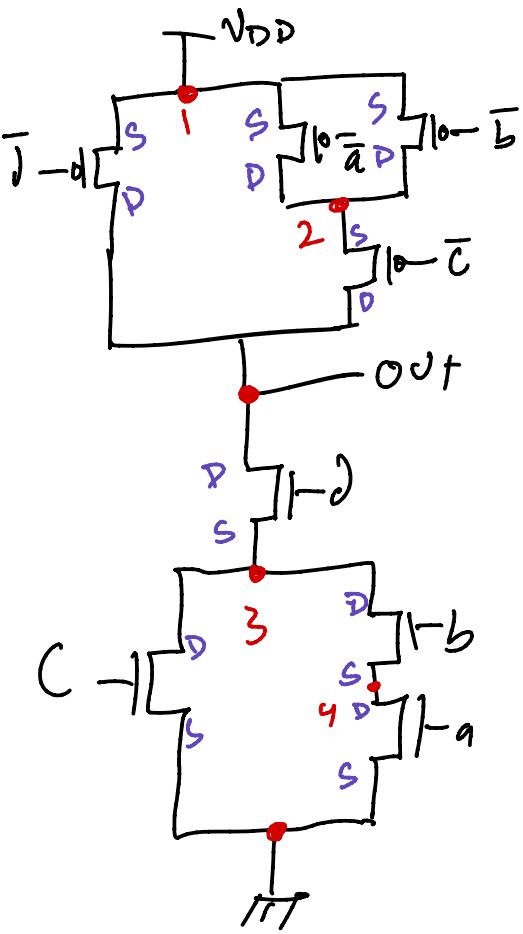
$$12 > 2 \rightarrow$$

in saturation

(b) (10 points) Draw the stick diagram using the Euler path method for the following Boolean expression:

PV: x w/ interface inputs

PD: PV^T PV

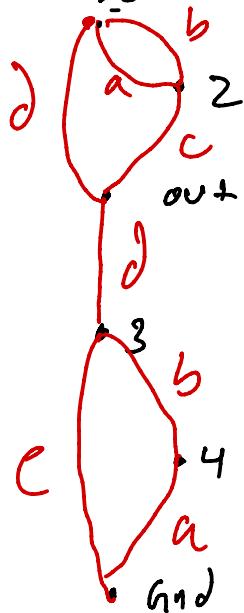


$$PDN = [a \bar{b} + \bar{c}]$$

$$OUT = (\bar{a} + \bar{b}) \cdot \bar{c} + \bar{d}$$

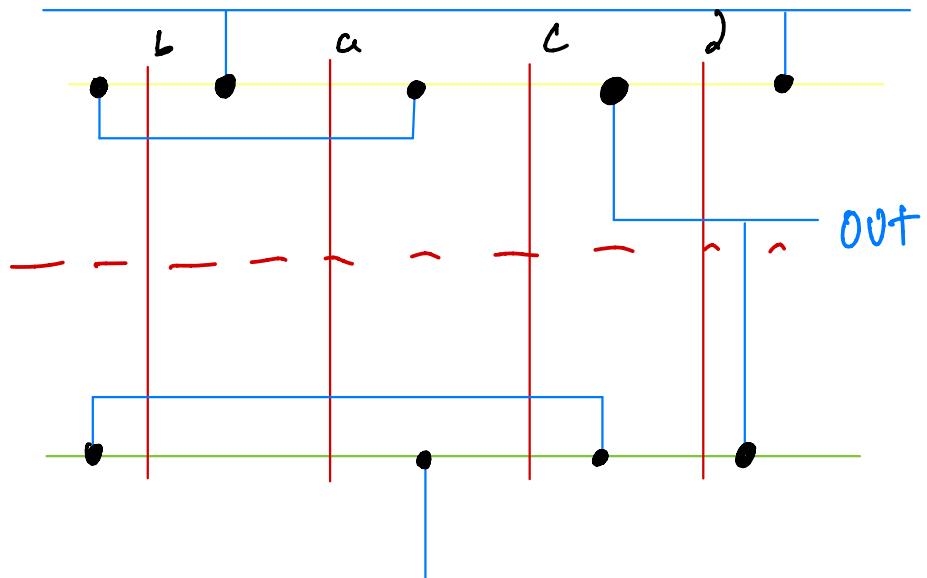
$$\text{Dual } (\bar{a}\bar{b} + \bar{c}) \bar{d}$$

VDD

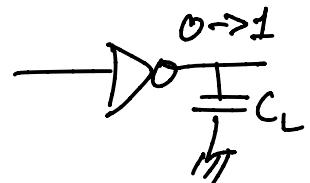
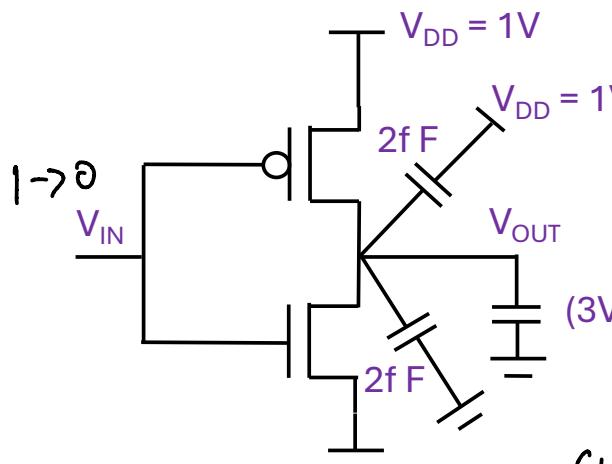
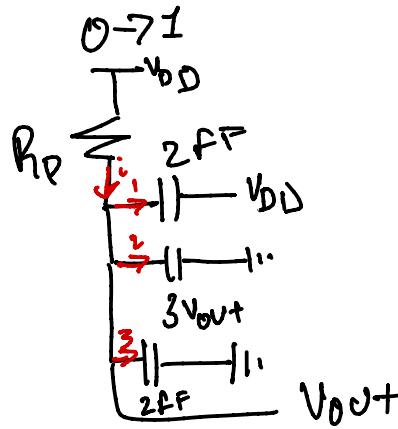


PV: {d, c, A, b}

PD: {d, c, a, -L}



3. (a) (10 points) Consider an inverter whose load capacitance is shown in the diagram below. Determine the (a) energy drawn from the supply ($V_{DD} = 1V$) as the input transitions from 1 to 0, (b) the stored energy on the capacitor and (c) the dissipated energy during charging.



$$C_L = 2fF + 2fF + 3V_{out}fF$$

$$a) E_{V_{DD}} = \int_0^\infty P(t) dt \Rightarrow P(t) = V_{DD} i(t); i(t) = \frac{d}{dt} Q = C_L V_{out}$$

$$i_{current}(t) = i_1 + i_2 + i_3 = [(V_0 - V_{DD})(2e^{-15}) + (3V_{out}e^{-15})(V_{out}) + (2e^{-15})(V_{out})] \frac{d}{dt}$$

$$i_c(t) = [2e^{-15}V_{out} - 2e^{-15}] \frac{d}{dt} + [(3e^{-15})(V_{out}^2)] \frac{1}{t} + [(2e^{-15})(V_{out})] \frac{d}{dt}$$

$$2(2e^{-15}) \frac{dV_{out}}{dt} + (3e^{-15}) V_{out}^2 \frac{dV_{out}}{dt} = i_c(t) \Rightarrow P = (4e^{-15} + 3e^{-15}V_{out}^2)V_{DD} \frac{dV_{out}}{dt}$$

$$\int_0^\infty P(t) dt \Rightarrow \int_0^\infty 4e^{-15}V_{DD} \frac{dV_{out}}{dt} dt + \int_0^\infty 3e^{-15}V_{out}^2 V_{DD} \frac{dV_{out}}{dt} dt$$

$$4e^{-15}V_{DD} (V_{DD}) + \frac{3e^{-15}V_{DD}}{3} \left[V_{out}^3 \right]_0^{V_{DD}} = 4e^{-15} + 1e^{-15} = \boxed{5e^{-15} J}$$

$$b) E_{cap} = \int P_{cap} dt \Rightarrow P_{cap}(t) = V_{out} i_c(t) = [4e^{-15}V_{out} + 3e^{-15}V_{out}^3] \frac{dV_{out}}{dt}$$

$$\int 4e^{-15}V_{out} dV_{out} + \int 3e^{-15}V_{out}^3 dV_{out}$$

$$\left[\frac{4e^{-15}V_{out}^2}{2} \right]_0^{V_{DD}} + \left[\frac{3e^{-15}V_{out}^4}{4} \right]_0^{V_{DD}} \Rightarrow 2e^{-15} + \frac{3}{4}e^{-15} J$$

$$= \boxed{2.75 fJ} \text{ on } C_{AP}$$

c) conservation of energy

$$\Rightarrow E_{\text{SUPP}} - E_{\text{CP-}} = E_{\text{DISS.}}$$

$$5e^{-15J} - 2.75e^{-15J} = \boxed{2.25e^{-15J}}$$

(b) (3 points) Determine the dissipated energy by the inverter when the input transitions from 0 to 1.

input 0 \rightarrow 1 \Rightarrow op 1 \rightarrow 0

Charge on Cap Dissipated

$$E = 2.75 \times 10^{-15} J$$

(c) (2 points) What role do the resistances of the transistors play in the total switching energy?

The Resistances are circuit elements
that dissipate energy during the switching
process as thermal energy. The charge
on capacitors (load and parasitic) flow thru
these resistances and release as heat.

$$W_P = \alpha W$$

$\overbrace{+}^{\text{NMOS}}$

$$V_n = \omega$$

4. Consider an inverter where the width of the NMOS and PMOS are W and αW respectively.

- (a) (7 points) An engineer is analytically studying the relationship between the delay of the inverter and the parametric value, W . Express the delay in the following form.

$$T_{INV} = \frac{T_1}{W}$$

Write down an expression for T_1 .

- (b) (8 points) The area of the inverter also increases as W increases. However, there is a constant area overhead that arises from the metallic routing and the contacts. Assume that the area of the inverter can be expressed in the form:

$$A_{INV} T_{INV} = A_1 T_1 + \frac{A_0 T_1}{W}$$

An important design criterion is the product of the delay and the area. Show, how you would choose the width of the NMOS, W to have the optimal Area X Delay.

a) We can use the CV/I model to derive Delay

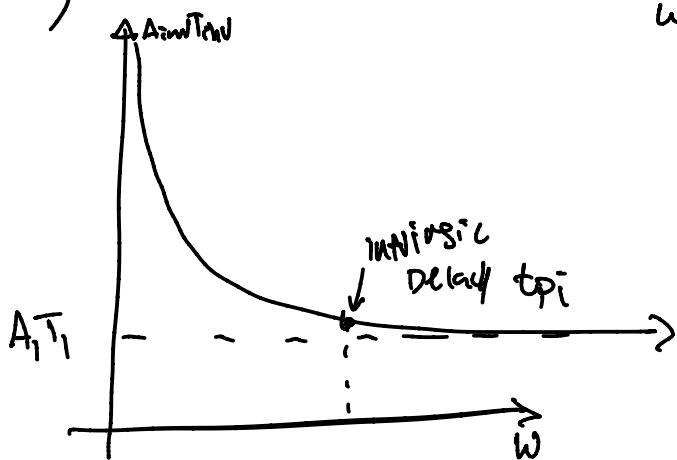
$$T_1 = \frac{C_{out}}{2V_{DD}} \left(\frac{1}{\alpha\beta} + \frac{1}{\beta} \right)$$

where C_{out} is the total capacitance of the load on the inverter and its parasitic elements, V_{DD} is supply

Beta (β) is the beta factor of each MOS device

$$\text{in the inverter, } \beta = \frac{C_{ox} N}{L}$$

$$B) A_{INV} T_{INV} = A_1 T_1 + \frac{A_0 T_1}{W} \rightarrow A_1 T_1 + \frac{A_0 T_1}{W} = \boxed{w A_1 T_1 + A_0 T_1}$$



$$\frac{d}{dW} \left[w^2 A_1 T_1 + w (A_0 T_1 - A_1 T_1) - A_0 T_1 \right]$$

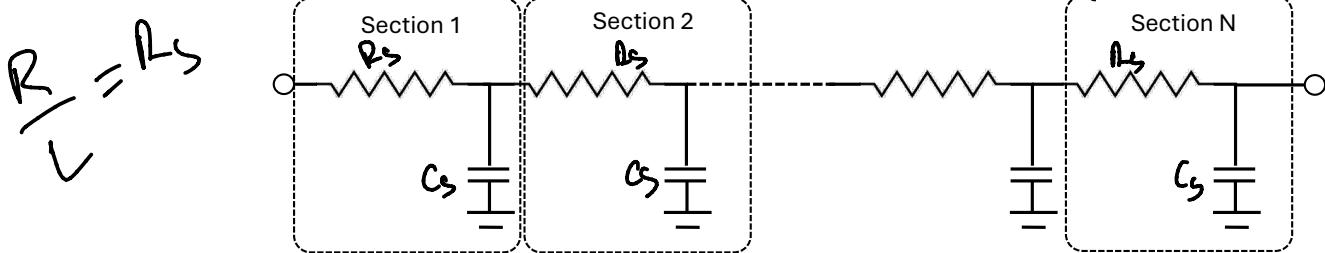
$$2w A_1 T_1 + A_0 T_1 - A_1 T_1 = 0$$

$$w = \frac{A_1 T_1 - A_0 T_1}{2 A_1 T_1} = \boxed{\frac{A_1 - A_0}{2 A_1}}$$

$$\frac{n(n-1)}{2}$$

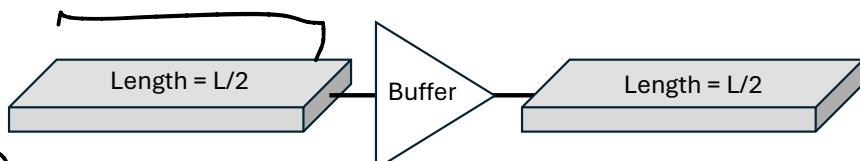
5. Consider a metallic interconnect of length L where the resistance per unit length is R_s and the capacitance per unit length is C_s .

- (a) (5 points) Determine the total delay of the interconnect by dividing it into N smaller parts as shown in the picture below.



- (b) (5 points) Find an expression for the delay as N approached infinity.

- (c) (5 points) You have inserted a buffer at the center of the interconnect to minimize the total delay. Determine the maximum delay of the buffer that will enable you to have a lower delay compared to part (b).



$$a) t_1 = \frac{R_s}{n} (C_s n) \quad t_2 = \frac{R_s}{n} (C_s (n-1)) \quad t_3 = \frac{R_s}{n} (C_s (n-2)) \dots$$

$$T = \sum_i^n t_i \Rightarrow \frac{R_s C_s}{n} \left(\frac{n(n+1)}{2} \right) = \boxed{\frac{R_s C_s}{2} (N+1)}$$

$$b) \lim_{N \rightarrow \infty} T = \frac{R_s C_s}{2} \left(\frac{n^2 + n}{n} \right) \text{ as } n \rightarrow \infty \Rightarrow \frac{R_s C_s}{2} (1 + \frac{1}{n}) \text{ or } \boxed{\frac{R_s C_s}{2}}$$

$$c) \frac{R_s C_s}{2} \left(\frac{2(2+1)}{2} \right) = 1.5 R_s C_s$$

$\therefore 2.5 R_s C_s$

6. A bit-slice of a 16b ripple carry adder has the following delay parameters: $T_{carry} = 1.2\text{ns}$ and $T_{sum} = 1.5\text{ns}$ where T_{carry} and T_{sum} are the delays to generate the output carry and the sum, respectively. The two operands are A and B. Consider the two scenarios:

Scenario (1): A = 0x3333 and B=0xBBB

$$(3)_{16} = (0011)$$

Scenario (2): A = 0xB BBB and B=0x00AA

1011

(7 points) Determine the delay of the adder in scenario (1).

(8 points) Determine the delay of the adder in scenario (2).

Hint: You can check the number of full-adder stages through which the carry propagates. As an example, the binary representation of the HEX number:

0x4ACF is 0100 1010 1100 1111

Scenario 1

$$\begin{array}{r}
 & 1 & 1 & 1 & 1 \\
 & 0011 & 0011 & 0011 & 0011 \\
 1011 & 1011 & 1011 & 1011 \\
 \hline
 1110 & 1110 & 1110 & 1110 \\
 \hline
 & 1 & 1 & 1 & 1
 \end{array}$$

8 Carry generation

$$8(1.2) + (1.5)$$

$$9.6 + 1.5 = \boxed{11.1 \text{ ns}}$$

Scenario 2:

$$\begin{array}{r}
 & 1 & 1 & 1 & 1 \\
 & 1011 & 1011 & 1011 & 1011 \\
 0000 & 0000 & 0010 & 1010 \\
 \hline
 1100 & 0111 & 0110 & 1011
 \end{array}$$

7 CARRY generation

$$\boxed{10 \times 5}$$

$$\begin{array}{r} 1011 \\ \times 1001 \\ \hline \end{array}$$

7. (Extra Credit Question - 10points) Perform 9×11 using the shift-and-add method in the 4bit unsigned format. Fill up the following table.

Step (i)	Bi	A	Product Register State	Results
0	1	1011	1011	1011
1	0	1011	0000	$\begin{array}{r} 1011 \\ 0000 \\ \hline 01011 \end{array}$
2	0	1011	0000	$\begin{array}{r} 01011 \\ 0000 \\ \hline 001011 \end{array}$
3	1	1011	1011	$\begin{array}{r} 001011 \\ 1011 \\ \hline 1100011 \end{array}$