

Q1 The square law model with correction for subthreshold current relating the drain current  $I_D$ , the drain voltage  $V_D$  and the gate voltage  $V_G$  in a long-channel MOSFET is as follows.

$$I_D = \begin{cases} W I_{sub-V_t} e^{\frac{q(V_G - V_t)}{mkT}} (1 - e^{\frac{-qV_D}{kT}}); & \text{when } V_G < V_t \text{ (sub-threshold)} \\ I_{sub-V_t} (1 - e^{\frac{-qV_D}{kT}}) + \mu C_{ox} \frac{1}{L} ((V_G - V_t)V_D - \frac{1}{2}V_D^2); & \text{when } V_G - V_t > V_D \text{ (linear)} \\ I_{sub-V_t} (1 - e^{\frac{-qV_D}{kT}}) + \mu C_{ox} \frac{1}{2L} (V_G - V_t)^2; & \text{when } V_G - V_t < V_D \text{ (saturation)} \end{cases}$$

We have also defined the on-current  $I_{ON}$  and the off-current  $I_{OFF}$  as follows.

$$\begin{aligned} I_{ON} &= I_D(V_G = V_D = V_{DD}) \\ I_{OFF} &= I_D(V_G = 0, V_D = V_{DD}) \end{aligned}$$

Here,  $V_{DD}$  is the power supply voltage, and  $qV_{DD} \gg kT$ .

Q1.1 Based on these relations, find expressions for  $I_{ON}$  and  $I_{OFF}$  in terms of  $V_{DD}$ ,  $V_t$ ,  $I_{sub-V_t}$ ,  $\mu$ ,  $C_{ox}$ ,  $W$  and  $L$ . Note that when  $V_G = V_D = V_{DD}$ , the MOSFET operates in the saturation region. [25 pts]

Q1.2 Based on the derived expressions, find how  $I_{ON}$  and  $I_{OFF}$  would change if  $V_t$  is increased. [25 pts]

1.1)  $I_{on} \Rightarrow V_g = V_D \Rightarrow V_g - V_t < V_t \Rightarrow$  Saturation Regn

$$I_D = \left[ I_{sub-V_t} (1 - e^{-2V_D/kT}) + \frac{\mu C_{ox}}{2L} (V_g - V_t)^2 \right] W$$

$$I_{on} = I_D \cdot V_{DD} \Rightarrow I_{on} = \left[ I_{sub-V_t} (1 - e^{-2V_D/kT}) + \frac{\mu C_{ox}}{2L} (V_g - V_t)^2 \right] W$$

$I_{off} \Rightarrow V_g = 0 < V_t \Rightarrow$  Subthreshold w/c

$$I_{off} = \left( I_{sub-V_t} \cdot e^{(V_g - V_t)/MkT} \left[ 1 - e^{-2V_D/kT} \right] \right) W \quad M = V_s/V_g$$

$$I_{off} = W I_{sub-V_t} \cdot e^{\frac{V_g - V_t}{MkT}} \left[ 1 - e^{-2V_D/kT} \right] W \quad \text{But } V_g = 0$$

$$I_{off} = W I_{sub-V_t} \cdot W \left[ 1 - e^{-2V_D/kT} \right] \quad \text{But } V_D \gg kT \Rightarrow \exp \rightarrow 0$$

$$I_{off} = W I_{sub-V_t}$$

1.2) If  $V_g$  were increased  $I_{off}$  and  $I_{on}$  would decrease

$$V_g = 3V \quad V_D = 2V$$

$$2.2.1) \quad V_g > V_t$$

2.  $V_G = 0.2 \text{ V}, V_D = 1 \text{ V}.$

$$3 - V_t \Rightarrow 3 - .3862 \text{ V}$$

3.  $V_G = 2.2 \text{ V}, V_D = 2 \text{ V}.$

$$= 2.6138 > V_D \Rightarrow$$

4.  $V_G = 2 \text{ V}, V_D = 1 \text{ V}.$

Saturation

5.  $V_G = 0.5 \text{ V}, V_D = 0.5 \text{ V}.$

$$I_D = \frac{W}{L} N_n C_{ox} \left[ (V_g - V_t) V_D - \frac{1}{2} V_D^2 \right]$$

6.  $V_G = 1.5 \text{ V}, V_D = 2 \text{ V}.$

$$(230e-4)(4.43e-3) [ (2.6138)(2) - 2 ]$$

$$= \boxed{1.972 \text{ mA}}$$

2.2.2)  $V_g < V_t \Rightarrow$  cut-off region,  $I_D = 0$  (cut-off)

2.2.3)  $V_g > V_t \Rightarrow V_g - V_t = 2.2 - .3862 = 1.81 < V_D \rightarrow$  saturation

$$I_D = \frac{W C_{ox} \omega}{2L} (V_g - V_t)^2 \Rightarrow \frac{6.11e-4}{2} (.1.81)^2 = \boxed{1.025 \text{ mA}}$$

2.2.4)  $V_g > V_t \Rightarrow V_g - V_t = 2 - .386 = 1.614 > V_D \rightarrow$  linear

$$I_D = \frac{W N_n C_{ox}}{L} \left[ (1.614)(1) - \frac{1}{2} \right] = \boxed{1.7502 \text{ mA}}$$

2.2.5)  $V_g > V_t \Rightarrow V_g - V_t = \frac{1}{2} - .386 = .11384 < V_D \rightarrow$  saturation

$$I_D = \frac{W n C_{ox} \omega}{2L} (.11384)^2 = \boxed{3.9588 \text{ mA}}$$

2.2.6)  $V_g > V_t \Rightarrow 1.5 - .386 = 1.11384 < V_D \rightarrow$  saturation

$$I_D = \frac{W n C_{ox} \omega}{2L} (1.11384)^2 = \boxed{.379 \text{ mA}}$$

**Q3 Power in a microprocessor:** Consider a microprocessor logic block that can operate at a maximum clock frequency ( $f$ ) of 2 GHz and 2.5 GHz when the power supply voltage ( $V_{DD}$ ) is 1.2 V and 1.5 V, respectively.

Based on simplest possible assumptions, at which clock frequency will the block consume more power: 2 GHz or 2.5 GHz? Briefly explain your answer. [50 pts]

$$f_{max} = 2 \text{ GHz} @ V_{DD} = 1.2 \text{ V}$$

$$f_{max} = 2.5 \text{ GHz} @ V_{DD} = 1.5 \text{ V}$$

When operating @  $V_{DD} = 1.5 \text{ V}$ . and consequently 2.5 GHz, the processor will be switching the MOS devices at a faster rate ( $1.25 \times$  Speedup). When switching these MOS devices at a fast rate, the capacitor formed @ the Gate metal, Poly silicon, and Body is constantly charged and discharged consuming more power over time.

Q4 Consider an inverter operating at a power supply voltage  $V_{DD}$ . Make the necessary assumptions to answer the following questions. [50 pts]

[Q4.1] How will the delay and active power per device change as you increase  $V_{DD}$ ? Explain with equations.

[Q4.2] How will the delay and active power per device change as you increase the doping density of both the N- and the P-MOSFET? Explain with equations.

4.1) Given that active Power  $P_{active} = C_L V_{DD}^2 f$   
 $\Rightarrow P_{active} \propto V_{DD}^2 \Rightarrow$  increasing  $V_{DD}$  will increase active power

$$\gamma = \frac{C_L V_{DD}}{I_{on}} \quad I_{on} = \frac{V_n C_{ox} \omega}{2L} \left[ V_g - V_t \right]^2$$

assuming  
device in  
saturation  
 $\Rightarrow V_g = V_{DD}$

$$\text{if } V_{DD} \uparrow \Rightarrow \gamma = \frac{V_{DD}}{(V_{DD} - V_t)^2} \Rightarrow \boxed{\gamma \downarrow}$$

4.2) Doping Density would increase implying  $V_t$  would

also increase dramatically  $\Rightarrow I_{on} \propto (V_g - V_t)^2 \Rightarrow I_{on} \downarrow$

$$\gamma = \frac{C_L V_{DD}}{I_{on}} \quad \text{if } I_{on} \downarrow \Rightarrow \boxed{\gamma \uparrow}$$

for Power,  $f V_{DD}^2 C_L \Rightarrow \frac{V_{DD}^2 C_L}{\gamma} \text{ if } \gamma \uparrow \Rightarrow \boxed{P_{active} \downarrow}$