Q1 According to the scaling model proposed by Dennard *et al.*, in every subsequent generation, all three physical dimensions (W, L, t_{ox}), the power supply voltage V_{DD} and the threshold voltage, V_t are downscaled by factor of x ($x > 1$). Show that in this scenario, the clock frequency can be increased by a factor of x while keeping the chip power density (in W/cm^2) keeping the same. [25 pts]

The Chip Power Density is a function of Area A. The # of transistors N for generation n (N_n) is $N_n = \frac{A}{W_n L_n}$

for $N_{n+1} = \frac{A}{(W/x)(L/x)} \Rightarrow N_n x^2$

The Delay $\tau_n = \frac{C L_n V_{DDn}}{I_{on,n}}$ Scaled By x

as $I_{on(n+1)} = \frac{I_{on,n}}{x}$ and $L_{n+1} = \frac{L_n}{x} \Rightarrow t_{n+1} = \frac{t_n}{x}$

$f_n = \frac{1}{\tau_n}$ & $f_{n+1} = \frac{1}{t_{n+1}} = \frac{1}{t_n/x} = \frac{x}{t_n} = f_n x$

if we see that the Chip Power, $n = C L_n V_{DD}^2 f_n$

* Scaling f_{n+1} By x Keeps the Power Density constant.

$P_{n+1} = C \frac{L_n}{x} \frac{V_{DD}^2}{x^2} f_n x$

$P_{n+1} = P_n / x^2$

$\Rightarrow P_{Chip\,n+1} = N_{n+1} P_{n+1}$

$P_{Chip\,n+1} = N_n x^2 \frac{P_n}{x^2}$

Q2 In the scenario where, in each subsequent generation, you could downscale only the three physical dimensions (W, L, t_{ox}) by a factor of x but had to keep V_{DD} and V_t fixed, how would you have changed the clock frequency? [25 pts]

Because the # of transistors is dependent on Area and Physical Dimensions W L t_{ox} $\Rightarrow$ # of transistors scales by x^2 still.

Capacitance also scales by $1/x$

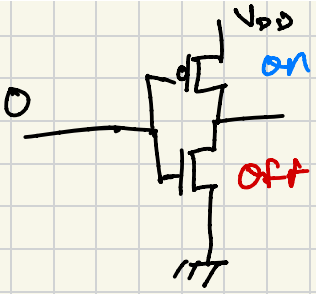
$$P_{n+1} = \frac{C L_n}{x} V_{DD}^2 f_{n+1} = \left(\frac{P_n f_{n+1}}{f_n x}\right) N_n x^2$$

if Chip Power is constant $\Rightarrow$ $x \frac{f_{n+1}}{f_n} = 1 \Rightarrow$

$$\boxed{f_{n+1} = \frac{f_n}{x}}$$

Q3 Consider an inverter with its input voltage $V_{in} = 0$. Why would the inverter dissipate power even in this case? [15 pts]

Leakage current !

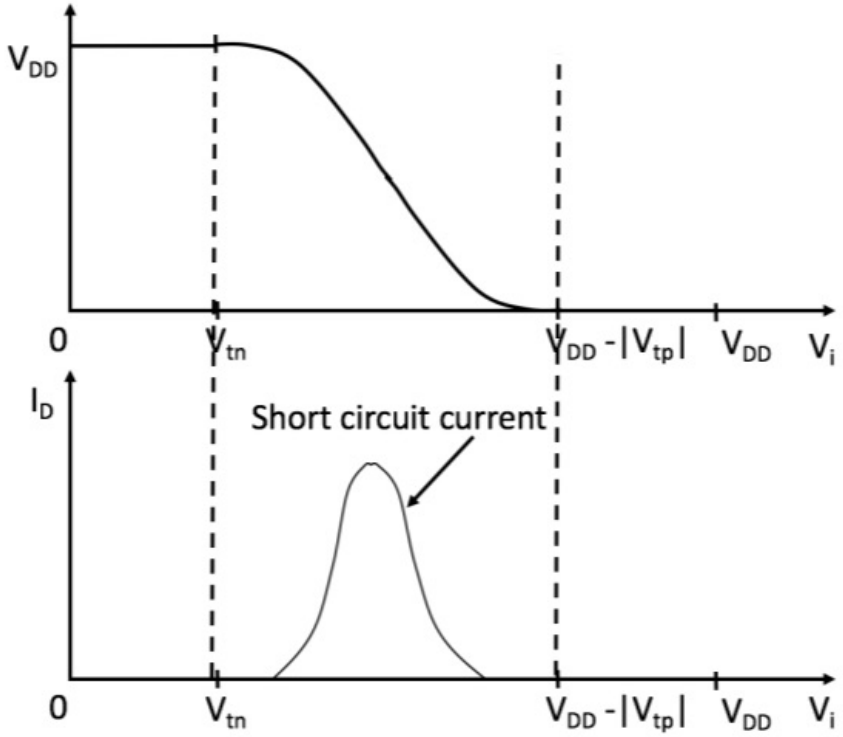


@ $V_{in} = 0$ ⇒ off state leakage current

$$I_{off} = I_0 \left(V_{gs\,n} = 0,\ V_{DS\,n} = V_{DD}\right)$$

$$\boxed{P = V_{DD} \cdot I_{off\,n}}$$

Q4 In an inverter, how will the power dissipated due to the short circuit current change if the inverter delay becomes larger? [20 pts]



Power is = IV or $P = \int I\,dV$

if the Delay is increased Drastically, the current switching would be Non zero for longer as $I = \frac{dV}{dt}$ ⇒ longer Delay implies a larger average short circuit current. in the case of MOS Physics $P_{sc} = V_{DD} I_{avg} t_{sc}$ where t_{sc} is the short CKT Duration.

↑ t_D ⇒ ↑ P Dissipated

Q5 Consider an inverter operating at V_{DD}=5 V. For the following cases, determine whether NM_L=NM_H or NM_L>NM_H or NM_L<NM_H? Assume that both the NMOSFET and PMOSFET has the same t_{ox} and μ_n=3μ_p. The analysis requires calculation of the middle voltage V_M and comparison of the transfer curves for different cases. [15 pts]

[Q1.1] $W_p = W_n$, $V_{t,n}$=$|V_{t,p}|$=1 V.

[Q1.2] $W_p = 3 \times W_n$, $V_{t,n}$=$|V_{t,p}|$=1 V.

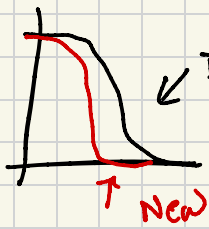
[Q1.3] $W_p = 3 \times W_n$, $V_{t,n}$=1.5 V, $|V_{t,p}|$=0.5 V.

Q5.1) Given that $\frac{\beta_p}{\beta_n} = \frac{\mu_p C_{ox} \frac{W_p}{L_p}}{\mu_n C_{ox} \frac{W_n}{L_n}} = \frac{\mu_p}{3\mu_n} = \frac{1}{3}$

$$\sqrt{\frac{\beta_p}{\beta_n}} = \sqrt{1/3}$$

$$V_M = \frac{\sqrt{\frac{\beta_p}{\beta_n}}\,(V_{DD} - |V_{tp}|) + V_{tn}}{1 + \sqrt{\frac{\beta_p}{\beta_n}}} \Rightarrow \frac{\sqrt{1/3} \cdot 5}{1+\sqrt{1/3}} \simeq 2.09\,V$$

$V_M < V_{DD}/2 \Rightarrow$



$\Rightarrow \boxed{NM_L < NM_H}$

Q5.2) $\sqrt{\frac{\beta_p}{\beta_n}} = \sqrt{\frac{\mu_p}{\mu_n}\frac{C_{ox}}{C_{ox}}\frac{W_p/L_p}{W_n/L_n}} = \frac{\mu_p}{3\mu_n}\frac{3W_n}{W_n} = 1$

$|V_{tp}| = V_{tn}$ ✓

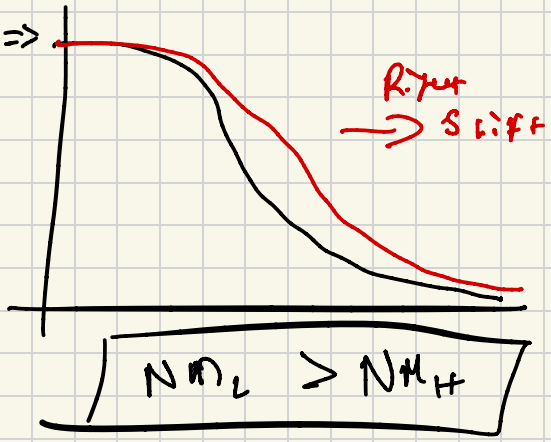
for Perfect Ratio $\Rightarrow V_M = \frac{V_{DD}}{2}$

$\Rightarrow$ VTC Ideal $\Rightarrow$ $\boxed{NM_H = NM_L}$

Q5.3) Same widths as (5-3)

$\Rightarrow V_n = \frac{(1)(5-.05)+1.5}{2} \Rightarrow 3V$

$3V > \frac{V_{DD}}{2} \Rightarrow$



$\boxed{NM_L > NM_H}$