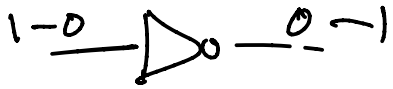
1. Consider a scenario where the the output capacitor (C_L) of an inverter is not a constant but depends on V_{OUT} as $C_L = C_0 . V_{OUT}$ (C_0 is a constant). Here V_{OUT} is the output voltage of the inverter. As the input of the inverter switches from VDD to 0, determine
   a. The total energy drawn from the supply
   b. The total energy stored on the output capacitor
   c. The total energy dissipated by the PMOS.

   Hint: Remember that current is I = d(Q)/dt and Q=C.V.



a) $P = I V \Rightarrow i(t)\, V_{out}$

$i_{C_L}(t) = \frac{d}{dt}(C_L V_{OUT}) \Rightarrow \frac{d}{dt}(C_0 V_{out}^2)$

$P = V_{DD} C_0 \frac{d}{dt}(V_{out}^2)$

$\mathcal{E} = \int_0^\infty P\, dt \Rightarrow \int_0^\infty V_{DD} C_0 \frac{d}{dt}(V_{out}^2)\, dt \Rightarrow V_{DD} C_0 \int_0^{V_{DD}} dV_{out}^2 = V_{DD} C_0 V_{out}^2 \Big|_0^{V_{DD}}$

$\mathcal{E}_{sup} \Rightarrow V_{DD}^3 C_0$

b) $P_{cap} = i(t)\, V_{out} \Rightarrow i_{out}(t) = \frac{d}{dt}(C_0 V_{out}^2)$

$\int P_{cap} = \int_0^\infty V_{out} C_0 \frac{d}{dt}(V_{out}^2)\, dt$

$\mathcal{E}_{cap} = 2C_0 \int_0^{V_{DD}} V_{out}^2\, dV_{out} = \frac{2}{3} C_0 V_{out}^3 \Big|_0^{V_{DD}}$

$$\mathcal{E}_{cap} = \frac{2}{3} C_{out} V_{DD}^3$$

c) $$\mathcal{E}_R = \frac{1}{3} C_{out} V_{DD}^3$$

2. Consider a digital circuit with 10M logic gates. Assume that the capacitance at the output of each logic gate is 20aF (1a = 10^{-18}). The supply voltage is 1.2V. The total leakage for each logic gate is 1nA. The switching activity is 5%. When the circuit is running at 1GHz, what is the total power dissipated by the circuit. (Ignore short circuit power).

$C_L = 20E\text{-}18\ F \quad V_{DD} = 1.2$ 0-1-0 transitions are 1e9

$\frac{E}{\text{second}} = E_{dyn} f \Rightarrow$ Rate @ which ~~Energy~~ Dissipated

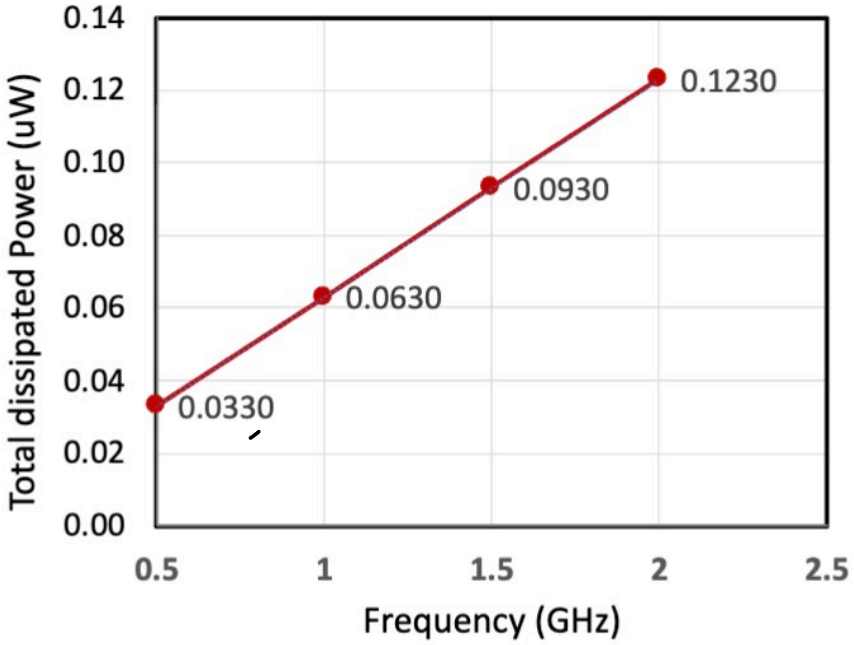
$= P_{power} = C_L V_{DD}^2 f$

$P_{dyn} = \left[\left[(20e\text{-}18)(1.2)^2(1e9)\right](.05) + V_{DD}(1e\text{-}9)\right] 10^7$

$= .0264$ Watts

26.4 W

3. Consider an inverter whose input in connected to a clock source with variable input frequency. Suppose you have measured the total power dissipated by the inverter and plotted it as a function of the frequency of the clock source (shown below). You also know that the switching time over which short circuit current flows is 1ps and the peak short circuit current is 10uA. From this information, determine the total capacitance at the output of the inverter (C_L) and the leakage current of the inverter. Assume V_{DD} = 1V.



$P_{avg} = P_{dyn} + P_{static}$ ← y intercept

$P_{dyn} = \left[C_L (1)^2 + (10e-6)(1)(1e-12)\right] f$

$\Rightarrow C_L + 1e-17 = \frac{.123e-6 - .033e-6}{(2-.05)(10^9)}$

extrapolate P_{static}

$\rightarrow 6e-17 - 1e-17 = \boxed{5e-17\,F}\ C_L$

$(.0630e-6) - (6e-17)(1e+9)$

$= \boxed{3e-9A = I_{Leak}}$