ECE 3030: Physical Foundations of Computer Engineering

Spring 2024

Midterm Test 2

April 3, 2024

Time: 1 hr 15 min

Instructor: Asif Khan

Name:

Instructions:

1. There are 8 pages in this test. Count the number of pages and notify the proctor if you are missing a page.
2. Read all the problems carefully and thoroughly before you begin working.
3. This is an OPEN everything EXCEPT FOR collaboration exam.
4. A list of constants and equations is provided on pages 7, 8.
5. You are required to answer all 4 questions. There are 100 total points. Observe the point value of each problem and allocate your time accordingly.

Q1	20 pts
Q2	20 pts
Q3	40 pts
Q4	20 pts
Total	100 pts

6. Show all your work and circle/underline your final answer. For numerical answers, write the units. Write legibly. If l cannot read it, it will be considered a wrong answer. Do all work on the space provided; use scratch paper when necessary. Turn in all scratch paper, even if it did not lead to an answer.
7. Download this template and write on your electronic device or print this template and write on the print if you can. Writing on a blank paper and clearly marking each questions is also fine. You are required to upload PDF/pictures of either the completed template or just your answers.
8. Report any and all ethics violations to the instructor/proctor.

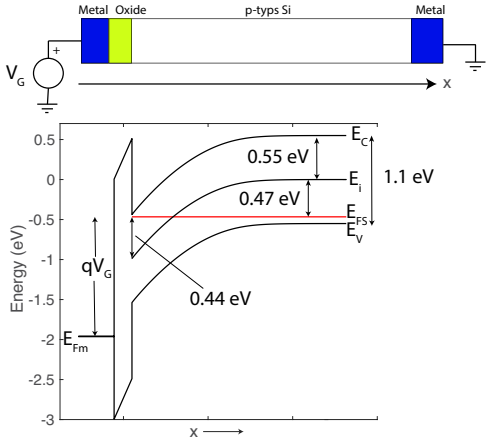
Sign your name on ONE of the two following cases:

I DID NOT observe any ethical violations during this exam:

I observed an ethical violation during this exam:

Q1 Circle the correct answer. All variables have their usual meaning. [Total 20 pts (5 × 4 pt)]

[Q1.1] For the band diagram of a MOS capacitor is shown in figure , is the gate voltage V_G larger than the threshold voltage V_t? **(Yes / No)**



[Q1.2] Increasing threshold voltage increases the off-current. **(True / False)**

[Q1.3] The on-current of a MOSFET does not depend on the power supply voltage. **(True / False)**

[Q1.4] In an inverter, when the input voltage is 0, the n-MOSFET is off and the p-MOSFET is on. **(True / False)**

[Q1.5] In a CMOS inverter, the p-type MOSFET has a larger width than that in the n-type MOSFET.**(True / False)**

Q2 **Current-voltage characteristics of a MOSFET:** The following figure shows how the drain current I_D in a long channel MOSFET changes as a function of the gate voltage V_{GS} at given value of the drain voltage V_{DS}. The range of the V_{GS} range for different modes of operation (cut-off, saturation and linear) also indicated. [Total 20 pts]

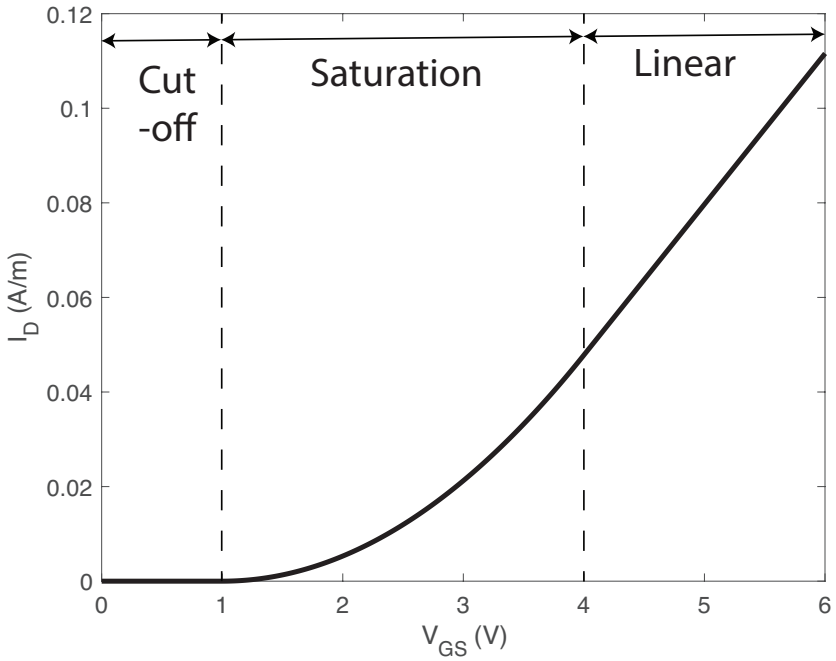


Figure 1: MOSFET $I_D - V_{GS}$ characteristics.

[Q2.1] What is the threshold voltage V_t of the MOSFET? [5 pts]

[Q2.2] What is the value of the drain voltage V_{DS}? [15 pts]

Q3 **Scaling:** Consider that all three physical dimensions of MOSFETs (W, L, t_{ox}) are downscaled by factor of x and the power supply voltage, V_{DD} and the threshold voltage, V_t are decreased by a factor of y in every subsequent generation. In addition, the total area of the chip, A_c, also increases by 5% in every subsequent generation. [Total 40 pts]

[Q3.1] If, in every subsequent generation, the total number of transistors doubles, what is the nominal value of x? [10 pts]

[Q3.2] Consider the clock frequency and the total active/dynamic chip power of the n-th generation are f_n and $P_{chip,n}$. Find an expression of the ratio of total chip powers of two subsequent generation, $P_{chip,n+1}/P_{chip,n}$ in terms of x, y, f_n and f_{n+1}. [20 pts]

[Space for Q3.2]

[Q3.3] What is the relation between f_{n+1} and f_n if you wanted the total active/dynamic chip power to remain the same across generations. [10 pts]

Q4 Explain in short why it necessary to have cache memories in today's microprocessor technology. [Total 20 pts]

Constants:
Electron charge q=1.6×10^{-19} C
Vacuum permittivity $\epsilon_\circ$=8.854×10^{-12} F/m Intrinsic carrier density of Si $n_i = 1.5 \times 10^{16}$ m^{-3} Relative dielectric constant of Si ϵ_{Si}=12
Relative dielectric constant of SiO_2 ϵ_{ox}=4
$N_C \approx N_V$=10^{25} m^{-3}
Bandgap of Si E_g=1.1 eV
Boltzmann constant k_B= 1.38 ×10^{-23} m^{2}kg s^{-2} K^{-1}
k_BT/q=26 mV (T=room temperature).

Equations:
Conductivity of a metal $\sigma = nq\mu$
Resistivity of a metal $\rho = 1/\sigma$
Intrinsic carrier density $n_i = \sqrt{N_C N_V} e^{-\frac{E_g}{2k_BT}}$; Electron density $n = N_C e^{\frac{E_F - E_C}{k_BT}}$; Hole density $p = N_V e^{\frac{E_V - E_F}{k_BT}}$
In a p-type semiconductor, hole density p=N_A and $n = \frac{n_i^2}{N_A}$.
In a n-type semiconductor, hole density $p = \frac{n_i^2}{N_D}$ and $n = N_D$.

p-n Junctions:
Built in potential $V_{bi} = \frac{k_BT}{q} \ln \frac{N_A N_D}{n_i^2}$
Depletion width $W = \sqrt{\frac{2\epsilon_\circ \epsilon_{Si}}{q}(\frac{1}{N_A} + \frac{1}{N_D})(V_{bi} - V)}$; V is the voltage applied across the pn junction. V is positive and negative when the pn junction is forward and reverse biased, respectively.
Depletion width in p-side $W_p = \frac{N_D}{N_A + N_D} W$
Depletion width in n-side $W_p = \frac{N_A}{N_A + N_D} W$
Maximum electric field $E_{max} = \frac{qN_A W_p}{\epsilon_\circ \epsilon_{Si}} = \frac{qN_D W_n}{\epsilon_\circ \epsilon_{Si}}$

MOS Capacitor:
Gate voltage $V_G = V_{ox} + \psi_s$; V_{ox} is the voltage drop across the oxide and ψ_S is the surface potential (electrostatic potential at the oxide-semiconductor interface).
Oxide capacitance $C_{ox} = \frac{\epsilon_\circ \epsilon_{ox}}{t_{ox}}$
Depletion width $W = \sqrt{\frac{2\epsilon_\circ \epsilon_{Si}}{qN_A}\psi_s}$
Maximum depletion width $W_{max} = \sqrt{\frac{2\epsilon_\circ \epsilon_{Si}}{qN_A} 2\psi_B}$
Threshold voltage $V_t = \frac{\sqrt{4\epsilon_\circ \epsilon_{Si} qN_A \psi_B}}{C_{ox}} + 2\psi_B$; ψ_B=$\frac{|E_i - E_F|}{q}$

MOSFET:
Long channel MOSFET (square law model):

$$\frac{I_D}{W} = \begin{cases} 0; \text{ when } V_G < V_t \\ \mu C_{ox} \frac{1}{L}((V_G - V_t)V_D - \frac{1}{2}V_D^2); \text{ when } V_G - V_t > V_D \\ \mu C_{ox} \frac{1}{2L}(V_G - V_t)^2; \text{ when } V_G - V_t < V_D \end{cases}$$

Long channel MOSFET (square law model with correction for subthreshold current):

$$\frac{I_D}{W} = \begin{cases} I_{sub-V_t} e^{\frac{q(V_G-V_t)}{mkT}}(1-e^{\frac{-qV_D}{kT}}); \text{ when } V_G < V_t \text{ (sub-threshold)} \\ I_{sub-V_t}(1-e^{\frac{-qV_D}{kT}}) + \mu C_{ox}\frac{1}{L}((V_G-V_t)V_D - \frac{1}{2}V_D^2); \text{ when } V_G - V_t > V_D \text{ (linear)} \\ I_{sub-V_t}(1-e^{\frac{-qV_D}{kT}}) + \mu C_{ox}\frac{1}{2L}(V_G-V_t)^2; \text{ when } V_G - V_t < V_D \text{ (saturation)} \end{cases}$$

Body factor $m = 1 + \frac{C_D}{C_{ox}}$, where $C_D = \frac{\epsilon_\circ \epsilon_{Si}}{W}$ (depletion capacitance).

Velocity saturated MOSFET: $I_{D,sat} = \mu C_{ox} W v_{sat}(V_G - V_t)$; where v_{sat} is the saturation velocity of the carriers.
Inverter:

$$\text{Middle voltage } V_M = \frac{\sqrt{\frac{\beta_p}{\beta_n}}(V_{DD} - |V_{tp}|) + V_{tn}}{1 + \sqrt{\frac{\beta_p}{\beta_n}}}$$

where β_i=$\mu_i C_{ox}(\frac{W_i}{L_i})$, $i \equiv p, n$. μ_i=mobility, W_i=i-type MOSFET width; L_i=i-type MOSFET gate length. MOSFET effective resistance $R_t = \frac{10V_B+3V_t}{6\beta V_B^2} = \frac{10V_{DD}-7V_t}{6\beta(V_{DD}-V_t)^2}$
where $V_B = V_{DD} - V_t$; β=$\mu C_{ox}(\frac{W}{L})$. μ=mobility, W= MOSFET width; L= MOSFET gate length.

Inverter delay is proportional to $R_t C_L$. $C_L = C_{g,p} + C_{g,n}$ where $C_{g,i}$=gate capacitance of i-type MOSFET = $\epsilon_\circ \epsilon_{ox} W_i L_i / t_{ox}$, $i \equiv p, n$.

Power dissipation due to charging and discharging = $C_L V_{DD}^2 f$; f being the frequency.

Resistance of a wire $R = \rho \frac{\text{Length}}{\text{Area}}$; ρ being the resistivity.
Capacitance of a parallel plate capacitor $C = \frac{\epsilon_\circ \epsilon_{ox} \text{Area}}{\text{Thickness}}$.

Elmore delay $\delta_E = \sum_{1 \le i \le n} c_i \sum_{1 \le j \le i} r_j$, c_i and r_j being the capacitance and the resistance of i-th and j-th section respectively.
If all the segments have the same resistance and capacitance $\delta_E = n(n+1)rc/2$, n being the number of segments.

Chip junction temperature $T = T_A + P R_{thermal}$, T_A, P and $R_{thermal}$ being the ambient temperature, power and thermal resistance, respectively.
Thermal time constant $\tau_{thermal} = R_{thermal} C_{thermal}$, $C_{thermal}$ being the thermal capacitance.