1. Use algebraic techniques to simply the following Boolean equations in terms of the variables P, Q, R and S.

$$F = P.S + P.\overline{Q}.\overline{S} + P.Q.S$$

$$G = F.P + R.P + (\overline{P} + \overline{S}).(\overline{P} + Q).R$$

$\overline{P}\,\overline{P} + \overline{S}\,\overline{P} + \overline{P}\,Q + \overline{S}\,Q$

Note that G is a function of F, which is given by the first equation.

Finally, simplify:

$$H = F.G$$

$PS + P\bar{Q}\bar{S}$

$P(S + \bar{Q}\bar{S}) \Rightarrow P(S + \bar{Q}) \Rightarrow \boxed{PS + P\bar{Q} = F}$

$G = (PS + P\bar{Q})P + RP + (\bar{P}\bar{P} + \bar{S}\bar{P} + \bar{P}Q + \bar{S}Q)R$

$G = PS + P\bar{Q} + RP + \bar{P}R + \bar{S}\bar{P}R + \bar{P}QR + \bar{S}QR$

$PS + P\bar{Q} + R(P + \bar{P}) + \bar{S}\bar{P}R + \bar{P}QR + \bar{S}QR$

$PS + P\bar{Q} + R + \bar{S}\bar{P}R + \bar{P}QR + \bar{S}QR$

$PS + P\bar{Q} + R(1 + \bar{S}\bar{P} + \bar{P}Q + \bar{S}Q)$

$G = PS + P\bar{Q} + R \quad H = FG$

$(PS + P\bar{Q})(PS + P\bar{Q} + R)$

$H = (PS + P\bar{Q})PS + (PS + P\bar{Q})P\bar{Q} + (PS + P\bar{Q})R$

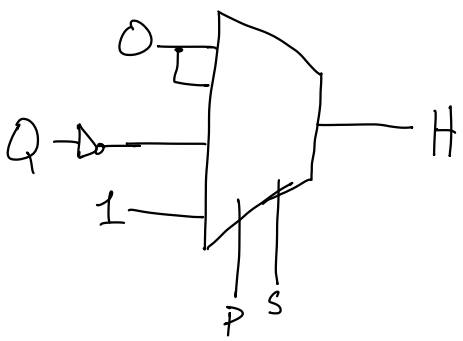
$PS + P\bar{Q}S + P\bar{Q}S + P\bar{Q} + PSR + P\bar{Q}R$

$PS + P\bar{Q}(S + S + 1 + R) + PSR$

$PS + P\bar{Q} + PSR \Rightarrow PS(1 + R) + P\bar{Q} \Rightarrow \boxed{PS + P\bar{Q}}$

2. Use the smallest possible multiplexer to implement the simplified Boolean expression H that you obtained in 1(a). Note that H should be expressed in terms of the input variables P, Q, R and S.

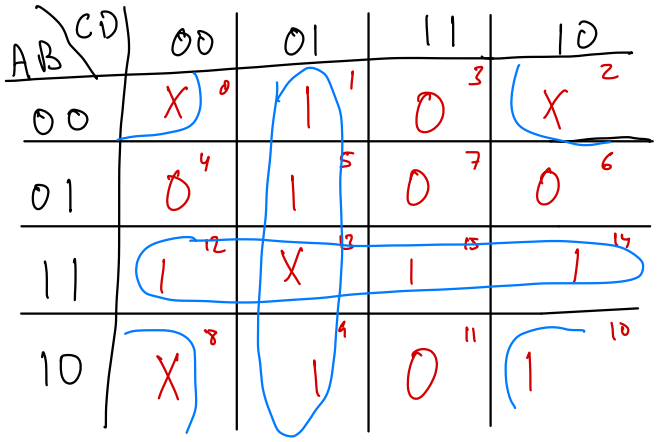
P	S	Q	$\bar{Q}$	H	
0	0	0	1	0	0
0	0	1	0	0	
0	1	0	1	0	0
0	1	1	0	0	
1	0	0	1	1	$\bar{Q}$
1	0	1	0	0	
1	1	0	1	1	1
1	1	1	0	1	



Made with Goodnotes

3. K-Maps: Write down a simplified SOP expression for the following using K-Maps:

$$F(A,B,C,D) = \Pi M(3,4,6,7,11) + d(0,2,8,13)$$



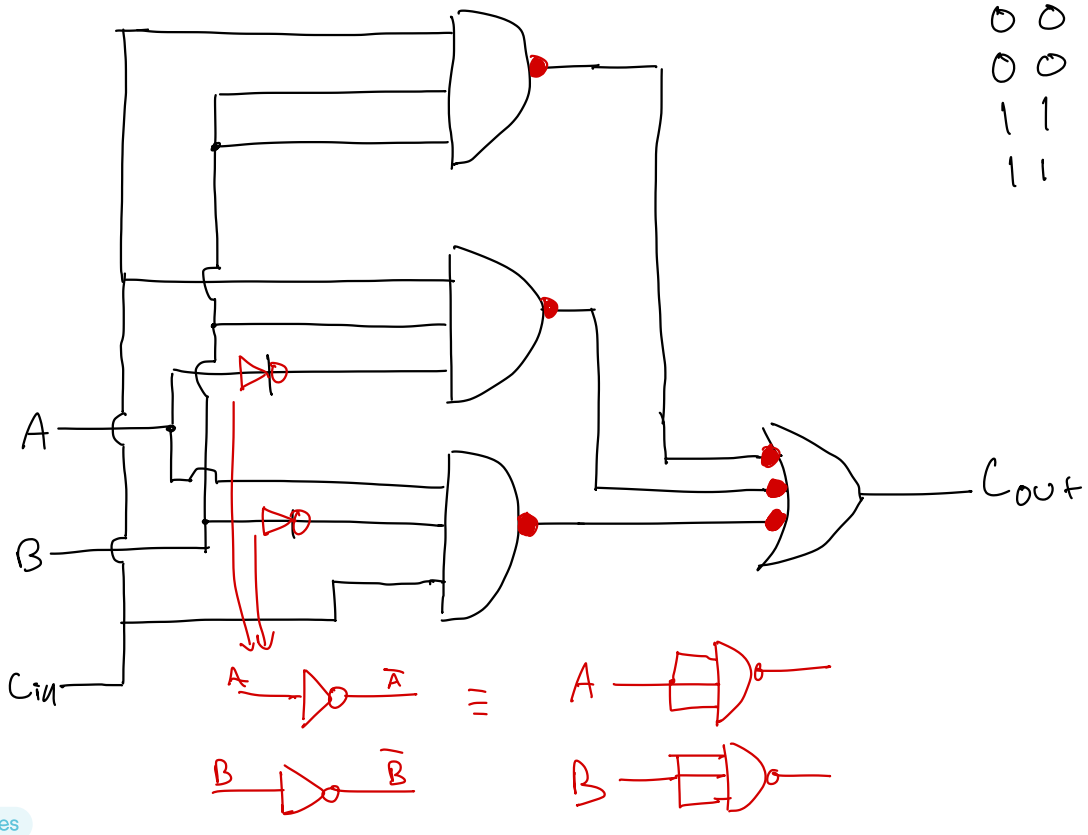
$F(A,B,C,D) = \bar{C}D + AB + \bar{B}\bar{D}$

4. Mixed Logic Synthesis: Use the mixed logic design style to implement the output carry (C_{OUT}) of a FULL ADDER using 3-input NAND gates only. Count the total number of transistors.

$$C_{out} = AB + C_{in}(A \oplus B) \Rightarrow AB + C_{in}(\bar{A}B + A\bar{B})$$
$$AB + C_{in}\bar{A}B + C_{in}A\bar{B}$$

AND

A	A	B	F
0	0	0	0
0	0	1	0
1	1	0	0
1	1	1	1



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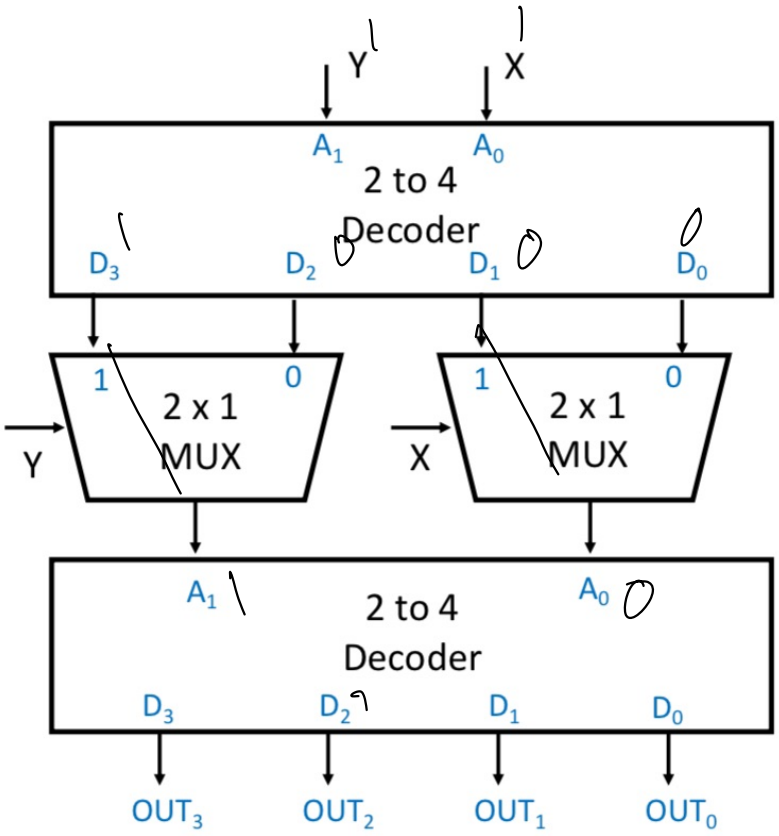
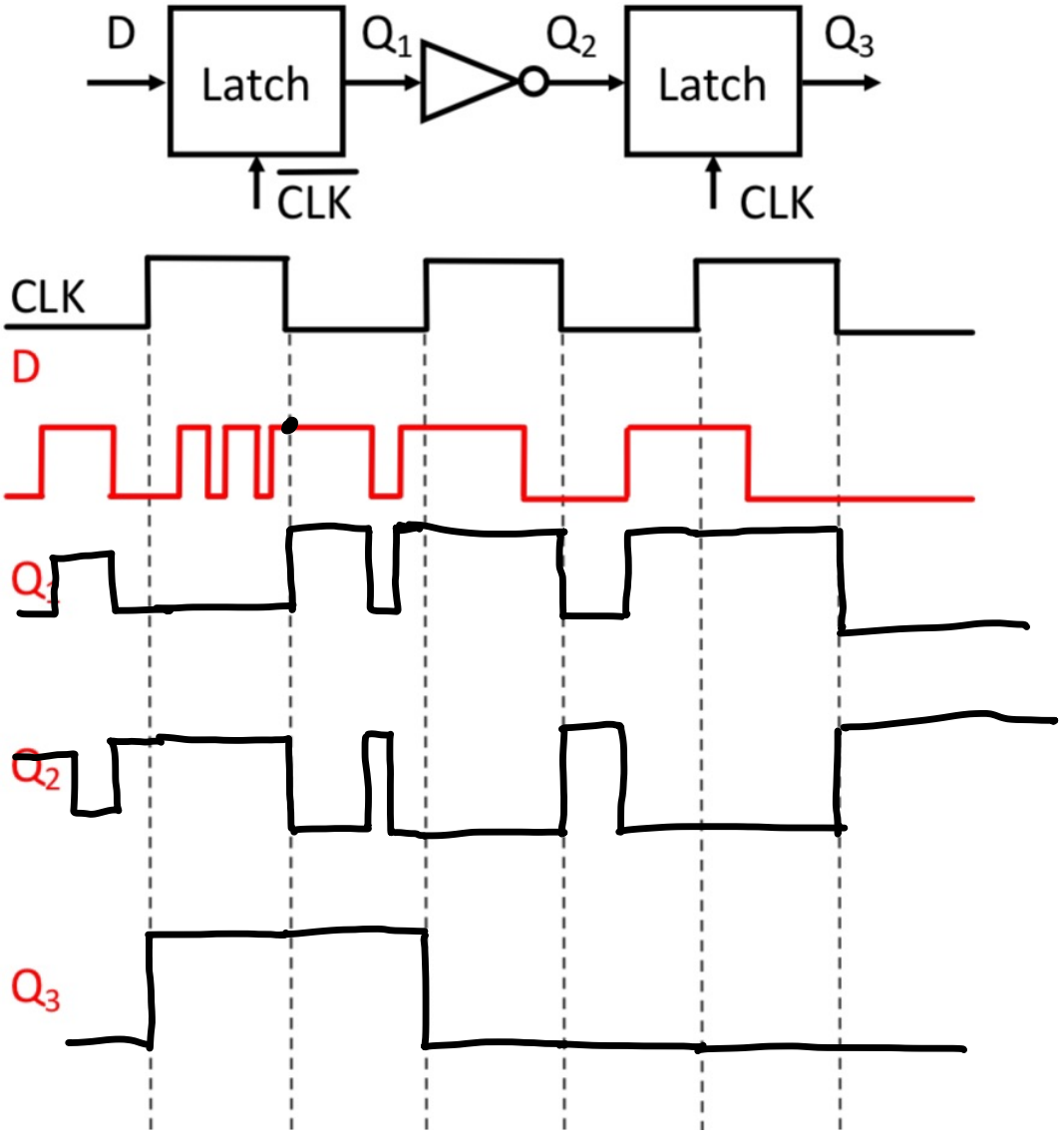
5. Consider the combinational circuit below. Use this circuit to fill out the truth table shown below.



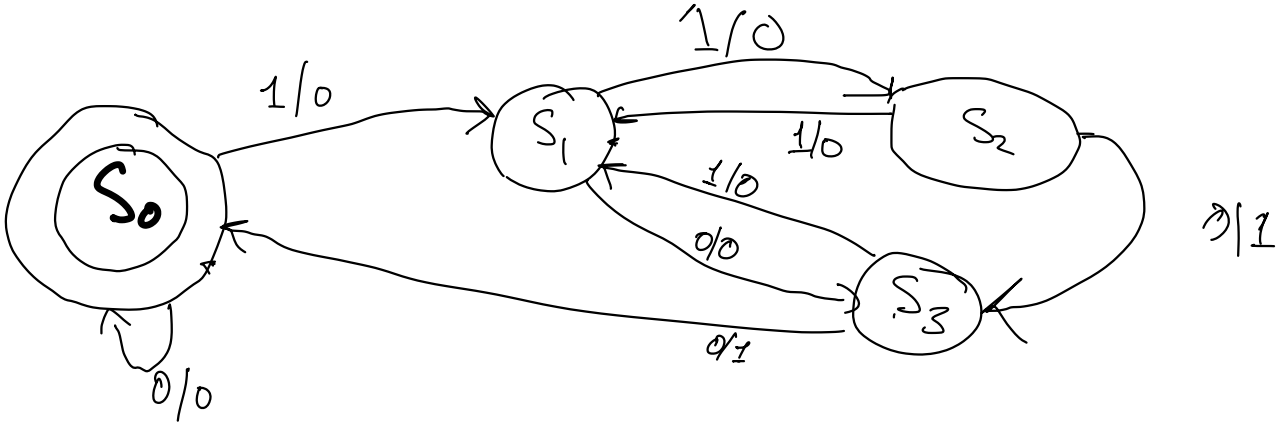
X	Y	OUT_3	OUT_2	OUT_1	OUT_0
0	0	0	0	1	0
0	1	0	0	0	1
1	0	0	0	1	0
1	1	0	1	0	0

Made with Goodnotes

6. Complete the following timing diagram. Assume Q_1 and Q_3 are initialized to zero. Be careful when you are copying the timing diagram.

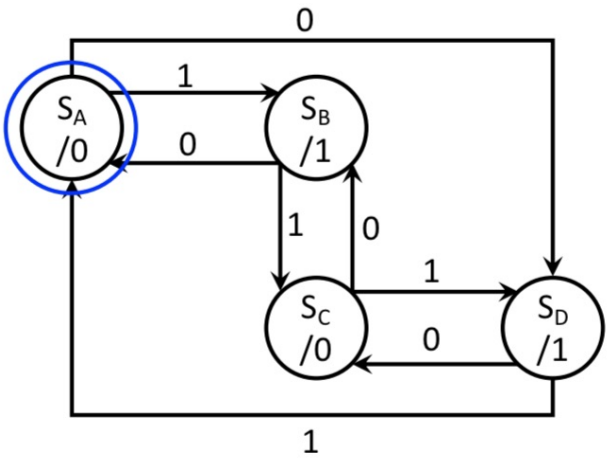


7. Pattern Detection with FSM: You have been asked to design a Mealy machine which can detect a pattern 1X0, where X is a DON'T CARE condition. Hence it will produce a 1 for both 110 and 100. Draw the state diagram of the FSM.



Made with Goodnotes

8. For the state diagram shown below, write down the state transition table and draw the corresponding sequential circuit diagram.



S_A – 00
S_B – 01
S_C – 10
S_D – 11

Q_1	Q_2	input	$N(Q_1)$	$N(Q_2)$	output
0	0	0	1	1	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	0	0	1

$N(Q_1) = \bar{Q}_1\bar{Q}_2\bar{i} + \bar{Q}_1 Q_2 i + Q_1 Q_2 \bar{i} + Q_1\bar{Q}_2 i$

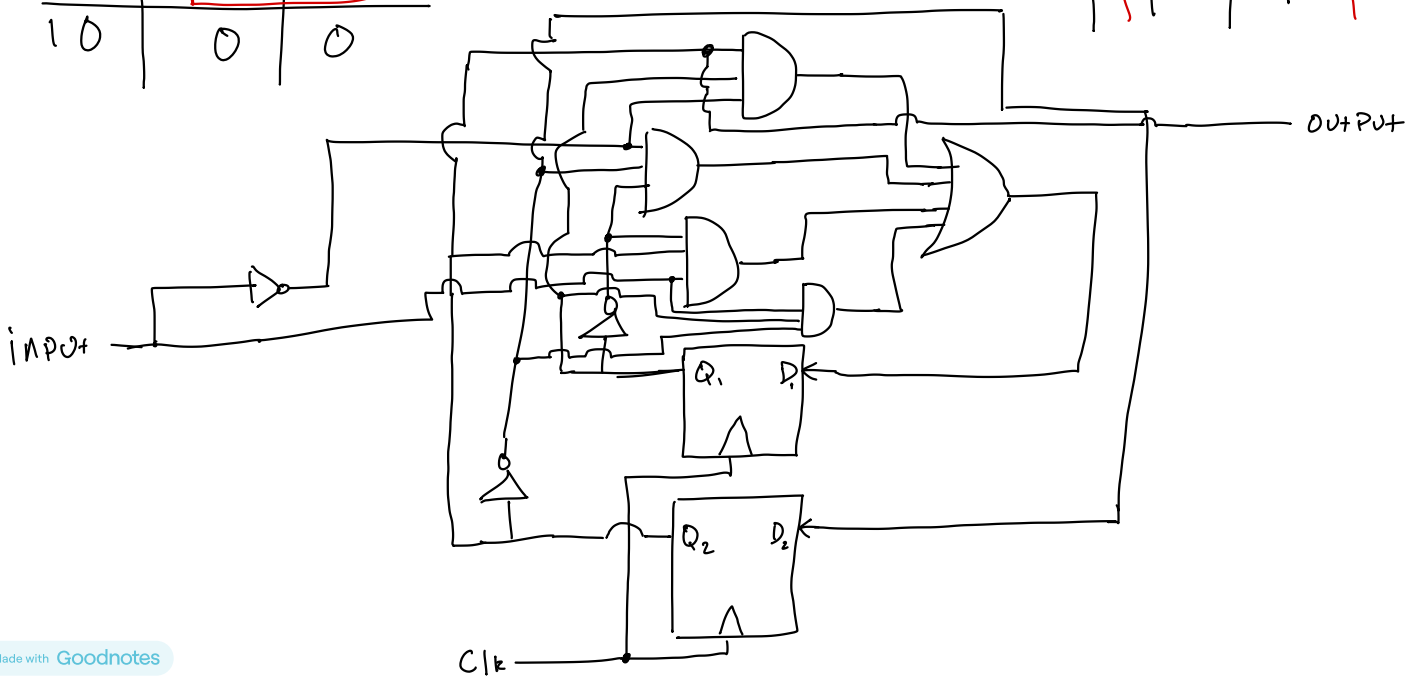
Q_1Q_2 \ input	0	1
00	1	0
01	0	1
11	1	0
10	0	1

$N(Q_2) = \bar{Q}_2$

Q_1Q_2 \ input	0	1
00	1	1
01	0	0
11	0	0
10	1	1

output $= Q_2$

Q_1Q_2 \ input	0	1
00	0	0
01	1	1
11	1	1
10	0	0

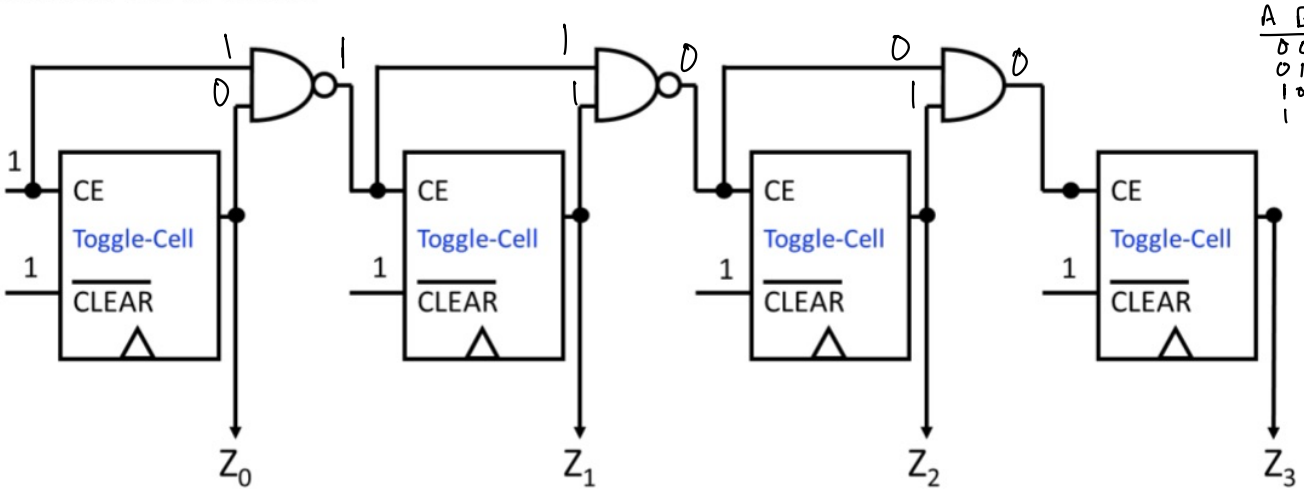


Made with Goodnotes

9. Consider the following modified synchronous counter. Assume that the counter is initialized to 0010.

NAND

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0



Complete the following table.

Cycle	Z0	Z1	Z2	Z3
0	0	0	1	0
1	1	1	0	1
2	0	1	1	1
3	1	0	1	1

Made with Goodnotes