ECE 3030: Physical Foundations of Computer Engineering

Fall 2022

Final Exam

December 8, 2022

Time: 2 hour 50 min

Instructor: Asif Khan

Instructions:

1. There are 11 pages in this test. Count the number of pages and notify the proctor if you are missing a page.
2. Read all the problems carefully and thoroughly before you begin working.
3. You are allowed to use 4 sides of notes as well as a calculator.
4. A list of constants and equations is provided on pages 10, 11.
5. You are required to answer all 7 questions. There are 100 total points. Observe the point value of each problem and allocate your time accordingly.

Q1	5 pts
Q2	30 pts
Q3	20 pts
Q4	20 pts
Q5	10 pts
Q6	10 pts
Q7	5 pts
Total	100 pts

6. Show all your work and circle/underline your final answer. For numerical answers, write the units. Write legibly. If l cannot read it, it will be considered a wrong answer. Do all work on the space provided; use scratch paper when necessary. Turn in all scratch paper, even if it did not lead to an answer.
7. Report any and all ethics violations to the instructor/proctor.

Sign your name on ONE of the two following cases:

I DID NOT observe any ethical violations during this exam:

I observed an ethical violation during this exam:

Q1 **Semiconductor physics:** Draw the band diagram (the relative positions of conduction band edge E_C, valence band edge E_v, Fermi level E_F) for Si wafer with acceptor doping N_A=5×10^{23} m^{-3} and no donor doping. Clearly indicate the values of $E_C - E_F$, $E_F - E_V$, $E_i - E_F$, $E_G = E_C - E_V$. E_i is the intrinsic Fermi level. Assume N_C=N_V=10^{25} m^{-3}, E_G=1.1 eV, n_i=1.5×10^{16} m^{-3}, kT=0.026 eV. [Total 5 pts]

Solution to Q1.1:

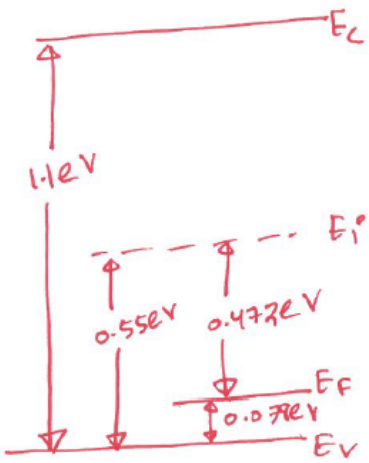
$$P = N_A = 5 \times 10^{23}\ m^{-3}$$

$$\Rightarrow N_A = N_V\, e^{\frac{E_V - E_F}{K_B T}}$$

$$\Rightarrow E_V - E_F = K_B T \ln \frac{N_A}{N_V}$$

$$= 0.026 \ln \frac{5 \times 10^{23}}{10^{25}}$$

$$= -0.078\ eV$$



Q2 **MOSFETs and Delay and Power in Inverter:** If decrease the doping density N_A in a MOSFET with all the parameters unchanged, how will the following quantities change? [Total 30 pts]

[Q2.1] The MOSFET threshold voltage, V_t. [5 pts]

Solution to Q2.1:

$$V_t = \frac{\sqrt{4\varepsilon_0\varepsilon_{Si} N_A \psi_B}}{C_{ox}} + 2\psi_B$$

Although ψ_B also depends on N_A, it is a weak function of N_A. $\therefore$ V_t can be considered proportional to N_A.

$\therefore$ if $N_A \downarrow \Rightarrow V_t \downarrow$

[Q2.2] The on-state current, I_{ON} of the MOSFET. [5 pts]

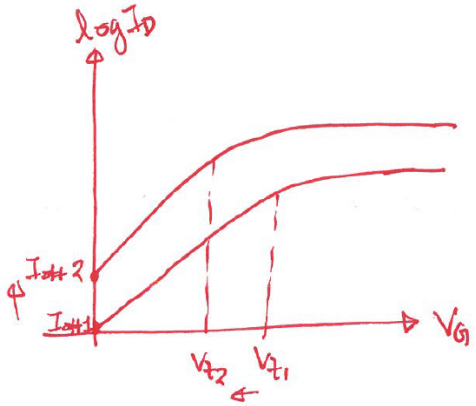
Solution to Q2.2:

$$I_{ON} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

If $N_A \downarrow \Rightarrow V_t \downarrow \Rightarrow I_{ON} \uparrow$

[Q2.3] The off-state leakage current, I_{OFF} of the MOSFET. [5 pts]

Solution to Q2.3:



~~If V_t~~

If $N_A \downarrow \Rightarrow V_t \downarrow \Rightarrow I_{off} \uparrow$

[Q2.4] The corresponding inverter delay. [5 pts]

Solution to Q2.4:

$$\text{Delay, } t_d = \frac{C_L V_{DD}}{I_{ON}}$$

If $N_A \downarrow \Rightarrow V_t \downarrow \Rightarrow I_{ON} \uparrow \Rightarrow t_d \downarrow$

[Q2.5] The active power in the corresponding inverter. The clock frequency did not change. [5 pts]

Solution to Q2.5:

$P_{act} = C_L V_{DD}^2 f$

$\therefore$ P_{act} do not depend on N_A (or any function of N_A).

$\therefore$ If $N_A \downarrow$ $\Rightarrow$ P_{act} remains the same.

[Q2.6] The off-state leakage power in the corresponding inverter. [5 pts]

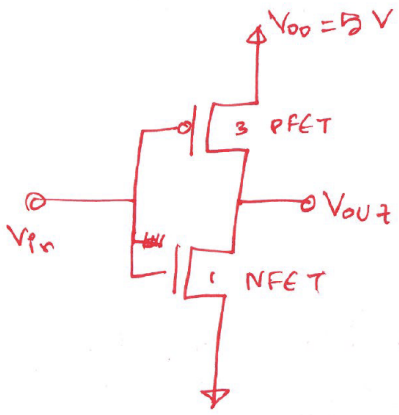
Solution to Q2.6:

$P_{off} = V_{DD} I_{off}$

If $N_A \downarrow \Rightarrow V_t \downarrow \Rightarrow I_{off} \uparrow \Rightarrow P_{off} \uparrow$

Q3 **Inverter:** Consider an inverter where $V_{t,n} = |V_{t,p}|$=1 V, $W_n = W_p/3$, $L_n = L_p$, $\mu_n = 3 \times \mu_p$ and V_{DD}=5 V. All the variables have their usual meaning. [Total 25 pts]

[Q3.1] Draw the circuit diagram of an inverter. [5 pts]
Solution to Q3.1:



[Q3.2] If the input is a logical 1, what are the states of the n-MOSFET and the p-MOSFET (*i.e.*, on or off)? [5 pts]
Solution to Q3.2:

If $V_{in} = V_{DD}$ → NMOS will turn on

PMOS will turn off.

[Q3.3] Calculate the middle voltage of the inverter. [5 pts]

Solution to Q3.3:

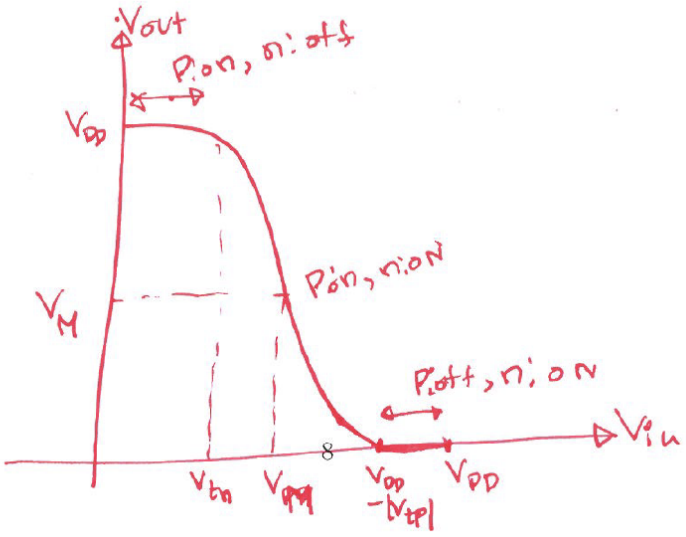
$$\frac{\beta_p}{\beta_n} = \frac{\mu_p W_p/L_p}{\mu_n W_n/L_n} = \frac{\mu_p}{\mu_n} \cdot \frac{W_p}{W_n} \cdot \frac{L_n}{L_p} = \frac{1}{3} \cdot 3.1 = 1$$

$$\therefore V_M = \frac{\sqrt{\frac{\beta_p}{\beta_n}}(V_{DD} - |V_{tp}|) + V_{tn}}{1 + \sqrt{\frac{\beta_p}{\beta_n}}} = \frac{1 \cdot \frac{1}{1}(5-1)+1}{1+1}$$

$$= 2.5\,V$$

[Q3.4] Draw the approximate shape of the voltage transfer curve (VTC) of the inverter. Clearly indicate the middle voltage and all the relevant voltages in the curve. [5 pts]

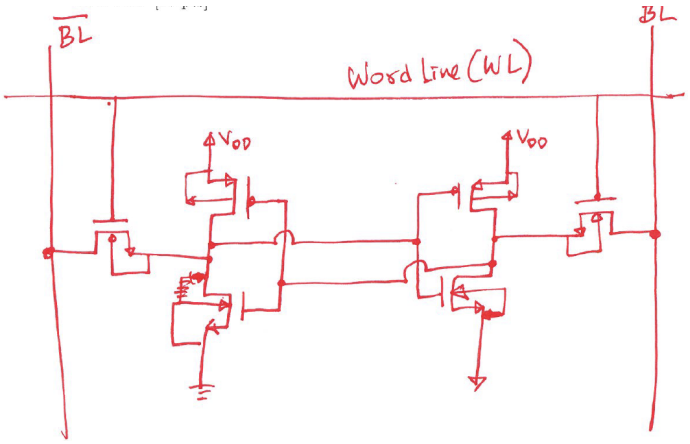
Solution to Q3.4:



Q4 **Memory technologies.**

[Q4.1] **SRAM:** Draw the circuit diagram of a 6T SRAM cell. Clearly show the bit lines and the word line. [5 pts]

Solution to Q4:



[Q4.2] **DRAM:** In DRAMs, why is it necessary to perform a restore operation after every time a cell is read. [5 pts]

Solution: The read operation in a DRAM is destructive–*i.e.*, after a DRAM cell is read, the data is lost. As such, the data read needs to be re-written after a cell has been read.

[Q4.3] **Magnetic Hard Drives:** Briefly explain why the magnetic hard drive technology is not classified as a random access memory technology by clearly stating what random memory access means. [5 pts]

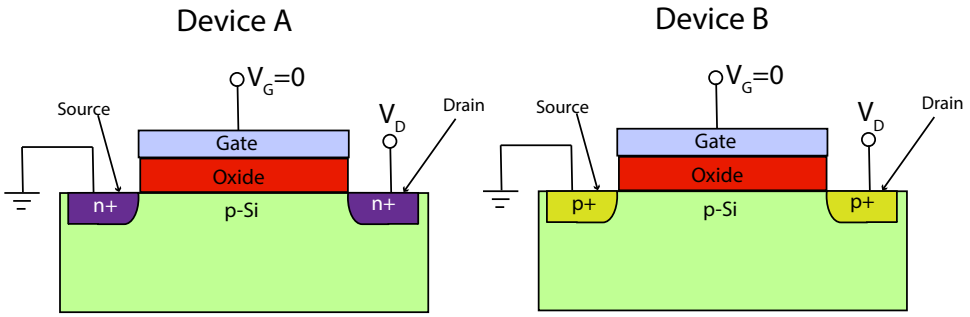
Solution: A random access memory device allows data items to be read or written in almost the same amount of time irrespective of the physical location of data inside the memory. In a magnetic hard drive, the read head first needs to move to the target track on the magnetic disk, then the disk needs to rotate such the target section comes under the head and finally the entire sector is read by the head. As such, the total amount of time to retrieve the data depends in the initial position of the head and the physical location of the data–*i.e.*, the access time depends on the physical location of the data. Hence, the magnetic hard drive technology is not classified as a random access memory technology.

[Q4.4] Briefly explain why it is necessary to have multiple levels of cache memory in today's microprocessor technology. Why was it not necessary in the 1980s? [Total 5 pts]

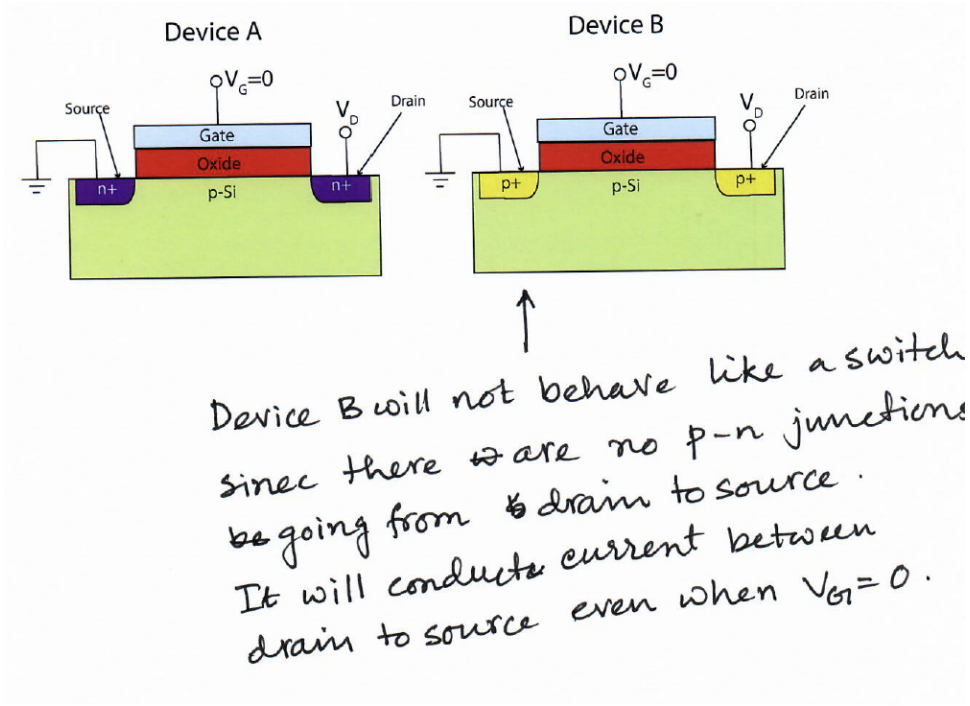
Solution to Q4.4:

Cache memory is used to decrease the average time or energy to access data from the main memory. The microprocessor clock period has become significantly smaller than the average main memory access/retrival times (aka memory wall), hence if there is no cache memory, having to access the main memory frequently will reduce the performance of the overall system. In the 1980s, there was much less difference between clock rate & memory access time, which is why it was not necessary to have cache memory

Q5 **MOSFET Physics:** Consider the two devices shown in the following figure. Device A is the MOSFET structure that we discussed in the class and in which the source and drain are n^+-type (heavily doped n-type). On the other hand, in device B source and drain are p^+-type (heavily doped p-type). Based on what we discussed in class, do you think device B will behave like a switch–*i.e.* will device B be able to block current from flowing between the drain and the source terminal when the gate voltage V_G is zero (or less than the threshold voltage)? Provide justification for your answer. [Total 5 pts]



Solution to Q5:



Q6 **Dynamic Voltage and Frequency Scaling (DVFS):** Consider the logic blocks shown in figure 1. Logic block 2 and 3 receives input from logic block 1 at the same time. Logic block 5 needs inputs from blocks 3 and 4 for generate the final output. Logic block 3 receives input from logic block 2. Logic block 2, 3 and 4 requires 50, 10, and 30 cycles, respectively, to generate the respective output.

Based on what you have learned in class, how will you apply DVFS in these system? For which logic block(s), will you increase or decrease the power supply voltage and by how much? How much energy will you save in your prescribed process? Explain your answer. Make necessary and simplest possible reasonable assumptions. [Total 35 pts]

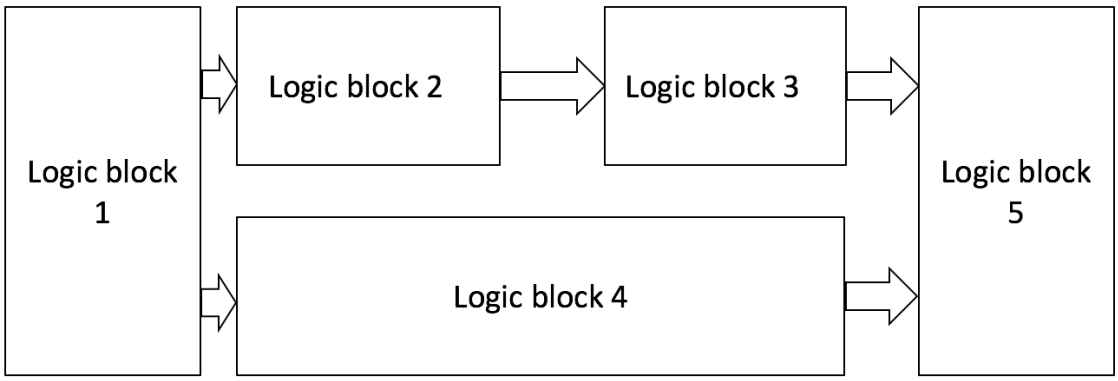
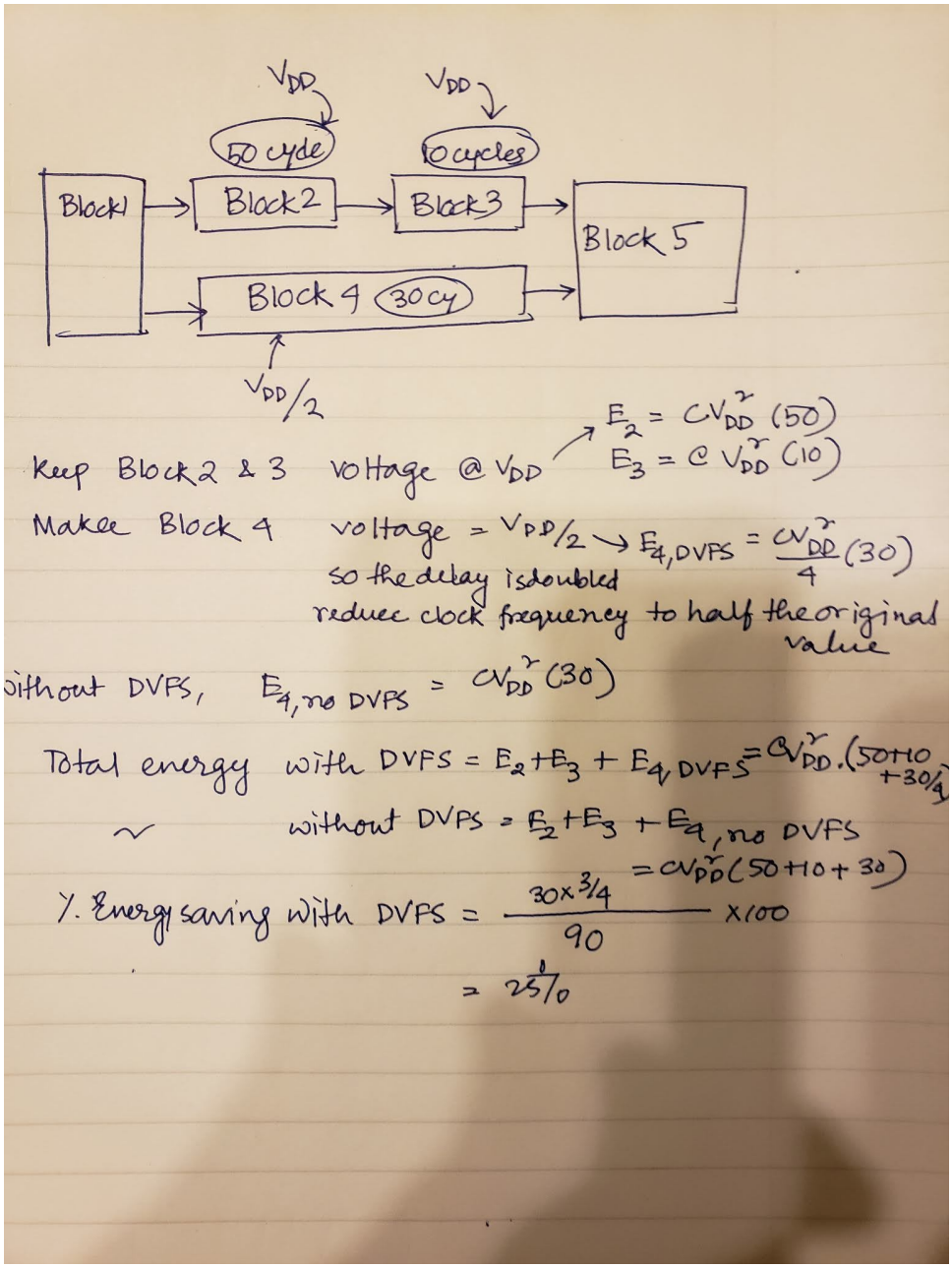


Figure 1: Dynamic Voltage and Frequency Scaling (DVFS).

Solution to Q6:



Q7 Circle the correct answer. The statements/questions are straightforward, no tricks are intended in the statements. [Total 5 pts (5 × 1 pt)]

[Q7.1] An increase in the power supply voltage decreases the interconnect delay. **(True/False)**

[Q7.2] Increasing the mobility of the semiconductor material increases the on-current of the MOSFET. **(True/False)**

[Q7.3] In a DRAM/cache system, if the hit rate is very low, DRAM access speed does not matter. **(True/False)**

[Q7.4] In p-type Si, the dopant is a group-III element. **(True/False)**

[Q7.5] Which technique is the most effective one when the off-state leakage (not capacitor charging and discharging) is the dominant consumption mode? **(Dynamic voltage and frequency scaling/Race-to-dark)**

Constants:
Electron charge q=1.6×10^{-19} C
Vacuum permittivity $\epsilon_\circ$=8.854×10^{-12} F/m Intrinsic carrier density of Si $n_i = 1.5 \times 10^{16}$ m^{-3} Relative dielectric constant of Si ϵ_{Si}=12
Relative dielectric constant of SiO_2 ϵ_{ox}=4
$N_C \approx N_V$=10^{25} m^{-3}
Bandgap of Si E_g=1.1 eV
Boltzmann constant k_B= 1.38 ×10^{-23} m^{2}kg s^{-2} K^{-1}
k_BT/q=26 mV (T=room temperature).

Equations:
Intrinsic carrier density $n_i = \sqrt{N_C N_V} e^{-\frac{E_g}{2k_BT}}$; Electron density $n = N_C e^{\frac{E_F - E_C}{k_BT}}$; Hole density $p = N_V e^{\frac{E_V - E_F}{k_BT}}$
In a p-type semiconductor, hole density p=N_A and $n = \frac{n_i^2}{N_A}$.
In a n-type semiconductor, hole density $p = \frac{n_i^2}{N_D}$ and $n = N_D$.

p-n Junctions:
Built in potential $V_{bi} = \frac{k_BT}{q} \ln \frac{N_A N_D}{n_i^2}$
Depletion width $W = \sqrt{\frac{2\epsilon_\circ \epsilon_{Si}}{q}(\frac{1}{N_A} + \frac{1}{N_D})(V_{bi} - V)}$; V is the voltage applied across the pn junction. V is positive and negative when the pn junction is forward and reverse biased, respectively.
Depletion width in p-side $W_p = \frac{N_D}{N_A + N_D} W$
Depletion width in n-side $W_p = \frac{N_A}{N_A + N_D} W$
Maximum electric field $E_{max} = \frac{qN_A W_p}{\epsilon_\circ \epsilon_{Si}} = \frac{qN_D W_n}{\epsilon_\circ \epsilon_{Si}}$

MOS Capacitor:
Gate voltage $V_G = V_{ox} + \psi_s$; V_{ox} is the voltage drop across the oxide and ψ_S is the surface potential (electrostatic potential at the oxide-semiconductor interface).
Oxide capacitance $C_{ox} = \frac{\epsilon_\circ \epsilon_{ox}}{t_{ox}}$
Depletion width $W = \sqrt{\frac{2\epsilon_\circ \epsilon_{Si}}{qN_A}\psi_s}$
Maximum depletion width $W_{max} = \sqrt{\frac{2\epsilon_\circ \epsilon_{Si}}{qN_A} 2\psi_B}$
Threshold voltage $V_t = \frac{\sqrt{4\epsilon_\circ \epsilon_{Si} q N_A \psi_B}}{C_{ox}} + 2\psi_B$; $\psi_B = \frac{|E_i - E_F|}{q}$

MOSFET:
Long channel MOSFET (square law model):

$$\frac{I_D}{W} = \begin{cases} 0; \text{ when } V_G < V_t \\ \mu C_{ox} \frac{1}{L}((V_G - V_t)V_D - \frac{1}{2}V_D^2); \text{ when } V_G - V_t > V_D \\ \mu C_{ox} \frac{1}{2L}(V_G - V_t)^2; \text{ when } V_G - V_t < V_D \end{cases}$$

Long channel MOSFET (square law model with correction for subthreshold current):

$$\frac{I_D}{W} = \begin{cases} I_{sub-V_t} e^{\frac{V_G - V_t}{m k_B T}} (1 - e^{\frac{-qV_D}{k_B T}}); \text{ when } V_G < V_t \\ I_{sub-V_t}(1 - e^{\frac{-qV_D}{k_B T}}) + \mu C_{ox} \frac{1}{L}((V_G - V_t)V_D - \frac{1}{2}V_D^2); \text{ when } V_G - V_t > V_D \\ I_{sub-V_t}(1 - e^{\frac{-qV_D}{k_B T}}) + \mu C_{ox} \frac{1}{2L}(V_G - V_t)^2; \text{ when } V_G - V_t < V_D \end{cases}$$

Body factor $m = 1 + \frac{C_D}{C_{ox}}$, where $C_D = \frac{\epsilon_\circ \epsilon_{Si}}{W}$ (depletion capacitance).

Velocity saturated MOSFET: $I_{D,sat} = \mu C_{ox} W v_{sat}(V_G - V_t)$; where v_{sat} is the saturation velocity of the carriers.

On-state current at a given power supply voltage V_{DD}, $I_{ON} = I_D(V_{GS} = V_{DS} = V_{DD})$
Off-state leakage current at a given power supply voltage V_{DD}, $I_{OFF} = I_D(V_{GS} = 0, V_{DS} = V_{DD})$

Inverter:

$$\text{Middle voltage } V_M = \frac{\sqrt{\frac{\beta_p}{\beta_n}}(V_{DD} - |V_{tp}|) + V_{tn}}{1 + \sqrt{\frac{\beta_p}{\beta_n}}}$$

where β_i=$\mu_i C_{ox}(\frac{W_i}{L_i})$, $i \equiv p, n$. μ_i=mobility, W_i=i-type MOSFET width; L_i=i-type MOSFET gate length. MOSFET effective resistance $R_t = \frac{10V_B + 3V_t}{6\beta V_B^2} = \frac{10V_{DD} - 7V_t}{6\beta(V_{DD} - V_t)^2}$
where $V_B = V_{DD} - V_t$; β=$\mu C_{ox}(\frac{W}{L})$. μ=mobility, W= MOSFET width; L= MOSFET gate length.

Inverter delay is proportional to $R_t C_L$. $C_L = C_{g,p} + C_{g,n}$ where $C_{g,i}$=gate capacitance of i-type MOSFET = $\epsilon_\circ \epsilon_{ox} W_i L_i / t_{ox}$, $i \equiv p, n$.

Power dissipation due to charging and discharging = $C_L V_{DD}^2 f$; f being the frequency.

Resistance of a wire $R = \rho \frac{\text{Length}}{\text{Area}}$; ρ being the resistivity.
Capacitance of a parallel plate capacitor $C = \frac{\epsilon_\circ \epsilon_{ox} \text{Area}}{\text{Thickness}}$.

Elmore delay $\delta_E = \sum_{1 \le i \le n} c_i \sum_{1 \le j \le i} r_j$, c_i and r_j being the capacitance and the resistance of i-th and j-th section respectively.
If all the segments have the same resistance and capacitance $\delta_E = n(n+1)rc/2$, n being the number of segments.

Chip junction temperature $T = T_A + P R_{thermal}$, T_A, P and $R_{thermal}$ being the ambient temperature, power and thermal resistance, respectively.
Thermal time constant $\tau_{thermal} = R_{thermal} C_{thermal}$, $C_{thermal}$ being the thermal capacitance.