VLSI & Advanced Digital Design

Project 2

Problem 1: Inverter Layout

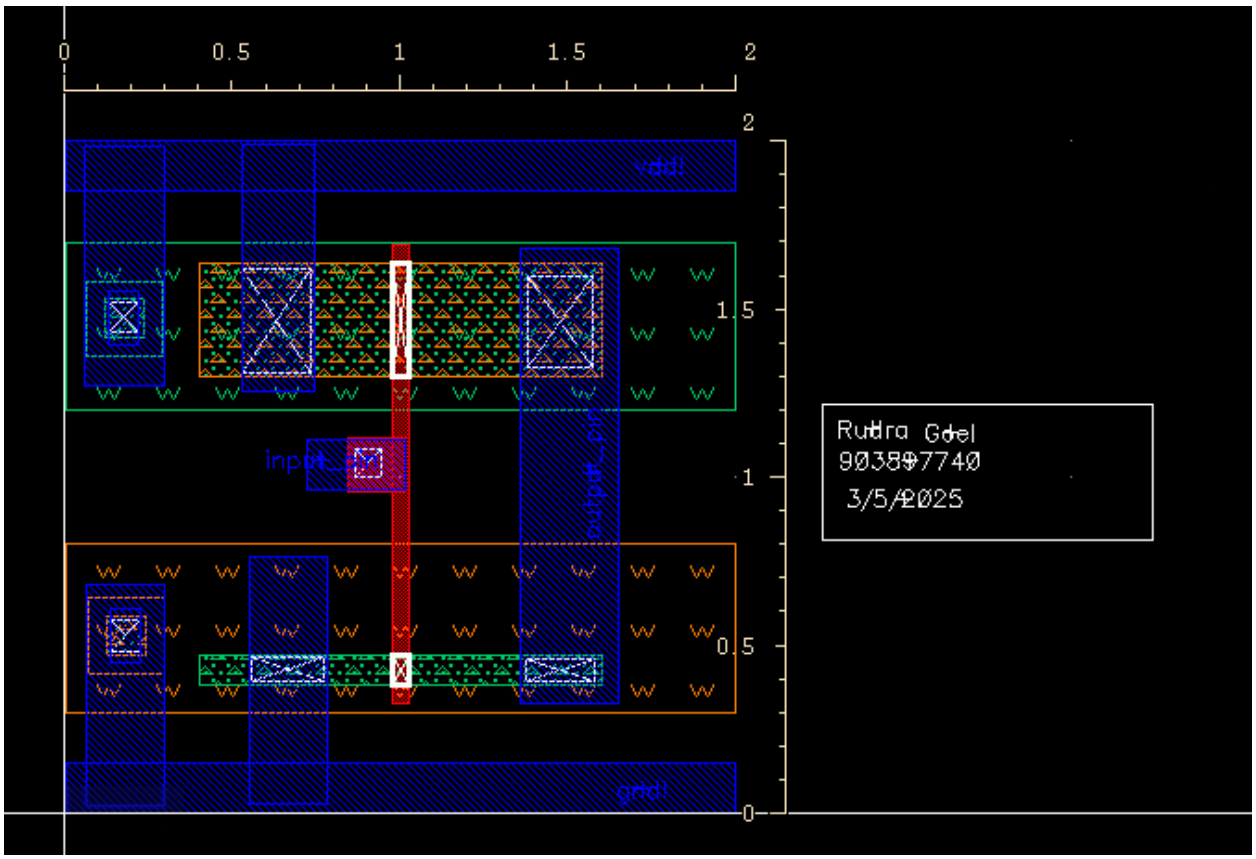

Figure 1. Inverter Layout With Height and Width of 2µm

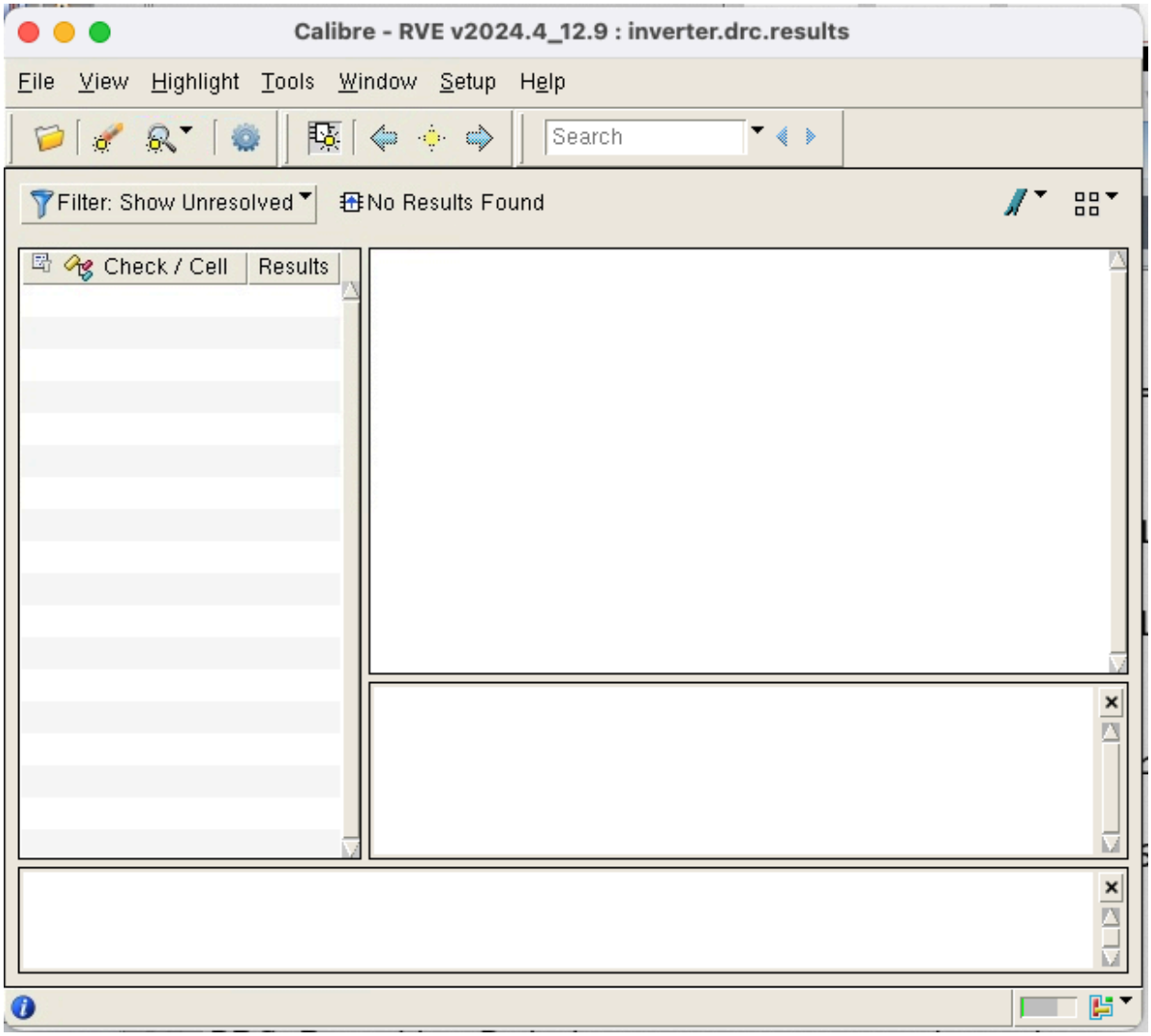

Figure 2. Inverter Passes Design Rules Check (DRC) With No Errors

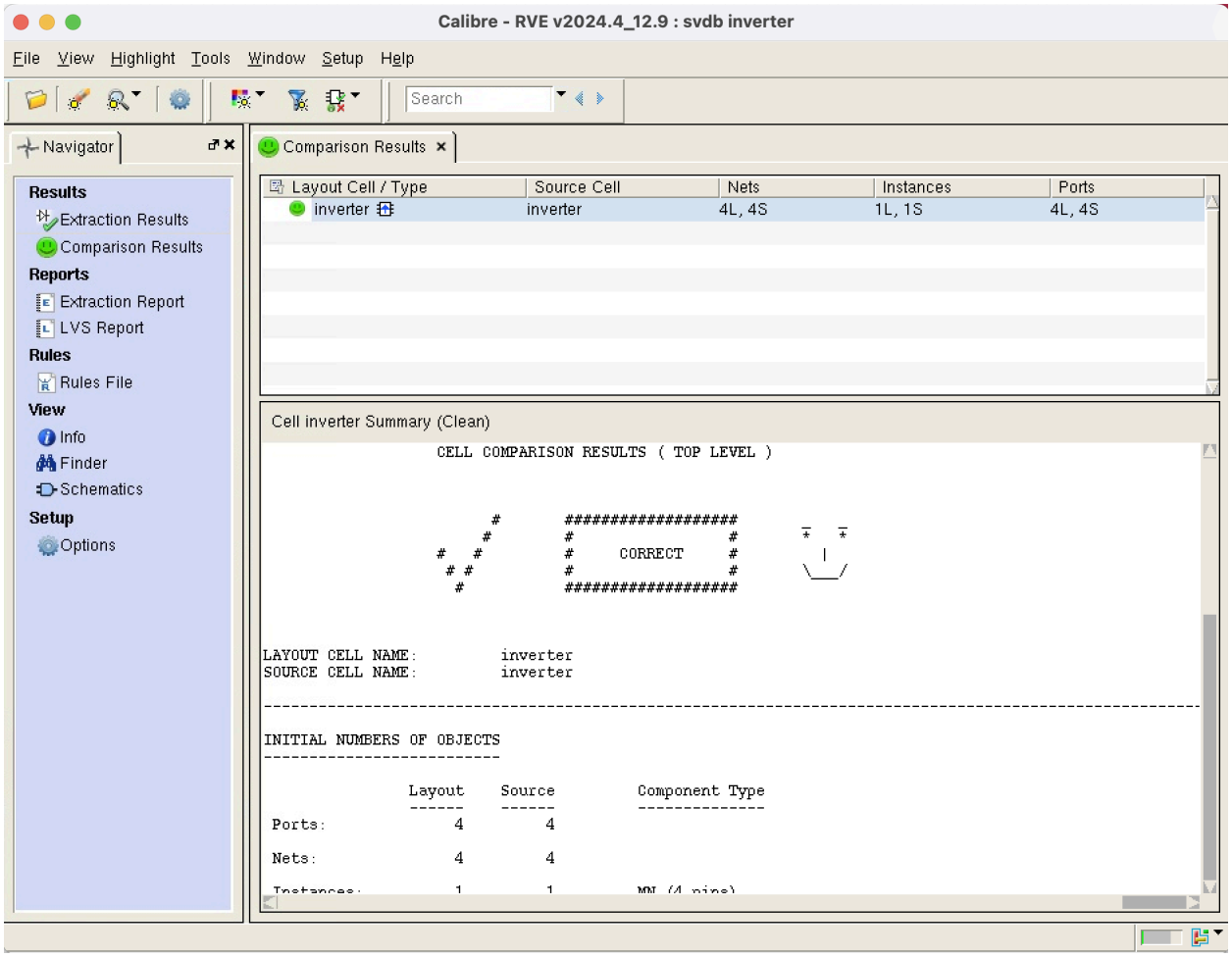

Figure 3. Inverter Passes Layout vs Schematic (LVC) with No Errors

Problem 2: NAND2 Layout

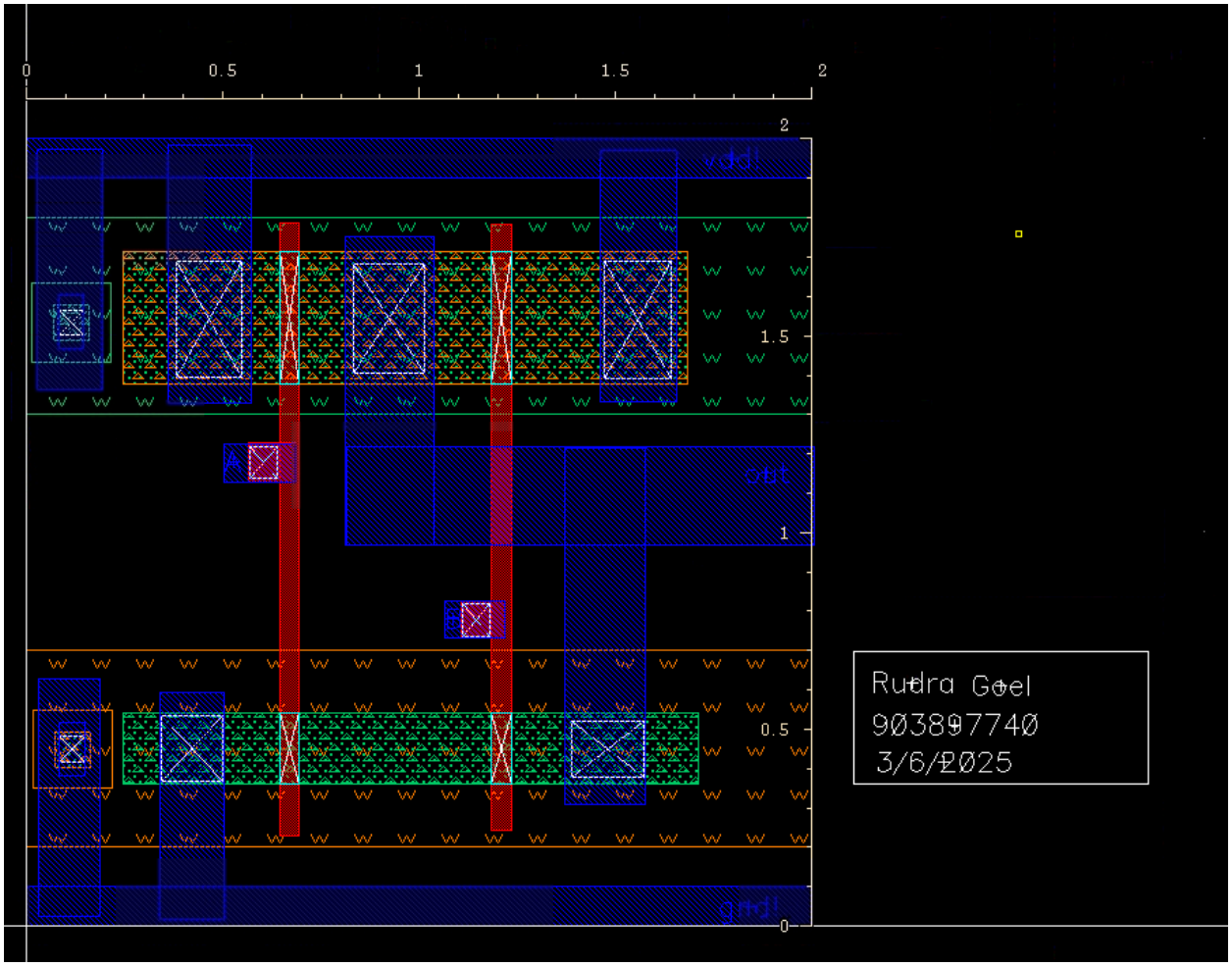

Figure 4. NAND2 Layout With Height and Width of 2µm

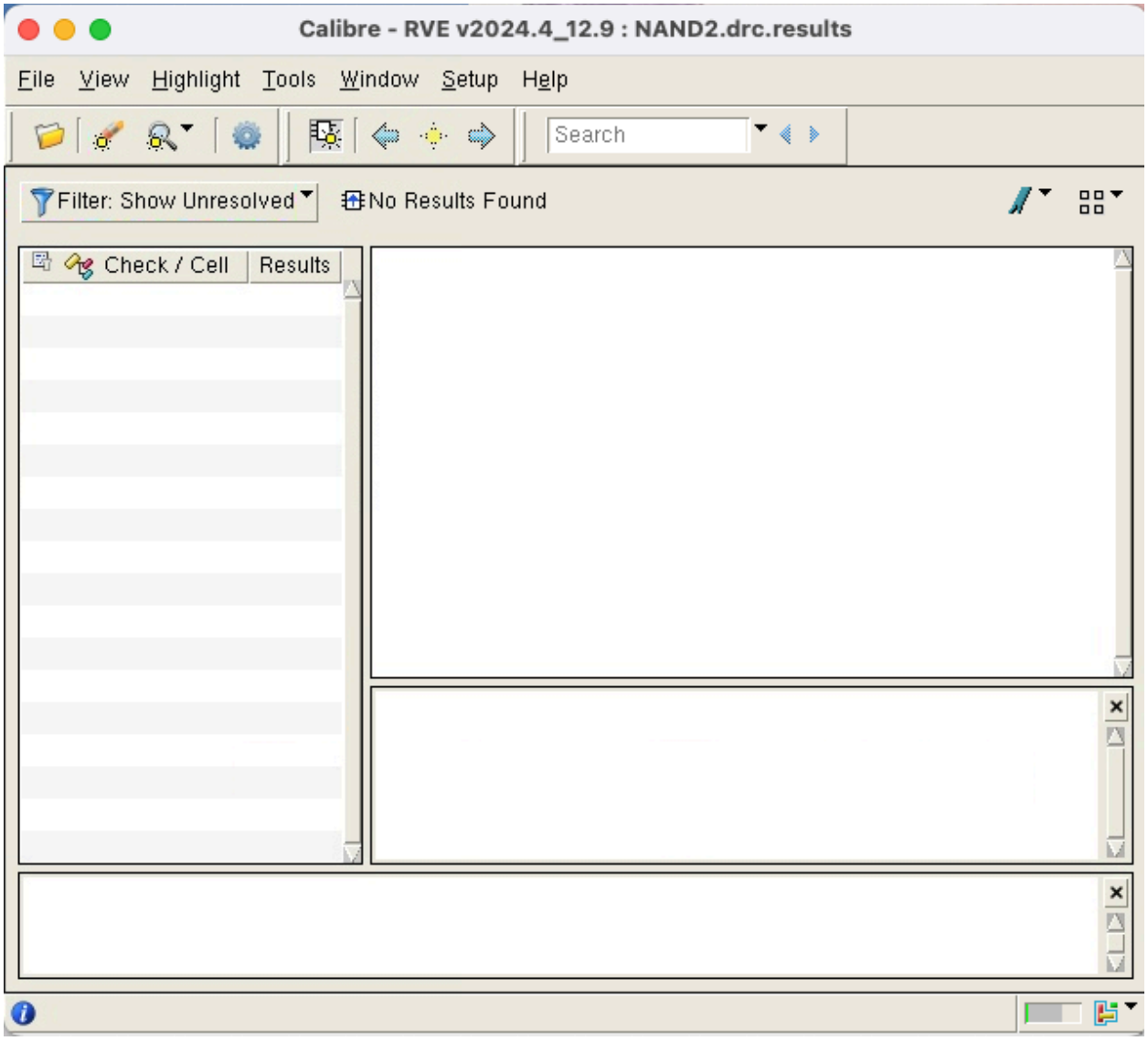

Figure 5. NAND2 Gate passing DRC With No Errors

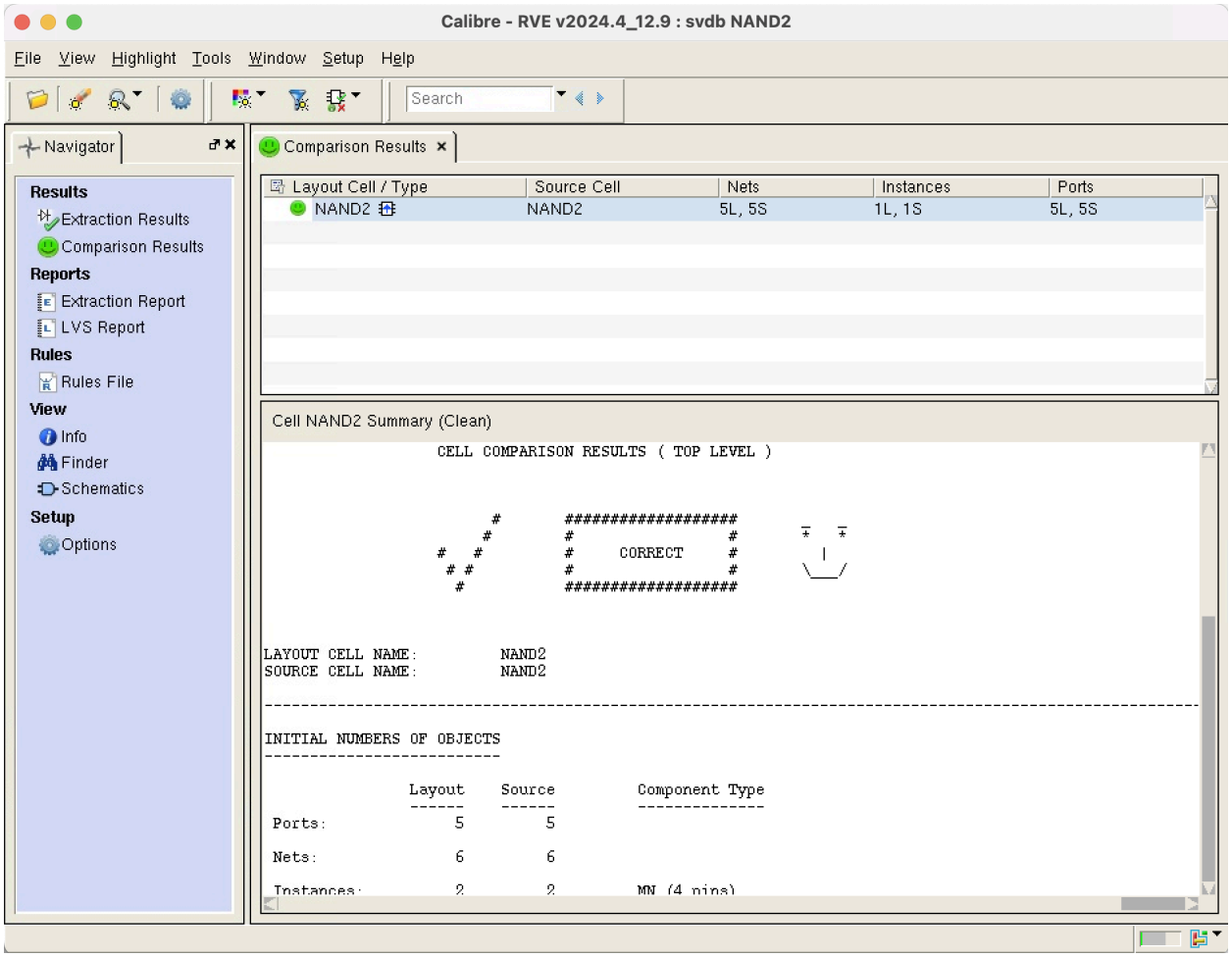

Figure 6. Inverter Passes Layout vs Schematic (LVC) with No Errors

Problem 3: XOR2 Layout

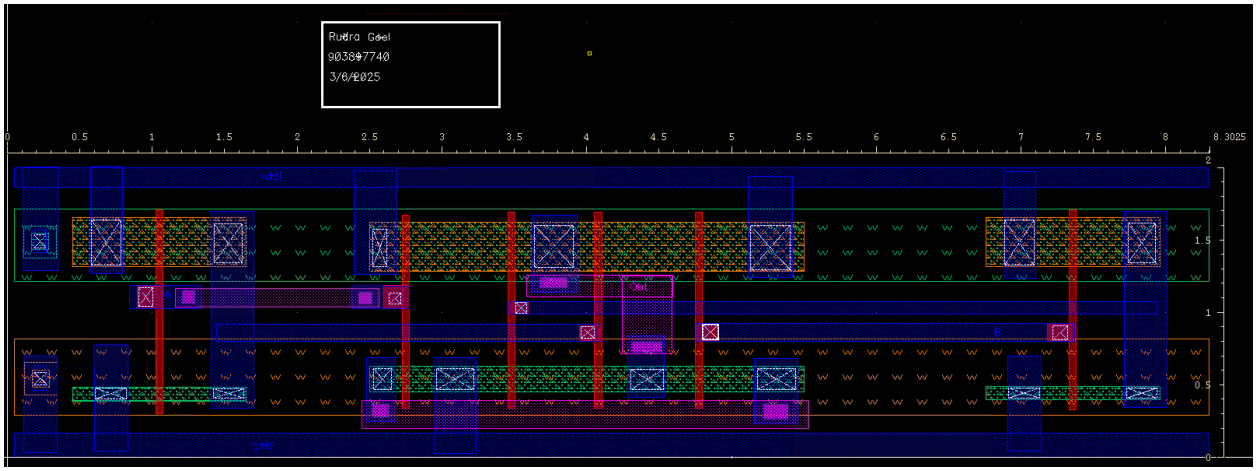

Figure 7. XOR2 Layout With Height of 2µm

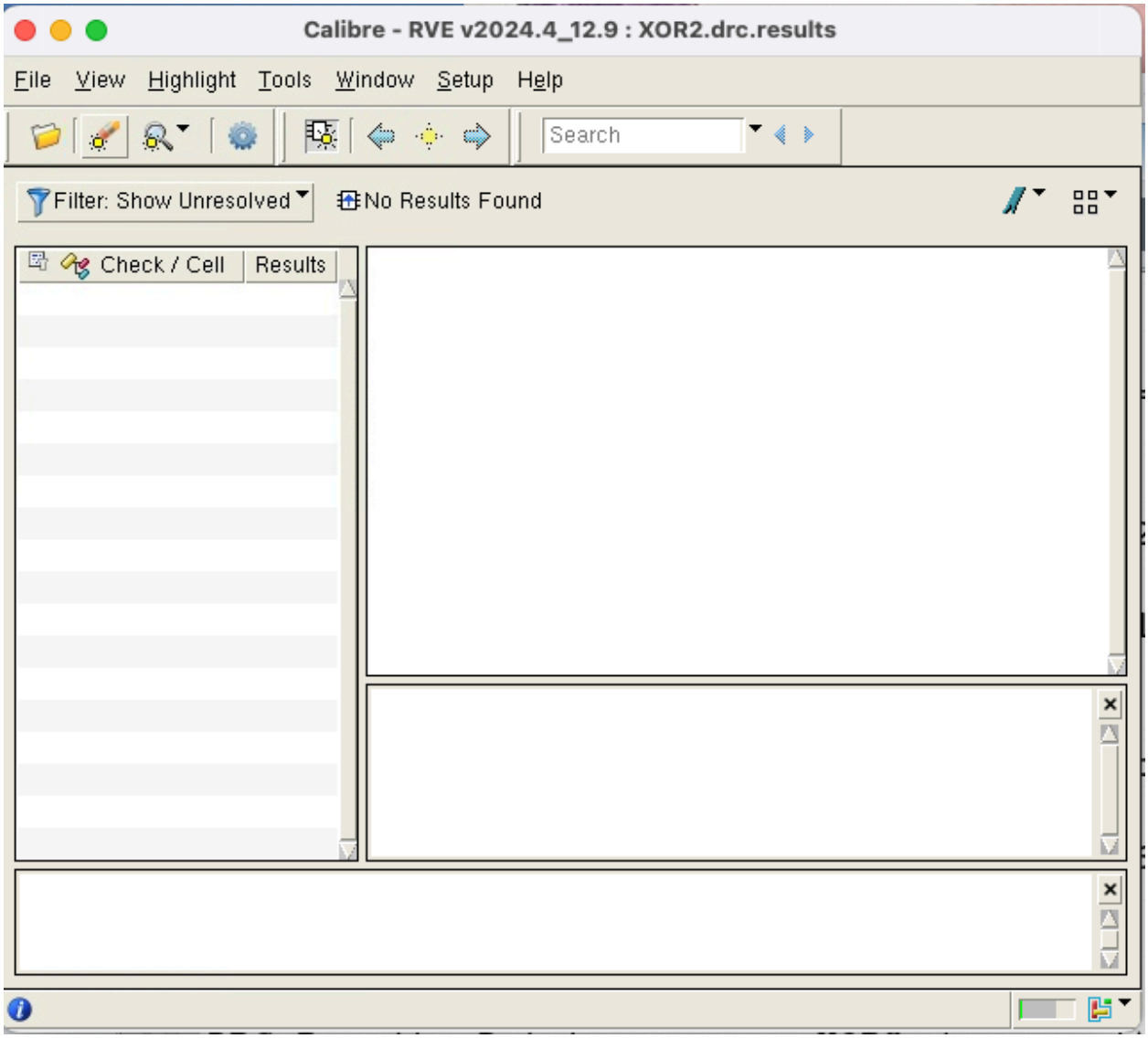

Figure 8. XOR2 Passes DRC With No Errors

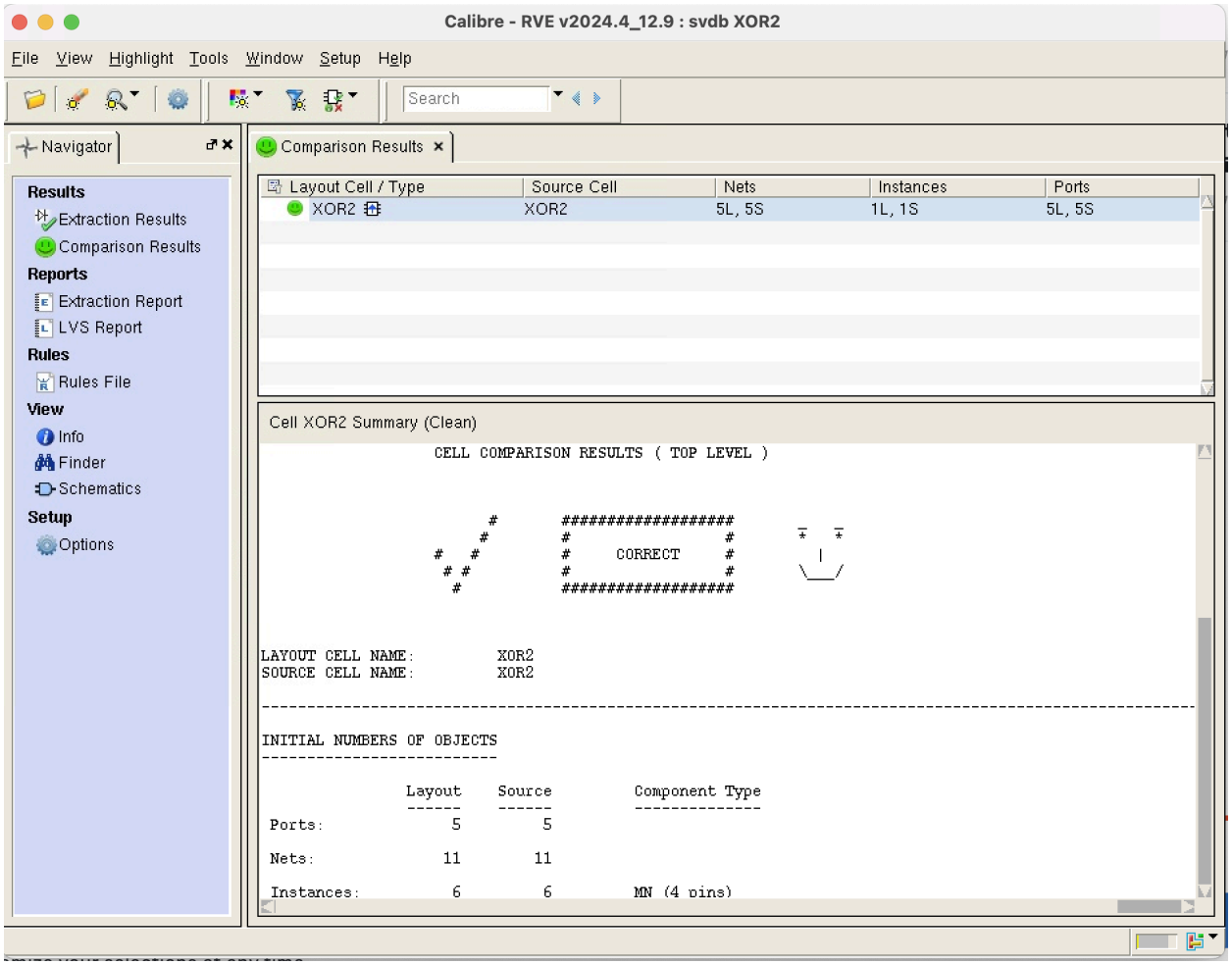

Figure 9. XOR2 Passes Layout vs Schematic (LVC) With No Errors

Problem 4: NAND2 Abutted with NOT Gate

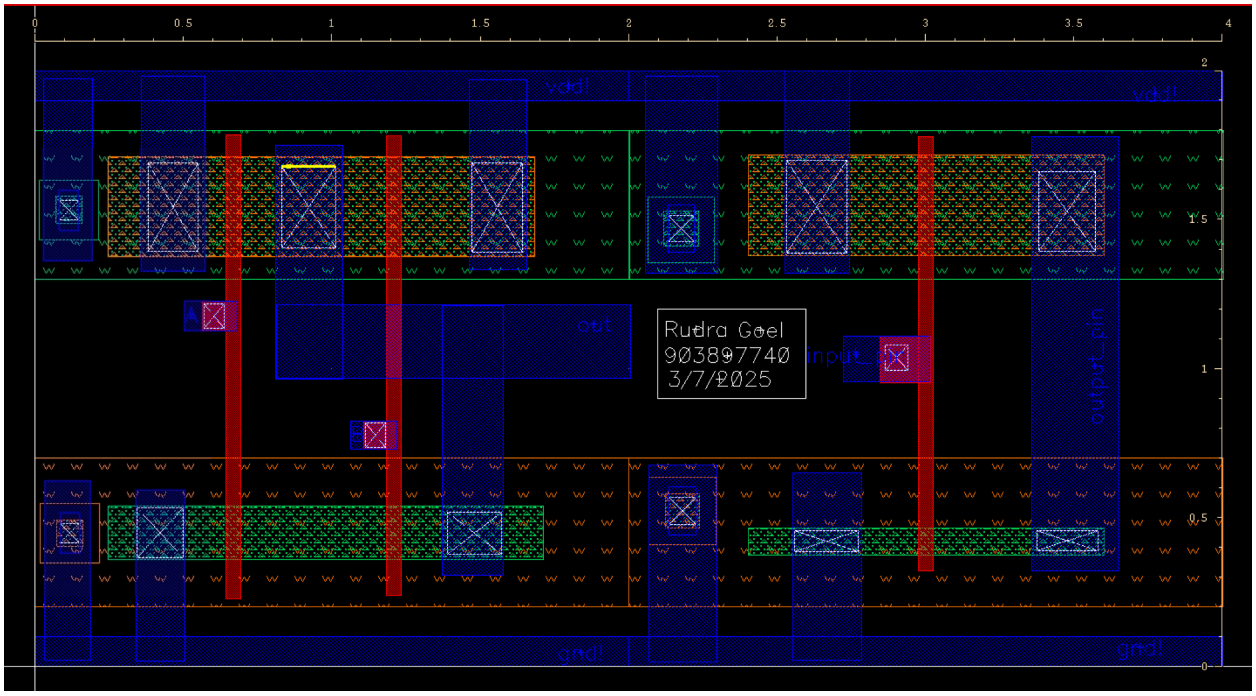

Figure 10. NAND2 Abutted With Inverter Layout

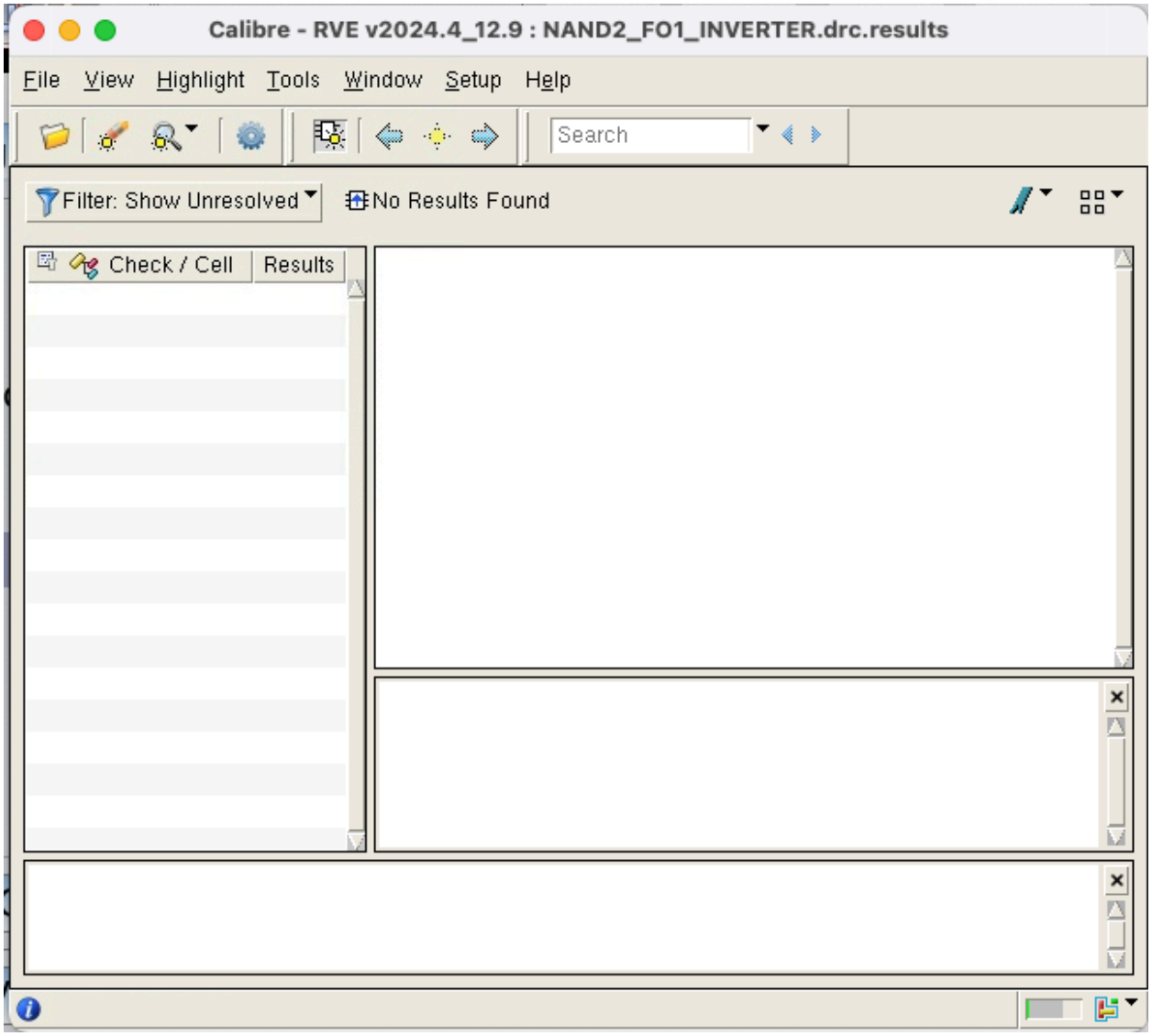

Figure 11. NAND2 With Inverter Passes DRC

For Project 2, I dedicated approximately five hours to complete this project. During the LVS (Layout Versus Schematic) verification stage, I encountered some significant challenges related to syntax errors between the schematics and the layout. Specifically, I named the width of the PMOS to be “337.5 nnM” instead of “337.5 nM” which could not resolve during LVS. This issue was frustrating since there was no apparent error message in the Calibre window; the error message was only present in the Virtuoso Studio Log window. Despite these hurdles, I found the project to be an enjoyable learning experience.