ECE3030_Hw1

Tuesday, January 28, 2025 9:31 AM

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ECE 3030: Physical Foundations of Computer Engineering
Spring 2025
Homework 1—Total points 200
Due on Thursday 1/30/2025 at 11.59am.

Q1 The following figure shows how the microprocessor clock frequency evolved over the last four decades. Note that clock frequency stopped increasing after 2005. Explain why. [40 pts]

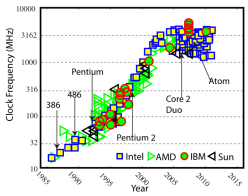
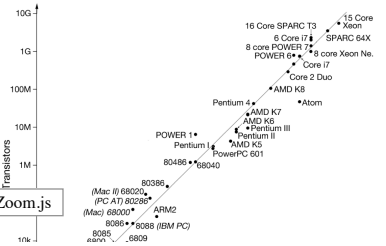


Figure 1: Ref: Andrew Danowitz et al. CPU DB: recording microprocessor history. In: Communications of the ACM 55.4 (2012), pp. 55-63.

From ACM 55.4 CPU DB: Recording microprocessor history. Processor frequencies have stagnated since ~2005 because it is more efficient to design machines to do more work per pipeline stage, rather than reduce the length of each stage by reducing the clock period despite improved gate design & transistor technology. "short-tick" machines consume more energy and it is advantageous to pipeline more instructions in one stage rather than increase fo for faster, more energy consumed, 1 processes.

Q2 The Moore's law is an observation that the number of transistors per square area of a state-of-the-art microprocessor chip doubles approximately every two years. This has remained valid since early 1970s till now. How is that achieved while the size of the chip has remained almost the same? Why is it advantageous? [30 pts]



→ Transistor technology has improved dramatically owing the size of the FET's transistor to reduce. with the transition from MOSFETs (~15nm) to FinFET technology (< 5nm), the number of transistors which a processor can increase while still retaining the overall chip size.

→ By reducing the size of the transistors, the operating voltage for the FETs also decrease. with lower voltages to enable operating states, the overall energy consumption also decreases.

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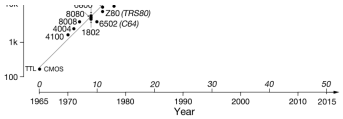


Figure 2: Ref: https://www.elektormagazine.com/articles/moores-law

Q3 What is the largest transistor count in a microprocessor? [Apple A14 Bionic chipset in iPhone 12 has ∼11.8 billion transistors. There are other chips with higher transistor counts.] [30 pts]

-> as of June 2023, highest is in Apples M2 Ultra SoC ~ 134 billion transistors (Microprocessor)

-> Micron NAND-V Flash Memory containing 5.3 trillion transistors

Q4 Figure 3 shows the cross-section of an Intel Broadwell chip (2014). Clearly identify different classes materials in this cross-section. How many layers of metal are there in this chip as visible in this cross-sectional image? [20 pts]

13 layers

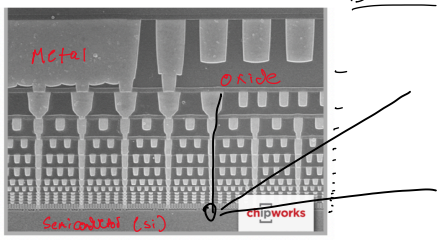


Figure 3: Image source: Extremetech

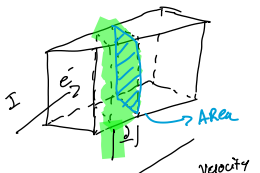
Q5 Starting with the Ohm's law derive the equation $v = \mu E$. All variables carry their usual meanings. Explicitly state the meaning of all variables used in the derivation. [20 pts]

Q6 Show that $\sigma = \frac{n\tau q^2}{m}$. All variables carry their usual meanings. Explicitly state the meaning of all variables used in the derivation. [20 pts]

Q7 The mobility and carrier density of Al are 1.2×10^{-3} m^2/Vs and 1.98×10^{29} m^{-3}, respectively. The mobility and carrier density of Cu are 4.32×10^{-3} m^2/Vs and 8.5×10^{29} m^{-3}, respectively. Which one would you use as interconnects in advanced CMOS nodes? [20 pts]

Q5) Given that $\vec{E} = \frac{\Delta V}{\Delta l}$

We can say $\Delta V = \vec{E}\,\Delta l$



$I = q\,A\,V_e\,n$ ↳ carrier Density

$\vec{J} = \frac{I}{A}$ (current Density

$\vec{J} \Rightarrow q\,V_e\,n$ ⟶ Charge Carrier Density

$V = IR$ (Ohms law

$\Rightarrow \Delta l\,\vec{E} = IR$

$\Delta l\,\vec{E} = (q\,V_e\,A\,n)(R)$

$V_e = \vec{E}\left(\frac{\Delta l}{nqAR}\right)$

μ = mobility of e^-

$\boxed{V_e = \mu\vec{E}}$

Q6) $\sum F = Ma = M\frac{dv}{dt} = q\vec{E} - \frac{M V_e}{\tau}$; M = mass of charge carrier, V_e = Drift velocity, τ = mean free time btw collisions

$V_e = \frac{q\tau E}{M} \Rightarrow \mu = \frac{q\tau}{M}$ ↳ Mobility of e^-

$\vec{J} = nqV_e$ where $\vec{J}$ is current Density

$\vec{J} = nq\left(\frac{q\tau}{m}\right)\vec{E}$

$\vec{J} = \sigma\vec{E}$ also $\Rightarrow \boxed{\sigma = \frac{nq^2\tau}{m}}$

Q7) $J_{Al} = (1.98\times10^{29})\,q\,(1.2\times10^{-3})\,\vec{E} = (2.376\times10^{26})(q\vec{E})$

$J_{Cu} = (8.5\times10^{29})\,q\,(4.32\times10^{-3})\,\vec{E} = (36.72\times10^{26})(q\vec{E})$

The current Density for $J_{Cu} >> J_{Al}$, with upwards of 15x. The Drift velocity (μE) is 3.6 times higher implying Faster Speeds for copper [illegible] when switching transistors & CMOS Networks:

Q8 Say you doped a wafer of pure (intrinsic) Si with P (doping density=10^{23} m^{-3}). Now the wafer has a lot more free electrons than it had before. Do you expect the piece of Si wafer to be charge neutral? Why or why not? Will your answer change had you doped it with Al? [20 pts]

→ Despite the # of free electrons inherently in the doped wafer of silicon, the dopant itself (P) is charge Neutral; Thus the Doped Si Remains charge Neutral. The answer is same for Al even though this dopant has more carriers, Al is Neutral => Si Doped w/ Al is Neutral net.