1. Reason 1: PMOSFET and NMOSFET should have the same rise and fall time, which is based on the effective resistance. The effective resistances are proportional to μ*W/L. Since $\mu_n > \mu_p$ (mobility of electrons is greater than holes), the width of PMOSFET would have to be greater than the width of NMOSFET to have the same rise and fall time.
   Reason 2: When the input is 0, the PMOSFET is connected from source to drain. A wider structure allows the PMOSFET to carry more current and have a higher pull-up strength.
2. Set WL2 to high, read data from BL1, BL2, BL3…, set WL2 to low, then set WL2 to high and write the data back into the cells.
3.
   3.1. delay is proportional to R_t
   $R_t = (10(V_{DD}-V_t) + 3V_t) / (6\beta(V_{DD}-V_t)^2)$
   delay $\propto V_{DD} / V_{DD}^2 \propto 1 / V_{DD}$
   As V_{DD} increases, the delay decreases

   $P_{active} = C_L V_{DD} f$
   As V_{DD} increases, P_{active} also increases

   3.2. delay is proportional to R_t
   $R_t = (10(V_{DD}-V_t) + 3V_t) / (6\beta(V_{DD}-V_t)^2)$
   delay $\propto 1 / (1 - V_t)^2$
   $V_t \propto$ doping density
   When doping density increases, V_t also increases, which means delay increases

   $P_{active} = E * f = (q^2 N^2 x^2) / 6\varepsilon_o * f$
   When doping density increases, P_{active} also increases

   3.3. To increase noise margin, the V_t has to increase
   $V_t \propto$ doping density
   If doping density increases, V_t would increase, which means noise margin would also increase
4. Fanout is the number of logic inputs that a logic output can drive.
   Reason 1: NMOSFETs have a natural advantage as pull-down devices, while PMOSFETs have a disadvantage as pull-up devices. Making the PMOSFET with a higher fanout will allow it to have similar strength for pull as an NMOSFET.
   Reason 2: To decrease the leakage current from V_{DD} to GND, making the PMOSFET will increase the equivalent resistance, which decreases the leakage current when the device is static.