

VLSI & Advanced Digital Design

Project 1 Part A

Problem 1: Inverter Design

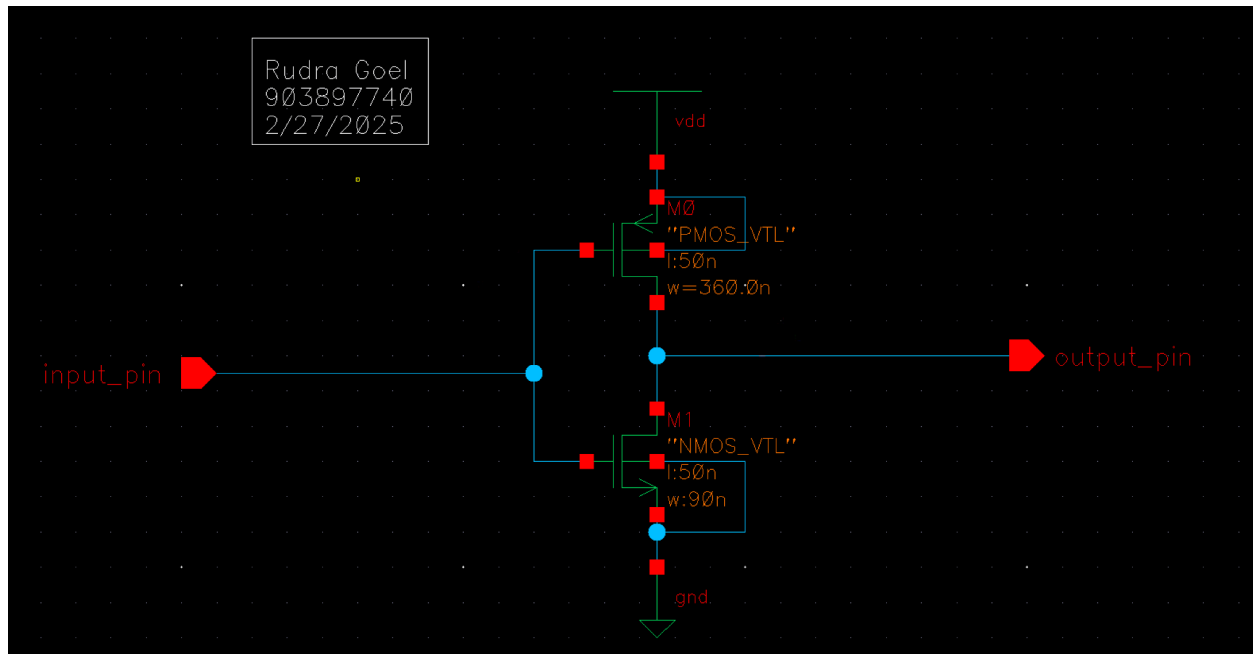


Figure 1. Inverter Gate Level Schematic

Width necessary for inverter design:

PMOS: 360nm

NMOS: 90nm

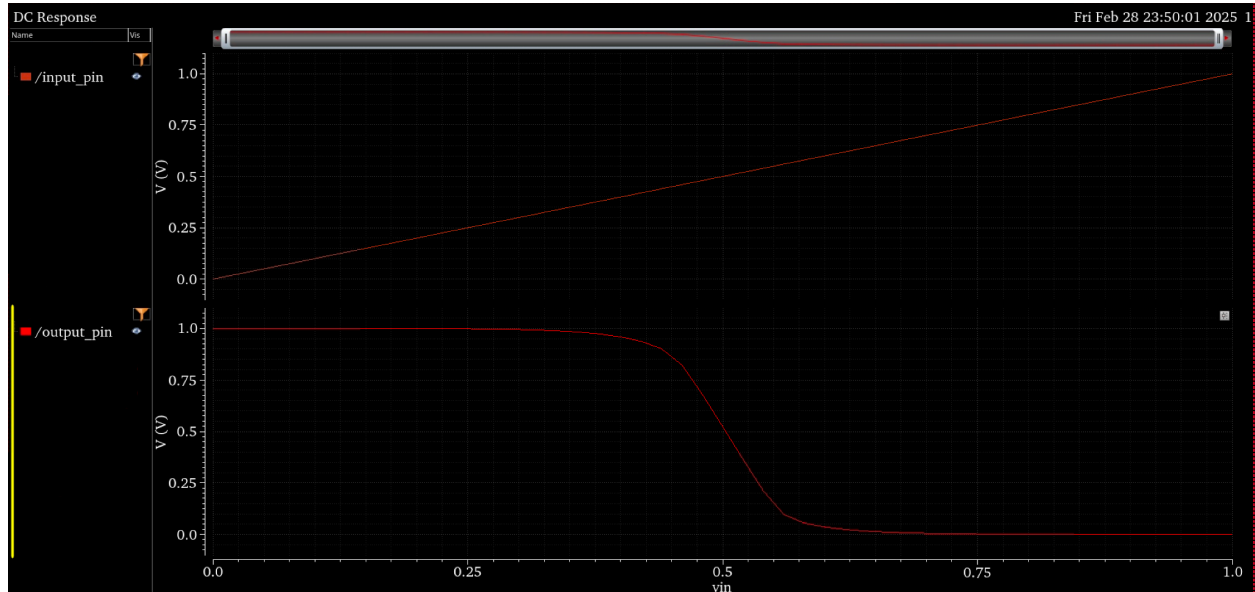


Figure 2. Inverter Voltage Transfer Characteristics

Having $V_{dd}/2$ is desirable as the inverter has noise properties that are symmetric; roughly the Noise Margin High (NMh) and Noise Margin Low (NML) are the the same so the inverter is not biased towards one specific pole.

Problem 2: Noise Parameters of Inverter

Noise Variables	
Vol	36.124 mV
Voh	941.75 mV
Vil	416.51 mV
Vih	599.62 mV
Nml	380.396 mV
Nmh	342.13 mV
Max Gain	7.85

Problem 3: Fanout Schematic & Transient Response

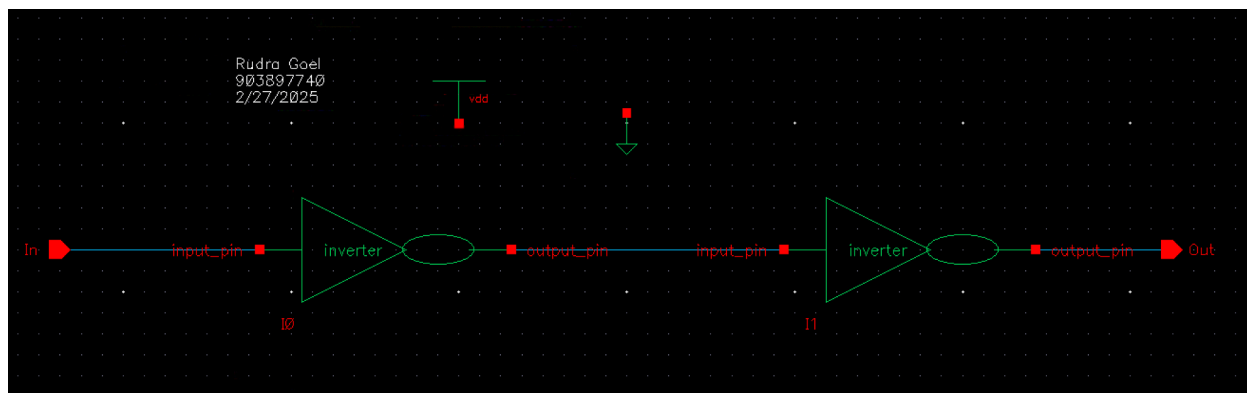


Figure 3. Inverter Fanout 1

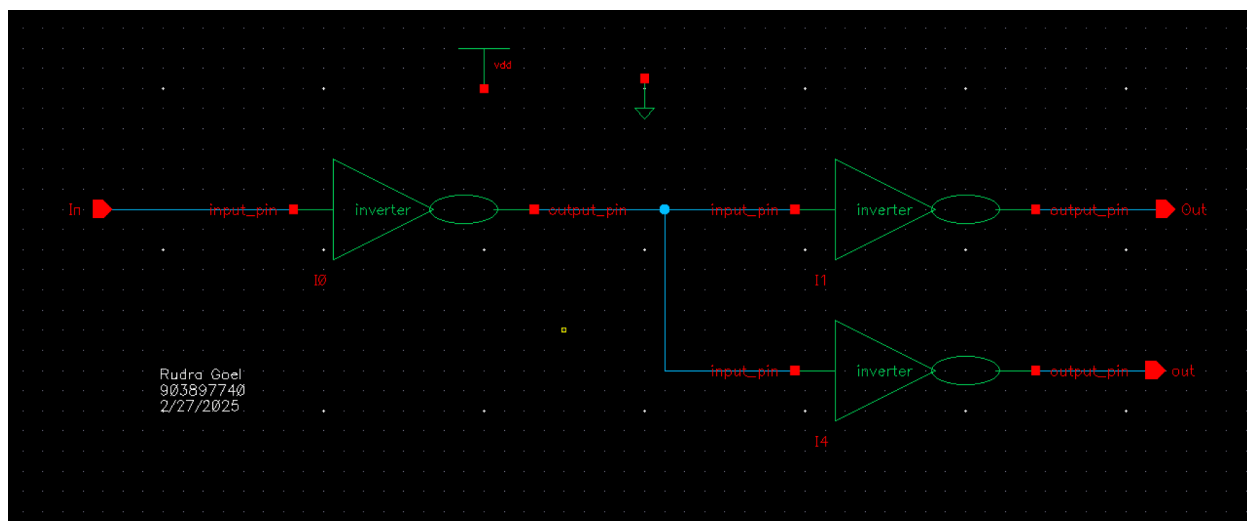


Figure 4. Inverter Fanout 2

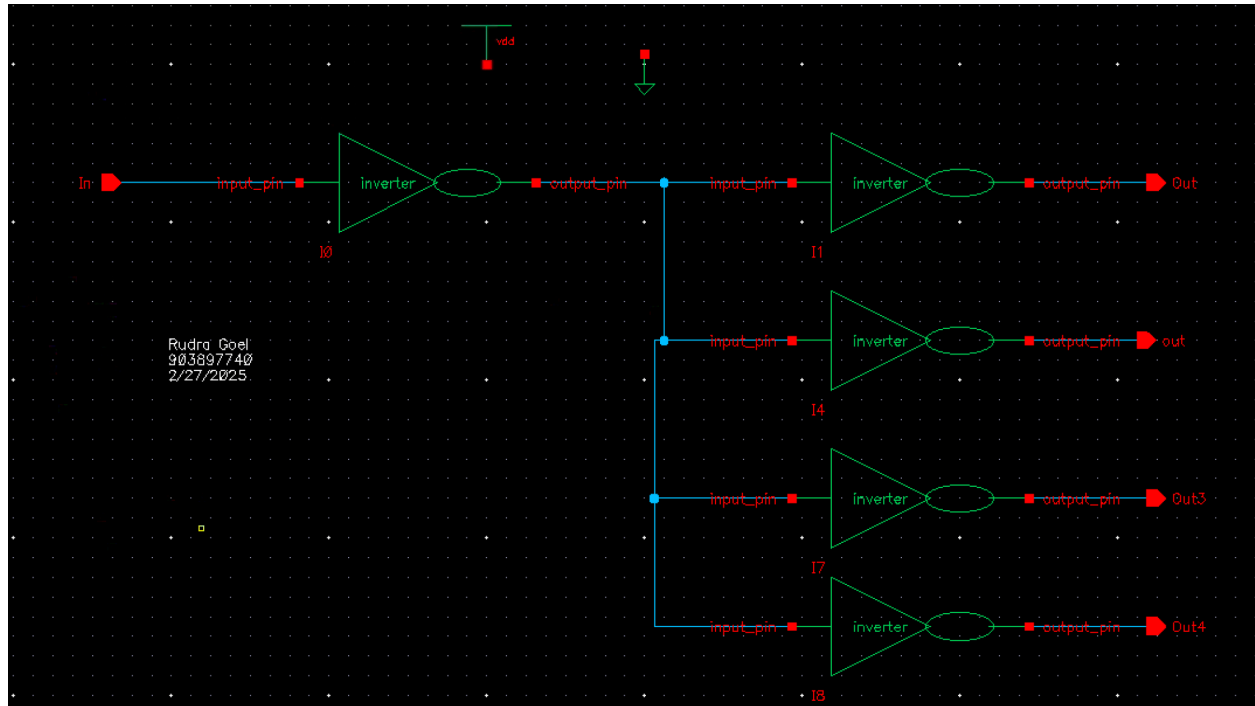


Figure 5. Inverter Fanout 4

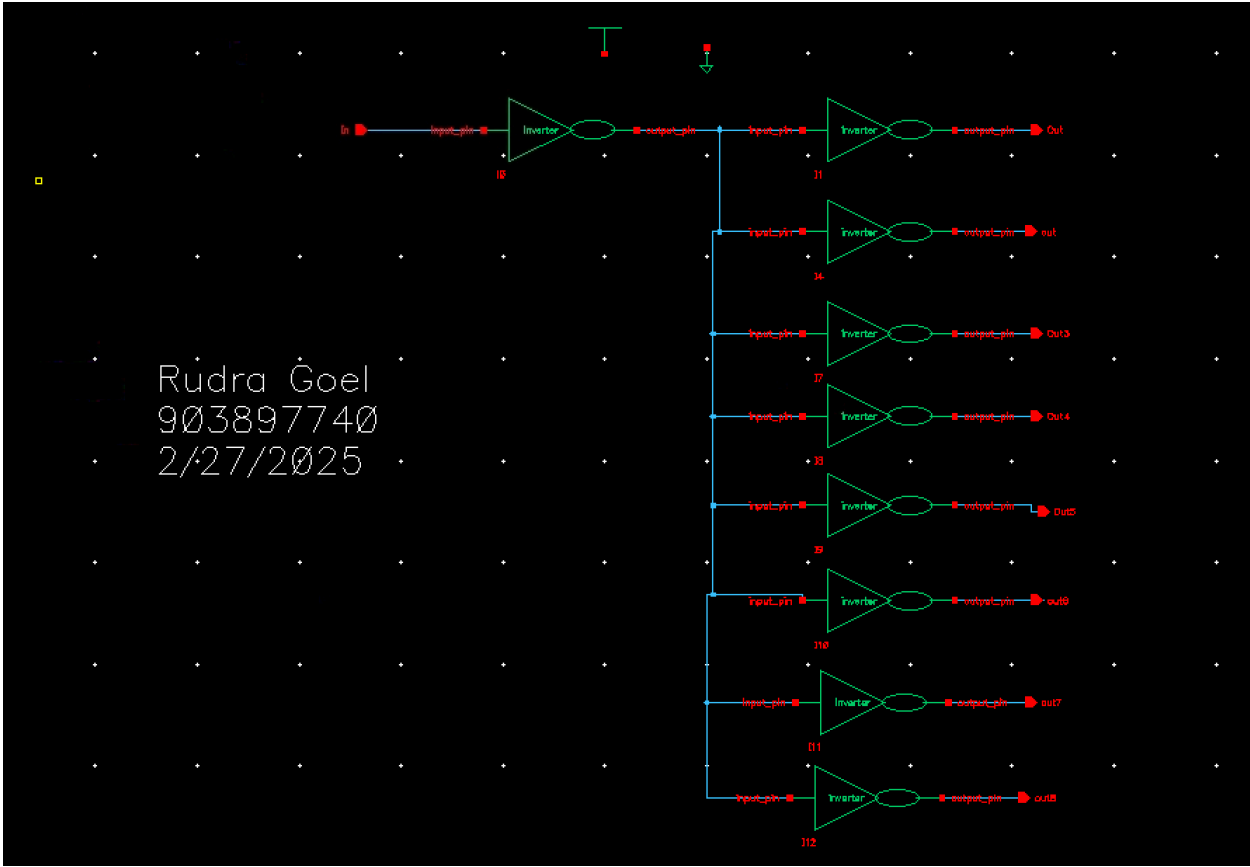


Figure 6. Inverter Fanout 8

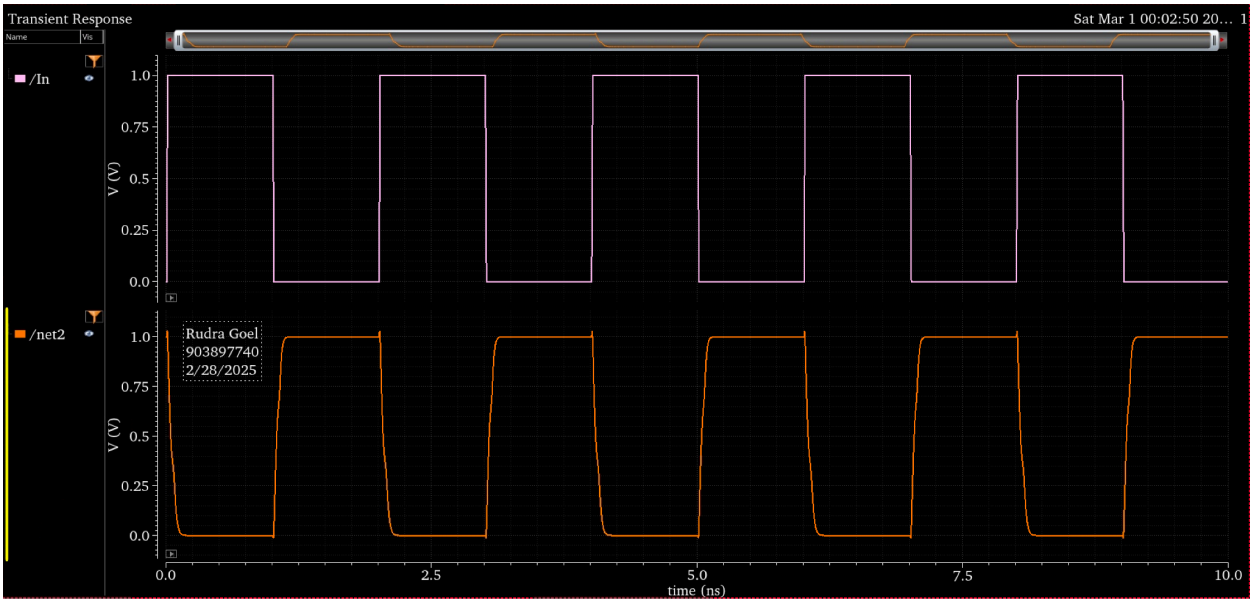


Figure 7. Transient Response of Fanout 8 Inverter Condition

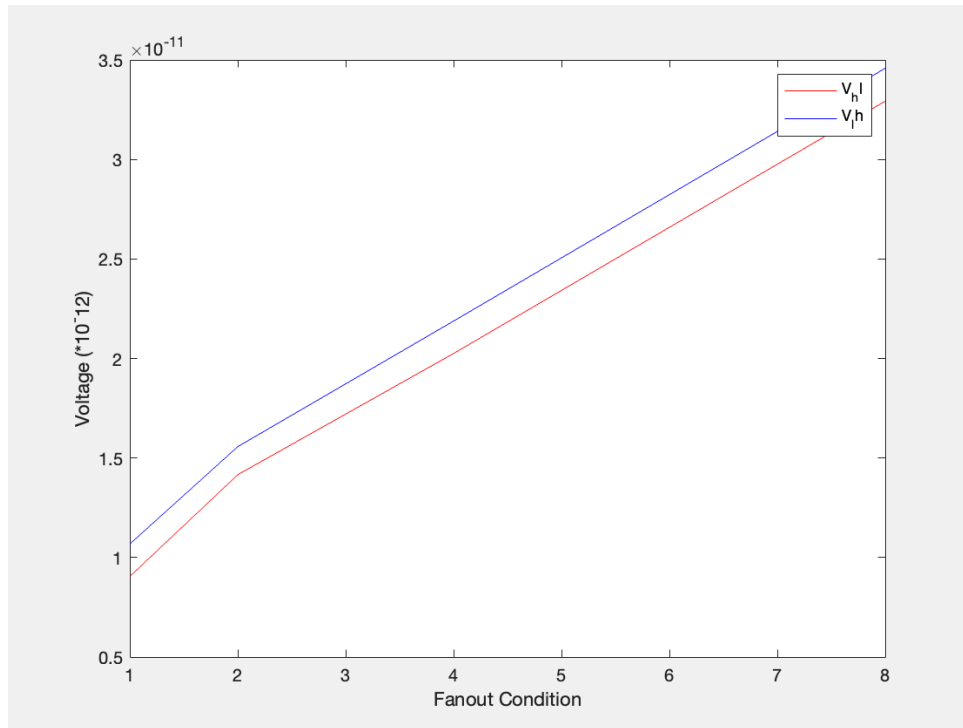


Figure 8. High-To-Low & Low-To-High Delays

Problem 4: Power Dissipation of Inverter at Various Frequencies

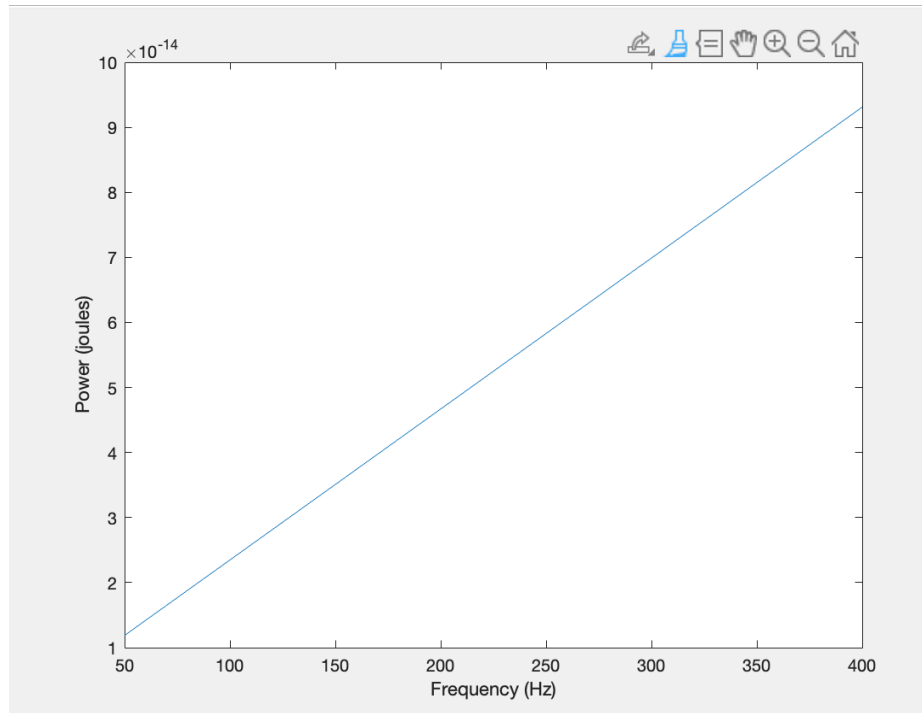
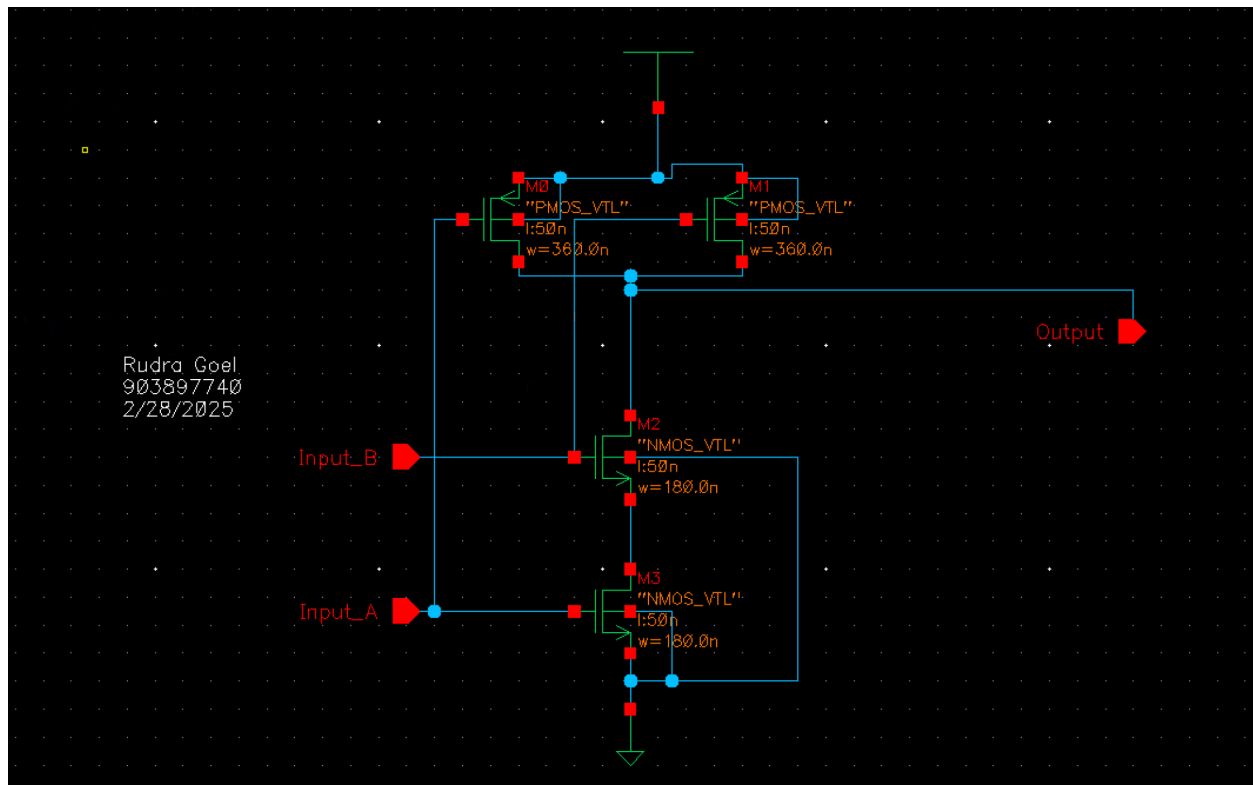


Figure 9. Power Dissipation for Different Frequencies

As the inputs of the gate operate at a higher and higher frequency, the power dissipated by the device increases linearly. This information can be further abstracted to how if you run any major computing device at a higher clock rate, your processor will consume more energy.

Problem 5: NAND2 Gate

**Figure 9.** NAND2 Gate Level Schematic

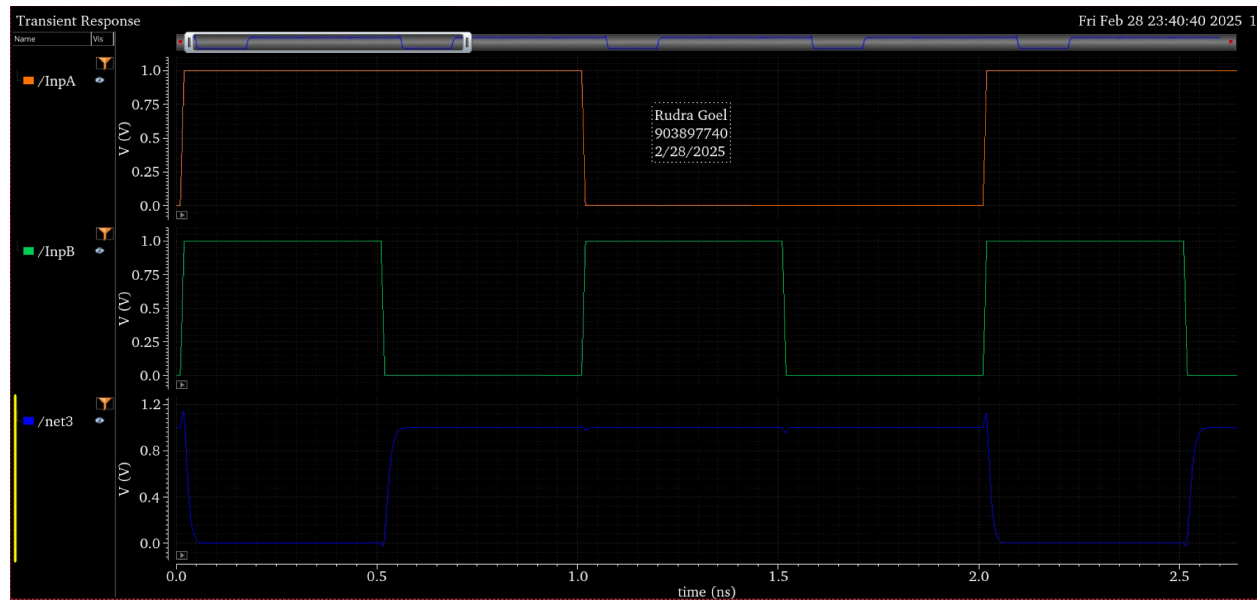


Figure 10. Transient Response of NAND2 Gate

The low to high delay (V_{LH}) is 13.8 ps

The high to low delay (V_{HL}) is 14.33ps

Problem 6: XOR2 Gate

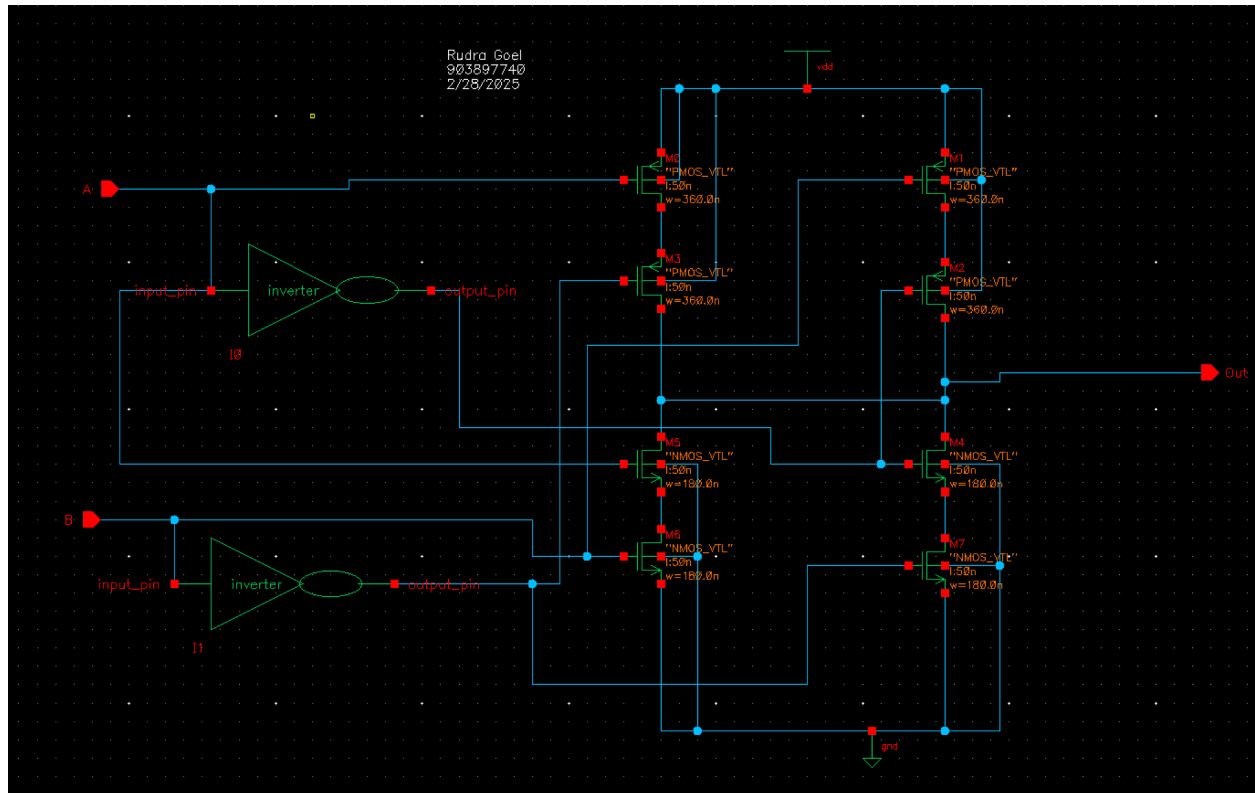


Figure 11. XOR2 Gate Level Schematic

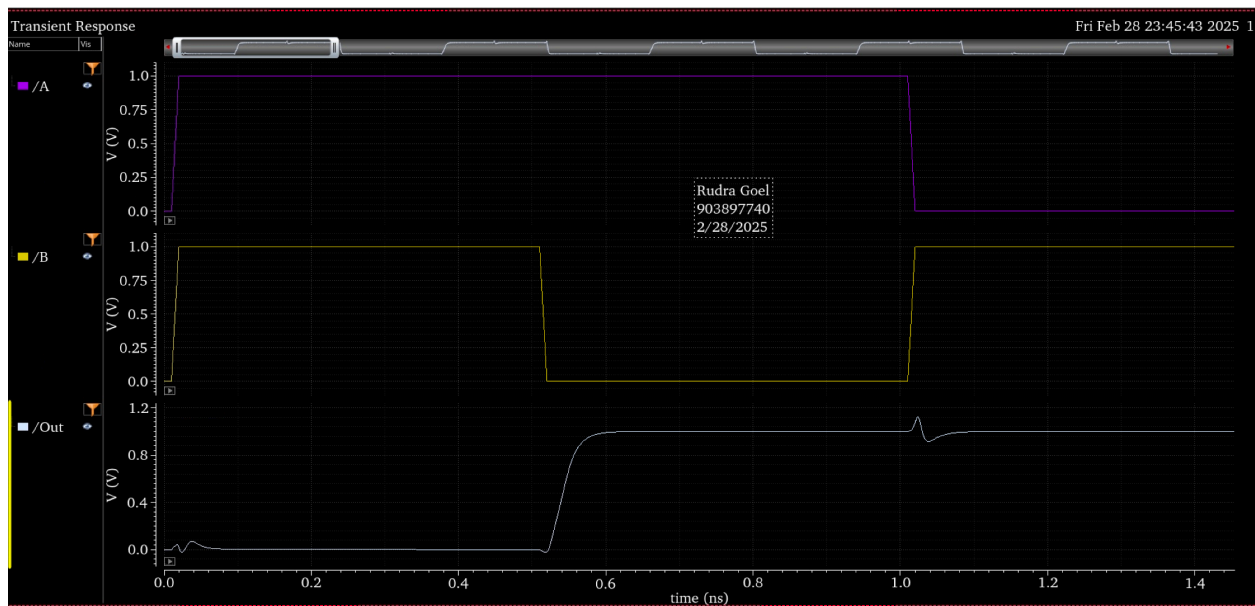


Figure 12. Transient Response of XOR2 Gate

The project took approximately 3 hours to complete. Challenges were encountered primarily with technical connectivity, specifically difficulties connecting to the GT VPN and repeatedly launching the Virtuoso software. Despite these hurdles, the project was enjoyable and engaging and I had a lot of fun doing it and learning the software.