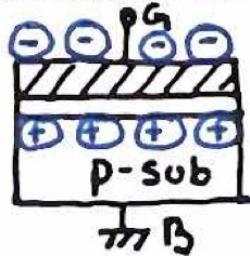


## MODULE 2 - PART B

### ELECTRICAL CHARACTERISTICS OF A MOSFET

In PART - A of Module 2 , we were looking at the MOS - Capacitor structure and we discussed the 3 regions of operation.

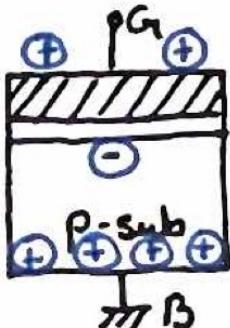
#### ① ACCUMULATION REGION →



Here, we applied a '-'ve voltage at the gate  $V_G < 0$  and as a result, '-'ve charges accumulated in

the G and consequently '+'ve charges accumulated on the surface of the Body. But since there is no continuity of charge , we have NO CURRENT .

#### ② DEPLETION REGION →



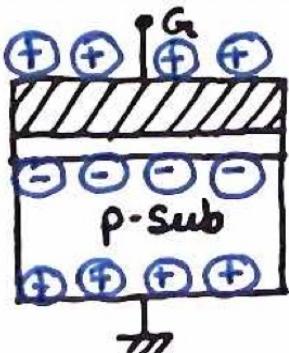
Here, we applied a small quantity of '+'ve voltage at the gate  $0 < V_G < V_t$  where,  $V_t$  is the threshold voltage of the transistor.

Now the '+'ve charges on the surface of the B are repelled and very little '-'ve charges are attracted (mostly ions) This small amount of '-'ve charge is not enough to sustain any significant CURRENT. We say all mobile charges have been DEPLETED in this region .

Very very little (insignificant) current flows in this region.

(Note:- The ionic charge is immobile and we will not consider this in our course)

### ③ INVERSION REGION →



Here, we applied a large quantity of '+ve voltage at the gate'  $V_G > V_t$

Hence, a lot of '+ve charges accumulated at the G and consequently, a lot of '-ve charges also accumulated at the surface of the Body or the p-substrate.

(Some of these will of course be the immobile ionic charges, but most of it will be mobile charges)

We had seen that CURRENT will flow in this region.

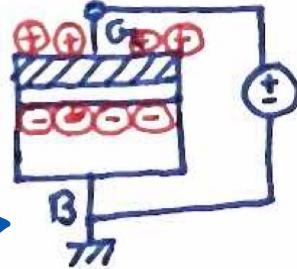
Now, we will see how we can take this MOS - capacitor and convert it to a MOSFET.

### MOS - CAPACITOR → MOSFET

- Here the charge characteristics will remain more or less the same
- Apart from the voltage we had applied to the gate,  $V_G$ , we

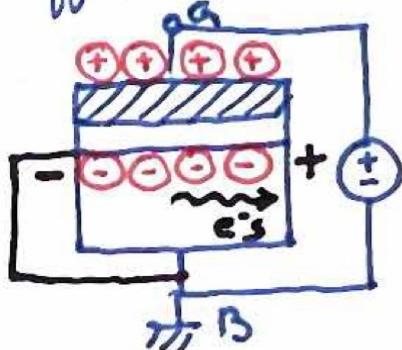
will also apply a LATERAL VOLTAGE

In the INVERSION region, we had '+ve charges on the G and '-ve charges on the surface of the B as shown here →



Now, we want to see, WHAT HAPPENS IF THE RIGHT SIDE IS MORE POSITIVE THAN THE LEFT?

So we want to set up a voltage difference in the lateral or x-dir<sup>n</sup>.



Since we want the right side to be more '+ve', e-'s will get

attracted to this side. Let us ground the '-ve left side i.e. connect it to the Body.

∴ We can say :-

①  $V_G \rightarrow$  is responsible for creating the inversion and bringing the e-'s to the surface (of the Body) and,

②  $V_{\text{lateral}} \rightarrow$  is responsible for moving the free electrons, in this case,

from left to right.

Now, in order to be able to apply this lateral, we cannot directly connect the voltage source to this lightly doped Body.

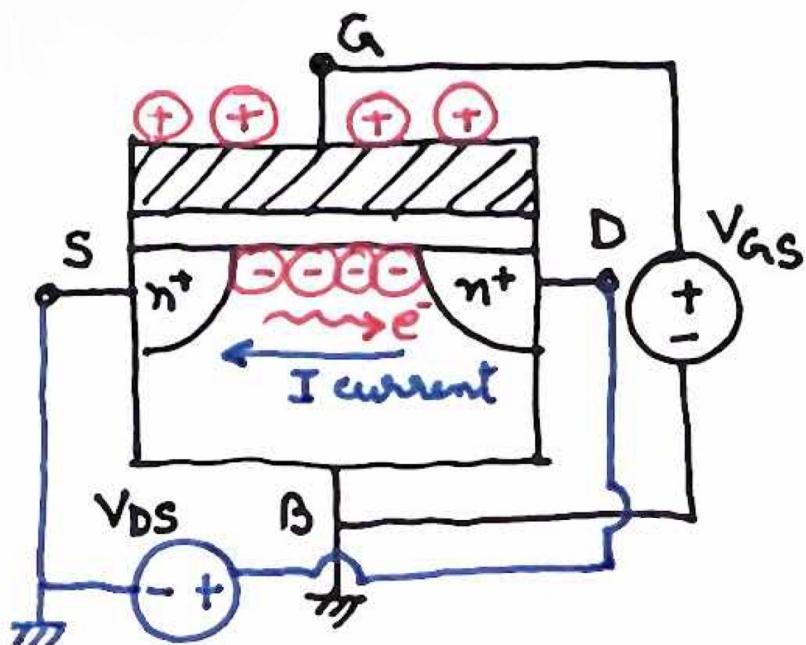
(since, then an additional barrier called the Schottky barrier will be formed.)

There is a separate device called Schottky diode based on this, but this is beyond the scope of this course)

We will therefore need a repository of e<sup>-</sup>s at both ends to supply & collect the e<sup>-</sup>s.

Hence, we have the heavily doped n<sup>+</sup> Source and n<sup>+</sup> Drain to the left & right respectively.

We apply the lateral voltage across these n<sup>+</sup> S & D. (Source and Drain)



This lateral voltage is thus known as the  $V_{DS}$  i.e. the Drain to Source voltage.

Also, since the S + the B are both grounded, the gate voltage can also be referred to the S and is known as  $V_{GS}$ .

$\therefore$  In this case, for the inversion region, we have the following conditions :-

$$\textcircled{1} \quad V_{GS} > 0$$

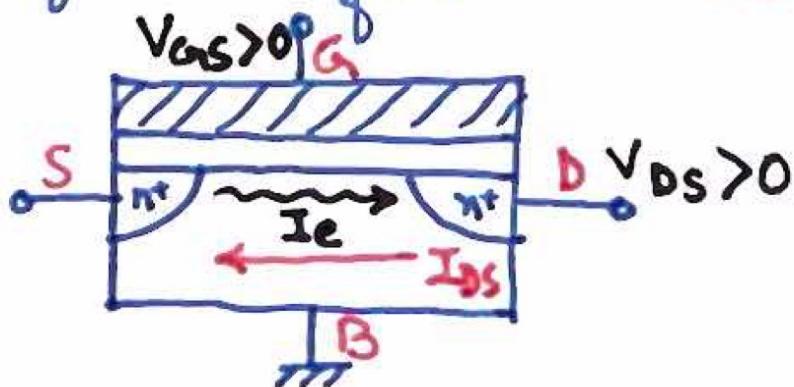
$$\textcircled{2} \quad V_{GS} > V_t$$

$$\textcircled{3} \quad V_{DS} > 0$$

∴ Intuitively speaking, what is happening is that we are applying a +ve  $V_{GS} > V_t$  to bring a lot of e<sup>-</sup>s to the surface of the Body and then we are applying a +ve  $V_{DS}$  to move these e<sup>-</sup>s + get a current in the channel.

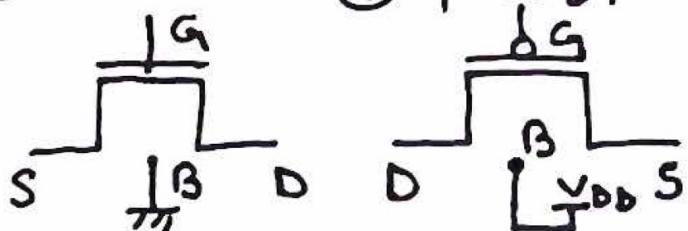
∴ We can say :-

- ① A positive GATE voltage  $V_{GS} > V_t$  creates an abundance of mobile e<sup>-</sup>s
- ② A positive voltage on the right side (D) allows e<sup>-</sup>s to move from left to right (S to D) and current to flow from right to left (D to S)  $I_{DS}$



There are 4 - terminals  
of this device :-

① nMOS :-    ② pMOS :-



We want the p-type Body  
of the nMOS to be connected  
to ground so that it does  
not conduct.

And we want the n-type  
Body of the pMOS to be  
connected to V<sub>DD</sub> so that it  
does not conduct.

∴ All typical designs  
require :-

$$\text{nMOS} : V_B = 0 \quad +$$

$$\text{pMOS} : V_B = V_{DD}$$

(V<sub>DD</sub> → supply)

So, in an

$$\text{nMOS} : V_B = V_S = 0$$

$$\text{pMOS} : V_B = V_S = V_{DD}$$

Also note that physically  
the D & the S are identical

In an :-

nMOS : the D is at a higher potential

than the Source

pMOS : the S is at a higher potential

than the drain

So the S + the D are set by whichever is at a higher voltage, depending on the device type

(pMOS or nMOS)

So, for an nMOS, where the carriers are e<sup>-</sup>s, the S is more negative (source of e<sup>-</sup>s) than the D.

And for a pMOS, where the carriers are holes, the S is more positive (source of holes) than the D.

Now we will go into a more deep dive into the nMOS. First, we will look at what is called the Water Model and then we will go into the equations for current.

We will not cover the pMOS since it is identical & complementary & just the parameters will change but everything else will remain the same.

### DEEP DIVE into nMOS :-

When talking about the nMOS, we have already seen the 3 regions of operation of the MOS-capacitor → accumulation, depletion and inversion. But we also have different regions of operation of the nMOS itself.

### REGIONS OF OPERATION OF AN NMOS

Let us first look at some assumptions which we will always make :-

#### ASSUMPTIONS :-

①  $V_B = 0$  (Body is always grounded in VLSI design for an nMOS.  
We do not use Body Biasing in VLSI design)

②  $V_S = 0$  (In this analysis, we will also assume that the Source is grounded. Later on you will see that the Source may not be 0, but in the current-voltage analysis we start by

Assuming that the  $S$  is 0, so that the picture of the MOSFET is a lot cleaner.

Under these operations, we can say that there are 3 regions of operation of an MOS device :-

- ① Cut-off (or the Subthreshold) Region
- ② Linear (or Triode in older lit.) Region
- ③ Saturation Region

We are going to explore the Current - Voltage relationships in each of these regions.

- Each Region has a different relationship between currents + voltages
- These relationships are based largely on  $V_{GS}$ ,  $V_{DS}$  &  $V_t$

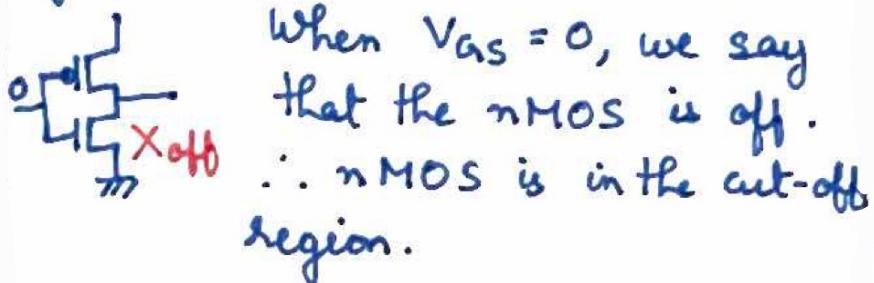
We will not look at the details of  $V_t$  or  $V_{th}$  but just note that after  $V_t$  is reached, there is a large amount of e's available for motion.

**NOTE :-**  $V_t$  and  $V_{th}$  are the same thing (threshold voltage) and we will use these interchangeably.

## FIRST REGION - CUT-OFF :-

- Simplest to analyze.
- This region is where the Gate Voltage  $V_{GS} < V_t$  or  $V_{th}$  which is the threshold voltage.

Eg:- Consider an inverter:-



- In this region there are not enough free electrons near the channel to create any noticeable current  $\therefore I_{DS} \approx 0$ , In reality  $I_{DS}$  is not exactly 0 but very small. Even when  $V_{GS} = 0$ ,  $I_{DS}$  is very, very small but not exactly 0. Later on, when we look at Power etc. we will see that this very small current also matters but for now, let us consider this to be almost 0.

We will change this assumption a little later when we have some more understanding of the transistor.

$$V_G = V_{GS} < V_t$$

A diagram showing three voltage levels. At the top is  $V_d$ . In the middle is  $V_s$ . At the bottom is  $V_g$ . Arrows point from  $V_d$  down to  $V_s$ , and from  $V_s$  down to  $V_g$ .

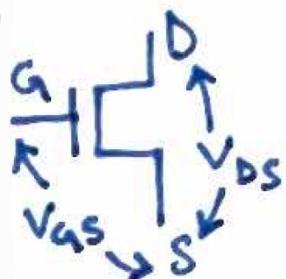
## SECOND REGION - LINEAR :-

• For the last region, note that we didn't talk of the  $V_{DS}$  at all. As long as  $V_{GS} < V_t$ , the nMOS is in cut-off irrespective of the  $V_{DS}$ .

• Here, in the linear region,  $V_{GS} > V_{th}$  so the device is ON

• But the  $V_{DS}$  is small,  $V_{DS} < (V_{GS} - V_{th})$

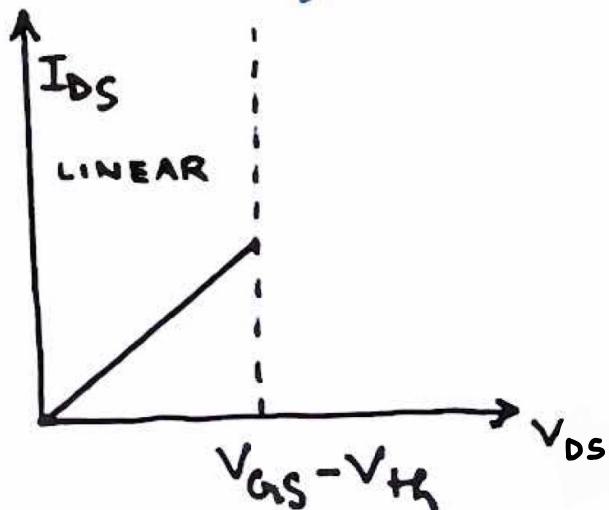
So the transistor is ON but it is weakly ON



This reminds us of the device whose I-V characteristics we had looked at earlier & whose Resistance depended on the voltage.



- In this region of operation as  $V_{DS} \uparrow$ , the current increases linearly (like Ohm's law).
- ∴ We call it the LINEAR REGION of operation.



The transistor here behaves as a LINEAR RESISTOR

- Note that this is for a particular value of  $V_{GS}$ . If  $V_{GS}$  changes, we will see what happens in a bit.

### THIRD REGION - SATURATION

- This region is characterized by :

$V_{GS}$  is still greater than  $V_{th}$   $\rightarrow$  so the device is still ON, but now,

$V_{DS} > V_{GS} - V_{th}$  which means that  $V_{DS}$  is also large.

So we have not only applied a large voltage to the G but also, applied a large  $V_{DS}$  so that the e<sup>-</sup>'s can move very fast and we thus, have a lot of current.

- When  $V_{DS}$  becomes sufficiently large, we have **SATURATION CURRENT**.

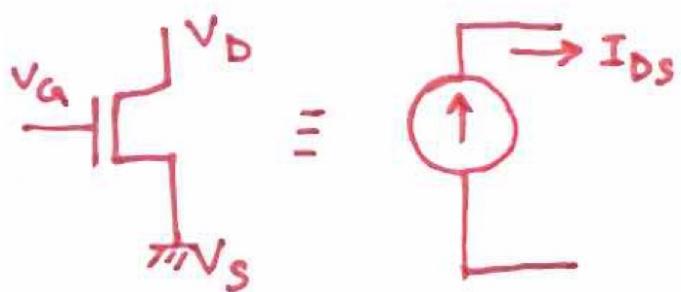
- In this condition, the transistor channel is said to be '**PINCHED OFF**'.

We will look at the water model in a bit which will enable us to understand what we mean by pinched off (intuitively)

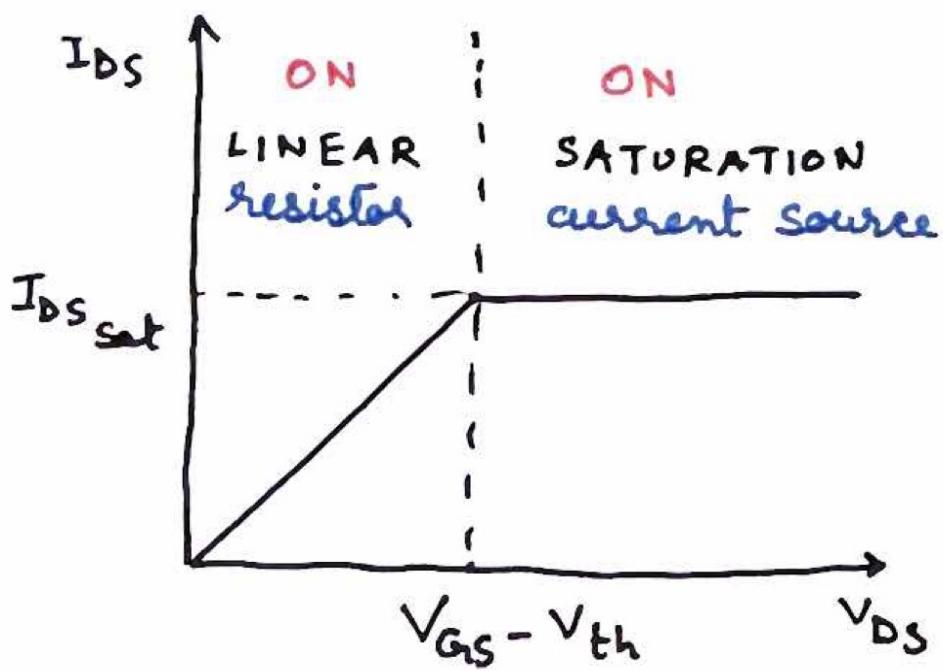
Electrically speaking, when the channel is pinched off,  $I_{DS}$  becomes independent of  $V_{DS}$  & we say that the current has SATURATED.

So 'pinch-off' is a condition where  $V_{DS}$  is so large already that increasing it further will not increase the current anymore. So we have reached the limiting cond<sup>n</sup> where we have the max<sup>m</sup> amount of current possible in the device.

$\therefore$  We have constant current and the device now behaves as a current source.



Going back to our I-V char, we can draw it as :-

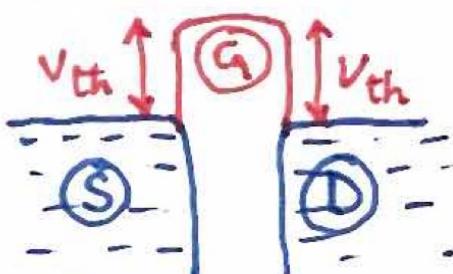


## WATER MODEL OF A MOSFET

- This is often used to explain the workings of a MOSFET to students who are just starting to learn about it.
- This gives us an intuitive understanding of what is going on.
- nMOS can be drawn as :-



- The Water Model assumes that the Source and Drain each have deep containers of water.
- Also, applying positive voltage lowers the top of the container (water level)  
∴ We can draw it as :-



- Assume that the Gate has

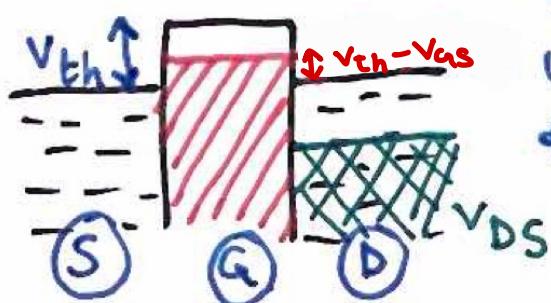
a plunger. So the Gate is like a barrier and the height of this is  $V_{th}$  (above the surface)

This prevents the flow of water.

- A positive gate voltage lowers the plunger.

Now, keeping these assumptions in mind, let us look at the different regions of operation.

### I CUT-OFF REGION :-



- Let us start with  $V_{DS} = 0$  +  $V_{GS} = 0$

- The height of the barrier is now  $V_{th}$

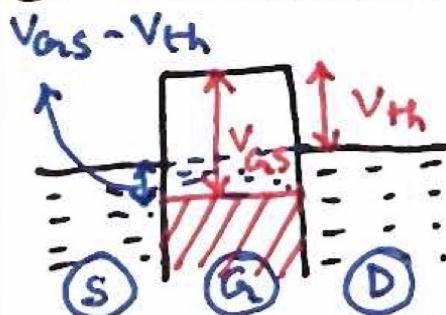
- Now say we apply a finite  $V_{GS}$ . This is still less than  $V_{th}$  so we are still in the cut-off region. But the barrier is lowered a little by the applied  $V_{GS}$ .

The height of the barrier is now  $(V_{th} - V_{GS})$  (see figure)

- Now if we apply a finite  $V_{DS}$ , the drain side is lowered but there is still a barrier ( $V_{th} - V_{GS}$ ) on the Source Side. Hence, water cannot flow and we are still in CUT-OFF. (see figure)

Here the Gate Plunger is still above the Source level and hence no WATER FLOWS.

## II LINEAR REGION :-



- Here, starting with the original figure that we had, let us increase  $V_{GS}$  further so that  $V_{GS} > V_{th}$

(see figure)

- $\therefore$  The Gate is lower than the Surface by an amount  $V_{GS} - V_{th}$ . This is called the

OVERDRIVE VOLTAGE, and is the amount by which we are overdriving the Gate.

(Gate is lower than the surface level)

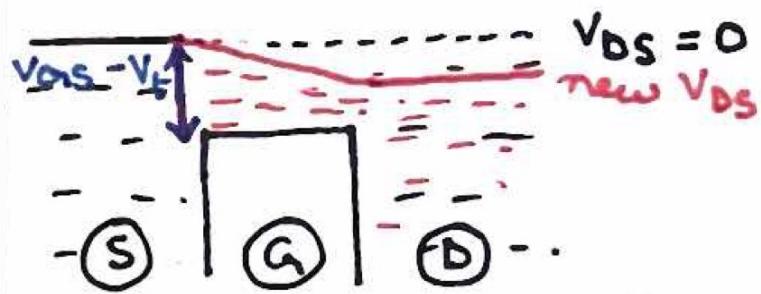
Now the 2 levels will be in equilibrium and there is water above the Gate & the height of this water column is  $V_{GS} - V_{th}$ . But still there is NO FLOW OF WATER.

(hence NO CURRENT)

Note :- There is water in the channel now, available for motion but no flow as yet, hence the CURRENT is still zero.

For a flow to happen, there needs to be a bias, i.e. a difference in level bet<sup>n</sup> the S & the D.

∴ We will now slowly start to increase the  $V_{DS}$



When we apply a finite  $V_{DS}$ , the drain side is lowered and as we can see in the figure, there is flow of water.

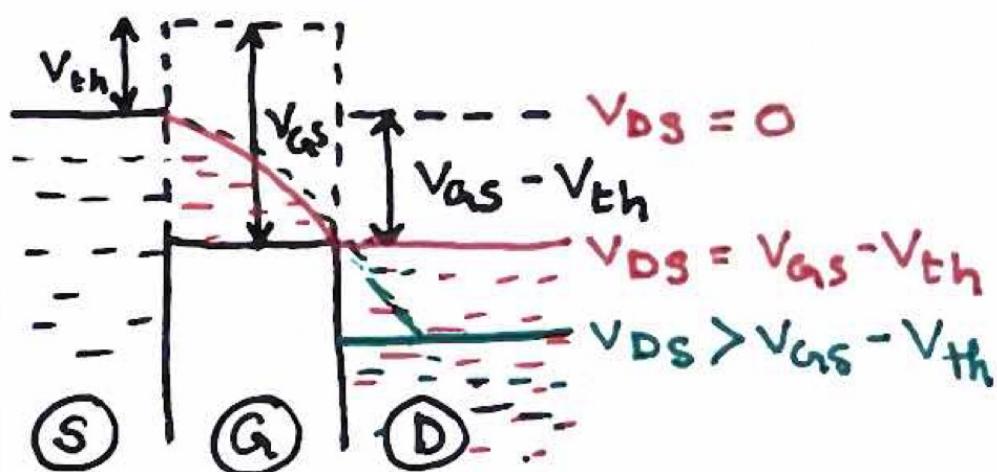
This will therefore be our current in the LINEAR REGION.

In this region we can see that as  $V_{DS} \uparrow$ , we will have more flow and thus the current  $I_{DS}$  increases linearly with  $V_{DS}$ . And the device will act as a RESISTOR.

### III SATURATION REGION:-

Now we will proceed and will further increase  $V_{DS}$ .

Consider the following scenario :-



When the water level on the drain side is the same as the height of the Gate Barrier then we see that,

$$V_{DS} = V_{GS} - V_{th}$$

Now, the water flowing to the drain is not limited by the height of the Drain anymore but is limited by the height of the Gate Plunger. ( $V_{GS}$ )

This is known as the PINCH-OFF, where increasing the drain bias ( $V_{DS}$ ) does not affect the flow of water i.e the current any more.

Now we increase the drain bias even further.

$$\therefore V_{DS} \gg V_{GS} - V_{th}$$

(see figure) We can see that the flow will not change. We are only limited by how much water can come from the Source side and eventually get collected in the Drain side (injection limited)

(limited by doping, velocity of e's etc. which is beyond the scope of this course)

$\therefore$  We are limited by the total volume of water that can flow on top of the gate & is NOT DEPENDANT on how low the water level at the Drain is.

$\therefore$  The current is now independent of  $V_{DS}$ . i.e. the drain level is so low that the  $V_{DS}$  does not matter any more.

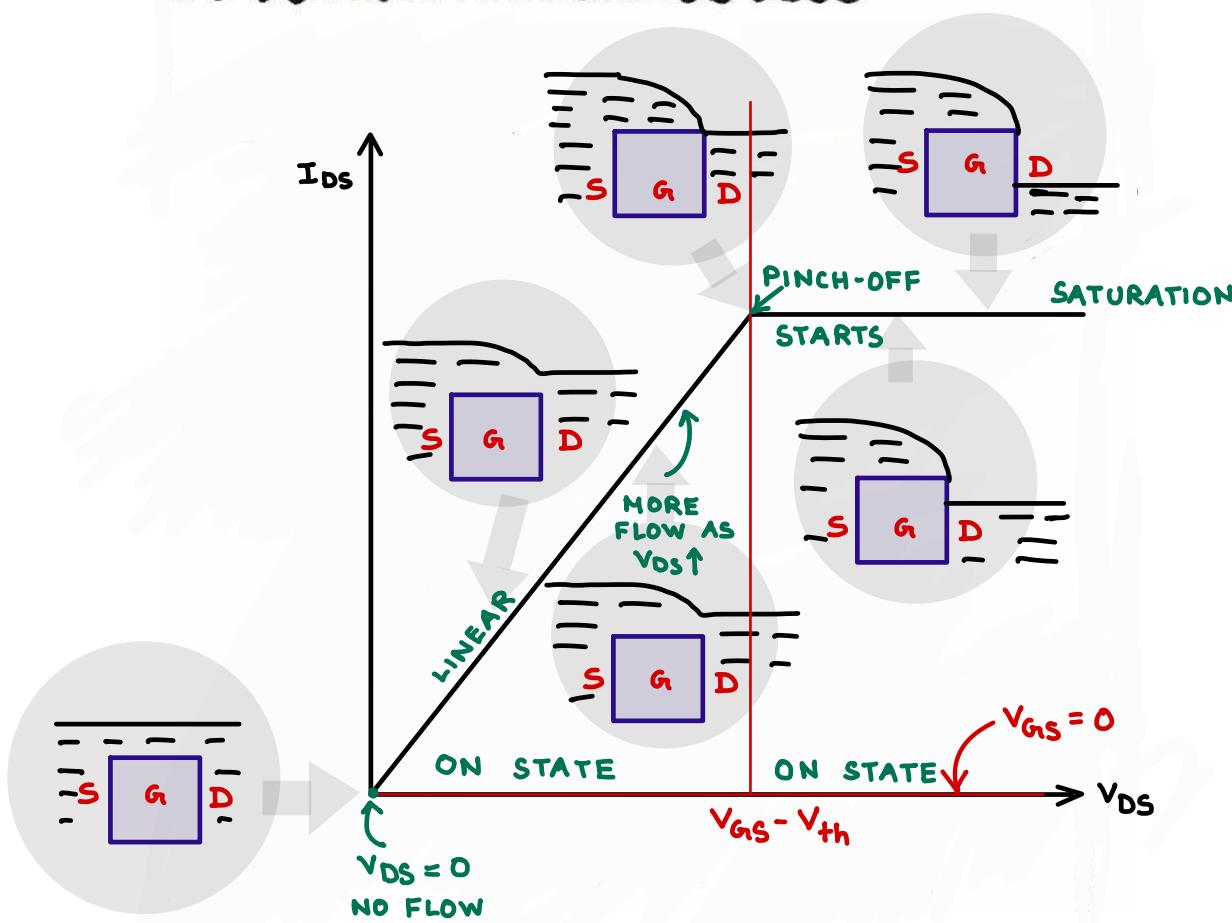
$\therefore$  The flow of water is constant i.e. the current is constant and this is known as the SATURATION REGION.

This is the basic model of water flow + how it relates to the different regions of the MOSFET.

Now we draw the:

IDEALIZED MOSFET I-V char.

USING THE WATER MODEL



## MATHEMATICAL MODEL OF A LONG CHANNEL MOSFET

Let us first start by defining a long channel and we will refine this definition as we proceed in this course.

- Long channel MOS eq<sup>n</sup>s. have remained true for channel lengths that are 250 nm ( $\frac{1}{4}\mu\text{m}$ ) and above.

(here the eq<sup>n</sup>s of the long channel model works very well).

- Short channel device characteristics show up for channel lengths that are 100 nm & below.

In bet<sup>n</sup> this 100 nm and 250 nm technology nodes, we have a 130 nm & a 180 nm technology node. Here we start seeing some of the short channel effects but the long channel eq<sup>n</sup>s. are still pretty much

valid. So we can get away using the long channel eq<sup>n</sup>'s. although we need some short channel corrections.

Let us start with some:-

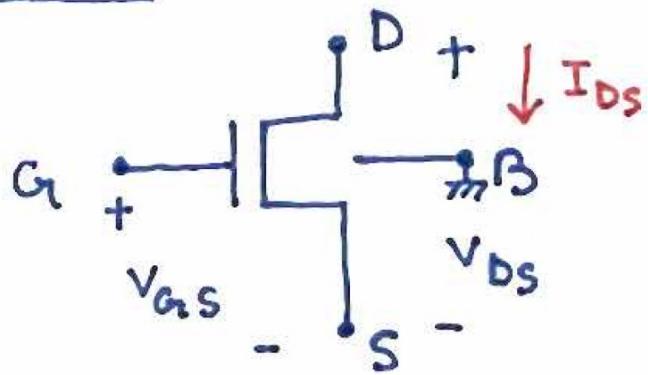
### MOS DEVICE NOTATIONS:

- $V_{DS}$  is the voltage at the Drain relative to the Source. Also  $V_{DS} = -V_{SD}$

We will sometimes use uppercase + lowercase interchangably. Don't worry too much whether its DC or ac.

- $V_{GS}$  is the voltage at the Gate relative to the Source
- $I_{DS}$  also written as  $I_D$  is the current flowing INTO the Drain i.e. from the Drain to the Source.

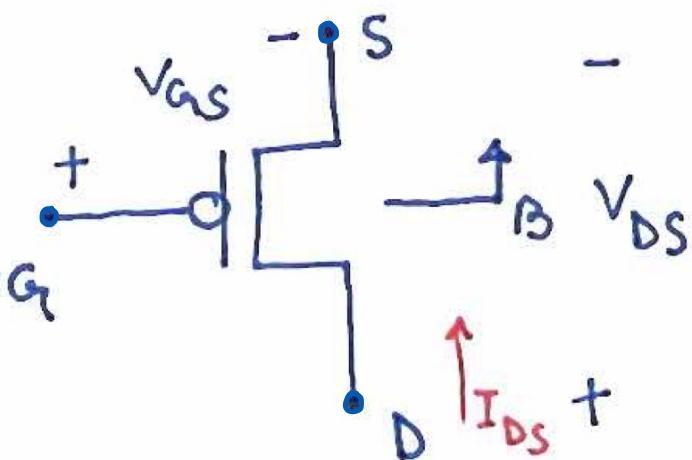
## n MOS :-



i.e.

$$\begin{aligned} V_{DS} &\geq 0 \\ V_{GS} &\geq 0 \\ I_{DS} &\geq 0 \end{aligned} \quad \left. \begin{array}{l} \text{typical} \\ \text{operating} \\ \text{range of} \\ \text{an nMOS} \end{array} \right\}$$

## pMOS :-



i.e.

$$\begin{aligned} V_{DS} &\leq 0 \\ V_{GS} &\leq 0 \\ I_{DS} &\leq 0 \end{aligned} \quad \left. \begin{array}{l} \text{typical} \\ \text{operating} \\ \text{range of a} \\ \text{pMOS} \end{array} \right\}$$

With this convention in mind, let us look at the nMOS transistor and see how the I-V characteristics will look like :-

## NMOS I-V CHARACTERISTICS :-

(equations)

① Cut-off Region:-

$$I_{DS} = 0$$

② Linear Region :-

In the linear region

$I_{DS}$  depends on :-

a) How much charge  
is in the channel ?

b) How fast is this charge  
moving ?

i.e.  $I_{DS} = \frac{Q_{\text{channel}}}{t} \frac{(\text{Charge})}{(\text{Time})}$

where,  $Q_{\text{channel}} \rightarrow$  charge  
in the  
channel

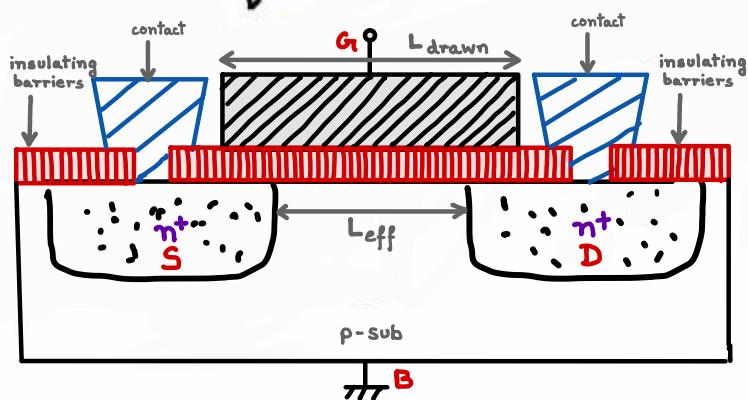
$t \rightarrow$  time taken by this  
charge to transit  
the channel (S to D)

$\therefore$  If we can estimate the  
 $Q_{\text{channel}}$  & the  $t$ , we will  
have a decent approximation  
or model of  $I_{DS}$ .

Before we do this we need to understand the geometry of the MOSFET, since we need to find quantities like time & charge & distance etc.

### SIDE VIEW OF THE MOSFET :

- This is a little more realistic than what we had drawn before.



$L \rightarrow$  drawn length of the channel.

(because the fabrication of the MOSFET is like a printing process and when we are drawing the geometry, this is what we will draw)

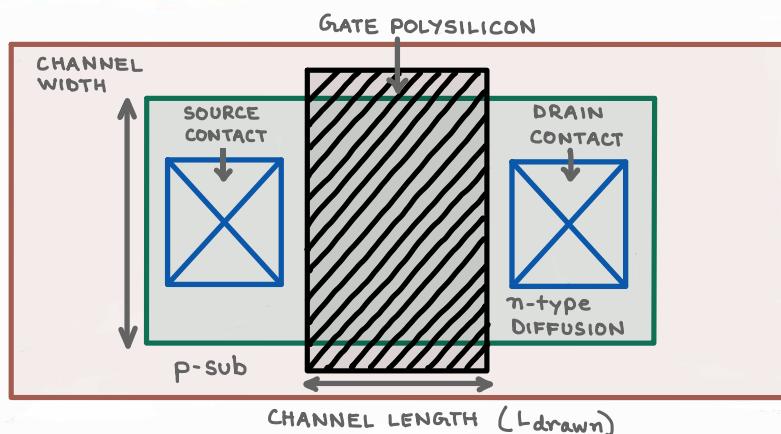
S + D  $\rightarrow$  aren't perfectly aligned with the Gr, there is an overlap.

$\therefore$  The effective length of the channel is  $L_{eff}$  &  
 $L_{eff} < L_{drawn}$

We also need to make contacts on the S + D

(as shown in figure)  
(these are metallic stubs)

### TOP VIEW OF THE MOSFET:



- Whenever the Gate - polysilicon crosses the n-type diffusion , we get an nMOS .
- The Metal contacts (S + D) are there to supply voltage and to connect to other devices .