

MODULE 2 - PART D

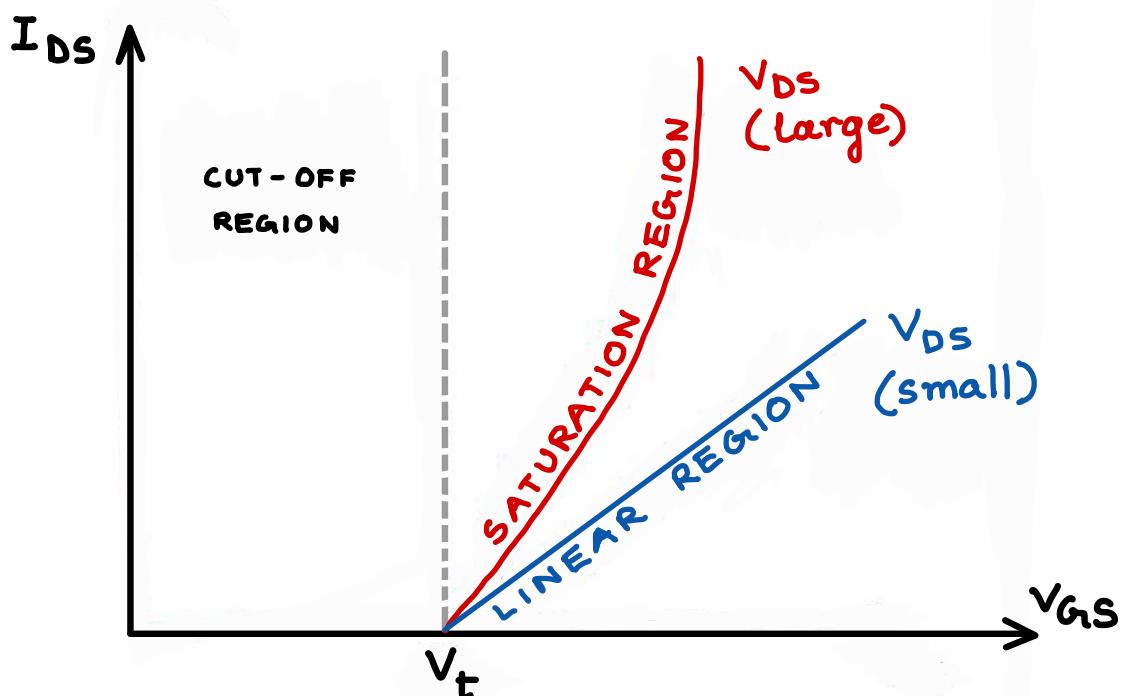
ELECTRICAL CHARACTERISTICS OF A MOSFET

We had looked at the OUTPUT CHARACTERISTICS of the MOSFET in the last part (PART C) of MODULE 2.

Apart from the OUTPUT characteristics of the MOSFET, we can also plot I_{DS} vs V_{GS} .

This is known as the :-

TRANSFER CHARACTERISTICS



- When V_{GS} is less than V_t , there will be almost no current (just the leakage current). This is the sub-threshold or the

cut-off region.

- For small V_{DS} , i.e.

$V_{DS} < V_{GS} - V_t$, the MOSFET is in the LINEAR REGION and $I_{DS} \approx \beta V_{GT} V_{DS}$

$$\text{i.e. } I_{DS} \propto V_{GS}$$

\therefore Plot will be linear (straight line)

- For large V_{DS} i.e when

$V_{DS} > V_{GS} - V_t$, the MOSFET is in the SATURATION REGION.

(Current in the cut-off is still 0)

$$I_{DSat} = \beta \frac{V_{GT}^2}{2}$$

$$\text{i.e. } I_{DSat} \propto V_{GS}^2$$

\therefore The plot here will be PARABOLIC

This plot where we have the input voltage on the gate (V_{GS}) vs the output current (I_{DS}) is called the TRANSFER characteristics.

Before we proceed any further, as circuit designers we should know what are the parameters that are in our control.

KNOBS FOR DESIGNERS
to change :-

Typically, a logic designer will have no control over the following parameters :-

- ① ϵ_{ox} (oxide permittivity)
- ② t_{ox} (oxide thickness)
- ③ μ (carrier mobility)
- ④ V_t (threshold voltage)

These are known as the TECHNOLOGY PARAMETERS given to the circuit designer and varies from one technology node to another.

KNOBS left for us to work with are :-

① V_{DD} → supply voltage
This is typically selected at the circuit + system level. (jointly optimized)

② L → length of the channel

(we can change this parameter in the circuit design phase only)

However, in modern digital process technologies L is also fixed and we cannot change it

(sometimes there may be more than one L to choose from in some processes)

However in analog processes we may have more choices for L .

③ W → width of the transistor MOSFET

This is the most important

parameters that we have at our disposal as ckt. designers.

For example :-

Doubling W will double the current (I_{DS})

What we have seen so far, was the FIRST APPROACH of deriving the I-V char. of the MOSFET. This approach didn't require Calculus.

- We have also seen that the different APPROACHES are actually for finding the CHANNEL VOLTAGE (V_{GC}) (which is actually the voltage betⁿ the gate and the channel)

- In the FIRST APPROACH, we had assumed that the voltage in the channel changes linearly.

i.e. the channel voltage is the average of the $V_{GC\text{ source}}$ + $V_{GC\text{ drain}}$

$$V_{GC} = \frac{V_{GC\text{ source}} + V_{GC\text{ drain}}}{2}$$

$$\text{or, } V_{GC} = \frac{V_{GS} + (V_{GS} - V_{DS})}{2}$$

$$\text{or, } V_{GC} = V_{GS} - \frac{V_{DS}}{2}$$

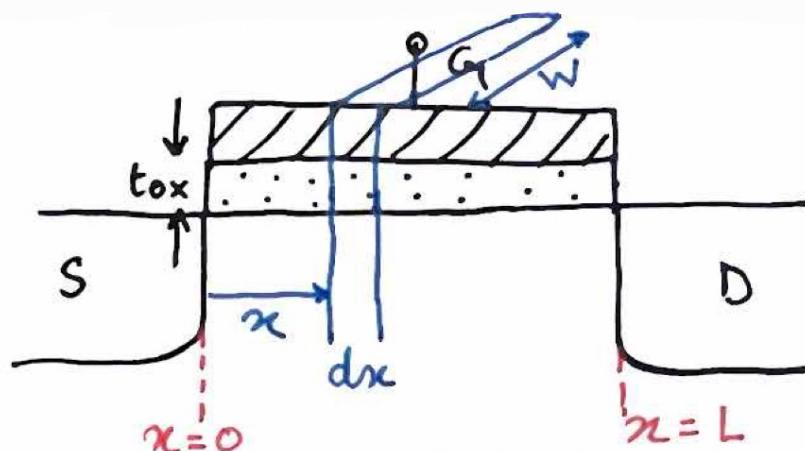
- Now we will start with:-

APPROACH 2 :-

This approach involves careful accounting of channel voltage variation.

Here we will not assume that the right side (D) and the left side (S) has different voltages and then take an average. We will use Calculus.

Let us draw the side view of the MOSFET :-



Here, we will look at a particular section of the channel, that is ' x ' distance from the Source (S) and is ' dx ' distance in length and the charge in this section is say, $dQ(x)$ say, the voltage here is given by $V(x)$

Note the points $x=0$ & $x=L$
in the figure above.

We are trying to first find
the Charge in this section

$dQ(x)$. Charge = Voltage \times Capacitance

The Capacitor voltage at this

point is given by $V_{\text{Ground}} - V(x)$

$$= V_{GS} - V_{th} - V(x)$$

The Capacitance is given by :-

(see figure) $\rightarrow W C_{ox} dx$

where $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ cap/area

$$\therefore dQ(x) = (V_{GS} - V_{th} - V(x)) W C_{ox} dx$$

Now, the velocity of the electrons
we have seen in the last part, is

$$v_e = \mu E \quad \mu \rightarrow \text{mobility of e}^-$$

$E \rightarrow$ electric field

$$\therefore v_e = \mu \frac{dV(x)}{dx}$$

We had derived in the last

class that,

$$E = \frac{F}{q} = \frac{V_2 - V_1}{L}$$

In our first APPROACH,
this was $E = \frac{V_{DS}}{L}$

$$\therefore E \text{ here} = \frac{dV(x)}{dx}$$

i.e. Voltage / length

Also, we know, $I_{DS} = \frac{dQ}{dt}$

Let us substitute $I_{DS} = I$.

$$\therefore I = \frac{dQ}{dt} \text{ or, } Idx = \frac{dQ}{dt} dx$$

$$\text{or, } Idx = dQ \left(\frac{dx}{dt} \right) = dQ V_e$$

We can now substitute the
value of $V_e = \mu \frac{dV(x)}{dx}$
here.

$$\therefore Idx = dQ \left(\mu \frac{dV(x)}{dx} \right)$$

Now if we substitute the
value of $dQ(x)$ or dQ
in this equation, we will
get :-

$$I dx = (V_{GS} - V_{th} - V(x)) W C_o x dx$$

$$(\mu \frac{dV(x)}{dx})$$

Now if we integrate along the length of the channel on both sides, we get

(Note that the current flowing across the channel is continuous and is a constant)

$$\therefore \int_0^L I dx = I \cdot L$$

Now, for the RHS,

$$\int (V_{GS} - V_{th} - V(x)) W C_o x dx \cdot \mu \frac{dV(x)}{dx}$$

dx gets canceled and we are left with an integration over voltage $dV(x)$

The limits of this integration is given by,

→ when $x = 0$,
 $V(x) = 0$ since the
Source in an nMOS
is grounded.

NOTE → this is the
voltage in the channel
and NOT the voltage
across the capacitor
and hence the gate
voltage does not feature
in here.

→ when $x = L$,
 $V(x) = V_{DS}$ which
is the voltage applied
to the Drain.

∴ We integrate :-

$$\left(\mu C_o x w \right) \int_0^{V_{DS}} (V_{GS} - V_{th} - V(x)) dV(x)$$

We can take out
 $\mu C_{ox} W$ since these
are constant terms.

\therefore We get,

$$\int_0^{V_{DS}} (V_{GS} - V_{th}) dV(x)$$

$$- \int_0^{V_{DS}} v(x) dV(x)$$

$$= (V_{GS} - V_{th}) V_{DS}$$

$$- \frac{V_{DS}^2}{2}$$

$\therefore I.L =$

$\mu C_{ox} W.$

$$\left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

or,

$$I = \frac{\mu C_{ox} W}{L} .$$

$$\left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Now if :-

β (beta factor)

$$= \frac{\mu C_0 \times W}{L}$$

$$\text{and, } V_{DS} - V_{TH} = V_{GATE}$$

We can write,

$$I_{DS} = \beta \left(V_{GATE} - \frac{V_{DS}}{2} \right) V_{DS}$$

which is the same
equation we got using
APPROACH 1.

Now we can write
the equations for
current as we had
done before in the
various regions .

$$I_{DS} \approx 0 ; V_{GS} < V_{TH}$$

CUT-OFF

REGION

$$= \beta \left(V_{Gt} - \frac{V_{DS}}{2} \right) V_{DS}$$

when $V_{DS} < V_{DSat}$

$$\begin{aligned} V_{DSat} &= V_{Gt} \\ &= V_{GS} - V_{TH} \end{aligned}$$

LINEAR REGION

$$= \frac{\beta V_{Gt}^2}{2}$$

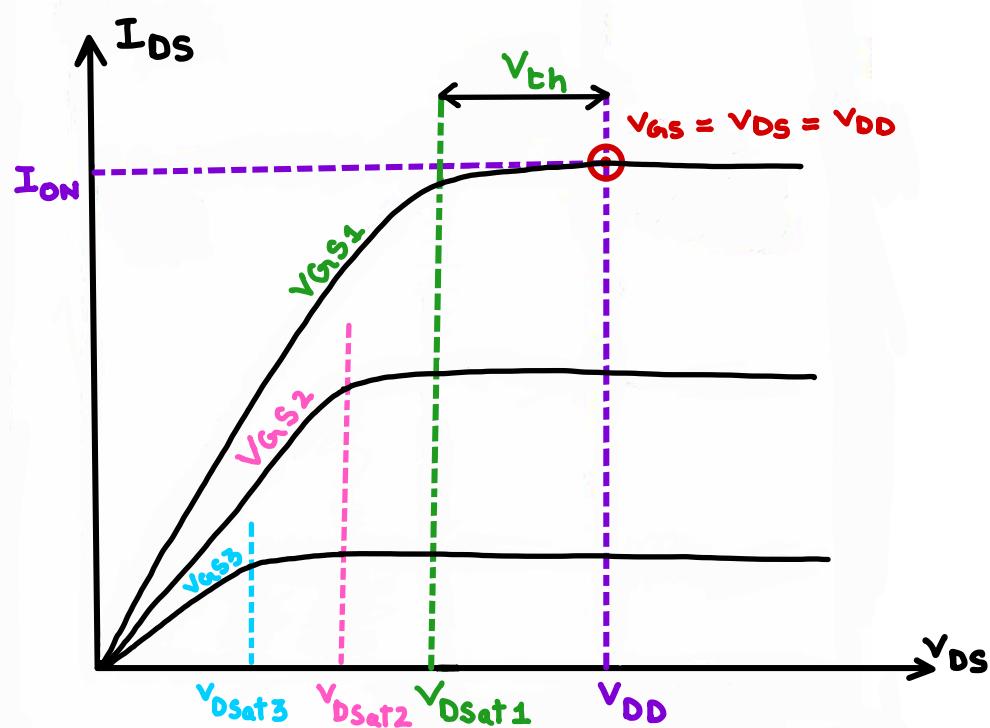
when $V_{DS} > V_{DSat}$

SATURATION REGION

These equations were first proposed by William Shockley in 1952. These are the first-order transistor model eq's. which are still popular and still widely used in transistor design.

Apart from the output characteristics & the transfer characteristics, that we had looked at, let us also define a few other parameters which are also useful.

Let us draw the output characteristics I_{DS} vs V_{DS} of the nMOS.



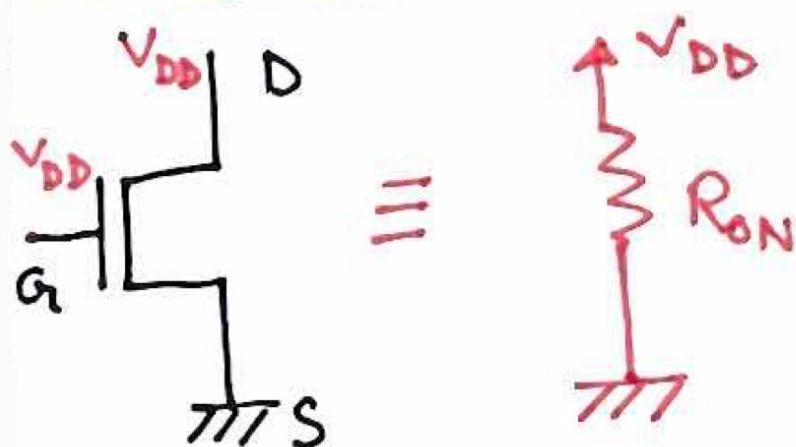
In this output characteristics we can define a few other useful parameters.

I_{ON} is the device current when $V_{GS} = V_{DS} = V_{DD}$

(supply voltage)

(see plot). This

represents the maximum current delivered by the device.



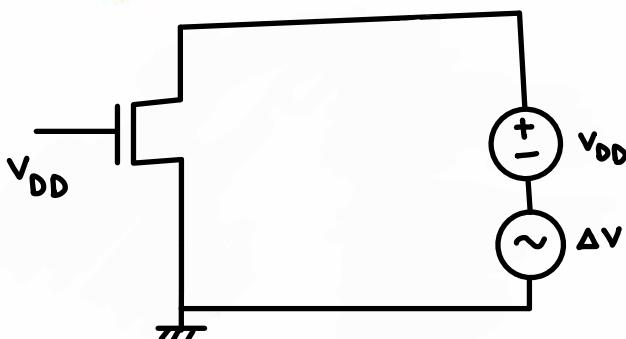
In this condition, the DC on resistance R_{ON} is defined as :-

$$R_{ON} = \frac{V_{DS}}{I_{DS}} = \frac{V_{DD}}{I_{ON}}$$

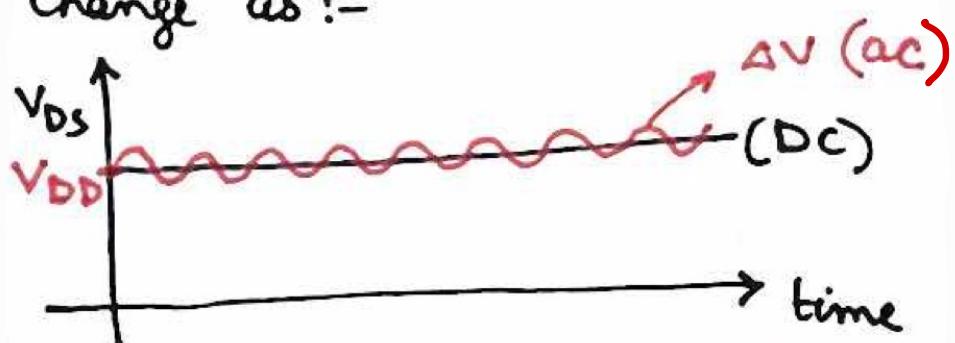
This represents the DC on resistance of an nMOS in the ON state.

Apart from the DC R_{ON} , we can also measure the ac on resistance of the device.

This is measured by applying a small voltage change at the Drain on top of the supply V_{DD} (ΔV) (sinusoidal)



We can also draw this small change as :-



This condition is called the ac or the SMALL SIGNAL CONDITION

In this condition, we can define, an ac or small signal resistance as :-

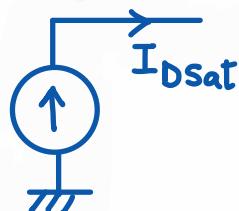
$$r_{ds\text{ ON}} = \frac{\delta V_{DS}}{\delta I_{DS}} \left(\because \text{Slope of the plot is } \frac{dy}{dx} \right)$$

This resistance is measured as the inverse of the SLOPE of the output characteristics

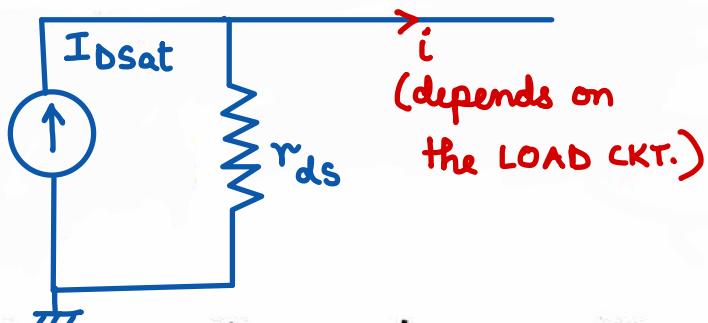
In an IDEAL MOSFET, r_{ds} in the Saturation region is ∞ (since the slope is 0)

r_{ds} is often called the output impedance of the transistor.

\therefore In the Saturation region an ideal mosfet is just a current source

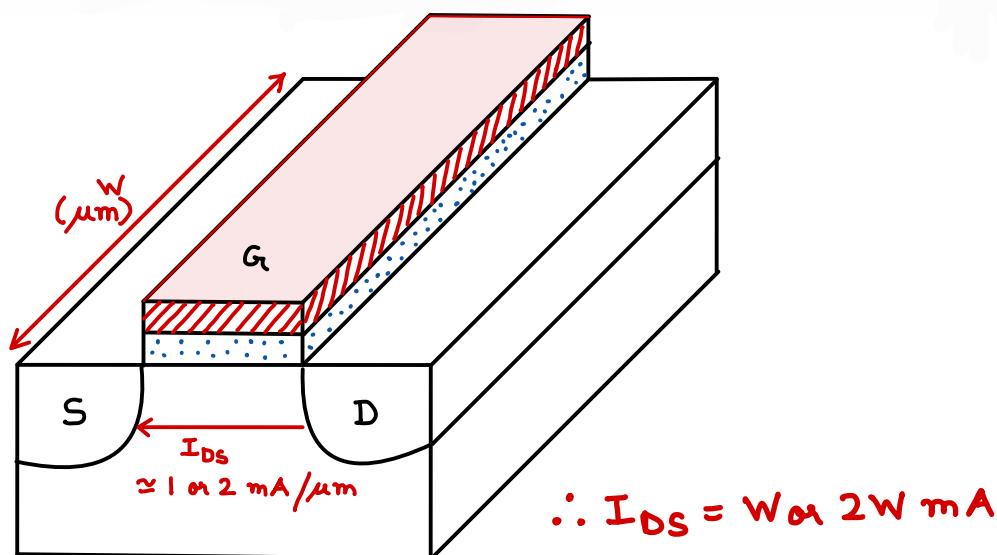


But for a practical device
there will be an **OUTPUT**
IMPEDANCE associated with
this current source just like
we have for a **NORTON SOURCE**.



In today's technology, the I_{ON} of a transistor is between 1 to 2 milliAmps (mA) per micrometer (μm)

Here $\frac{1}{\mu\text{m}}$ refers to the transistor width.



$$\therefore I_{DS} = W \left(\frac{\mu C_{Ox}}{L} \right) \left(\frac{V_{Gt}^2}{2} \right)$$

where, $\left(\frac{\mu C_{Ox}}{L} \right) \left(\frac{V_{Gt}^2}{2} \right)$ is 1 or $2 \text{ mA}/\mu\text{m}$

In practical devices why is this
 $r_{ds} < \infty$?

ANSWER:-

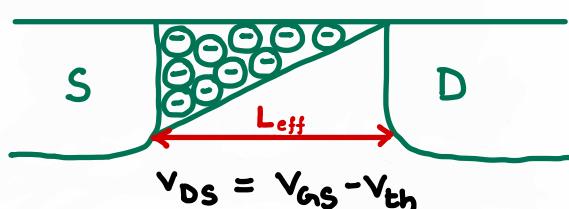
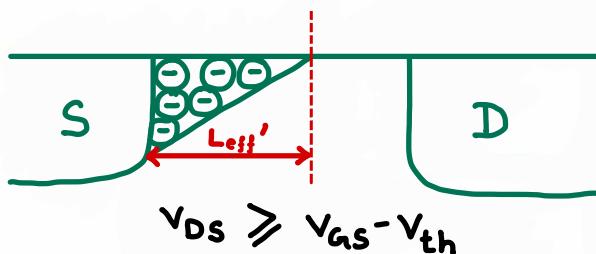


fig 1



Here,
 $L_{eff}' < L_{eff}$
 fig 2

When ($V_{DS} = V_{GS} - V_{th}$), the channel gets PINCHED-OFF at the Drain end.

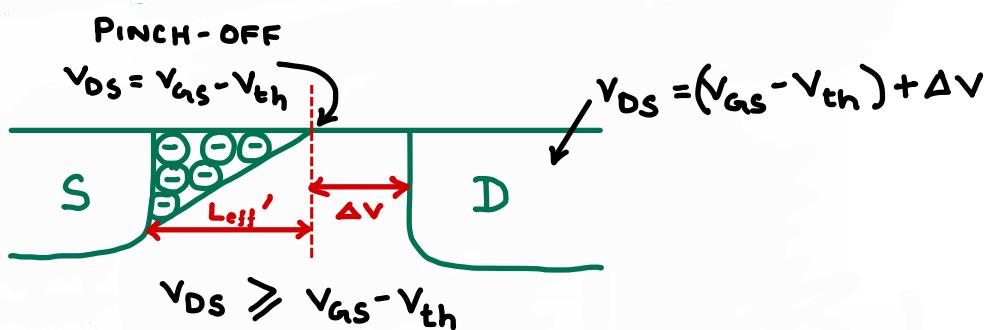
(you have seen this in PART-C)

If V_{DS} is increased even further, the point of PINCH-OFF moves further into the channel (fig. 2)

The POINT in the channel where the voltage is ($V_{GS} - V_{th}$), marks the beginning of the PINCH-OFF.

When, $V_{DS} = (V_{GS} - V_{th})$, this point occurs at the DRAIN end. If,

$V_{DS} = (V_{GS} - V_{th}) + \Delta V$, then the channel voltage is, $(V_{GS} - V_{th})$ somewhere in the channel away from the Drain. This is the NEW PINCH-OFF POINT. The additional voltage ΔV , drops between that NEW PINCH-OFF POINT and the Drain because the Drain is fixed at V_{DS} which is equal to $(V_{GS} - V_{th}) + \Delta V$



The effective length, (L_{eff}) is the distance from the Source to the point of PINCH-OFF, since there is no INVERSION CHARGE beyond this point.

As V_{DS} increases, ΔV increases and the pinch-off point moves further into the channel.

As a result, L_{eff} decreases to L_{eff}' . Since $L_{eff}' < L_{eff}$ and we know that $I_{DS} \propto \frac{1}{L}$,

we see that I_{DS} increases with increasing V_{DS} . This represents a non-ideal MOSFET.

We simply use a fitting parameter to represent this dependence

$$I_{DS}^{\text{non-ideal}} = I_{DS}^{\text{ideal}} [1 + \lambda V_{DS}]$$

This λ is obtained through measurement and curve-fitting and is typically very small ($\lambda V_{DS} < 0.1$)