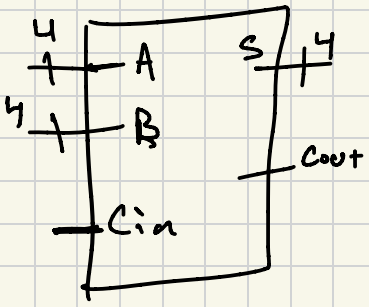
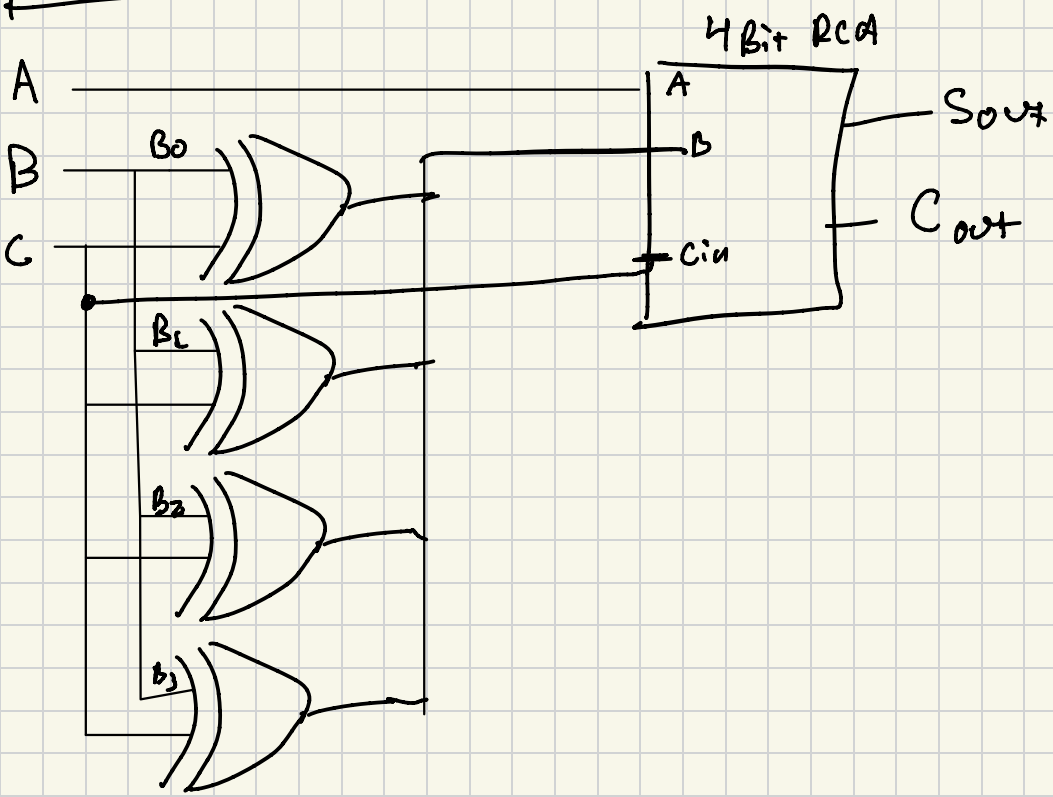
1. Demonstrate how a 4 bit ripple carry adder can be modified to a 4 bit subtractor with a single bit control (C), such that when C = 0, the circuit acts as an adder and when it is 1, the circuit acts as a subtractor.

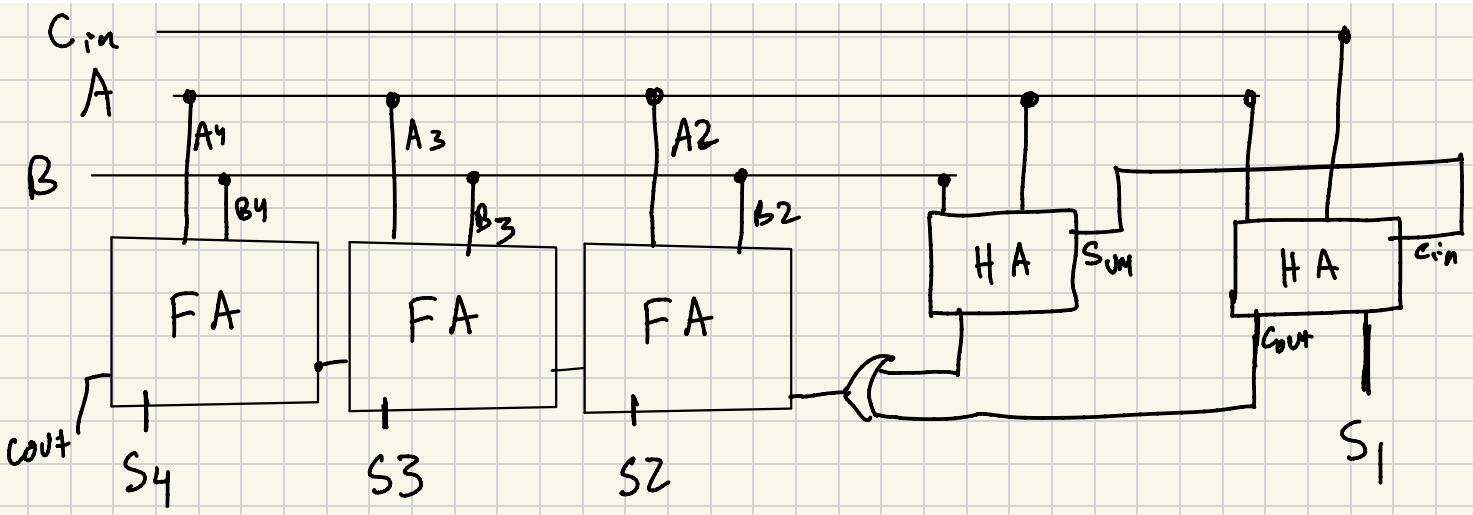
Given a 4 Bit Ripple Carry adder



We can create a XOR Network on Input B



2. Design a RippleCarry 4bit adder using 3 Full Adders, 2 Half Adders and an OR gate. You can draw full adders and half adders as blocks labeled with “FA” and ”HA” respectively.



3. Calculate the worst-case delay of a 4-bit CLA where the delay of any gate can be approximated by $T = T_0.N^2$ where T_0 = 1ns and N is the fan-in of the gate. Do not assume that the propagate and generate signals have already been generated.

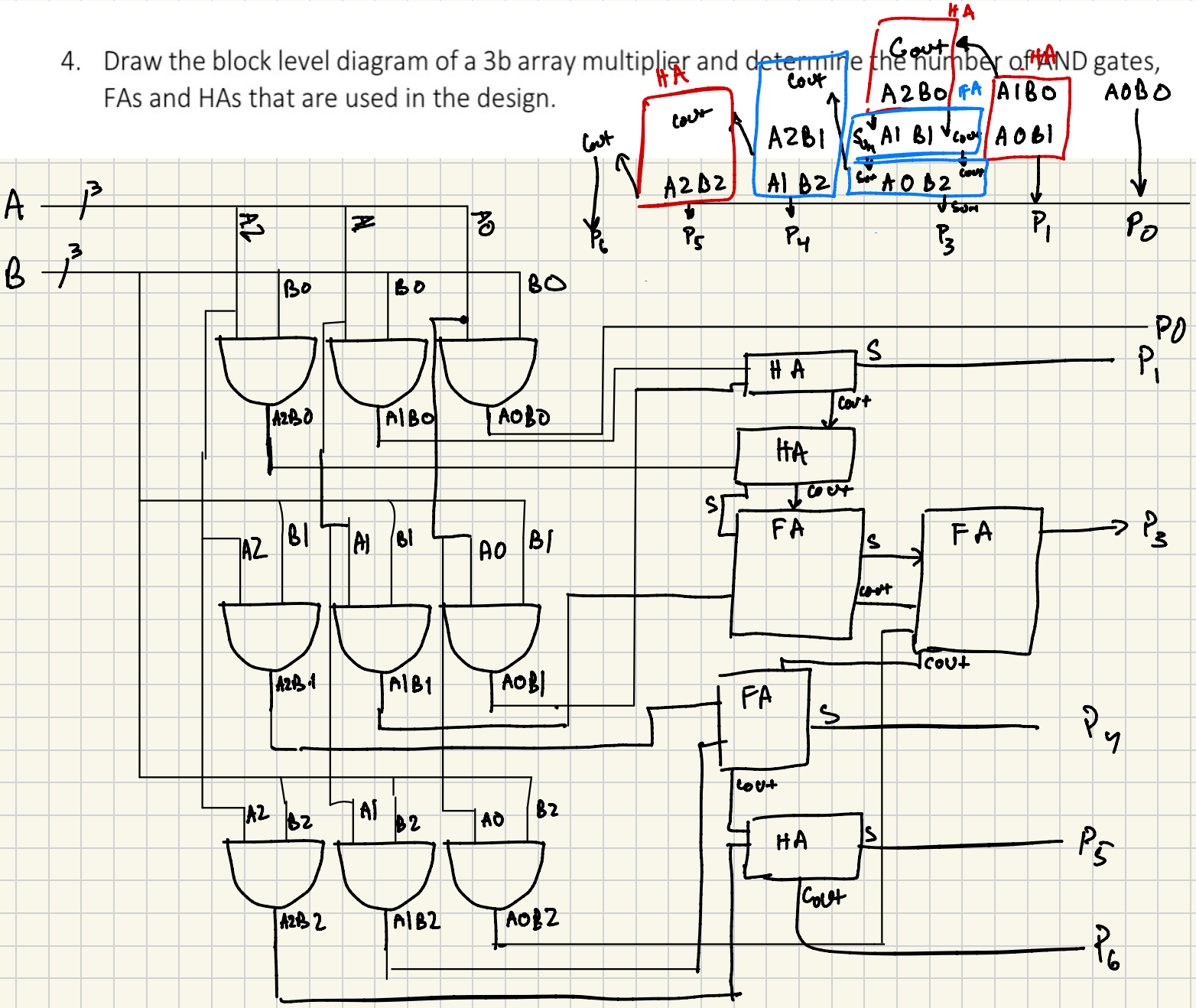
The worst case Delay of the 4 Bit CLA is Generating the 4 Carryout C_4

Because P & G is Generated Prior → C_4 only is Delayed Critical path of 5-input AND + 5 inp OR

1.25 + 1.25 = 50 ns

P & G Take 1 ns each → 50 + 1 = 51 ns

4. Draw the block level diagram of a 3b array multiplier and determine the number of AND gates, FAs and HAs that are used in the design.



9 AND GATES
3 HALF ADDERS
3 FULL ADDERS

$(3)_{10} = (0011)_2$

5. Perform 3 x 11 using the shift and add method in the 4 bit unsigned format. Fill up the following table. $(11)_{10} = (1011)_2$

Step (i)	Bi	A	Product Register State	Result

Step	Bi	A	Prod Reg	Res
0	1	1011	1011	1011
1	1	1011	1011	100001
2	0	1011	00000	100001
3	0	1011	00000	100001