

Solution

ECE 3030: Physical Foundations of Computer Engineering

Summer 2018

Final Exam

July 27, 2018

Time: 2 hour 15 min

Instructor: Asif Khan

Instructions:

1. There are 11 pages in this test. Count the number of pages and notify the proctor if you are missing a page.
2. Read all the problems carefully and thoroughly before you begin working.
3. You are allowed to use 3 sides of notes as well as a calculator.
4. A list of constants and equations is provided on pages 10, 11.
5. You are required to answer all 6 questions. There are 100 total points. Observe the point value of each problem and allocate your time accordingly.

Q1	10 pts
Q2	30 pts
Q3	20 pts
Q4	25 pts
Q5	10 pts
Q6	5 pts
Total	100 pts

6. Show all your work and circle/underline your final answer. For numerical answers, write the units. Write legibly. If I cannot read it, it will be considered a wrong answer. Do all work on the space provided; use scratch paper when necessary. Turn in all scratch paper, even if it did not lead to an answer.
7. Report any and all ethics violations to the instructor/proctor.

Sign your name on ONE of the two following cases:

I DID NOT observe any ethical violations during this exam:

I observed an ethical violation during this exam:

Q1.1 Draw the band diagram (the relative positions of conduction band edge E_C , valence band edge E_v , Fermi level E_F) for Si wafer with acceptor doping $N_A=5\times 10^{23} \text{ m}^{-3}$ and no donor doping. Clearly indicate the values of $E_C - E_F$, $E_F - E_V$, $E_i - E_F$, $E_G = E_C - E_V$. E_i is the intrinsic Fermi level. Assume $N_C = N_V = 10^{25} \text{ m}^{-3}$, $E_G = 1.1 \text{ eV}$, $n_i = 1.5 \times 10^{16} \text{ m}^{-3}$, $kT = 0.026 \text{ eV}$. [Total 5 pts]

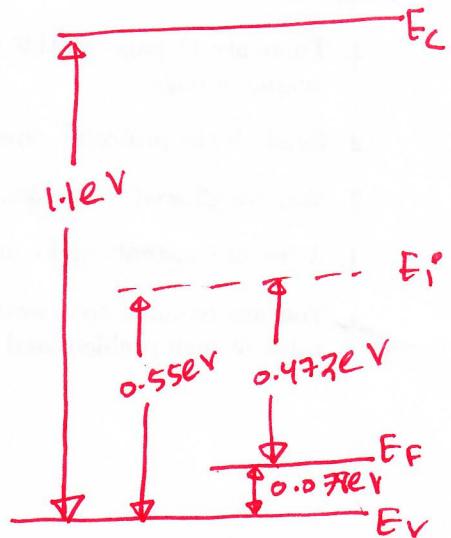
$$P = N_A = 5 \times 10^{23} \text{ m}^{-3}$$

$$\Rightarrow N_A = N_g e^{\frac{E_V - E_F}{k_B T}}$$

$$\Rightarrow E_V - E_F = k_B T \ln \frac{N_A}{N_g}$$

$$= 0.026 \ln \frac{5 \times 10^{23}}{10^{25}}$$

$$= -0.078 \text{ eV}$$



Q1.2 Briefly explain why it is necessary to have multiple levels of cache memory in today's microprocessor technology. Why was it not necessary in the 1980s? [Total 5 pts]

Cache memory is used to decrease the average time or energy to access data from the main memory. The microprocessor clock period has become significantly smaller than the average main memory access/retrieval times (aka memory wall), hence if there is no cache memory, having to access the main memory frequently will reduce the performance of the overall system. In the 1980s, there was much less difference between clock rate & memory access time, which is why it was not necessary to have cache memory.

Q2 MOSFETs and Delay and Power in Inverter: If decrease the doping density N_A in a MOSFET with all the parameters unchanged, how will the following quantities change? [Total 30 pts]

[Q2.1] The MOSFET threshold voltage, V_t . [5 pts]

$$V_t = \frac{\sqrt{4\epsilon_0 \epsilon_s N_A \Phi_B}}{C_{ox}} + 2\Phi_B$$

Although Φ_B also depends on N_A , it is a weak function of N_A . $\therefore V_t$ can be considered proportional to N_A .

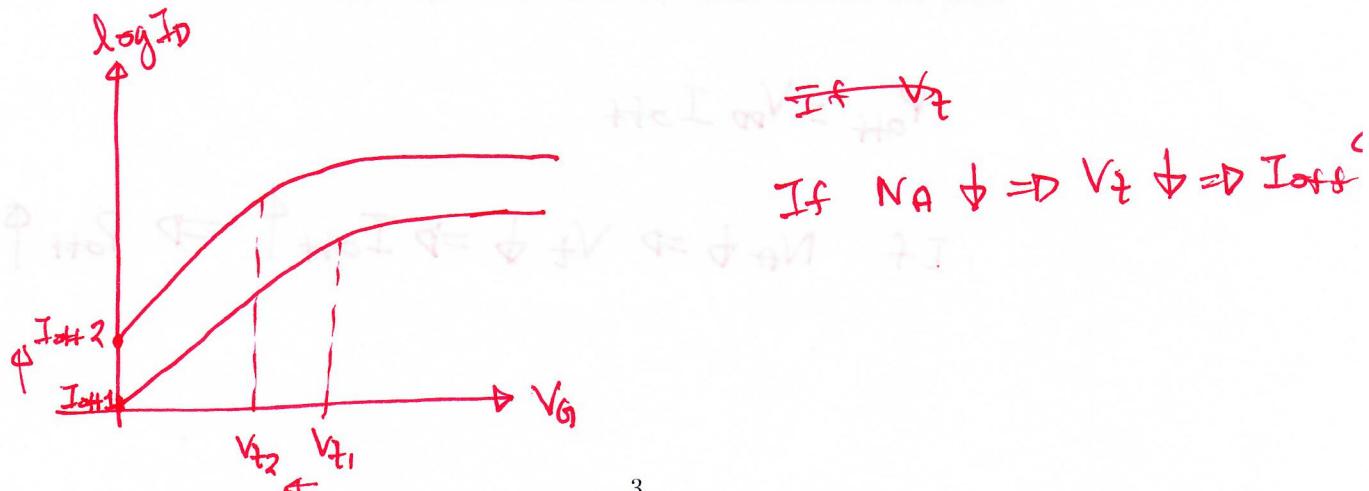
\therefore if $N_A \downarrow \Rightarrow V_t \downarrow$

[Q2.2] The on-state current, I_{ON} of the MOSFET. [5 pts]

$$I_{ON} = I_{DN} C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

If $N_A \downarrow \Rightarrow V_t \downarrow \Rightarrow I_{ON} \uparrow$

[Q2.3] The off-state leakage current, I_{OFF} of the MOSFET. [5 pts]



[Q2.4] The corresponding inverter delay. [5 pts]

$$\text{Delay, } t_d = \frac{C_L V_{DD}}{I_{ON}}$$

If $N_A \downarrow \Rightarrow V_t \downarrow \Rightarrow I_{ON} \uparrow \Rightarrow t_d \downarrow$

[Q2.5] The active power in the corresponding inverter. The clock frequency did not change. [5 pts]

$$P_{act} = C_L V_{DD}^2 f_{clock} = mI$$

$\therefore P_{act}$ does not depend on N_A (or any function of N_A)

\therefore If $\nexists N_A \downarrow \Rightarrow P_{act}$ remains the same

[Q2.6] The off-state leakage power in the corresponding inverter. [5 pts]

$$P_{off} = V_{DD} I_{off}$$

If $N_A \downarrow \Rightarrow V_t \downarrow \Rightarrow I_{off} \uparrow \Rightarrow P_{off} \uparrow$

Q3 Scaling: According to the Dennard scaling law, all three physical dimensions (W , L , t_{ox}), the power supply voltage V_{DD} and the threshold voltage, V_t are downscaled by factor of x in every subsequent generation. [Total 20 pts]

[Q3.1] How will the delay change in every subsequent generation? Show your calculations. [Total 5 pts]

$$\begin{aligned} V_{DD} &\rightarrow V_{DD}/x \\ W &\rightarrow W/x \\ L &\rightarrow L/x \\ V_t &\rightarrow V_t/x \\ t &\rightarrow t \cdot x \rightarrow t/x/x \end{aligned}$$

$$t_{d,n} = \frac{C_n V_{DD,n}}{I_{on,n}}$$

$$C_{n+1} = \frac{C_n}{x} \Rightarrow V_{DD,n+1} = \frac{V_{DD,n}}{x}$$

$$I_{on,n} = I_{on,n} C_{ox,n} \frac{W_n}{2L_n} (V_{DD,n} - V_{t,n})^2$$

$$\begin{aligned} I_{on,n+1} &= I_{on,n+1} C_{ox,n+1} \frac{W_{n+1}}{2L_{n+1}} (V_{DD,n+1} - V_{t,n+1})^2 \\ &= I_{on,n}/x \cdot C_{ox,n} \cdot x \cdot \frac{W_n/x}{2L_n/x} \left(\frac{V_{DD,n} - V_{t,n}}{x} \right)^2 \\ &= I_{on,n}/x \end{aligned}$$

$$t_{d,n+1} = \frac{C_{n+1} V_{DD,n+1}}{I_{on,n+1}}$$

$$\begin{aligned} &= \frac{C_n/x \cdot V_{DD,n}}{I_{on,n}/x} \\ &= \frac{t_{d,n}}{x} \end{aligned}$$

[Q3.2] How will you change the clock frequency in subsequent generations such that the total chip power remains the same across all generations. Assume that the total area of the chip remains the same across all generation. Ignore the contribution of the off-state leakage to the total chip power. [Total 5 pts]

$$P_{\text{chip}} = C_L V_{DD}^2 f$$

$$P_n N_n = P_{n+1} N_{n+1}$$

$$\Rightarrow C_n V_{DD,n}^2 f_n N_n = C_{n+1} V_{DD,n+1}^2 f_{n+1} N_{n+1}$$

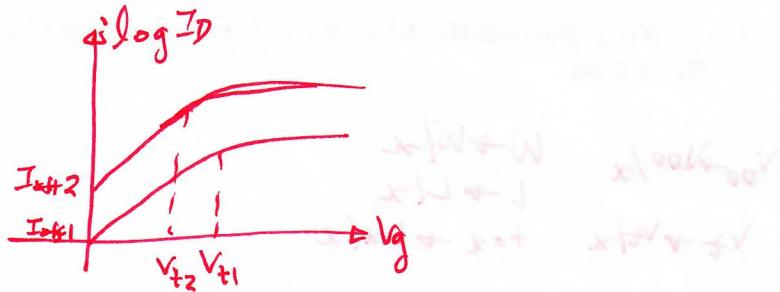
$$\Rightarrow C_n V_{DD,n}^2 f_n N_n = \frac{C_n}{x} \left(\frac{V_{DD,n}}{x} \right)^2 f_{n+1} \cdot N_n \cdot x^2$$

$$\Rightarrow f_n = \frac{1}{x} f_{n+1}$$

$$\therefore f_{n+1} = x \cdot f_n$$

∴ frequency increases by x .

[Q3.3] In recent years, why is it not possible to reduce the threshold voltage of the MOSFETs in subsequent generations? Use necessary figures. [Total 5 pts]



If $V_t \downarrow \Rightarrow I_{off} \downarrow \Rightarrow$ Leakage \downarrow

This is since leakage power increases as V_t is reduced, it is not possible to reduce V_t anymore.

[Q3.4] With necessary calculations, show that the inability to scale down the threshold voltage prevents the increase of the clock frequency in subsequent generations as per the Dennard's scaling law. [Total 5 pts]

V_t remains the same

$$\therefore V_{DD} \propto n \cdot n \cdot n$$

$$\therefore P_{n+1} N_{n+1} = P_n N_n$$

$$\Rightarrow C_{n+1} V_{DD,n+1}^2 f_{n+1} N_{n+1} = C_n V_{DD,n}^2 f_n N_n$$

~~$$\Rightarrow \frac{C_n}{\chi} \left(\frac{V_{DD,n}}{\chi} \right)^2 \cdot f_{n+1} \cdot N_n \cdot x^2 = C_n V_{DD,n}^2 f_n N_n$$~~

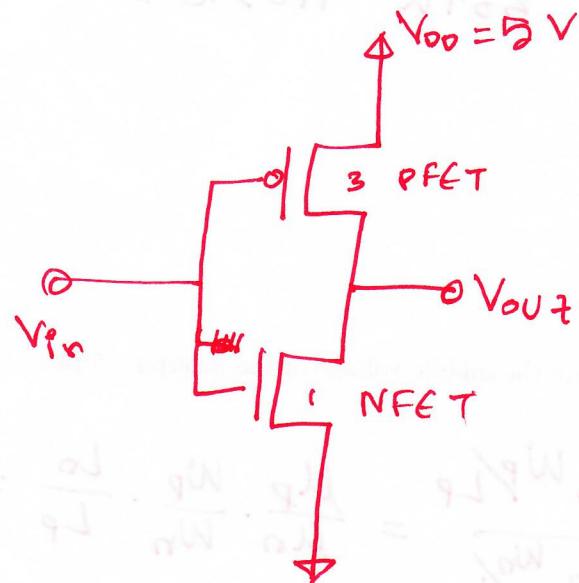
~~$$\Rightarrow \frac{C_n}{\chi} \cdot V_{DD,n}^2 f_{n+1} N_n \cdot x^2 = C_n V_{DD,n}^2 f_n N_n$$~~

$$\Rightarrow f_{n+1} = \frac{f_n}{x}$$

- frequency decreases by x^6

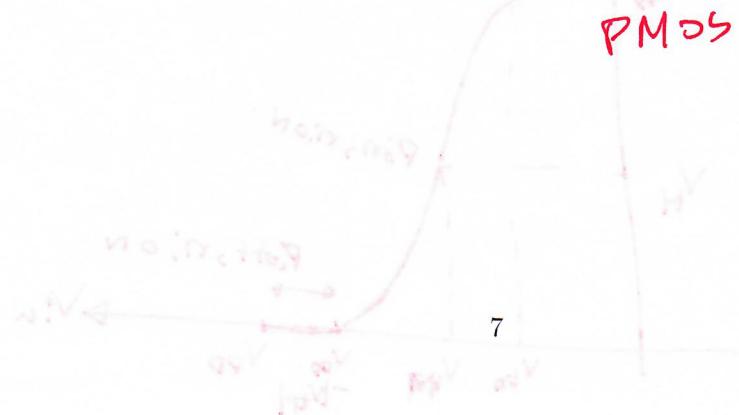
Q4 Inverter: Consider an inverter where $V_{t,n} = |V_{t,p}| = 1$ V, $W_n = W_p/3$, $L_n = L_p$, $\mu_n = 3 \times \mu_p$ and $V_{DD} = 5$ V. All the variables have their usual meaning. [Total 25 pts]

[Q4.1] Draw the circuit diagram of an inverter. [5 pts]



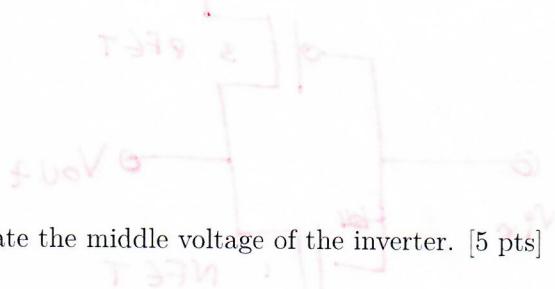
[Q4.2] If the input is a logical 1, what are the states of the n-MOSFET and the p-MOSFET (i.e., on or off)? What is the [5 pts]

If $V_{in} = V_{DD}$ \rightarrow NMOS will turn on
PMOS will turn off.



[Q4.3] If the input voltage is 2.5 V, what are the states of the n-MOSFET and the p-MOSFET (i.e., on or off)? [5 pts]

Both Mosfets will be ON.

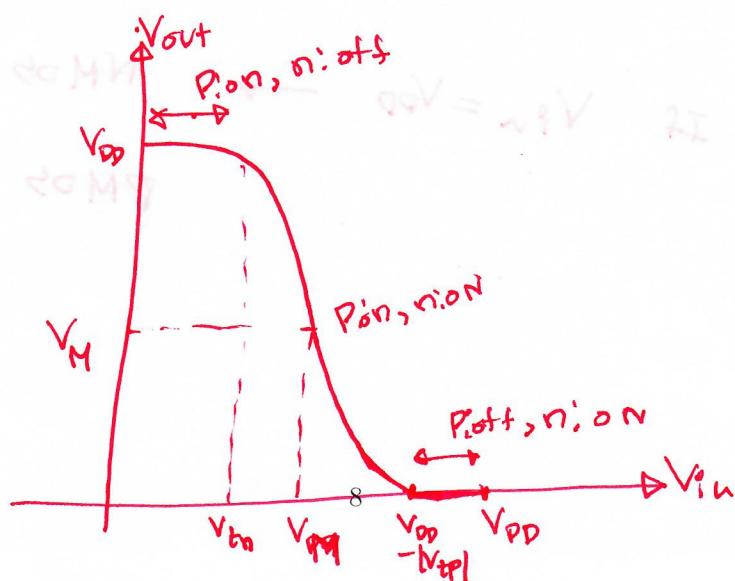


[Q4.4] Calculate the middle voltage of the inverter. [5 pts]

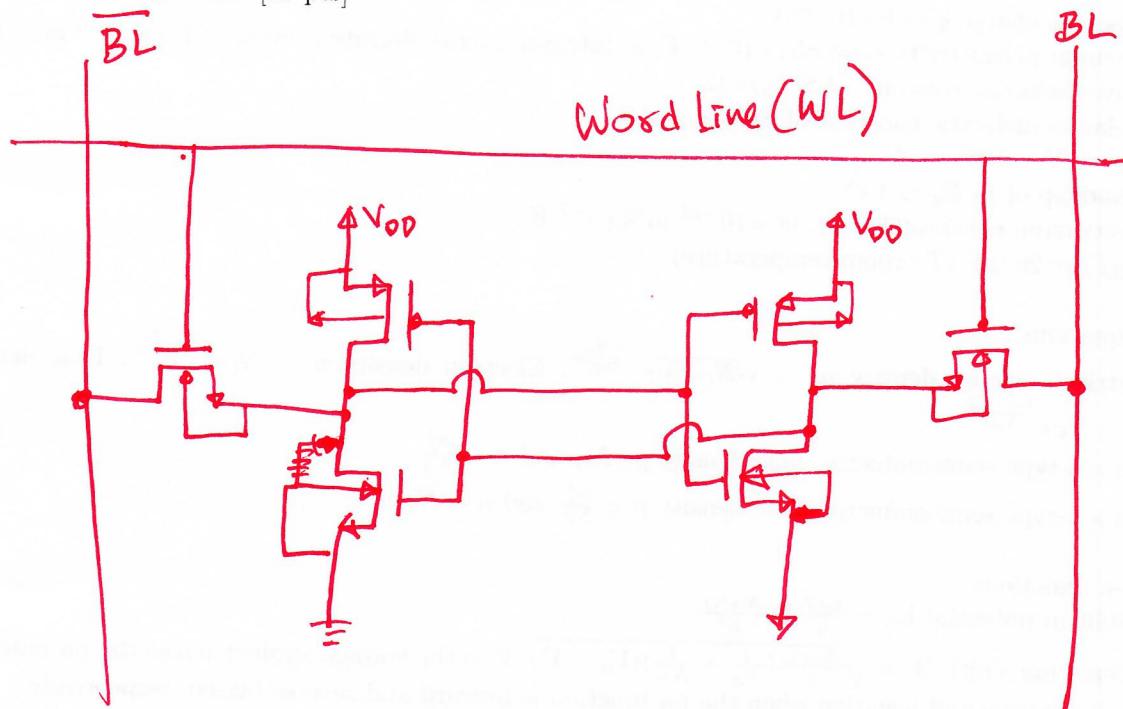
$$\frac{\beta_p}{\beta_n} = \frac{I_{Dp} W_p / L_p}{I_{Dn} W_n / L_n} = \frac{\mu_p}{\mu_n} \cdot \frac{W_p}{W_n} \cdot \frac{L_n}{L_p} = \frac{1}{3} \cdot 3 \cdot 1 = 1$$

$$\therefore V_M = \frac{\sqrt{\frac{\beta_p}{\beta_n}} (V_{DD} - |V_{tp}|) + V_{TN}}{1 + \sqrt{\frac{\beta_p}{\beta_n}}} = \frac{1 \cdot \frac{1}{\sqrt{3}} (5 - 1) + 1}{1 + 1} = 2.5 V$$

[Q4.5] Draw the approximate shape of the voltage transfer curve (VTC) of the inverter. Clearly indicate the middle voltage and all the relevant voltages in the curve. [5 pts]



Q5 SRAM: Draw the circuit diagram of a 6T SRAM cell. Clearly show the bit lines and the word line. [10 pts]



Q6 Circle the correct answer. The statements/questions are straightforward, no tricks are intended in the statements. [Total 5 pts (5×1 pt)]

[Q6.1] An increase in the power supply voltage decreases the interconnect delay. (True/~~False~~)

[Q6.2] Increasing the mobility of the semiconductor material increases the on-current of the MOSFET. (~~True/False~~)

[Q6.3] In a DRAM/cache system, if the hit rate is very low, DRAM access speed does not matter. (~~True/False~~)

[Q6.4] In p-type Si, the dopant is a group-III element. (~~True/False~~)

[Q6.5] Which technique is the most effective one when the off-state leakage (not capacitor charging and discharging) is the dominant consumption mode? (Dynamic voltage and frequency scaling/~~Race-to-dark~~)

$$\frac{I_D}{W} = \begin{cases} I_{sub-V_t} e^{\frac{V_G - V_t}{mk_B T}} (1 - e^{\frac{-qV_D}{k_B T}}); & \text{when } V_G < V_t \\ I_{sub-V_t} (1 - e^{\frac{-qV_D}{k_B T}}) + \mu C_{ox} \frac{1}{L} ((V_G - V_t)V_D - \frac{1}{2}V_D^2); & \text{when } V_G - V_t > V_D \\ I_{sub-V_t} (1 - e^{\frac{-qV_D}{k_B T}}) + \mu C_{ox} \frac{1}{2L} (V_G - V_t)^2; & \text{when } V_G - V_t < V_D \end{cases}$$

Body factor $m = 1 + \frac{C_D}{C_{ox}}$, where $C_D = \frac{\epsilon_0 \epsilon_{Si}}{W}$ (depletion capacitance).

Velocity saturated MOSFET: $I_{D,sat} = \mu C_{ox} W v_{sat} (V_G - V_t)$; where v_{sat} is the saturation velocity of the carriers.

On-state current at a given power supply voltage V_{DD} , $I_{ON} = I_D(V_{GS} = V_{DS} = V_{DD})$

Off-state leakage current at a given power supply voltage V_{DD} , $I_{OFF} = I_D(V_{GS} = 0, V_{DS} = V_{DD})$

Inverter:

$$\text{Middle voltage } V_M = \frac{\sqrt{\beta_p} (V_{DD} - |V_{tp}|) + V_{tn}}{1 + \sqrt{\frac{\beta_p}{\beta_n}}}$$

where $\beta_i = \mu_i C_{ox} (\frac{W_i}{L_i})$, $i \equiv p, n$. μ_i =mobility, W_i = i -type MOSFET width; L_i = i -type MOSFET gate length. MOSFET effective resistance $R_t = \frac{10V_B + 3V_t}{6\beta V_B^2} = \frac{10V_{DD} - 7V_t}{6\beta(V_{DD} - V_t)^2}$

where $V_B = V_{DD} - V_t$; $\beta = \mu C_{ox} (\frac{W}{L})$. μ =mobility, W = MOSFET width; L = MOSFET gate length.

Inverter delay is proportional to $R_t C_L$. $C_L = C_{g,p} + C_{g,n}$ where $C_{g,i}$ =gate capacitance of i -type MOSFET $= \epsilon_0 \epsilon_{ox} W_i L_i / t_{ox}$, $i \equiv p, n$.

Power dissipation due to charging and discharging $= C_L V_{DD}^2 f$; f being the frequency.

Resistance of a wire $R = \rho \frac{\text{Length}}{\text{Area}}$; ρ being the resistivity.

Capacitance of a parallel plate capacitor $C = \frac{\epsilon_0 \epsilon_{ox} \text{Area}}{\text{Thickness}}$.

Elmore delay $\delta_E = \sum_{1 \leq i \leq n} c_i \sum_{1 \leq j \leq i} r_j$, c_i and r_j being the capacitance and the resistance of i -th and j -th section respectively.

If all the segments have the same resistance and capacitance $\delta_E = n(n+1)rc/2$, n being the number of segments.

Chip junction temperature $T = T_A + PR_{thermal}$, T_A , P and $R_{thermal}$ being the ambient temperature, power and thermal resistance, respectively.

Thermal time constant $\tau_{thermal} = R_{thermal} C_{thermal}$, $C_{thermal}$ being the thermal capacitance.

Constants:

Electron charge $q=1.6 \times 10^{-19} \text{ C}$

Vacuum permittivity $\epsilon_0=8.854 \times 10^{-12} \text{ F/m}$ Intrinsic carrier density of Si $n_i = 1.5 \times 10^{16} \text{ m}^{-3}$ Relative dielectric constant of Si $\epsilon_{Si}=12$

Relative dielectric constant of $\text{SiO}_2 \epsilon_{ox}=4$

$N_C \approx N_V = 10^{25} \text{ m}^{-3}$

Bandgap of Si $E_g=1.1 \text{ eV}$

Boltzmann constant $k_B = 1.38 \times 10^{-23} \text{ m}^2 \text{ kg s}^{-2} \text{ K}^{-1}$

$k_B T/q=26 \text{ mV}$ ($T=\text{room temperature}$).

Equations:

Intrinsic carrier density $n_i = \sqrt{N_C N_V} e^{-\frac{E_g}{2k_B T}}$; Electron density $n = N_C e^{\frac{E_F - E_C}{k_B T}}$; Hole density $p = N_V e^{\frac{E_V - E_F}{k_B T}}$

In a p-type semiconductor, hole density $p=N_A$ and $n = \frac{n_i^2}{N_A}$.

In a n-type semiconductor, hole density $p = \frac{n_i^2}{N_D}$ and $n = N_D$.

p-n Junctions:

Built in potential $V_{bi} = \frac{k_B T}{q} \ln \frac{N_A N_D}{n_i^2}$

Depletion width $W = \sqrt{\frac{2\epsilon_0 \epsilon_{Si}}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (V_{bi} - V)}$; V is the voltage applied across the pn junction. V is positive and negative when the pn junction is forward and reverse biased, respectively.

Depletion width in p-side $W_p = \frac{N_D}{N_A + N_D} W$

Depletion width in n-side $W_n = \frac{N_A}{N_A + N_D} W$

Maximum electric field $E_{max} = \frac{q N_A W_p}{\epsilon_0 \epsilon_{Si}} = \frac{q N_D W_n}{\epsilon_0 \epsilon_{Si}}$

MOS Capacitor:

Gate voltage $V_G = V_{ox} + \psi_s$; V_{ox} is the voltage drop across the oxide and ψ_s is the surface potential (electrostatic potential at the oxide-semiconductor interface).

Oxide capacitance $C_{ox} = \frac{\epsilon_0 \epsilon_{ox}}{t_{ox}}$

Depletion width $W = \sqrt{\frac{2\epsilon_0 \epsilon_{Si}}{q N_A} \psi_s}$

Maximum depletion width $W_{max} = \sqrt{\frac{2\epsilon_0 \epsilon_{Si}}{q N_A} 2\psi_B}$

Threshold voltage $V_t = \frac{\sqrt{4\epsilon_0 \epsilon_{Si} q N_A \psi_B}}{C_{ox}} + 2\psi_B$; $\psi_B = \frac{|E_i - E_F|}{q}$

MOSFET:

Long channel MOSFET (square law model):

$$\frac{I_D}{W} = \begin{cases} 0; & \text{when } V_G < V_t \\ \mu C_{ox} \frac{1}{L} ((V_G - V_t)V_D - \frac{1}{2} V_D^2); & \text{when } V_G - V_t > V_D \\ \mu C_{ox} \frac{1}{2L} (V_G - V_t)^2; & \text{when } V_G - V_t < V_D \end{cases}$$

Long channel MOSFET (square law model with correction for subthreshold current):