Midterm 2

● Graded

Student

Guan-Shi Chen

Total Points

100 / 100 pts

Question 1

Q1

20 / 20 pts

✔ **– 0 pts** Correct

– 4 pts One Incorrect

– 8 pts Two Incorrect

– 12 pts Three Incorrect

Question 2

Q2

20 / 20 pts

✔ **– 0 pts** Correct

– 5 pts incorrect 2.1

– 5 pts incorrect 2.2

Question 3

Q3

40 / 40 pts

Q3.1 [10 pts]

✔ **– 0 pts** Correct

– 2 pts Missing $N_n = \frac{A_{c,n}}{W_n L_n}$

– 3 pts Express the chip area and transistor area in terms of the scaling factors (x for dimensions, 1.05 for chip area increase) incorrectly

– 3 pts The equation was set up to solve x incorrectly
$\frac{N_{+n+1}}{N_n} = 2$

– 2 pts wrong answer x

Q3.2 [20 pts]

✔ **– 0 pts** Correct answer

– 10 pts incorrect chip power
chip power = power per transistor * number of transistor,

– 10 pts incorrect the ratio of number of transistor for two subsequent generations
$N_{n+1} = 1.05x^2 N_n$

– 4 pts incorrect power per transistor

– 4 pts incorrect total gate Cap of a transistor

– 1 pt Wrong answer

– 4 pts f_n is not equal to f_{n+1}

– 4 pts incorrect scaling for V_{DD}

Q3.3 [10 pts]

✔ **– 0 pts** Correct answer

– 2 pts Wrong answer because of wrong answer in Q3.2

– 10 pts Wrong answer & missing $\frac{P_{chip,n+1}}{P_{chip,n}} = 1$

Question 4

Q4

20 / 20 pts

✔ **– 0 pts** Correct

No questions assigned to the following page.

ECE 3030: Physical Foundations of Computer Engineering

Spring 2024
Midterm Test 2
April 3, 2024
Time: 1 hr 15 min
Instructor: Asif Khan

Name: Guan-Shi Chen

Instructions:

1. There are 8 pages in this test. Count the number of pages and notify the proctor if you are missing a page.
2. Read all the problems carefully and thoroughly before you begin working.
3. This is an OPEN everything EXCEPT FOR collaboration exam.
4. A list of constants and equations is provided on pages 7, 8.
5. You are required to answer all 4 questions. There are 100 total points. Observe the point value of each problem and allocate your time accordingly.

Q1	20 pts
Q2	20 pts
Q3	40 pts
Q4	20 pts
Total	100 pts

6. Show all your work and circle/underline your final answer. For numerical answers, write the units. Write legibly. If I cannot read it, it will be considered a wrong answer. Do all work on the space provided; use scratch paper when necessary. Turn in all scratch paper, even if it did not lead to an answer.
7. Download this template and write on your electronic device or print this template and write on the print if you can. Writing on a blank paper and clearly marking each questions is also fine. You are required to upload PDF/pictures of either the completed template or just your answers.
8. Report any and all ethics violations to the instructor/proctor.

Sign your name on ONE of the two following cases:

Guan-Shi Chen

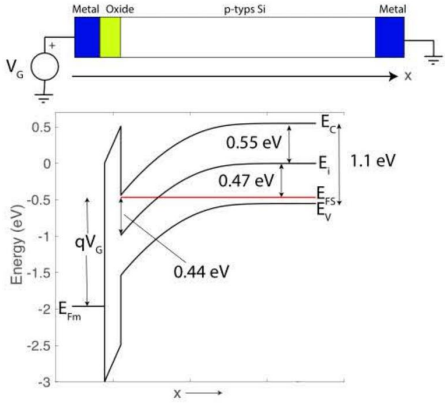
I DID NOT observe any ethical violations during this exam:

I observed an ethical violation during this exam:

Question assigned to the following page: 1

Q1 Circle the correct answer. All variables have their usual meaning. [Total 20 pts (5 × 4 pt)]

[Q1.1] For the band diagram of a MOS capacitor is shown in figure , is the gate voltage V_G larger than the threshold voltage V_t? **(Yes / No)**



[Q1.2] Increasing threshold voltage increases the off-current. **(True / False)**

[Q1.3] The on-current of a MOSFET does not depend on the power supply voltage. **(True / False)**

[Q1.4] In an inverter, when the input voltage is 0, the n-MOSFET is off and the p-MOSFET is on. **(True / False)**

[Q1.5] In a CMOS inverter, the p-type MOSFET has a larger width than that in the n-type MOSFET. **(True / False)**

Question assigned to the following page: 2

Q2 **Current-voltage characteristics of a MOSFET:** The following figure shows how the drain current I_D in a long channel MOSFET changes as a function of the gate voltage V_{GS} at given value of the drain voltage V_{DS}. The range of the V_{GS} range for different modes of operation (cut-off, saturation and linear) also indicated. [Total 20 pts]

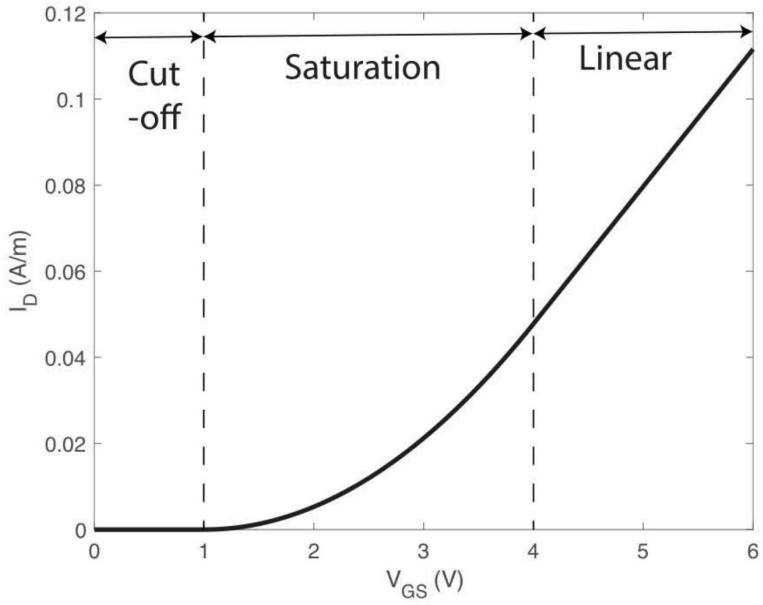


Figure 1: MOSFET $I_D - V_{GS}$ characteristics.

[Q2.1] What is the threshold voltage V_t of the MOSFET? [5 pts]

$V_t = 1\,V$

[Q2.2] What is the value of the drain voltage V_{DS}? [15 pts]

$V_{DS} = V_{GS} - V_t = 4\,V - 1\,V = 3\,V$

Question assigned to the following page: 3

Q3 **Scaling:** Consider that all three physical dimensions of MOSFETs (W, L, t_{ox}) are downscaled by factor of x and the power supply voltage, V_{DD} and the threshold voltage, V_t are decreased by a factor of y in every subsequent generation. In addition, the total area of the chip, A_c, also increases by 5% in every subsequent generation. [Total 40 pts]

[Q3.1] If, in every subsequent generation, the total number of transistors doubles, what is the nominal value of x? [10 pts]

$$N_n = \frac{A_c}{W_n \cdot L_n} \qquad \frac{1.05 A_c}{\frac{L_n}{x}\frac{W_n}{x}} = 1.05 x^2 \frac{A_c}{W_n \cdot L_n} = 2 \frac{A_c}{W_n \cdot L_n}$$

$$1.05 x^2 = 2 \rightarrow x = 1.38$$

[Q3.2] Consider the clock frequency and the total active/dynamic chip power of the n-th generation are f_n and $P_{chip,n}$. Find an expression of the ratio of total chip powers of two subsequent generation, $P_{chip,n+1}/P_{chip,n}$ in terms of x, y, f_n and f_{n+1}. [20 pts]

(Assume # of transistor does NOT double) $P_n = C_{L,n} V_{DD,n}^2 \cdot f_{,n} \rightarrow P_{chip,n} = C_{L,n} \cdot V_{DD,n}^2 \cdot f_n \cdot N_n$

$$N_{n+1} = \frac{A_{chip} \cdot 1.05}{\frac{1}{x^2} W_n L_n} = 1.05 x^2 N_n$$

$$P_{chip,n+1} = \frac{1}{xy^2} C_{L,n} \cdot V_{DD,n}^2 \cdot f_{n+1} \cdot 1.05 x^2 N_n$$

$$= \frac{1.05x}{y^2} f_{n+1} \cdot C_{L,n} V_{DD,n}^2 \cdot N_n$$

$$\frac{P_{chip,n+1}}{P_{chip,n}} = \boxed{\frac{1.05x}{y^2} \frac{f_{n+1}}{f_n}}$$

Question assigned to the following page: 3

[Space for Q3.2]

[Q3.3] What is the relation between f_{n+1} and f_n if you wanted the total active/dynamic chip power to remain the same across generations. [10 pts]

$$\frac{P_{chip,n+1}}{P_{chip,n}} = \frac{1.05X}{Y^2} \cdot \frac{f_{n+1}}{f_n} = 1$$

$$f_{n+1} = \frac{Y^2}{1.05X} f_n$$

f_n would increase by a factor of $\frac{Y^2}{1.05X}$ every subsequent generation

Question assigned to the following page: 4

Q4 Explain in short why it necessary to have cache memories in today's microprocessor technology. [Total 20 pts]

Cache memory is neccessary in modern day microprocessors because the other memory types, like DRAM, FLASH, and Magnetic drives. If lower speed memory were used, there would be CPU clock cycles that are not used. The time waiting to fetch memory will result in wasted clock cycles. The cache is faster, which means more clock cycles can be used for processing data.