**ECE 3030: Physical Foundations of Computer Engineering**
Fall 2021
Homework 8—Total points 100
Due on Saturday 11/20/2021 at 11.59am. In case of a late submission, you will be penalized by 50 points for each day after the submission deadline has passed. You will receive no score if you submit after the solution has been posted.

Q1 According to the scaling model proposed by Dennard *et al.*, in every subsequent generation, all three physical dimensions ($W$, $L$, $t_{ox}$), the power supply voltage $V_{DD}$ and the threshold voltage, $V_t$ are downscaled by factor of $x$ ($x > 1$). Show that in this scenario, the clock frequency can be increased by a factor of $x$ while keeping the chip power density (in W/cm$^2$) keeping the same. [40 pts]

Q2 In the scenario where, in each subsequent generation, you could downscale only the three physical dimensions ($W$, $L$, $t_{ox}$) by a factor of $x$ but had to keep $V_{DD}$ and $V_t$ fixed, how would you have changed the clock frequency? [30 pts]

Q3 Consider an inverter with its input voltage $V_{in} = 0$. Why would the inverter dissipate power even in this case? [20 pts]

Q4 In the first generation, assume delay is 20ns and a chip consumed 1.3W. After 20 generations with scaling of x=2 at each generation, what should be a chip's gate delay and power consumption? [10 pts]