ECE 3030: Physical Foundations of Computer Engineering
Fall 2022
Homework 10—Total points 100
Due on at .

Q1 What are the reasons that, in an inverter, you would want the PMOSFET to be wider than the NMOSFET? Write at least two reasons. [Total 30 pts]
Solution to Q1:

(a) To make the delays associated with both logic level $0 \rightarrow 1$ and $1 \rightarrow 0$ transitional (or equivalently voltage level $0 \rightarrow V_{DD}$ and $V_{DD} \rightarrow 0$ transitions, respectively) at the inverter output equal to each other.

(b) To make the voltage transfer curve of an inverter symmetric.

Q2 **SRAM Array:** Consider the SRAM array shown in figure 1. Say you want to read all the cells in row 2. What is the sequence of operation you will need to perform? Make sure that, after your prescribed operations, you keep the data in the cells you read intact. [Total 40 pts]

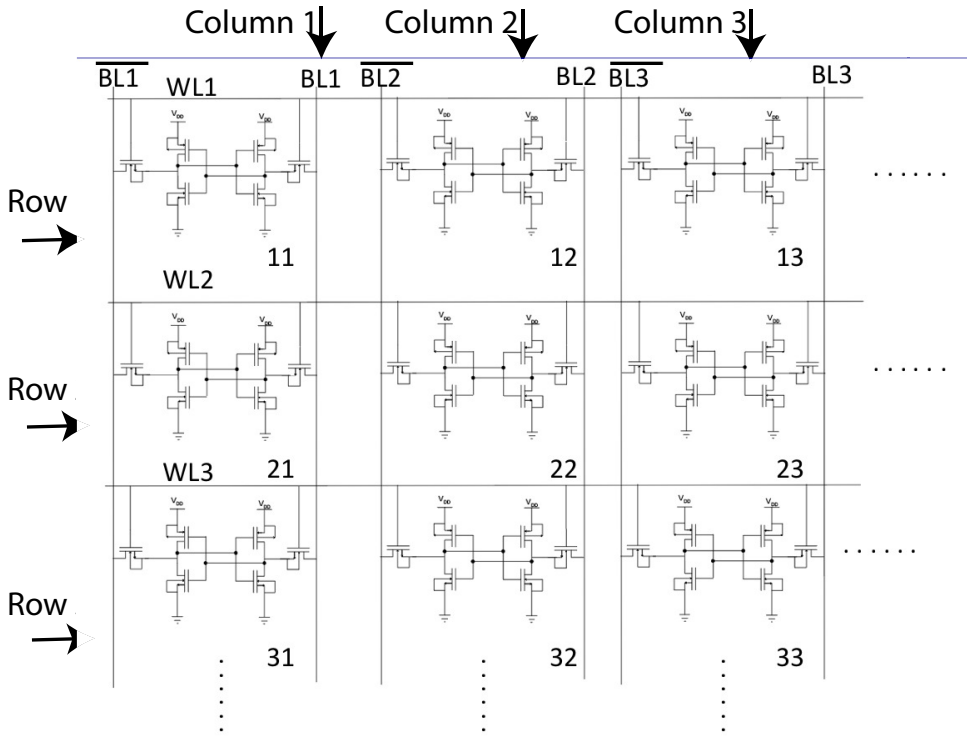


Figure 1: An SRAM array.

Solution to Q2:

Ans: The sequence of operation we will need to perform is:

1. Precharge BL1, $\overline{BL1}$, BL2, $\overline{BL2}$, BL3, $\overline{BL3}$ to VDD
2. Set WL2=VDD, while keeping WL1 and WL3 to 0 (In this way we can read all the cells is row 2 simultaneously).
3. Compare VBL1 and V$\overline{BL1}$. If VBL1>V$\overline{BL1}$, read = 1, if VBL1<V$\overline{BL1}$, read=0.
4. Similarly read the other two cells as well by comparing VBL2, V$\overline{BL2}$ and VBL3, V$\overline{BL3}$ respectively.
   In SRAM, data in the cells remains intact after the read operation because depending on the data stored in the cells, the voltages of the Bitlines change, which we then compare to perform the read operation. The data stored in the cells do not change.

Q3 Consider an inverter operating a power supply voltage V_{DD}. Assume that $\mu_n/\mu_p = 3$ and $(W_p/L_p)/(W_n/L_n) = 3$. Make the necessary assumptions to get to an answer for the following questions. [30 pts]

[Q3.1] How will the delay and active power per device change as you increase V_{DD}? Explain with equations.

[Q3.2] How will the delay and active power per device change as you increase the doping density of both the N- and the P-MOSFET? Explain with equations.

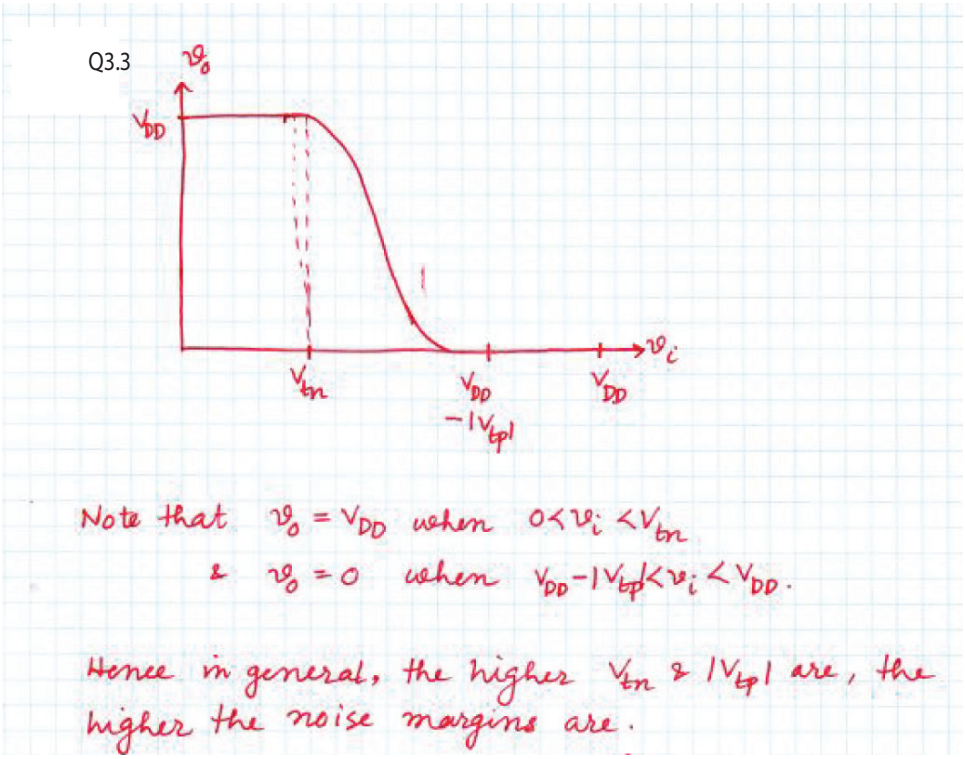
[Q3.3] How will the noise margins change as you increase the doping density of both the N- and the P-MOSFET? Explain with equations and figures.

Solution to Q3:

Delay $\tau = \frac{C_L V_{DD}}{I_{ON}}$. Active power per device $P_{active} = C_L V_{DD}^2 f$.

Q3.1: Frequency f is constant; $V_{DD} \uparrow$.
$I_{ON} \propto (V_{DD} - V_t)^2$
$V_{DD} \uparrow \Rightarrow \tau \propto \frac{V_{DD}}{(V_D D - V_t)^2} \downarrow$
$V_{DD} \uparrow \Rightarrow P_{active} = C_L V_{DD}^2 f \uparrow$

Q3.2: Frequency f is constant; Doping density$\uparrow$.
Doping density$\uparrow \Rightarrow V_t \uparrow \Rightarrow I_{ON} \propto (V_{DD} - V_t)^2 \downarrow \Rightarrow \tau \downarrow$
Doping density$\uparrow \Rightarrow P_{active} = C_L V_{DD}^2 f$ remains constant.



Q4 Explain the concept of fanout and its significance in CMOS inverter design. Discuss why it is advisable to have a higher fanout for the PMOSFET compared to the NMOSFET in CMOS inverters. Provide at least two reasons. [20 pts]

Solution to Q3: Having a higher fanout for the PMOSFET compared to the NMOSFET in CMOS inverters helps to improve voltage level restoration, enhance noise immunity, and maintain signal integrity, ultimately leading to more reliable and robust circuit performance.