

MODULE 2 - PART A

ELECTRICAL CHARACTERISTICS OF A MOSFET

In this module we are going to look at MOSFETs. We will look at both nMOSes and pMOSes and their current - voltage ($I-V$) characteristics as well as their Capacitance Characteristics.

That is, we will discuss :-

① Current - Voltage characteristics of MOS transistors (often called the $I-V$ characteristics)

Within this there are 3 main sub-topics :-

- nMOS long channel MOSFET
→ the word 'long' is subjective here
We will define what we mean by 'long' later.
- water model of a MOS transistor

The water model gives a very intuitive picture of what goes on in a MOSFET.

Since this is not a device course, we will not have the opportunity

to go into the physics of these devices to a great extent and so the water model is a good way of intuitively grasping the main concepts without having to write down equations or understanding the underlying physics in the almost details.

This takes us to the Shockley Model.

- Shockley Model of a MOSFET

This is of course named after Shockley who was one of the pioneers of semiconductors and the inventor of the transistor. The Shockley model is based on some of the initial models that he had derived all the way back in the 50s and the 60s.

② Capacitances of a MOSFET

Again this is something we are going to just give you an overview of. The capacitance of a MOSFET is a lot more complex, & there are several

non-linearities involved which we are not going to discuss in this course. If you take advanced courses on VLSI or a course on devices down the road, you will find a more detailed description and treatment of capacitance.

③ Advanced MOSFET topics

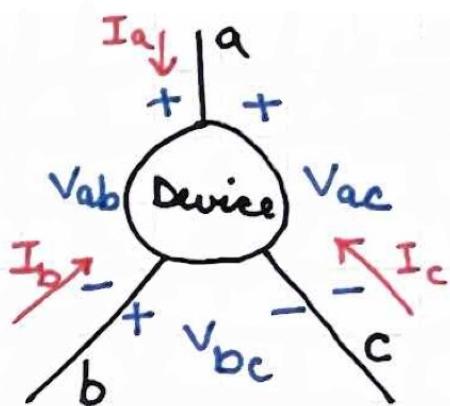
We will look at the challenges of the modern day MOSFET and a new phenomenon that happens because as opposed to the long channel MOSFETs, today's MOSFETs are what we call 'short channel' MOSFETs.

Now let's start with some basic notations.

IEEE Standard Device Notations

From ECE 2040, we know that if we have a 3-terminal device with terminals a, b & c,

- V_{ab} is the voltage betⁿ
 $V_a + V_b$ where
 a is '+ve'
 + b is '-ve'



and $V_{ab} = V_a - V_b$

If $V_{ab} > 0$, then a is at a higher potential than b. i.e.
 $V_a > V_b$.

Also, $V_{ba} = V_b - V_a = - (V_b + V_a)$
 $= - (V_a - V_b) = - V_{ab}$

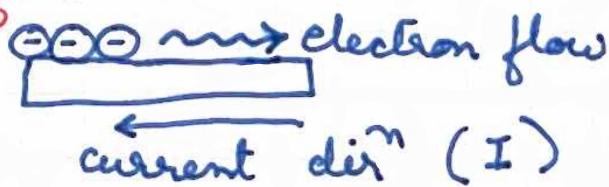
- V_a is the voltage of terminal a relative to some standard terminal (which is typically GND) i.e.

$$V_a = V_a - V_{GND} = V_a - 0 = V_a$$

$$\therefore V_{GND} = 0 \text{ (same for } V_b \text{ & } V_c\text{)}$$

- I_a is the current flowing into terminal 'a'. By convention current flowing 'into' a terminal is '+ve' and 'away' from a terminal is '-ve'.

Note:- e's flow in the opp. dirⁿ to that of the current.



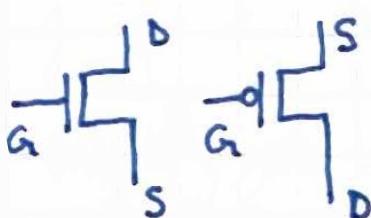
- Typically, we use uppercase V, I to denote DC values and lowercase v, i to denote ac values.

Let us now look at the working principles of a TRANSISTOR.

In ECE 2020, we treated transistors as IDEAL SWITCHES.

We can draw a table showing the relⁿ betⁿ the gate-to-source voltage V_{GS} and the operation of the nmos & the pmos.

VOLTAGE CONDN	nMOS	VOLTAGE CONDN	pMOS
$V_{GS} = V_{DD}$ (supply or i)	 ON ($G_s = 1$)	$V_{GS} = -V_{DD}$	 ON ($G_s = 0$)
$V_{GS} = 0$ (gnd; 0)	 OFF ($G_s = 0$)	$V_{GS} = 0$	 OFF ($G_s = 1$)



For an:-
nMOS \rightarrow D is at a higher potⁿ than S

pMOS \rightarrow S is at a higher potⁿ than D

We treated transistors as switches and were only concerned with the 2 states ON + OFF of the nMOS + the pMOS.

IN ECE 2020,

We had built inverters, NAND gates, CMOS logic, F/Fs etc using this principle. (switch-level understanding)

Now, in this course, we want to understand not only the logic characteristics but also the electrical characteristics.

This means :- ① We no longer will consider the nMOS/pMOS as a perfect short in the ON state. But will assume they have finite resistances & carry finite current.

The corollary to this is that :-

- ② The nMOS & the pMOS in the OFF state is not a perfect open i.e. even with $V_{GS} = 0$, there is a little amount of current called leakage current or cut-off current (not desired but still happens) flowing through the device.

So instead of thinking of the transistor as a switch (like we did in 2020), we will start thinking of it as a DIMMER.

So when we turn it on, it is not a perfect short and when we turn it off, it is not a perfect open.
($R_{ON} \neq 0$ and $R_{OFF} \neq \infty$)

To understand the electrical characteristics of the transistor, we need to:-

- ① Model the I-V (current-voltage) char. of a MOSFET **AND,**
- ② Understand the power / performance characteristics of logic blocks (adder, multiplier, F/F etc) which are designed using these transistors.

To understand the power / performance, just knowing the I-V char. is not enough.

Now, **WHAT** do we mean by **PERFORMANCE?**

For example,

When the input of an inverter switches from 0 to 1, the output switches from 1 to 0, but this does not happen instantaneously.

Like every other physical process, there is a **DELAY** involved, no matter how small (pico secs/nano-
secs for an electronic switch using these transistors)

To understand & model this delay, let us start by looking at the eqⁿ. for current.

$$I = C \frac{\Delta V}{\Delta t} \text{ or, } \Delta t = \left(\frac{C}{I} \right) \Delta V$$

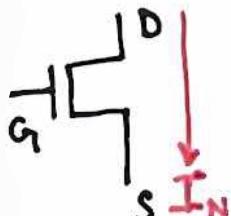
where, Δt = Time to charge or discharge the capacitor C

From this eqⁿ, we see that, if we know only the I-V char. (i.e. I & ΔV) then this won't be enough to model the performance. ∵ Apart from the I-V char., we also need to know the Capacitance Model of the MOSFET.

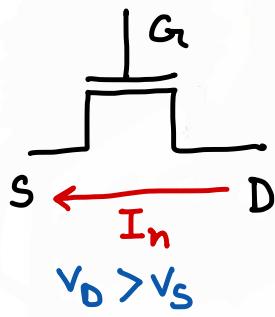
The capacitances determine how fast the transistor can switch on & off (i.e. how fast the nodes are charging & discharging). ∵ Capacitances will help us to determine the speed of devices & ckt's.

This is what we will discuss in this Module.

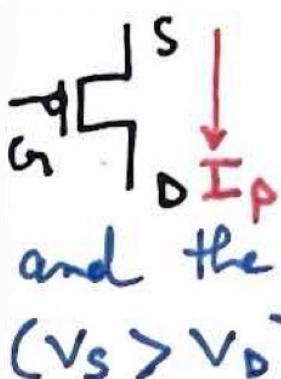
Let us consider an nMOS Transistor



The D & the S are physically identical.



What sets these apart is that for an nMOS, D is at a higher potential than the S (opposite is true for a pMOS)



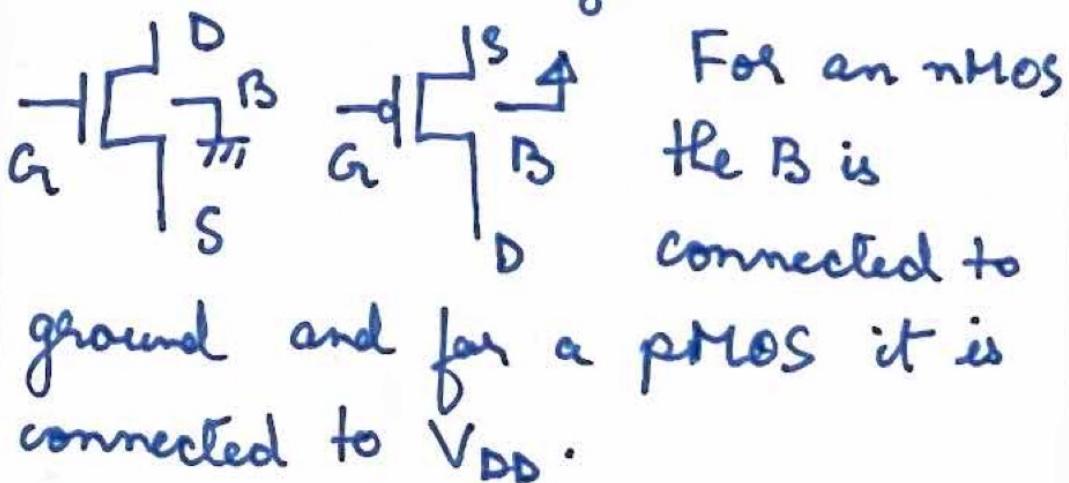
In the case of an nMOS current flows from D to S and the opp. is true for a pMOS.
($V_S > V_D$)

Here the voltages, V_S , $V_D + V_G$ are all in reference to (w.r.t) the Body terminal of the nMOS which is connected to ground.

In this course, we will look at what the BODY of the transistor is, briefly, but we will not go into great details. That would again take us to device physics which we don't want to do.

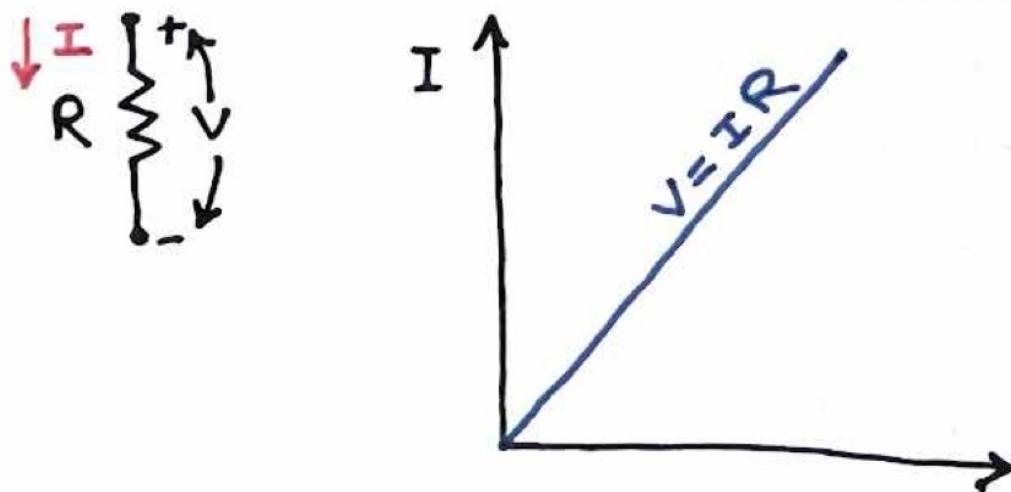
So, apart from the 3 active terminals of a MOSFET, which are responsible for the transistor action (I & V), we also have a fourth terminal which plays a

SECONDARY ROLE in the behaviour of a transistor and this is called the Body (B).



Let us start to model the I-V char. of a transistor. But we will do this intuitively without looking at any eq's. Equations are only a way of expressing our intuitions, so start with intuitions all the time. We will start with a very basic understanding of current & voltage. When we talk of I & V, we always put I on the y-axis & V on the x-axis because voltage is the independent variable & I is the dependent variable in our case.

Experimentally, we apply voltage to the terminals, and measure the terminal currents.



We apply a particular voltage and measure the current and plot it on this $I-V$ curve.

Sometimes we may apply a negative voltage and then we will plot in the 3rd quadrant, but we will go into that later on.

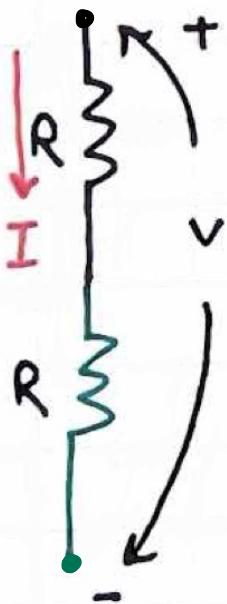
- Let us start with a very basic $I-V$ char. of a resistor (above) Ohm's Law holds in this case.

We apply a voltage V across the resistor R and I is the current that flows through it.

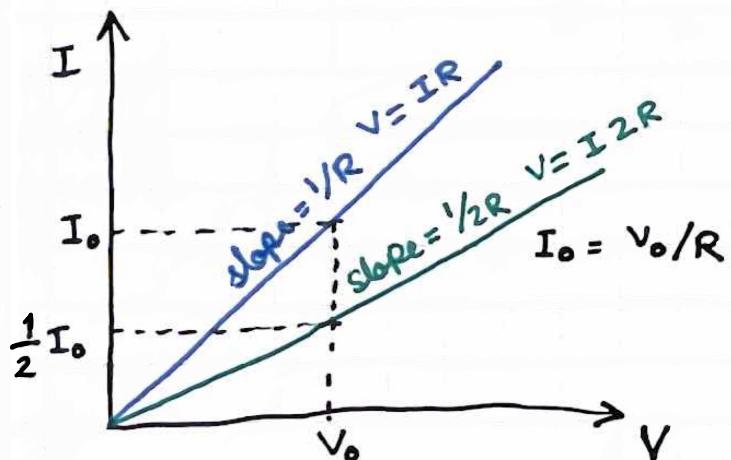
Ohm's Law dictates $V = IR$.

∴ This will be a straight line. $I = \frac{V}{R}$

Now let us modify this a little bit and add another identical resistor in series.



Here, the voltage V is applied across the entire series connection and hence the total resistance is $2R$. ∴ As per Ohm's Law, $V = I 2R$ ∴ For a given voltage, now the current will be half $I = \frac{1}{2} \left(\frac{V}{R} \right)$



We often characterize the I-V characteristics by the slope of this curve.

For the 1st curve (straight line) the slope is $1/R$ ($y = mx$, where m is the slope)

For the 2nd line, the slope reduces to $1/2R$

\therefore The more resistance we have, the lesser the current and the flatter the curve (I-V char.)

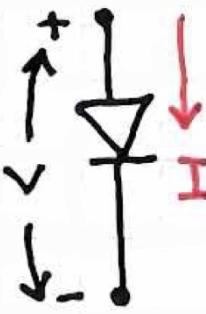
Now, this is easy to understand.

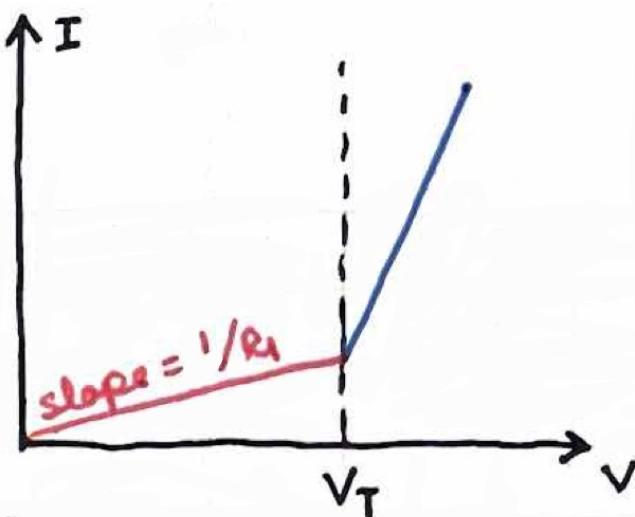
Let us take this to the next level. We will now look at another 2-terminal device - a DIODE.

I-V Characteristics of a Diode :-

As ckt. designers, here we will not think about the physics of operation of the DIODE (depletion, diffusion, p-n etc.)

What we are only concerned about is,
if we apply a voltage,
how much current we get
out of this device.

 We apply a voltage v across the terminals of this diode and observe the current I flowing across it.



Let us try to draw the $I-v$ char. of this diode.

We can consider the diode to be like a resistance but its resistance is NOT CONSTANT.

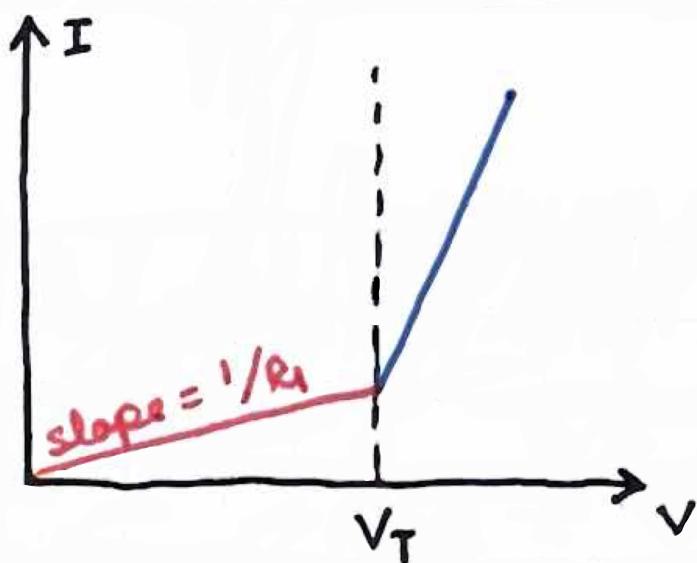
The resistance of a diode is what is known as piece-wise resistance.

There are 2 different resistances depending on the voltage applied across its terminals.

$R = \begin{cases} R_1 \text{ (which is a large resistance)} & \text{when the voltage } V < V_T, \\ & \text{(where } V_T \rightarrow \text{ a particular voltage)} \\ \text{AND,} \\ R_2 \text{ (which is a small resistance)} & \text{when the voltage } V \geq V_T \end{cases}$

V_T in the case of a DIODE is called the cut-in voltage.

The current however cannot change abruptly and is thus, continuous.



In the 1st region where $V < V_T$, R_1 is large and hence the curve/line is flatter. The slope of this line is $1/R_1$.

In the 2nd region where $V > V_T$, R_2 is small and the line is steeper and the slope here is $1/R_2$ and the current will be much higher.

Now if you've seen before how a diode works, you will recognize this as the I-V char. of a DIODE. But of course in a TRUE DIODE the current is exponential and there are more complicated things going on. But as a GENERAL ABS-TRACTION, we can think of the DIODE as a linear

device with 2 linear regions.
∴ We can call this a
PIECEWISE LINEAR I-V
CHARACTERISTICS.

While this is not the
best way of representing
the behaviour of a DIODE
(since the current is
exponential) but it is
good enough for us as
ckt. designers and for this course.

When we are thinking in terms
of 3150 or VLSI in general,
abstractions are very important.

We don't want to
complicate the analysis
of a full μ -processor

by thinking about how
exponential the current is.

We want to remove all
these details aside and
think of the diode as a
piecewise linear device

with a high resistance
and a low resistance
separated by a cut-in
voltage (V_T).

We have looked at :-

- ① Simple Resistors
- ② Resistors with a switching threshold (V_T)
(Diodes)

Now, we will look at :-

- ③ Devices with voltage sensitive resistances
(theoretical devices). While :-

- ① was linear
- ② was piecewise linear

Now ③ will be NON-LINEAR.

Let us draw this
voltage sensitive resistor.



We want to
draw the I-V char.

of this device.

Let us assume that
the resistance R is a

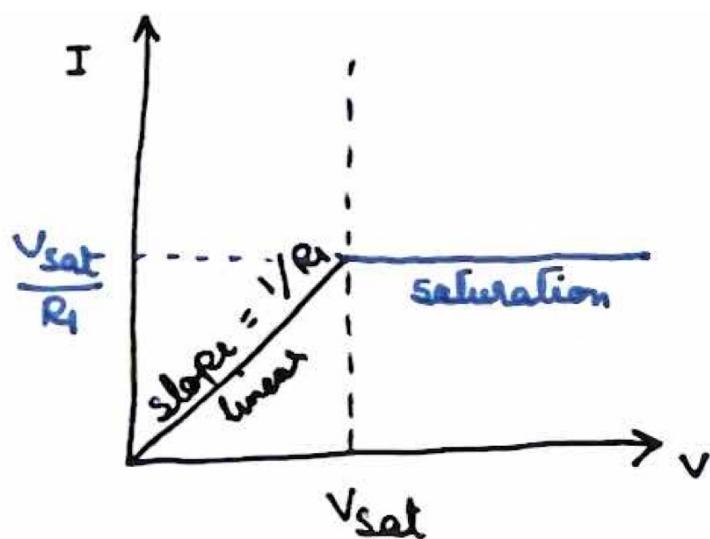
function of V , such that,

$$R = \begin{cases} R_1 \text{ (a constant)} \\ \text{when } V < V_{sat} \\ \text{AND,} \\ V \left(\frac{R_1}{V_{sat}} \right) \text{ when} \\ V > V_{sat} \end{cases}$$

Please realize that when we are talking about resistances in this context, we are not talking about TRUE resistances but rather the DIFFERENTIAL Resistances.

i.e. R is not V/I but $\Delta V / \Delta I$ which is actually the (slope) of the $I-V$ char.

When the voltage V is less than V_{sat} , we will have a linear plot ($I-V$ char.)



and the Slope here is $1/R_1$

When v reaches v_{sat} , then

$$R = \frac{v}{\frac{R_1}{v_{sat}}} \text{ and the current}$$

$$I = \frac{v}{R} = \frac{v}{\frac{v}{\frac{R_1}{v_{sat}}}} = \frac{v_{sat}}{R_1}$$

which is a constant quantity.

And as v increases, R is still $\frac{v}{\frac{R_1}{v_{sat}}}$ and the I is still $\frac{v_{sat}}{R_1}$.

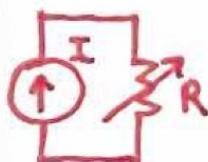
\therefore The current will be given by a straight line (slope = 0) and does not change with voltage anymore. This is the reason we use the subscript 'sat' in v_{sat} , to indicate that after this voltage is reached, the current saturates.

∴ Here we have 2 distinct regions

① Linear ② Saturation

This is in fact, the I-V char. of a transistor. It first behaves as a resistor and then after a certain voltage is reached, it acts as a current source.

We know from ECE 2040, that a current source delivers a constant current and the voltage across it is dependent on the external circuit only.

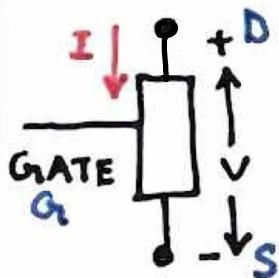


Voltage across R is given by IR . If R changes, v changes but I remains const.

Now we will extend this concept and look at the :-

I-V characteristics of a 3-terminal device

This will be very similar to what we just saw, except that, we will have a 3rd terminal known as the GATE.



Here too, we will assume that,

$$R = \begin{cases} R_1 (\text{const.}) & \text{for } V < V_{\text{sat}} \\ V \left(\frac{R_1}{V_{\text{sat}}} \right) & \text{for } V \geq V_{\text{sat}} \end{cases}$$

Now the difference here is, that R_1 is a function of the GATE to Source Voltage V_{GS} .

We can also mark the Gate G, Source S and Drain D, so that this device starts looking more and more like a transistor.

Now, if V_{GS} is high, R_1 is low

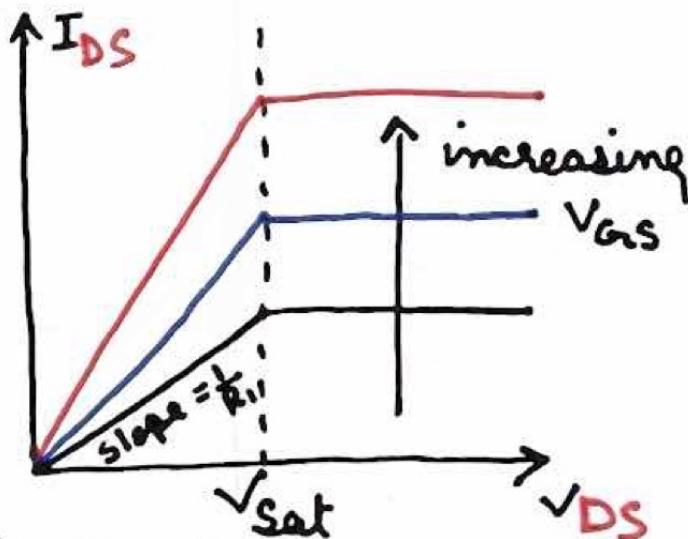
\therefore As V_{GS} increases, $\frac{1}{R_1}$ (slope) \uparrow

Also, as $V_{GS} \uparrow$, $\frac{V_{\text{sat}}}{R_1}$ also \uparrow

\therefore If we draw the I-V char. of this device, it will be very similar to the previous example except for the fact that now we have a third variable V_{GS} and as $V_{GS} \uparrow$, the slope of the linear region will become steeper and steeper and the saturation

current will also be higher
and higher (V_{sat} / R_i)

We can draw this as below:-



So this becomes a 3 terminal
device with a controlling terminal
 V_{GS} which determines R_i .

Also realize that we drew
the I-V char. here for I_{DS} +
 V_{DS} (Drain to Source current
and Voltage)

So this is a 3-terminal device
with some non-linearity that
has a current which is
dependant on the G voltage.

We will stop here with the I-V char. of basic elements and move on to looking at the structure of an actual MOSFET and see how this I-V char. translate for an actual transistor.

MOSFETs :-

(We want to specifically look at gate voltage and its effect on the channel)

Let us look at the structure of an nMOS. We will not look at the pMOS since it will just be complementary.

CONSTRUCTION OF THE NMOS :-

- Let us start with a piece of Silicon

- Then we have the Source & the Drain.

These are n^+ (heavily

doped with donor atoms
eg. Phosphorous P,
Arsenic As, GROUP V) and
thus, have an abundance of
electrons .

- The Body of the nMOS
is p-type and is called
the p-substrate . (starting
wafer) (sometimes it is
 $P^- \rightarrow$ lightly doped with
acceptor atoms eg .
Boron B, GROUP III)
- On top of the source +
the drain with a little bit
of an overlap on both sides ,
we have the GATE (G)
The whole thing is
called the GATE stack .
And we have the G
terminal on top of this .
The Gate stack is made

of 2 components →

① insulator below →
which used to be SiO_2
silicon dioxide for many
generations. Now we
have moved on to other
materials with higher ϵ
(permittivity) like hafnium
dioxide (HfO_2) + so on.

② Polysilicon / Metal
top → shaded (in figure below)

Used to be polysilicon
but now this is metallic
or a combⁿ of poly Si
and metal

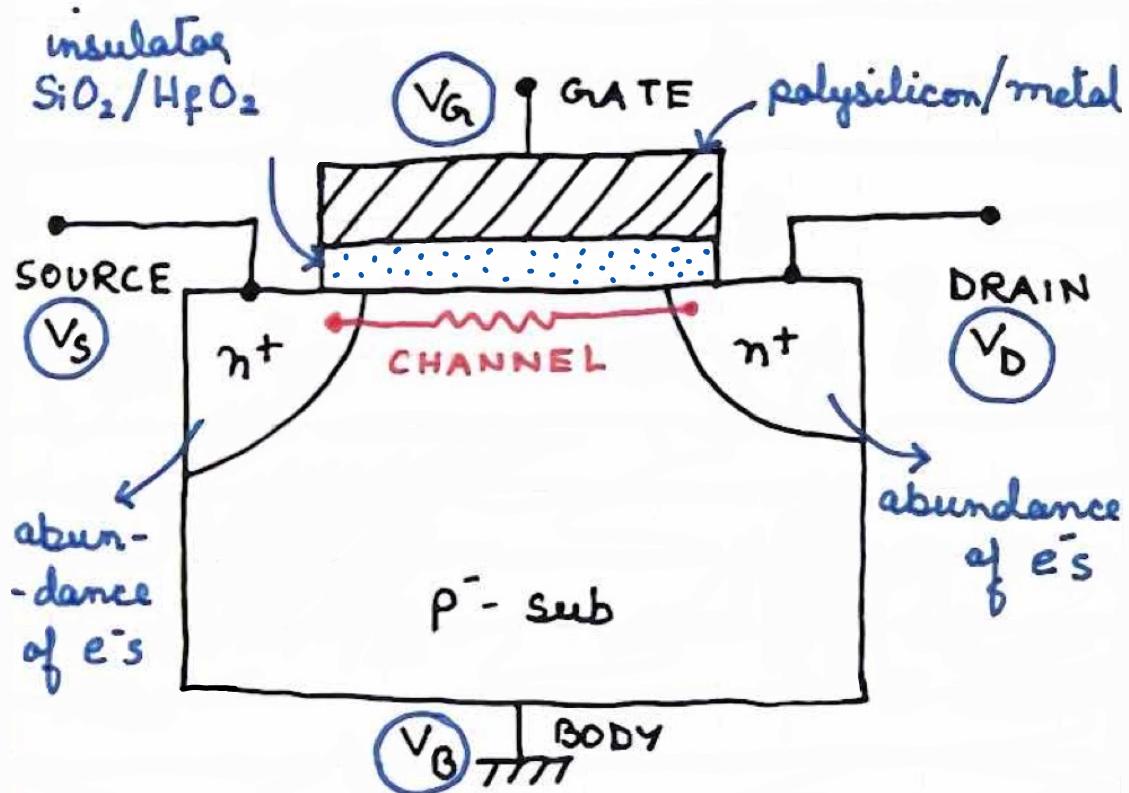
- Current flows from D to S and e⁻'s flow from S to D .
- This is the channel which offers a resistance to the flow of current . (drawn in red in the figure)

The charge flows through

This channel which is at the interface of the oxide + the Si

- The p-substrate has holes (not e's) and its other end is called the Body which is connected to the ground for an nMOS.

When we talk of voltages, we refer all of the voltages to the Body. Sometimes you will see that the voltages are also referred to the source (eg V_{GS} , V_{DS} etc.) This is because the source is the lower potential and in many cases we will tie the Source also to GND. (for an nMOS)



\therefore We can think of this nMOS as a resistor in series with a switch.

$$\text{---} \boxed{\text{L}} = \begin{cases} \text{---} \\ \text{---} \end{cases} \quad \begin{array}{l} \text{When, } V_{GS} = V_{DD} \\ \text{that is the ON state} \end{array}$$

of the nMOS, then the switch is closed

$$\therefore \begin{cases} \text{---} \\ \text{---} \end{cases} = \begin{cases} \text{---} \\ \text{---} \end{cases} \quad \begin{array}{l} \text{and it is just equivalent} \\ \text{to a resistor.} \end{array}$$

When, $V_{GS} = 0$, that is the OFF state of the nMOS, then the switch is open and it is just an open.

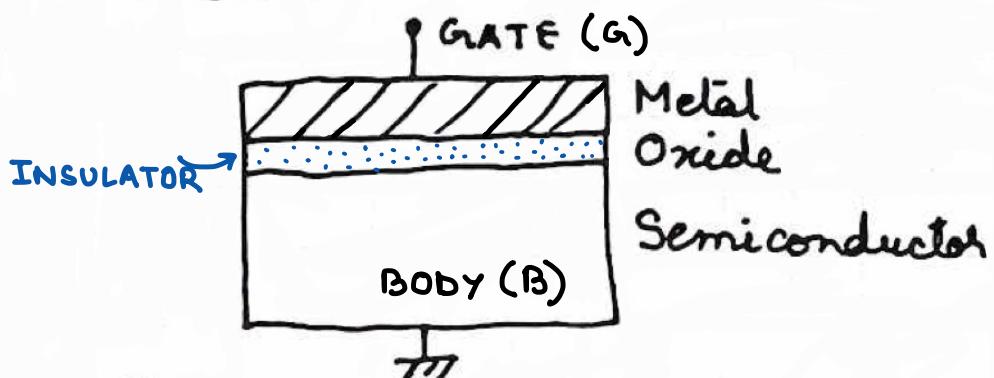
$$\therefore \begin{cases} \text{---} \\ \text{---} \end{cases} = \begin{array}{|c|} \hline \text{---} \\ \hline \text{---} \\ \hline \end{array}$$

If we look a little closely at the construction of an nMOS, we can see that, we have :-

- ① GATE that is METALLIC
(it has charge) M
- ② INSULATOR made of OXIDE O
- ③ SEMICONDUCTOR made S
of Si (Body)

And so we have the MOS structure.

This MOS structure shows us that the gate G and the body B of the MOSFET form a capacitance with the insulator sandwiched in between.



This is our MOS Capacitor.

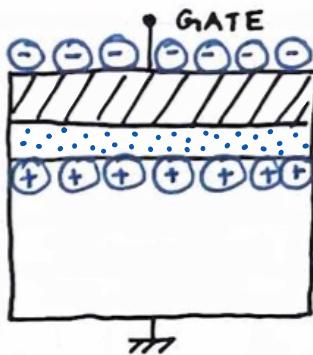
We will start by trying to understand the charge - voltage ($Q-V$) relationship in the MOS Capacitor.

Once we understand the charge, we will also understand the current.

So we will start with an intuitive understanding of the MOS Capacitor and then if we stick a Source & a Drain in there, it becomes a transistor.

So considering this capacitor first, there are 3 main regions of operation of the Capacitor that we are interested in.

ACCUMULATION REGION



$$\bullet V_G < 0$$

\therefore We have applied a negative potential.

There will be negative charge on the surface of the G.

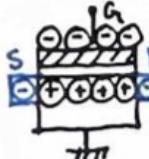
This will attract the holes in the p-substrate. But this will be close to the surface since there is an insulator present bet'n the metal & the Si.

\therefore We have a sandwich with the negative charge on one side and +ve charge on the other. This forms a capacitive structure & this is called the ACCUMULATION REGION. (charges get accumulated)

\bullet In this region :-

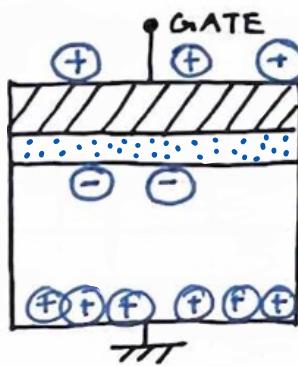
① Holes are attracted below the gate and form a +ve charge sheet.

② Since S + D have lots of e's and not holes, there is no continuity of charge and hence there is NO CURRENT



We need one type of charge for i to flow

DEPLETION REGION



- $V_G > 0$ but less than some voltage V_t which is the threshold voltage of the transistor.

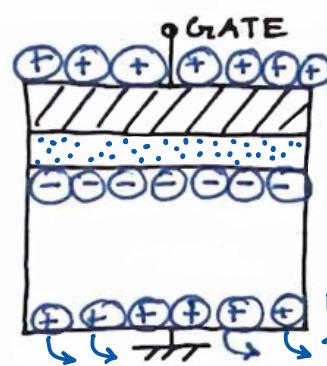
Now since V_G is a small quantity, we will have a small amount of +ve charge on the gate G.

This is still a capacitor so this small +ve charge will repel the charge built up on the surface of B. And the surface will now have a small amount of negative charge mostly from the ions *

This is called the DEPLETION REGION (since most mobile charges are now depleted from the surface of the B)

Here the barrier in the accumulation region is lowered but still only very energetic e's can cross this and so we will have very very little current since the quantity of e's that are able to cross the barrier isn't large enough. So this is still pretty much off & has not turned on yet.

INVERSION REGION



- Now we have the cond? where we turn on the gate with a large +ve voltage $V_G > V_t$ (threshold voltage)

This means we have a lot of +ve charge on the Gate surface and thus there will be a lot of e's on the Surface of the Body.

Here the barrier has been reduced to almost zero and the e's from the Source can easily enter the channel.

This is called the INVERSION REGION Here,

- Holes have moved further away
- Free electrons are attracted to the surface of the Body. Now there is a continuous path for e's to flow from S to channel to D and thus we have CURRENT flow.

* We will not consider this in our course

\therefore In a MOSFET, the gate voltage is responsible for bringing the e⁻s to the surface of the Body thereby lowering the barrier, and the voltage difference betⁿ the S & the D is responsible for the flow of e⁻s.

So the amount of charge is dictated by the gate and the current I_{DS} is dictated by V_{DS} .

So eventually we will see that we will come back to a current - voltage relationship that will look very similar to the I-V of the 3-terminal device that we had looked at earlier.

We looked at the charge + the voltage here and in the next part of Module 2 we will look at current.