

MODULE 3 - PART A

- In the last module (M2), we studied the operating principles of MOSFETS and we covered a little bit of the physics of these devices.

From this point onwards, we will not go into device physics any more but will continue to use the I-V characteristics that we had derived in M2.

- In this module, we will introduce the CMOS inverter.

In ECE 2020, we had treated the CMOS inverter as a binary logic gate. However, in this course (3150), we will look at the PHYSICAL CHARACTERISTICS of the CMOS inverter.

This includes :-

- ① DC characteristics of the CMOS inverter. This Module (3)
from the CMOS inverter, we can talk about other logic gates as well (Supplementary Material)
- ② Delay characteristics of CMOS gates and interconnects (M5)
- ③ Power Consumption of CMOS inverters and gates (M6)

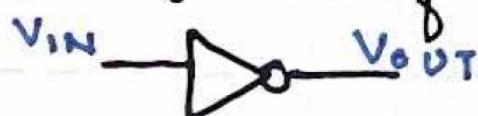
In this part (M3-P-A) of M3,
we will look at :-

DC characteristics of CMOS INVERTERS

DC characteristics → means
that after the changes in current
or voltage takes place, we
wait an infinite amount of
time so that all of these
parameters settle down, before
we start our measurements
(i.e. all switching effects are
gone → no transient and
hence we are in steady state)

From ECE 2020, we know :-

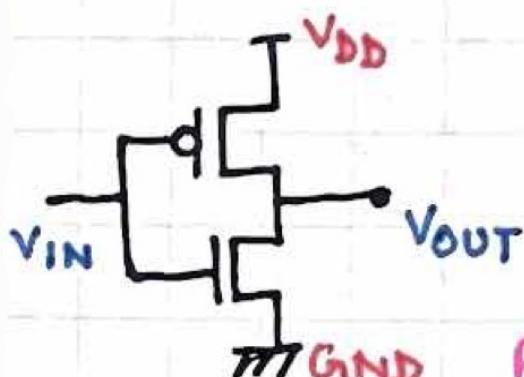
the symbol of an inverter is :-



the truth table of the inverter
is given by :-

V_{IN}	V_{OUT}	
0	1	$0 \rightarrow \text{ground}$
1	0	$1 \rightarrow \text{Supply}$ (V_{DD})

the CMOS circuit is drawn
as :-



You may remember from ECE 2020 that the pMOS

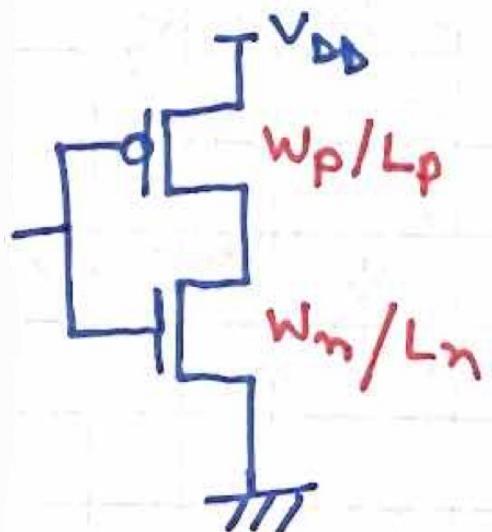
propagates a good 1 and the nMOS propagates a good 0. That is why we use pMOSes for the PUN and nMOSes for the PDN. (see supplementary material)

But this happens when we treat the inverter as a SIMPLE LOGIC GATE.

Now when we will study the DC characteristics, we will see what happens

When the input is neither 0 nor 1 but changes slowly from 0 to 1.

Let us start with the CMOS circuit of the inverter :-



Let the width of the PMOS be W_p & that of the nMOS be W_n .

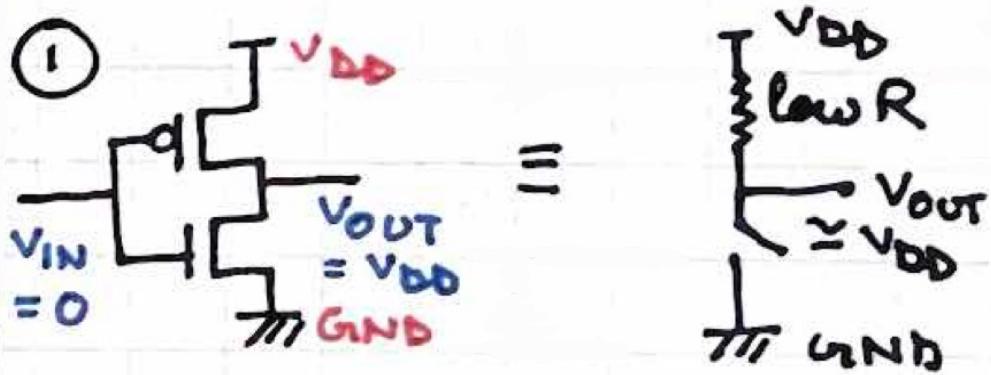
The length of the PMOS is L_p and the length of the nMOS is L_n .

In most cases we will assume the $L_p = L_n$

(given to us; in modern processes, we do not have much control over this)

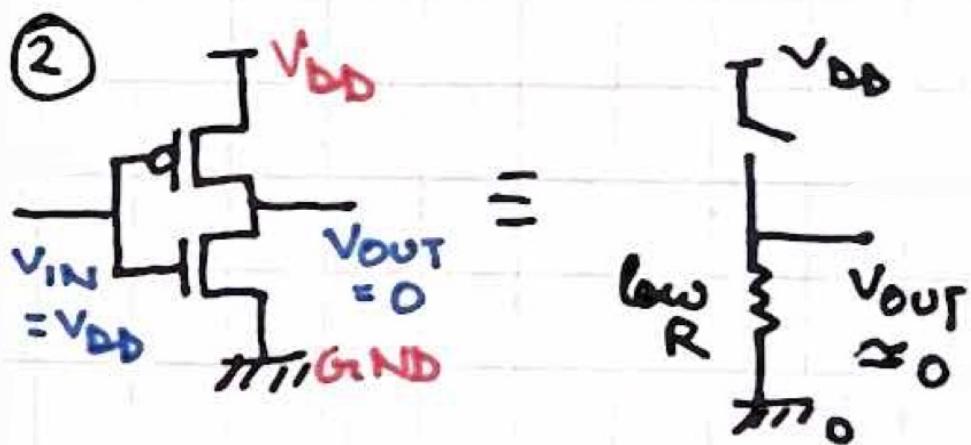
We will look at what happens with W_n and W_p

Let us again go back to ECE 2020 and look at the 2 DIGITAL conditions we had seen :-



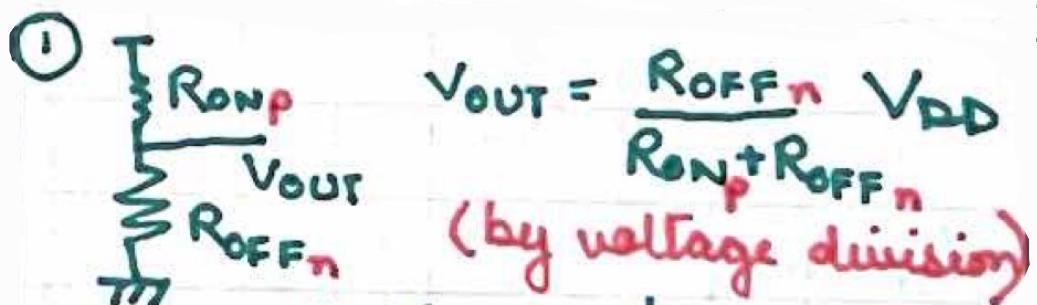
We can draw the resistance diagram as ↑

Here, nMOS → OFF
pMOS → ON



Here, nMOS → ON
pMOS → OFF

Why $V_{OUT} \approx V_{DD}$ in ① and $V_{OUT} \approx 0$ in ② ?



$$\text{or, } V_{OUT} = \frac{1}{1 + \frac{R_{ONP}}{R_{OFFn}}} \cdot V_{DD}$$

$R_{ON}/R_{OFF} \approx 10^3 \text{ to } 10^4$ modern
transistors \rightarrow similar for n + pmos

②

$$V_{OUT} = \frac{R_{ONn}}{R_{ONn} + R_{OFFP}} V_{DD}$$

$$= \frac{1}{1 + \frac{R_{OFFP}}{R_{ONn}}} \approx 0$$

as $\frac{R_{OFF}}{R_{ON}} \approx 10^3 \text{ to } 10^4$

Now we will study the DC characteristics of an inverter using the I-V models developed in M2.

Since this is a SIMPLE ANALYSIS for a long channel MOSFET (and here we are not considering short channel effects of nano-scaled transistors)

We will call this the
FIRST ORDER CMOS
ANALYSIS :-

In this analysis, we will consider the following :-

- ① The output level of the inverter, will be low when the input is high.

This output level is called V_{OL} , $V_{OL} \approx 0$

- ② The output level of the inverter will be high when the input is low.

This output level is called V_{OH} , $V_{OH} \approx V_{DD}$

- ③ The output level will have rail - to - rail voltage swing.

rail implies supply rail. Thus, the output level will swing from 0 to V_{DD} .

④ There is always a low impedance path to either V_{DD} or to GND but not to both. You know from ECE 2020 that the PUN & the PDN cannot be ON at the same time.

In Steady State there is no direct path from V_{DD} to GND.

⑤ No current is drawn into the GATE.

The Gate offers infinite input impedance and there is no DC path from the gate to any other terminal (G to S, D or B) (like you've seen in OP-AMPS in ECE 2040)

⑥ CMOS logic is ratio-less

This means that the ratio of W_p/W_n will not change the logic levels or the binary operations of the gate.

What do we mean by this?

We have seen that :-

① When $V_{out} \rightarrow \text{logic level 1}$

$$= V_{DD} \cdot \frac{1}{1 + \frac{R_{ONP}}{R_{OFFn}}}$$

Now, Current \propto Width

According to Ohm's Law,
we know,

$$\text{Current} \propto \frac{1}{\text{Resistance}}$$

\therefore We can say,

$$\text{Resistance} \propto \frac{1}{\text{Current}} \propto \frac{1}{\text{Width}}$$

\therefore From this, we can say,

$$\frac{R_{ONP}}{R_{OFFn}} \propto \frac{W_n}{W_p}$$

But the difference between the ON current and OFF current i.e. the difference betⁿ the ON resistance and the OFF resistance is so large ($\frac{R_{ON}}{R_{OFF}} = 10^{-3} \text{ to } 10^{-4}$) that the changes in W_n/W_p does not change the logic level 1 significantly.

Similarly,

② When $V_{OUT} \rightarrow \text{logic level 0}$

$$= V_{DD} \cdot \frac{1}{1 + \frac{R_{OFF}P}{R_{ON}n}} \text{ is}$$

also not affected by $\frac{W_p}{W_n}$

Now we will look at the
VOLTAGE TRANSFER
CHARACTERISTICS OF CMOS
INVERTER :-

Also known as the VTC.

Here we will :-

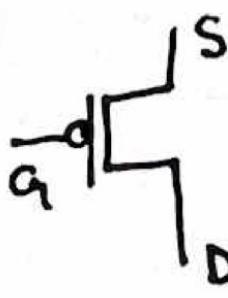
- ① Plot V_{OUT} as a function of V_{IN}
- ② Vary V_{IN} from 0 to V_{DD}
- ③ Find V_{OUT} at each value of V_{IN}

Observe :-

- ① When $V_{IN} = 0$, $V_{OUT} = V_{DD}$
 $\therefore (0, V_{DD})$ is a point in this plot
- ② When $V_{IN} = V_{DD}$, $V_{OUT} = 0$
 $\therefore (V_{DD}, 0)$ is also a point in this plot.

Before we start plotting the VTC, let us look at the characteristics of the PMOS:-

For the pMOS, the S is at


 a higher potential
 than the D.
 If the S is

fixed at V_{DD} (supply),
 we are gradually lowering
 the gate voltage V_G , so
 that $V_{SG} = V_S - V_G$ increases
 i.e. $V_{GS} = -V_{SG}$ decreases.

In the case of a pMOS, the
 threshold voltage is negative
 i.e. V_{thp} is a negative
 quantity.

Therefore, when the V_{GS} is
 more negative than this V_{thp} ,
 that is when the pMOS will
 turn ON.

$$\therefore V_{GS} \leq V_{thp} \text{ (both negative)}$$

$$|V_{GS}| \geq |V_{thp}| \rightarrow \begin{matrix} \text{ON} \\ \text{state} \end{matrix}$$

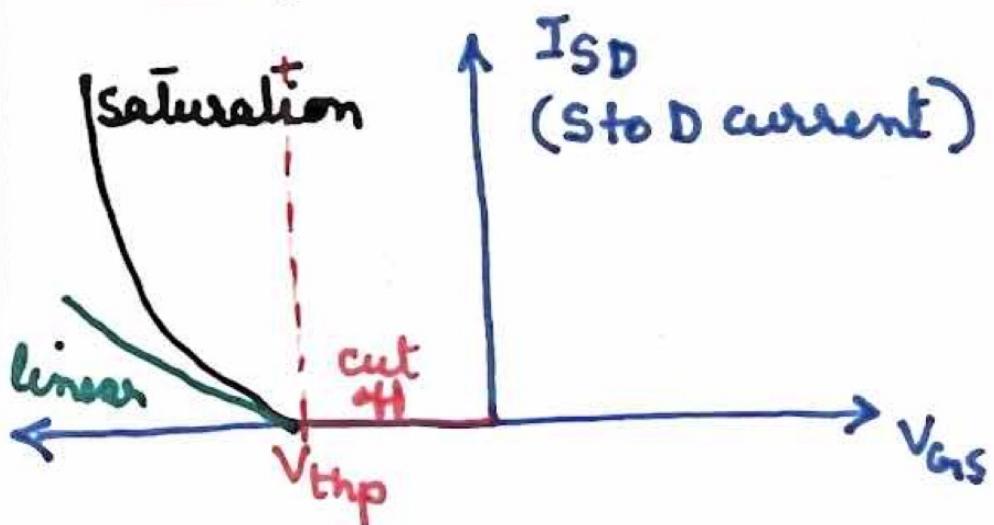
and, when,

$V_{GS} > V_{thp}$ (both negative)

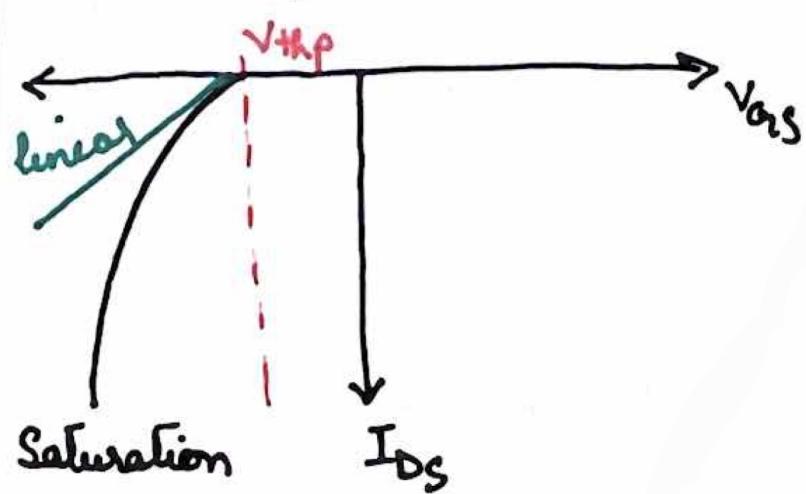
$|V_{GS}| < |V_{thp}| \rightarrow$ OFF
(cut-off)

Typically $V_{thn} \approx |V_{thpl}|$ is about 0.25 to 0.3 V

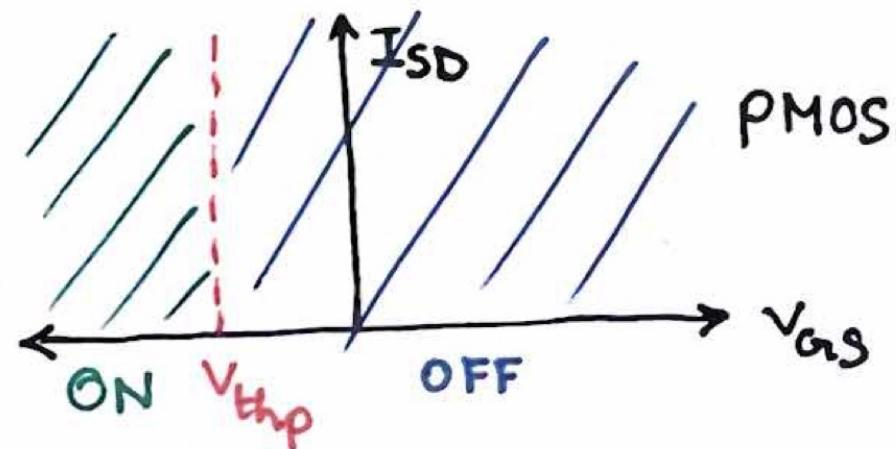
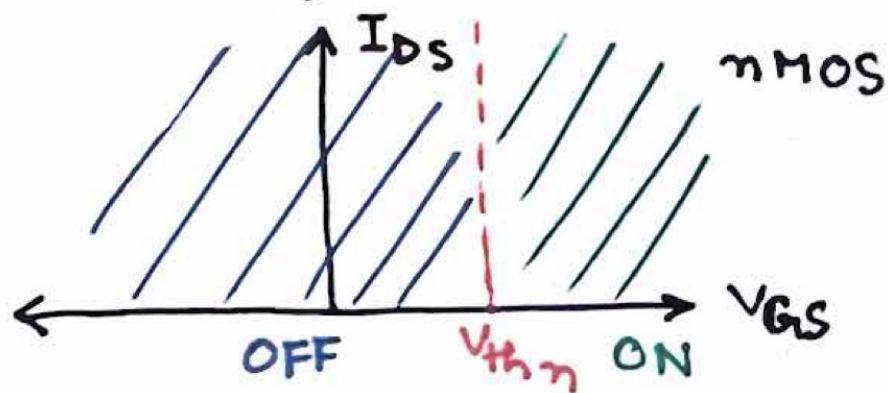
So if we draw the TRANSFER CHARACTERISTICS of the pMOS we have :-



Sometimes we can also draw this TRANSFER CHARACTERISTICS as I_{DS} vs V_{GS} (similar to that of the nMOS)



So if we compare this with the transfer characteristics of the nMOS,



Now, let us look at the OUTPUT CHARACTERISTICS of the pMOS :-

Here we are looking at I_{SD} vs V_{DS} for a particular V_G .

\therefore We fix V_{GS} and we are lowering V_D starting from V_{DD} towards 0.

$\therefore V_{SD} = V_S - V_D$ increases

i.e. $V_{DS} = -V_{SD}$ decreases

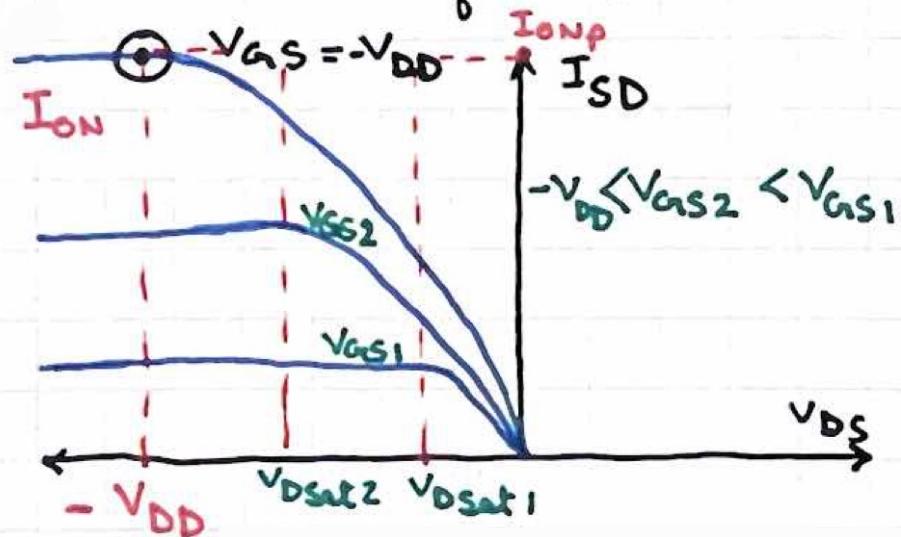
When $V_D \rightarrow V_{DD}$, V_{DS} is 0 since V_S is V_{DD} .

When $V_D \rightarrow 0$, V_{DS} is $-V_{DD}$

$\therefore V_{DS}$ goes from 0 to $-V_{DD}$

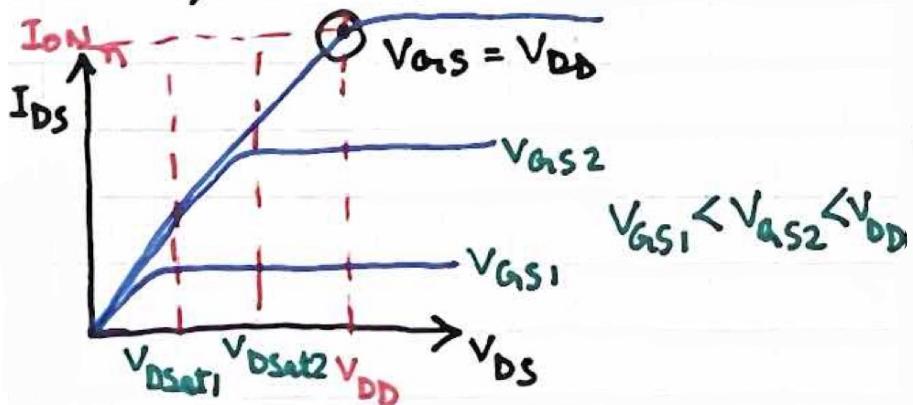
for each V_{GS} that we consider.

Now we draw the output characteristics of the pMOS as:-



\therefore The maximum current in this case is when $V_{GS} = -V_{DD}$ (we get I_{ONP})

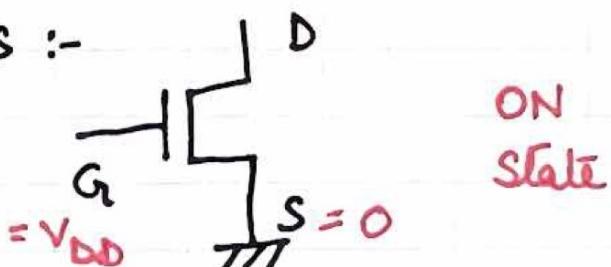
Whereas, in the case of an nMOS, we know :-



The maximum current in this case is when $V_{GS} = V_{DD}$
(we get I_{ONn})

Also, we see that, for an

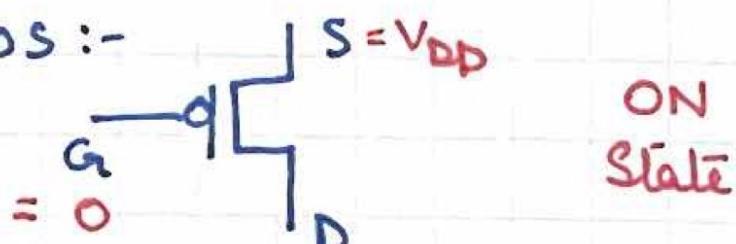
nMOS :-



As V_D goes from V_{DD} to 0,
the nMOS goes from
SATURATION TO LINEAR
region

For a pMOS, we see that,

pMOS :-

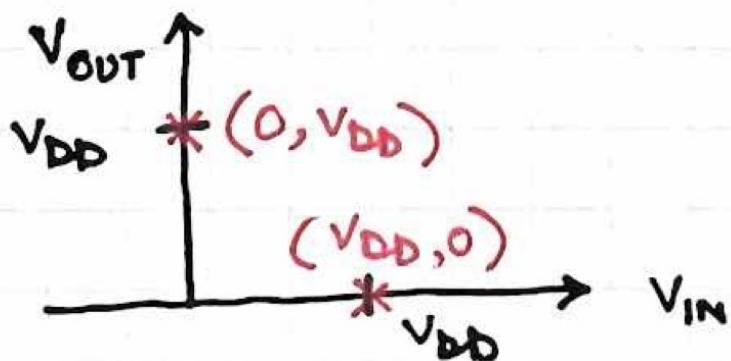


As V_D goes from V_{DD} to 0,

The pMOS goes from LINEAR to SATURATION region.

Now with this background we can start to draw the VTC of the CMOS inverter.

- ① We have already seen that when $V_{IN} = 0$; $V_{OUT} = V_{DD}$ and when $V_{IN} = V_{DD}$; $V_{OUT} = 0$
 $\therefore (0, V_{DD})$ and $(V_{DD}, 0)$ will be 2 points on this plot



Now we will study how to connect these 2 points on the V_{IN} vs V_{OUT} curve.

To do this, we will first

divide the plot into 5 separate REGIONS starting with $V_{IN} = 0$.

We will move along the x-axis, increasing V_{IN} and try to plot the corresponding V_{OUT} in the y-axis as we go.

This will be our task in the next part of MODULE 3.