

ECE 3150

Exam 2

Solutions



Question 1

5 pts

We use the same Euler path for PUN and PDN to prevent any cut or break in:

- contact and diffusion
- poly and diffusion
- diffusion and metal 1
- metal 1 and poly

EULER PATHS are an optimal path through a graph.

Using this principle we can figure out how to draw circuits with minimum diffusion region. We first find EULER PATHS for the PUN and the PDN separately so that we can draw continuous p-diffusion and n-diffusion lines. We then find a common EULER PATH for the PUN and PDN, so that the gate-ordering is the same for the PUN and the PDN. This ensures that the gate poly lines are continuous and there are no breaks between the gate polys of the PUN and those of the PDN.

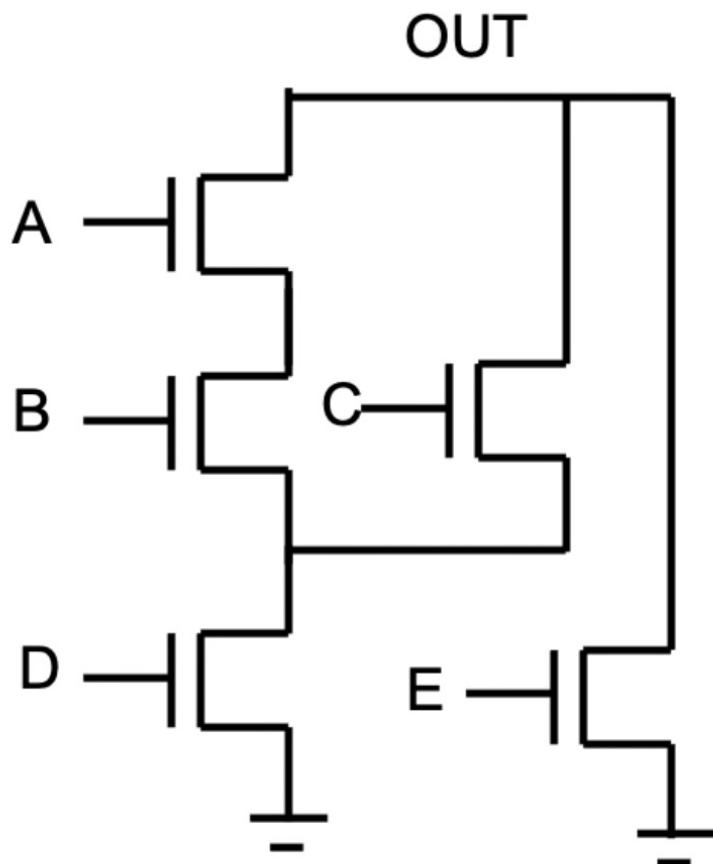
∴ Using the same EULER PATH for the PUN and the PDN prevents any cuts or breaks in the POLY and DIFFUSION.



Question 2

5 pts

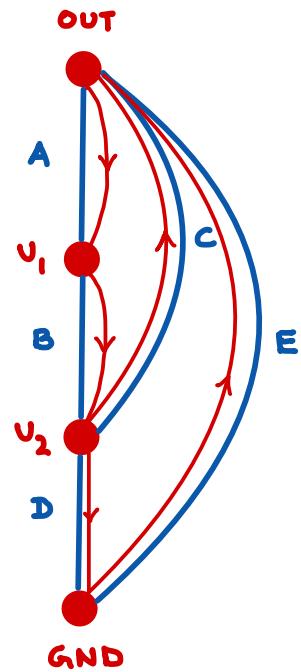
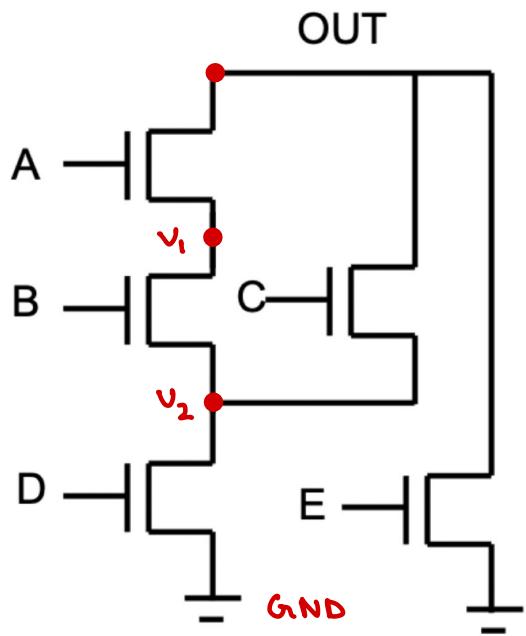
Consider the pull-down circuit shown below:



Which of the following statements is true?

-
- We cannot draw any Euler path even after rearranging the transistors
 - We do not have sufficient information to say if there is any Euler path in this circuit.
 - We can draw an Euler path of the PDN
 - We can draw a path with one diffusion break only
-

Here, we have a PULL-DOWN network. Let us try to draw the EULER PATH of this network.



The EULER PATH we have here is DEABC.

Please note that multiple EULER PATHS exist in this case
(eg. DECBA, ABDEC and so on)

∴ We can say that we can draw an EULER PATH of
the PDN.



Question 3

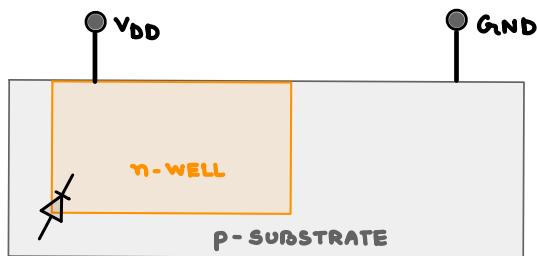
5 pts

The body of the transistor is connected to the supply in the following manner:

- VDD to NWELL and GND to p-sub to forward bias all the diodes
- VDD to p-sub and GND to NWELL to reverse bias all the diodes
- VDD to NWELL and GND to p-sub to reverse bias all the diodes
- GND to p-sub and NWELL to reverse bias all the diodes

We know that :-

if the p-n junction diodes are forward biased then current will flow from the p-substrate to the n-well and this causes unnecessary power consumption. So we want to reverse bias these diodes. These diodes are called PARASITIC DIODES.



So , all of the n-wells MUST be connected to V_{DD} and p-subs to G_ND as shown above to make sure that all of the parasitic diodes are reverse biased .

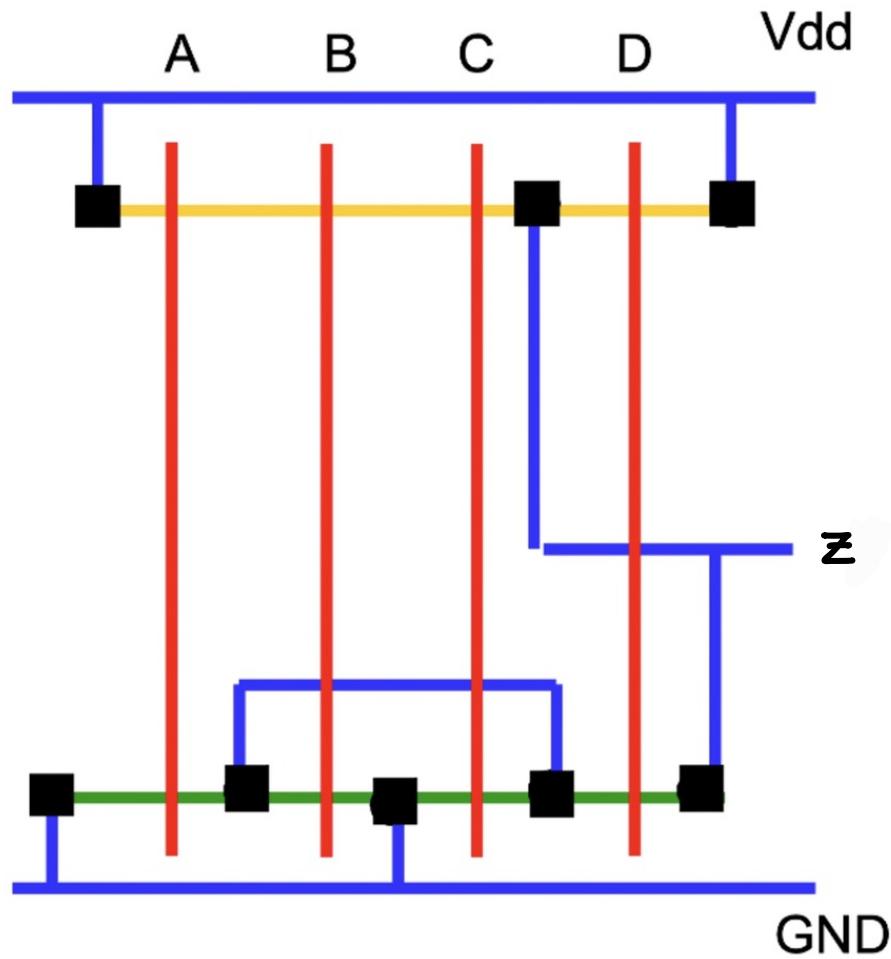
Thus , we connect V_{DD} to nWELL and G_ND to p-sub to reverse bias all the diodes .



Question 4

5 pts

Write down the Boolean expression corresponding to the following stick diagram:

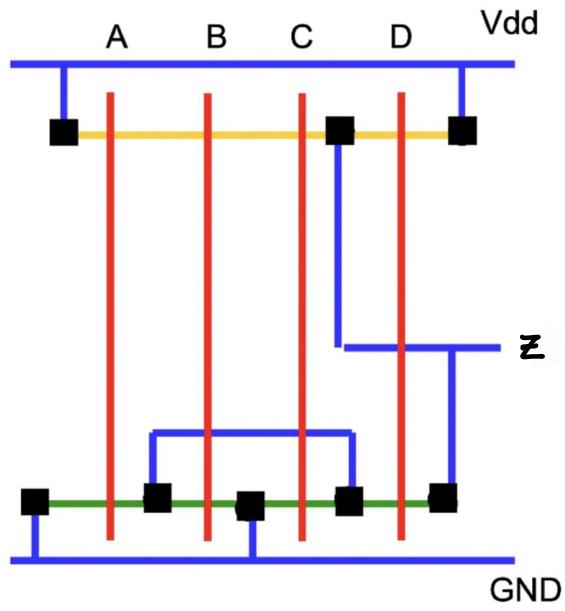


$$Z = A + \overline{BCD}$$

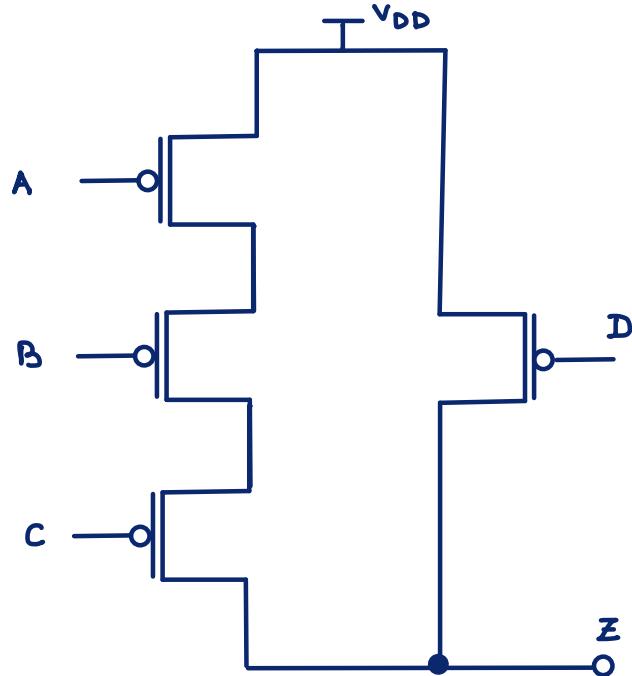
$$Z = \overline{ABC} + D$$

$$Z = \overline{(A + B + C)} \cdot D$$

$$Z = \overline{A + B + C} + D$$



The Pull-up Network can be drawn as below by inspecting the LAYOUT above.



From this PUN, we can write the BOOLEAN EXPRESSION for F

as,

$$Z = \bar{A}\bar{B}\bar{C} + \bar{D} = \bar{\bar{Z}} = \overline{\bar{A}\bar{B}\bar{C} + \bar{D}}$$

$$\text{or, } Z = \overline{\bar{A}\bar{B}\bar{C} \cdot \bar{D}} = (\bar{\bar{A}} + \bar{\bar{B}} + \bar{\bar{C}}) \cdot D$$

$$\text{or, } Z = \overline{(A + B + C) \cdot D}$$



Question 5

5 pts

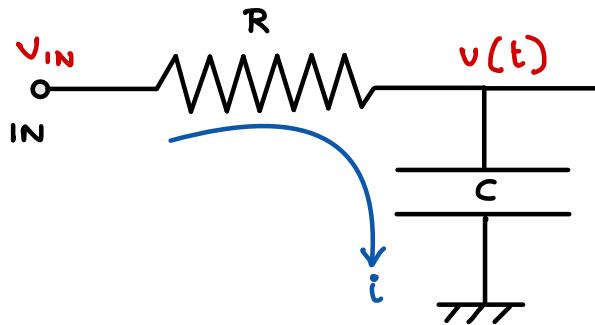
Consider an RC circuit where the capacitor voltage is initially charged to $V_{DD}/2$. The input signal now swings from $V_{DD}/2$ to V_{DD} . If we define the charging time (T_1) as the time for the capacitor voltage to reach $3/4 V_{DD}$, we can write:

T₁ = $\ln(2) RC$

T₁ = $\ln(4/3) RC$

T₁ = $\ln(1/2) RC$

T₁ = $\ln(3/4) RC$



The capacitor voltage is initially charged to $V_{DD}/2$.
i.e. $v(t) = V_{DD}/2$

The input v_{IN} now swings from $\frac{V_{DD}}{2}$ to V_{DD}

The current $i = \frac{V_{DD} - v(t)}{R} = C \frac{dv(t)}{dt}$

or, $\frac{dv(t)}{V_{DD} - v(t)} = \frac{1}{RC} dt$

or, $\int_{V_{DD}/2}^{v(t)} \frac{dv(t)}{V_{DD} - v(t)} = \frac{1}{RC} \int_0^t dt$ (integrating both sides)

or, $-\left[\ln(V_{DD} - v(t)) - \ln(V_{DD} - \frac{V_{DD}}{2}) \right] = \frac{1}{RC} t$

or, $\ln(V_{DD} - v(t)) - \ln \frac{V_{DD}}{2} = -\frac{1}{RC} t$

$$\text{or, } \ln \left(\frac{V_{DD} - v(t)}{V_{DD}/2} \right) = -\frac{1}{RC} t$$

$$\text{or, } \ln \left(2 - \frac{v(t)}{V_{DD}/2} \right) = -\frac{1}{RC} t$$

$$\text{or, } e^{-t/RC} = 2 - \frac{v(t)}{V_{DD}/2}$$

$$\text{or, } \frac{v(t)}{V_{DD}/2} = 2 - e^{-t/RC}$$

$$\text{or, } v(t) = \frac{V_{DD}}{2} (2 - e^{-t/RC})$$

given that, when $v(t) = \frac{3}{4}V_{DD}$, $t = T_1$ (charging time)

$$\therefore \frac{3}{4}V_{DD} = \frac{V_{DD}}{2} (2 - e^{-T_1/RC})$$

$$\text{or, } e^{-T_1/RC} = \frac{3}{2} - 2 = \frac{1}{2}$$

$$\text{or, } \ln \left(\frac{1}{2} \right) = -\frac{T_1}{RC}$$

$$\text{or, } T_1 = -RC \ln \left(\frac{1}{2} \right)$$

$$\text{or, } T_1 = RC \ln(2)$$



Question 6

5 pts

Using a CV/I model of delay, we can deduce that the charging delay of an inverter is:

- inversely proportional to the square of the PMOS mobility
- independent of the PMOS mobility
- inversely proportional to the square root of the PMOS mobility
- inversely proportional to the PMOS mobility

Using the $\frac{CV}{I}$ DELAY MODEL, we know that the expression for an inverter charging delay is given by :-

$$t_{PLH} = \frac{C_L V_{DD}}{\beta_p (V_{DD} - |V_{tp}|)^2} \quad \dots (i)$$

We know, $\beta_p = \frac{\mu_p C_{ox} W_p}{L}$

Substituting this value of β_p in equation (i), we have,

$$t_{PLH} = \frac{C_L V_{DD} L}{\mu_p C_{ox} W_p (V_{DD} - |V_{tp}|)^2}$$

From this equation, we can see that,

$$t_{PLH} \propto \frac{1}{\mu_p}$$

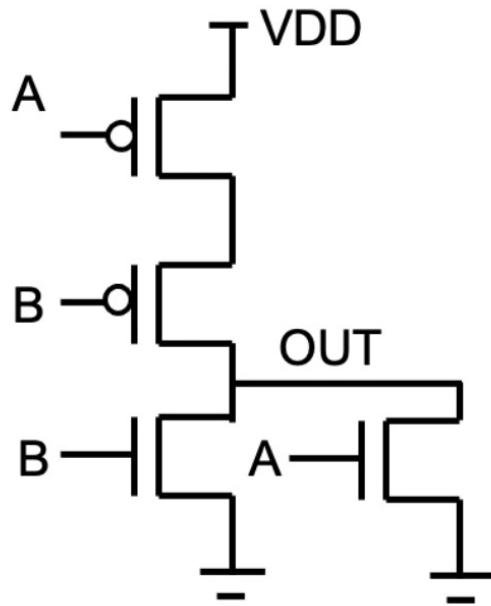
∴ The charging delay of an inverter is inversely proportional to the PMOS mobility.



Question 7

5 pts

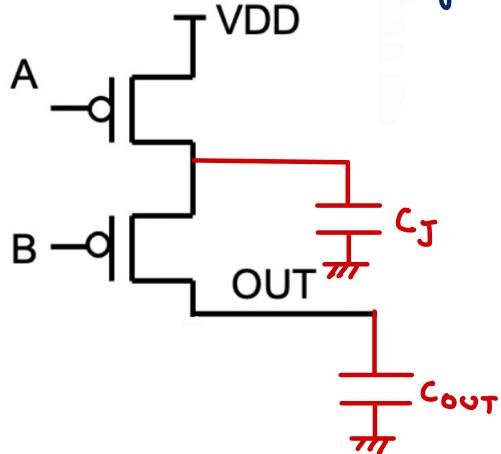
Consider a 2 input NOR gate as shown below:



Which of the following represents the worst case delay?

-
- B=0 and A switches from 1 to 0
 - A=1 and B switches from 0 to 1
 - A=0 and B switches from 1 to 0
 - A=0 and B switches from 0 to 1
-

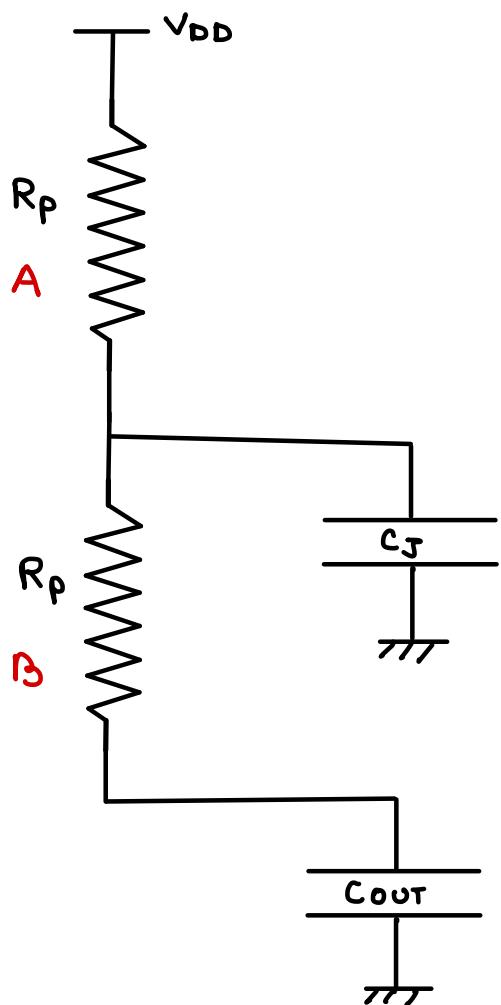
Let us look at the PUN because this will give us the worst case delay in this case as the transistors are in a stack (in series)



Let us consider the following possible scenarios in this case :-

- ① $B = 0$ and A switches from 1 to 0

The equivalent RC circuit will be as shown below :-



Here, $B = 0$

\therefore The resistor at the bottom (R_p) is already ON

But C_{out} does not have a path to V_{DD} as A is OFF.

i.e. C_{out} is NOT CHARGED.

Similarly, C_J too is NOT CHARGED as A is initially OFF.

When, A switches from 1 to 0, then the top resistor is ON and C_J and C_{out} can now be both charged up to V_{DD} .

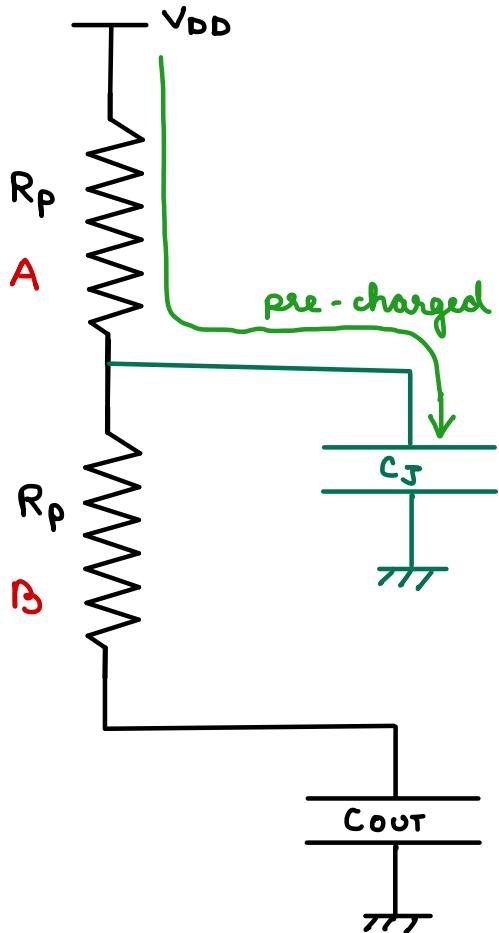
The charging delay will be given by,

$$T_{D1} = 0.69 \left[R_p (C_J + C_{OUT}) + R_p C_{OUT} \right]$$

$$\text{or, } T_{D1} = 0.69 \left[2 R_p C_{OUT} + R_p C_J \right] \dots (\text{i})$$

② A = 0 and B switches from 1 to 0

The equivalent RC circuit will be as shown below:-



Here, A = 0

\therefore The resistor at the Top is already ON

\therefore C_J has a path to charge up to V_{DD} as A is ON

i.e. C_J is PRE-CHARGED.

But C_{OUT} does not have a path to V_{DD} as B is OFF.

i.e. C_{OUT} is NOT CHARGED.

When, B switches from 1 to 0, then the bottom resistor is ON and C_{OUT} can now be charged.

The charging delay will now be given by,

$$T_{D2} = 0.69 \left[(R_p + R_p) C_{OUT} \right]$$

$$\text{or, } T_{D2} = 0.69 [2 R_p C_{OUT}] \dots (\text{ii})$$

∴ From (i) and (ii), we have,

$$T_{D1} - T_{D2} = 0.69 [R_P C_T]$$

$$\therefore T_{D1} > T_{D2}$$

Hence, we conclude that having the switching input (1 to 0) at the bottom of the stack will reduce the overall switching delay because the Junction Capacitance can pre-charge to V_{DD}.

∴ The worst case delay will be given by the condition when, B = 0 and A switches from 1 to 0.

For the remaining two cases,

③ A = 1 and B switches from 0 to 1

In this case, the output is already discharged and it is 0. As B switches from 0 to 1, the output does not change and there is no transition.

④ A = 0 and B switches from 0 to 1

In this case, the output starts to discharge.

However it discharges through one nMOS transistor only.

∴ The discharging delay is $T_{D4} = 0.69 R_n C_L$ which is smaller than T_{D1} .

∴ T_{D1} is the worst case delay.



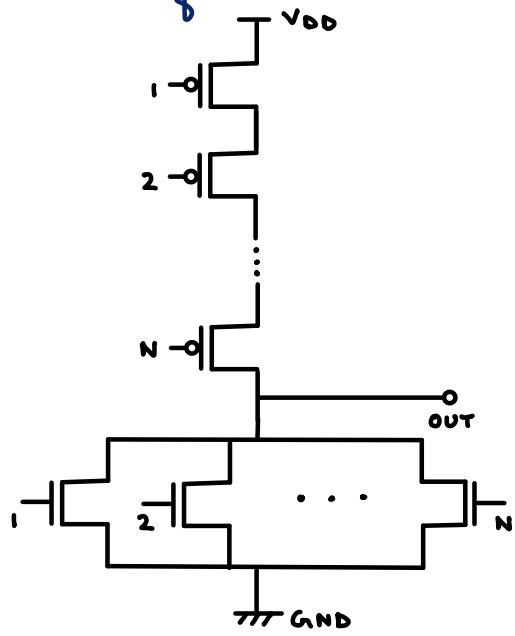
Question 8

5 pts

Assume that each NMOS and PMOS device in an N-input NOR gate has the same resistance. What is (approximately) the ratio of the slowest to the fastest propagation delay through the cell?

 N^3 $1/N^2$ N^2 N

Let us first look at an N-input NOR gate.



The worst case delay here is the charging delay since the PMOSes are in series (in a stack)

We know that the delay varies as N^2 where N is the number of inputs.

∴ The slowest delay, $T_{slow} \propto N^2$

When the NOR gate is discharging through the nMOS network, we will get the fastest delay. This will happen when all the nMOSes are ON simultaneously. Assuming that each nMOS has a resistance of R_n , the effective resistance of the PDN = $\frac{R_n}{N}$. ∴ $T_{fast} \propto \frac{1}{N}$

$$\therefore \frac{T_{slow}}{T_{fast}} \propto \frac{N^2}{1/N} \quad \text{or,}$$

$$\boxed{\frac{T_{slow}}{T_{fast}} \propto N^3}$$



Question 9

5 pts

The trip point of an inverter is at 0.7 VDD. What can we say about the relationship between the rise time (TR) and the fall time (TF)?

- TR>TF but the exact ratio cannot be determined
- TR=TF/0.7
- cannot be determined
- TR<TF

We know that the switching threshold or TRIP POINT of an inverter is defined as the input voltage V_M such that, the output voltage V_{OUT} is also equal to V_M . (see MODULE 3 - PART C)
We also know that, when the pMOS and nMOS are symmetric, $V_M = V_{DD}/2$. Here, $V_M = 0.7 V_{DD} > V_{DD}/2$.

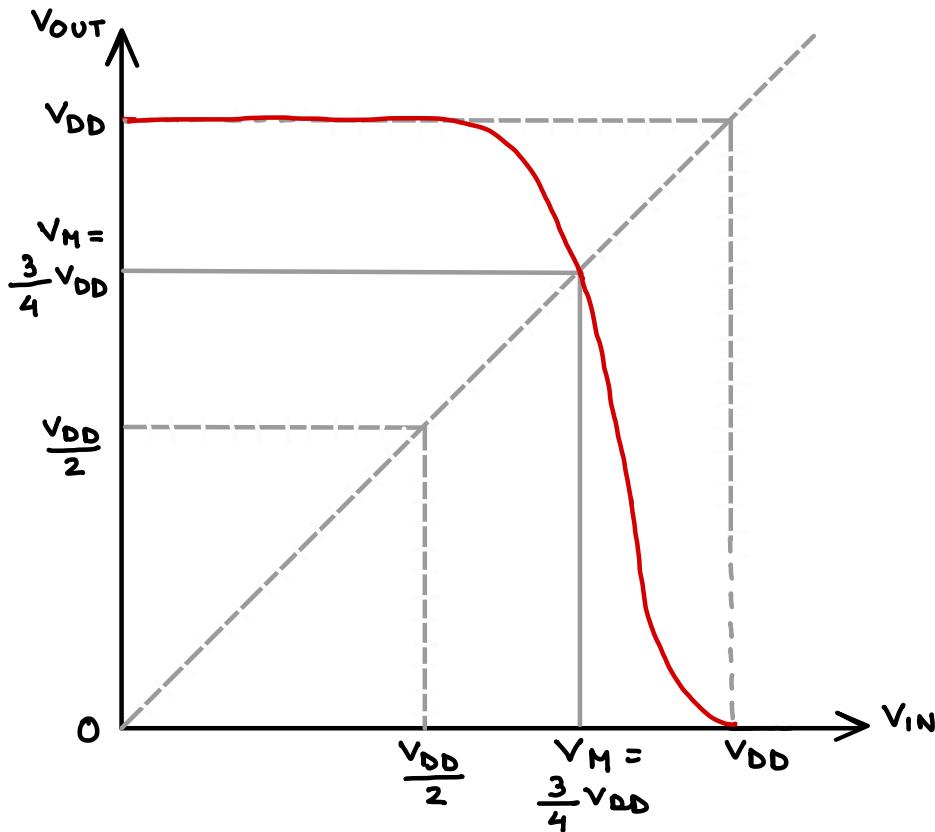
Let us try to draw this VTC. We can see that this is a

skewed inverter

(just like your
Homework 3, problem 3)

In this skewed inverter,
the pMOS is stronger
than the nMOS.

$$\therefore \beta_p > \beta_n$$



$$\therefore R_p < R_n \dots (i)$$

We know that the RISE TIME is given by,

$$T_R = (\ln 2) R_p C \text{ and, the FALL TIME is given by,}$$

$$T_F = (\ln 2) R_n C$$

Since, from (i), we have,

$$R_p < R_n$$

\therefore

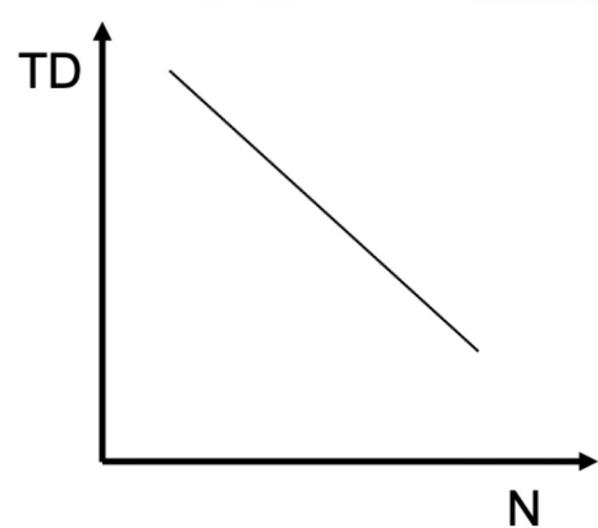
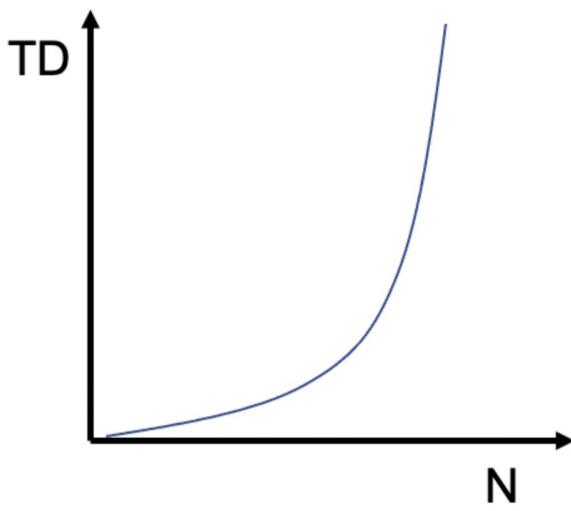
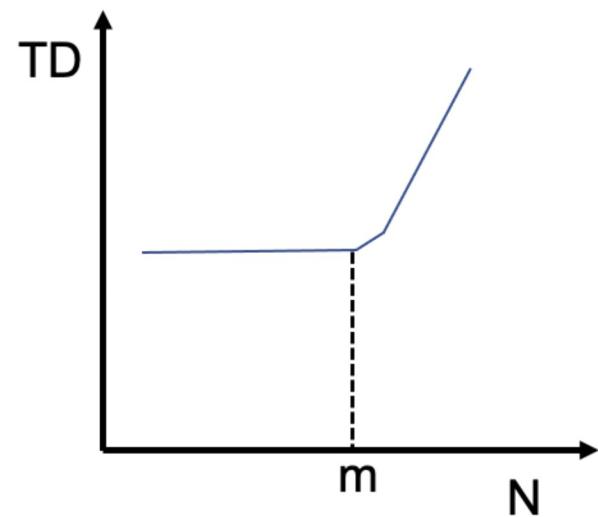
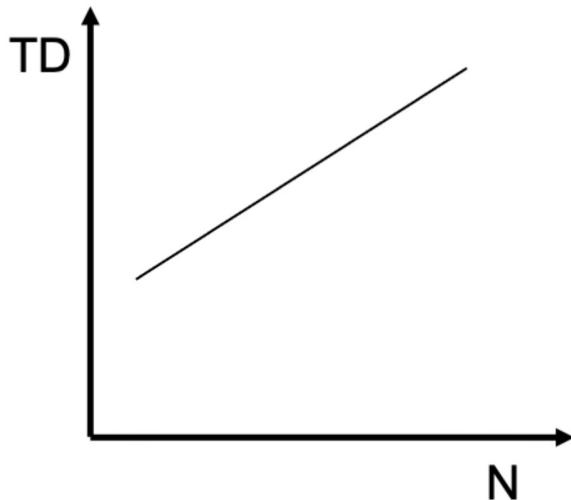
$$T_R < T_F$$



Question 10

5 pts

Consider an inverter driving a fanout of N identical inverters. The wire capacitance is equal to the input capacitance of m such inverters. Ignoring C_{OUT} , determine the correct plot between the propagation delay and N .



We know that the propagation delay is given by,

$$T_d = \frac{C_L}{2V_{DD}} \left(\frac{1}{\beta_p} + \frac{1}{\beta_n} \right)$$

We also know that, $C_L = C_{out} + C_{wire} + C_{in}$

Here, it is given that $C_{out} = 0$ and,

$$C_{in} = NC_{in}'$$

where, C_{in}' is the input capacitance of each inverter and N is the FAN-OUT.

Also, given $C_{wire} = m C_{in}'$

$$\therefore C_L = m C_{in}' + N C_{in}'$$

$$\text{or, } C_L = (m+N) C_{in}'$$

$$\therefore T_d = \frac{(m+N) C_{in}'}{2V_{DD}} \left(\frac{1}{\beta_p} + \frac{1}{\beta_n} \right)$$

$$\therefore T_d \propto (m+N)$$

Hence, T_d will be a straight line when plotted against N.



Question 11

5 pts

Consider an inverter where the VTH of the NMOS is 0.2V, VDD is 1.2V and the discharging delay is 10ps. If the VDD increases to 2V, what is the discharging delay of the inverter?

Hint: Use a CV/I model of delay.

19.4 ps

5.14 ps

10 ps

3.08 ps

Using the $\frac{CV}{I}$ model, the discharging delay is given by :

$$t_{PHL} = \frac{C_L V_{DD}}{\beta_n (V_{DD} - V_{tn})^2}$$

1st SCENARIO :- $V_{tn1} = 0.2 \text{ V}$

$$V_{DD1} = 1.2 \text{ V}$$

$$t_{PHL1} = 10 \text{ ps}$$

$$\therefore 10 \times 10^{-12} = \frac{C_L (1.2)}{\beta_n (1.2 - 0.2)^2} = \frac{C_L (1.2)}{\beta_n} \dots (i)$$

2nd SCENARIO :- $V_{tn2} = 0.2 \text{ V}$ (same as before)

$$V_{DD2} = 2 \text{ V}$$

$$\therefore t_{PHL2} = \frac{C_L (2)}{\beta_n (2 - 0.2)^2} = \frac{2C_L}{(1.8)^2 \beta_n} \dots \text{(ii)}$$

Dividing (ii) by (i),

$$\frac{t_{PHL2}}{10 \times 10^{-12}} = \frac{2C_L}{(1.8)^2 \beta_n} \times \frac{\beta_n}{1.2 C_L}$$

$$\text{or, } t_{PHL2} = \frac{2}{(1.8)^2 \times 1.2} \times 10 \times 10^{-12}$$

$$\text{or, } t_{PHL2} = 5.14 \text{ ps}$$



Question 12

5 pts

Consider an Euler representation of a PUN with vertices $\{v_1, v_2, v_3, v_4, v_5\}$. The degrees of each of these nodes are $\{3, 2, 1, 3, 4\}$. Which of the following is true:

- There is at least one diffusion break
- There is at least one diffusion and one poly break
- There is no diffusion break
- none of the above

We know that if there are more than 2 vertices with an odd degree (degree of a vertex is the number of edges connected to it), then an EULER PATH does not exist and there will be a break in the diffusion.

Here, we have 3 vertices with an odd degree.

$v_1 \rightarrow$ degree 3

$v_3 \rightarrow$ degree 1 and

$v_4 \rightarrow$ degree 3

\therefore We can say that, **there is at least one diffusion break.**



Question 13

5 pts

The resistance of a wire is 10 ohm/um and its capacitance is 1pF/um. Find the Elmore Delay of a 10um wire, using a distributed RC model.

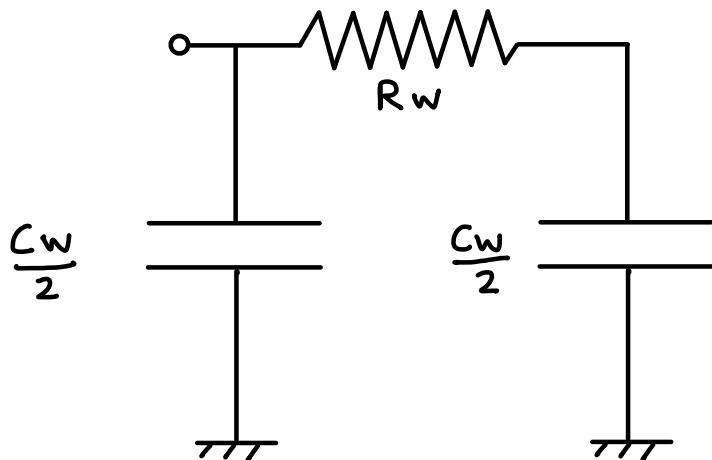
In a distributed RC model, we break up the interconnect into a large number of smaller segments in series.

345 ps

100 ps

0.028 ps

69 ps



We know that using a distributed model, the delay is given by :-

$$T_d = \frac{0.69 R_w C_w}{2}$$

(see HOMEWORK 5 - PROBLEM 2)

Here, $R_w = 10 \Omega/\mu\text{m}$ and the length of the wire is $10 \mu\text{m}$.

$$\therefore R_w = 10 \times 10 \Omega \text{ or, } R_w = 100 \Omega$$

$C_w = 1 \text{ pF}/\mu\text{m}$ and the length of the wire is $10 \mu\text{m}$.

$$\therefore C_w = 1 \times 10 \text{ pF} \text{ or, } C_w = 10 \text{ pF}$$

$$\therefore T_d = \frac{0.69 \times 100 \Omega \times 10 \text{ pF}}{2} \text{ or, } T_d = 345 \text{ ps}$$



Question 14

5 pts

A CMOS logic circuit with high activity factor, consumes 18 W when operated at a VDD of 1.5V. If the supply voltage is lowered to 0.5V, what will be a rough estimate of the total power when the circuit operates at the same frequency?

2 W

6 W

4 W

12 W

At high activity we can assume that the power is
SWITCHING POWER

$$\therefore P = \alpha C V_{DD}^2 f$$

1st SCENARIO :- $P_1 = (\alpha C) V_{DD_1}^2 f_1$

Given, $f_1 = f_2 = f$

$$\therefore P_1 = (\alpha C) (1.5)^2 f \dots (i)$$

2nd SCENARIO :- $P_2 = (\alpha C) V_{DD_2}^2 f_2$

Given, $f_1 = f_2 = f$

$$\therefore P_2 = (\alpha C) (0.5)^2 f \dots (ii)$$

Dividing (ii) by (i), we have,

$$\frac{P_2}{P_1} = \frac{(\alpha C) (0.5)^2 f}{(\alpha C) (1.5)^2 f} = \frac{1}{9} \quad \therefore P_2 = \frac{P_1}{9} \quad \text{or, } P_2 = \frac{18}{9} \text{ W}$$

or, P₂ = 2 W



Question 15

5 pts

Consider an inverter driving an output capacitor C_L . Consider an RC model for rise time and fall times, and assume that the peak short circuit current increases quadratically with V_{DD} . How does short circuit energy change with V_{DD} ? ($V_{DD} \gg V_t$)

increases quadratically

decreases quadratically

increases linearly

decreases linearly

We know that the SHORT CIRCUIT ENERGY is given

$$\text{by : } E_{sc} = I_{peak} V_{DD} \left(\frac{t_r + t_f}{2} \right)$$

Given that the $I_{peak} \propto V_{DD}^2$

We know that using the RC model, we can write

$$t_r = (\ln q) R_p C_L = \frac{(\ln q) C_L}{\beta_p (V_{DD} - V_{tp})} \quad (\text{linear region with low } V_{DS})$$

Since, $V_{DD} \gg |V_{tp}|$, we have,

$$t_r \propto \frac{1}{V_{DD}} . \text{ Similarly, } t_f \propto \frac{1}{V_{DD}}$$

$$\therefore E_{sc} \propto V_{DD}^2$$

\therefore The SHORT CIRCUIT ENERGY increases quadratically with V_{DD}



Question 16

5 pts

Consider an inverter driving its own output capacitor, a wire capacitance and a fixed external capacitor. As the width of the NMOS increases:

- Both charging and discharging switching energy increases
- Both charging and discharging switching energy remains constant
- Only switching energy during discharging increases
- Only switching energy during charging increases

The charging SWITCHING ENERGY is given by $\frac{1}{2} C V_{DD}^2$
Similarly, the discharging SWITCHING ENERGY is also
given by $\frac{1}{2} C V_{DD}^2$

Here, $C = C_{OUT} + C_{WIRE} + C_{EXTERNAL}$

We know that as W_n increases, C_{OUT} also increases

since, $C_{OUT} = C_{DBP} + C_{DBn}$

or, $C_{OUT} = W_p \widetilde{C_{DBP}} + W_n \widetilde{C_{DBn}}$

where, $\widetilde{C_{DBP}}$ and $\widetilde{C_{DBn}}$ are the drain to body capacitance per unit width of the pMOS and nMOS respectively.

∴ As C_{OUT} increases with W_n , C also increases
and hence, both charging and discharging
switching energy increases with the width of the
nMOS.



Question 17

5 pts

A microprocessor consisting of 10^9 logic gates has a total switched capacitance (i.e., total capacitance multiplied by the activity factor) of 2nF . The processor is running at 1.5GHz with an operating voltage of 1.2V . The average leakage current per gate is 1nA . Ignoring the short circuit energy, the total power dissipated is:

4.32 W

5.32 W

5.52 W

3.52 W

Given ,

$$\text{Number of logic gates } (N) = 10^9$$

$$\text{Total capacitance} \times \text{activity factor } (\alpha c) = 2\text{nF}$$

$$\text{Frequency of the processor } (f) = 1.5\text{ GHz}$$

$$\text{Operating voltage } (V_{DD}) = 1.2\text{ V}$$

$$\text{Average leakage current per gate } (I_{\text{leak}}) = 1\text{nA/gate}$$

$$\text{There are } 10^9 \text{ gates. } \therefore \text{Total } I_{\text{leak}} = 1\text{nA} \times 10^9 = 1\text{ A}$$

$$\text{Total leakage power} = I_{\text{leak}} \times V_{DD} = 1\text{ A} \times 1.2\text{ V} = 1.2\text{ W}$$

We are ignoring the short circuit power.

\therefore The dynamic power will be the switching power.

$$\text{Total switching power} = (\alpha c) V_{DD}^2 f = 2 \times 10^{-9} \times (1.2)^2 \times 1.5 \times 10^9 \text{ W}$$

$$\therefore \text{Total switching power} = 4.32 \text{ W}$$

$$\therefore \text{Total power} = \text{Dynamic power} + \text{Leakage power}$$

$$\text{or, Total power} = (4.32 + 1.2) \text{ W or, Total Power} = 5.52 \text{ W}$$



Question 18

5 pts

All circuits age over time and consequently the threshold voltages increase with time. However the capacitances do not change. Considering such an aging phenomenon, which of the following are true:

- All the other statements are correct
- The switching energy of circuits do not change over time
- We need to apply lower VDD as time progresses, to maintain constant speed
- Circuits get faster over time and dissipate more power

Given that with time the threshold voltage V_t increases but the capacitances do not change.

Hence, the switching energy which is given by $C V_{DD}^2$ does not change.

We know that the propagation delay using the $\frac{CV}{I}$ model is given by, $t = \frac{C_L V_{DD}}{\beta (V_{DD} - V_t)^2}$

\therefore as V_t increases, t also increases and the circuits get slower over time.

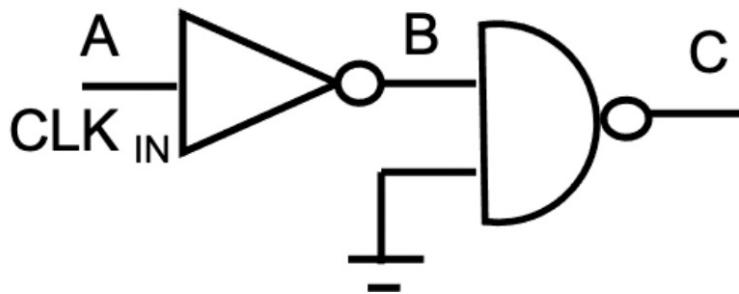
Further to maintain constant delay, we will need to apply higher V_{DD} as time progresses.



Question 19

5 pts

Consider the following circuit. The input signal to the node A is a clock running at 1GHz. The total capacitance at A is 1pF, at B the total capacitance is 1.5pF and at C the total capacitance is 2pF. If the switching power dissipated at node A is 1uW, what is the total power dissipated at nodes B and C combined (not including the power at node A). Ignore short circuit and leakage power. All the signals share a common supply (VDD).



1.5 uW

4.5 uW

2.5 uW

3.5 uW

Given that, $C_A = 1 \text{ pF}$; $C_B = 1.5 \text{ pF}$; $C_C = 2 \text{ pF}$

$$P_A = 1 \mu\text{W}.$$

Since, we have an inverter, if A switches, B also switches. $\therefore \alpha_A = \alpha_B$ (the activities of A and B are the same)

It is given that the signals share the same V_{DD} and f.

$$\therefore \frac{P_B}{P_A} = \frac{\alpha_B C_B V_{DD}^2 f}{\alpha_A C_A V_{DD}^2 f} = \frac{C_B}{C_A} = 1.5$$

$$\therefore P_B = 1.5 \text{ PA}$$

$$\text{or, } P_B = 1.5 \mu\text{W}$$

Now, since, one of the inputs of the NAND gate is grounded, the output C will always be held at 1. (see TRUTH TABLE of the NAND gate below)

x	y	\overline{xy}
0	0	1
0	1	1
1	0	1
1	1	0

\therefore The activity factor of C, $\alpha_c = 0$

$$\therefore P_c = \alpha_c C_c V_{DD}^2 f = 0 \text{ W}$$

\therefore The total power dissipated at nodes B and C is given by :-

$$P = P_B + P_c$$

$$\text{or, } P = 1.5 \text{ W} + 0 \text{ W}$$

$$\text{or, } P = 1.5 \text{ W}$$



Question 20

5 pts

A cell phone battery is rated at 3 KWhr. When the processor operates at 1GHz (at VDD = 1V) the battery lasts for 18 hours. If the processor operates at 2.0 GHz (at VDD = 1.2 V) the battery will last for:

(Ignore leakage power and short circuit power)

6 hours 15 mins

6 hours 30 mins

12 hours 45 mins

9 hours 10 mins

Let us assume that the total battery energy is

$$\mathcal{E} = 3 \text{ KWhr}$$

1st SCENARIO :- $P_1 = \alpha C V_{DD_1}^2 f_1 = \alpha C (1)^2 (1 \times 10^9) = 10^9 \alpha C$

Since the battery lasts for 18 hrs, we can write,

$$\mathcal{E} = P_1 \times (18 \text{ hrs})$$

or, $10^9 \alpha C \times 18 \text{ hrs} = \mathcal{E} \dots (i)$

2nd SCENARIO :- $P_2 = \alpha C V_{DD_2}^2 f_2 = \alpha C (1.2)^2 (2 \times 10^9)$

or, $P_2 = 2.88 \alpha C \times 10^9$

Here again,

$$\mathcal{E} = P_2 \times t = 2.88 \alpha C \times 10^9 t \dots (ii)$$

where, t is the time over which the battery will last.

\therefore From (i) and (ii), we have,

$$10^9 \alpha C \times 18 = 2.88 \alpha C \times 10^9 t$$

$$\text{or, } t = \frac{18}{2.88}$$

$$\text{or, } t = 6 \text{ hrs } 15 \text{ mins}$$