

## MODULE 4 - PART A

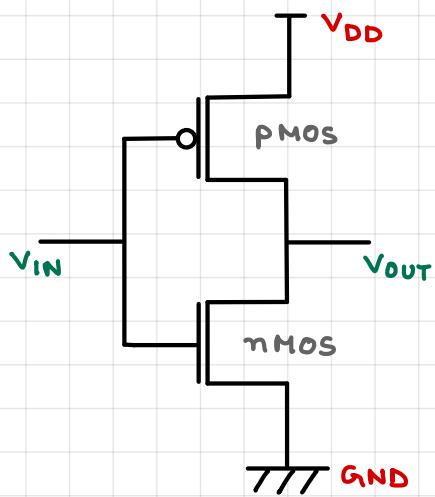
### LAYOUT AND LAYOUT TOOLS

In this MODULE, we are going to talk about LAYOUT DESIGN, but before we go into that, let us see what we mean by LAYOUT.

As a circuit designer, we will first design SCHEMATIC circuits.

FOR EXAMPLE :-

This is how a SCHEMATIC CIRCUIT will look like for an inverter :-



After drawing our SCHEMATIC CIRCUIT, we will keep on simulating this circuit till we 'MEET OUR SPECIFICATIONS'.

The Specifications can be based on DELAY, POWER, PERFORMANCE etc.

We will keep ITERATING our design till these specifications are met.

Once the specifications are met, and our SCHEMATIC is finalized, we will move on to the next stage which is LAYOUT DESIGN. The LAYOUT DESIGN is a diagrammatic representation of the circuit that will be fabricated.

We will again perform simulations on this LAYOUT

DESIGN, to meet our specifications.

Usually, we do not have to change a lot of things from the SCHEMATIC stage to the LAYOUT stage. Once the LAYOUT DESIGN is done and the specifications are met, we will go to the next stage, that is FABRICATION.

So why do we need to perform the simulations twice, once in the SCHEMATIC stage and again in the LAYOUT DESIGN stage?

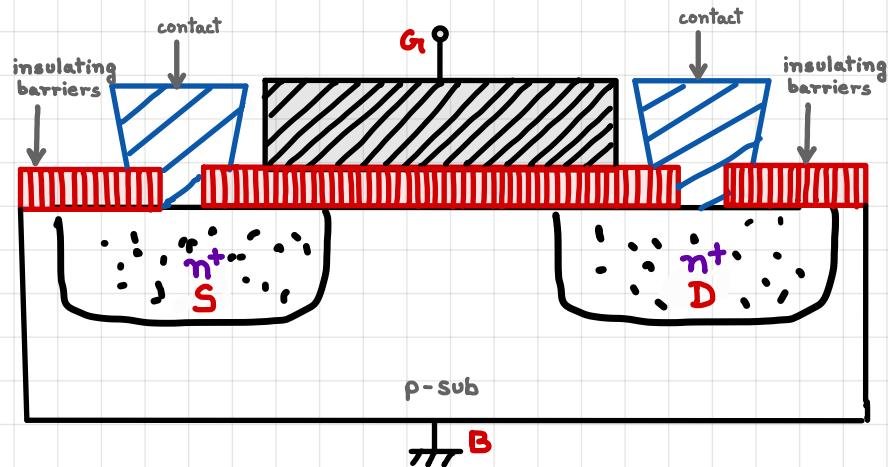
The LAYOUT DESIGN will mimic the transistors and we will learn how this is done. But the problem is, sometimes because of the LAYOUT, there will be additional parasitic resistances and capacitances that will come in which we need to account for and this cannot be addressed in the SCHEMATIC stage. So we will need to make sure that the specifications are met in the LAYOUT DESIGN stage as well and we will send this FINAL design for FABRICATION.

### CMOS LAYERS :-

When we talk about LAYOUT DESIGN, we will talk about the various CMOS layers.

Let us see what these layers are. We had seen the cross-sectional side view of the nMOS before and there, we had seen the various layers  $\rightarrow$   $n^+$  Source

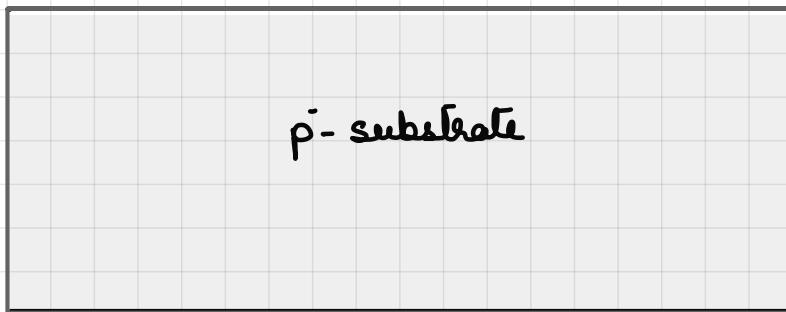
and Drain, p-substrate, oxide layer, Gate, contacts etc.



We are now going to look at some of these layers in a standard n-well process. Most of the microprocessors today are built on this n-well process.

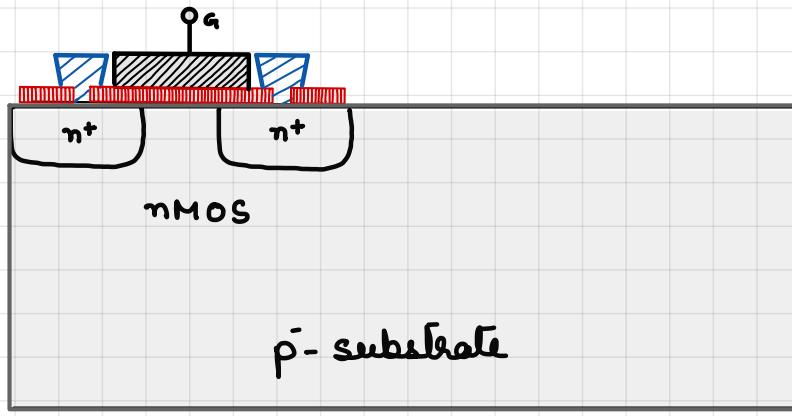
### STANDARD N-WELL PROCESS :-

- ① In n-well process starts with a p<sup>-</sup>-substrate (lightly doped p region)

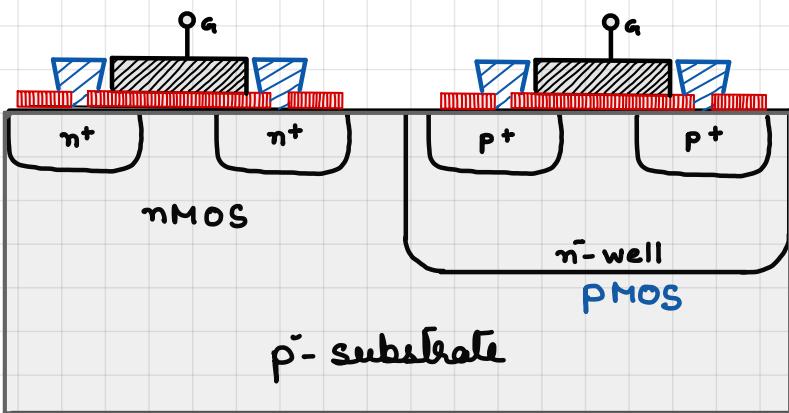


- ② When we want to build an n-MOS, we create the n<sup>+</sup> diffusion regions for the source and the drain. Then we have the oxide layer, Gate and contacts to finally create the nMOS.

This is shown below :-



- ③ When we want to build a p-MOS, we will have to first create an *n-well*. This *n-well* is an *n<sup>-</sup>* region within the p-substrate. On the *n-well*, we will have p<sup>+</sup> regions for the Source and the Drain. Finally, we will have the oxide layer, Gate and the contacts to create the pMOS.



So the *n-well* process is one where we create an *n<sup>-</sup>* region within the p-substrate, so that we can create both nMOS and pMOS of the CMOS logic within the same substrate.

There are a few other types of processes as well. For example, we have the p-well process where the starting wafer (substrate is n-type) and a twin well process where both types of wells, *n-well* and *p-well* exists.

But, we will continue our discussions using the n-well process because this is widely used and the cost of production is also lower compared to the other processes.

We will now talk about the standard n-well process because there can be some variance to the n-well process as well.

We will look at some typical layers in this process but realize that within this standard process too, there may be variations depending on the process nodes or Fabs.

### STANDARD n-WELL PROCESS :-

- ACTIVE LAYER (or, DIFFUSION LAYER) →

This defines the nMOS and the pMOS

- POLYSILICON LAYER →

This defines the GATE

- METAL LAYERS →

There are several metal layers (upto 9, nowadays)  
metal 1 (m1), metal 2 (m2), metal 3 (m3), ... etc.

- VIA LAYERS →

There are several via layers too (upto 9). These connect one metal layer to another.

Via 1 connects metal layer 1 to metal layer 2

via 1 connects metal layer 1 to metal layer 2

∴ via  $n$  connects metal layer  $n$  to metal layer  $(n+1)$

- POLY-CUT LAYER →

This layer connects the polysilicon layer to the metal 1 layer. (Also called poly contact layer or via 0)

- ACTIVE-CUT LAYER →

This layer connects the diffusion layer to the metal 1 layer. (Also called contact layer or source/drain contact layer or, via 0)

- N-WELL LAYER →

This layer as we have seen is for pMOS fabrication

- SELECT LAYERS →

- n-SELECT LAYER
  - p-SELECT LAYER
- } The select layers along with the active layers are used to create n-type and p-type MOS devices

We will now look at these layers one by one and learn to draw their layout, with respect to the cross-section.

Please note that the LAYOUT is a top down view of the various layers.

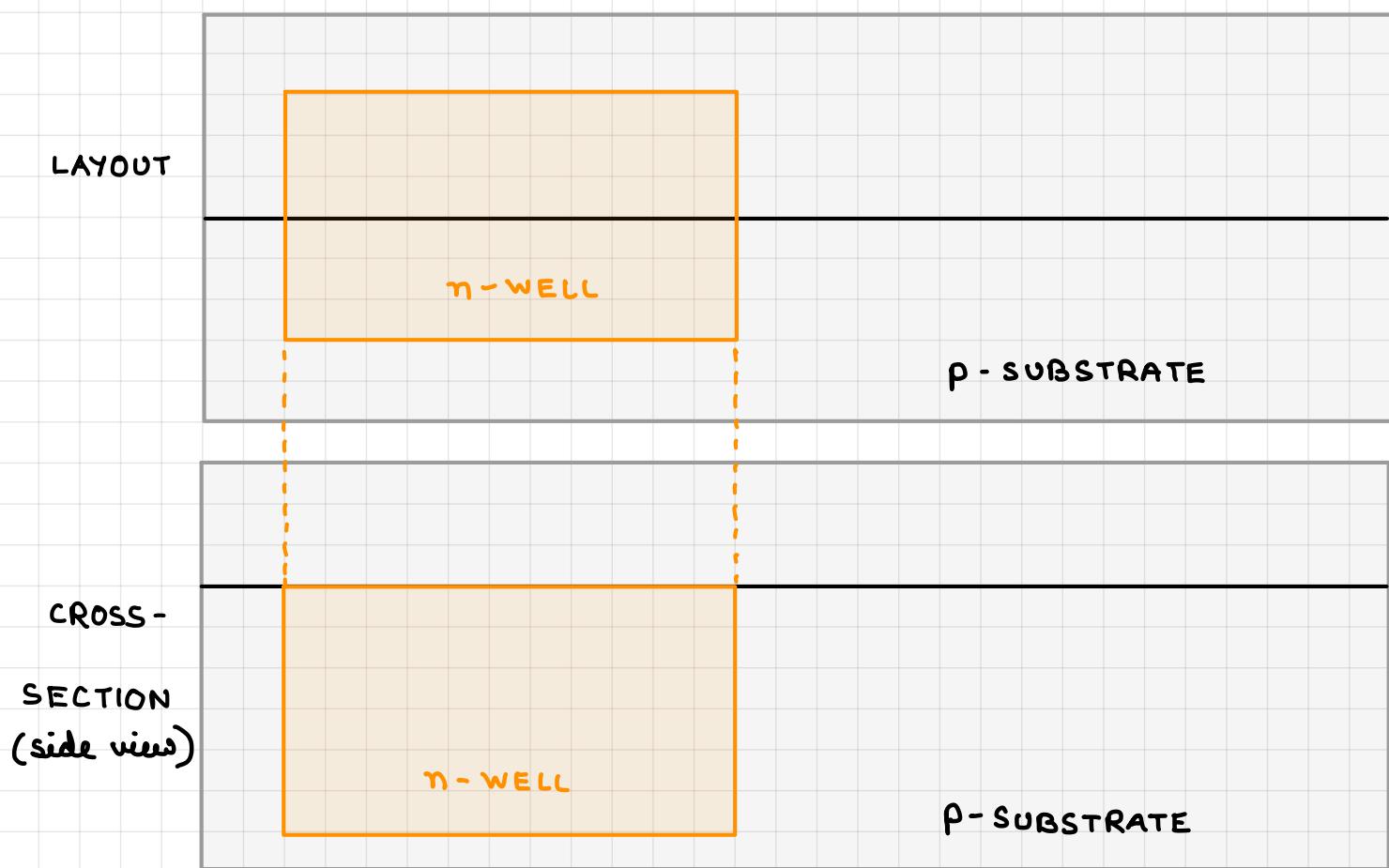
We will use different colors for the various layers so that it is easier to identify each layer.

## STEPS FOR DRAWING THE LAYOUT :-

- ① We will assume that the blank space we start with is the p-substrate.

NOTE :- Here, we are drawing the layout on the top and we will project this (using dotted lines) and draw the cross-section at the bottom.

- ② Firstly, we will draw the n-well. Wherever, there is no n-well, we have the p-substrate.

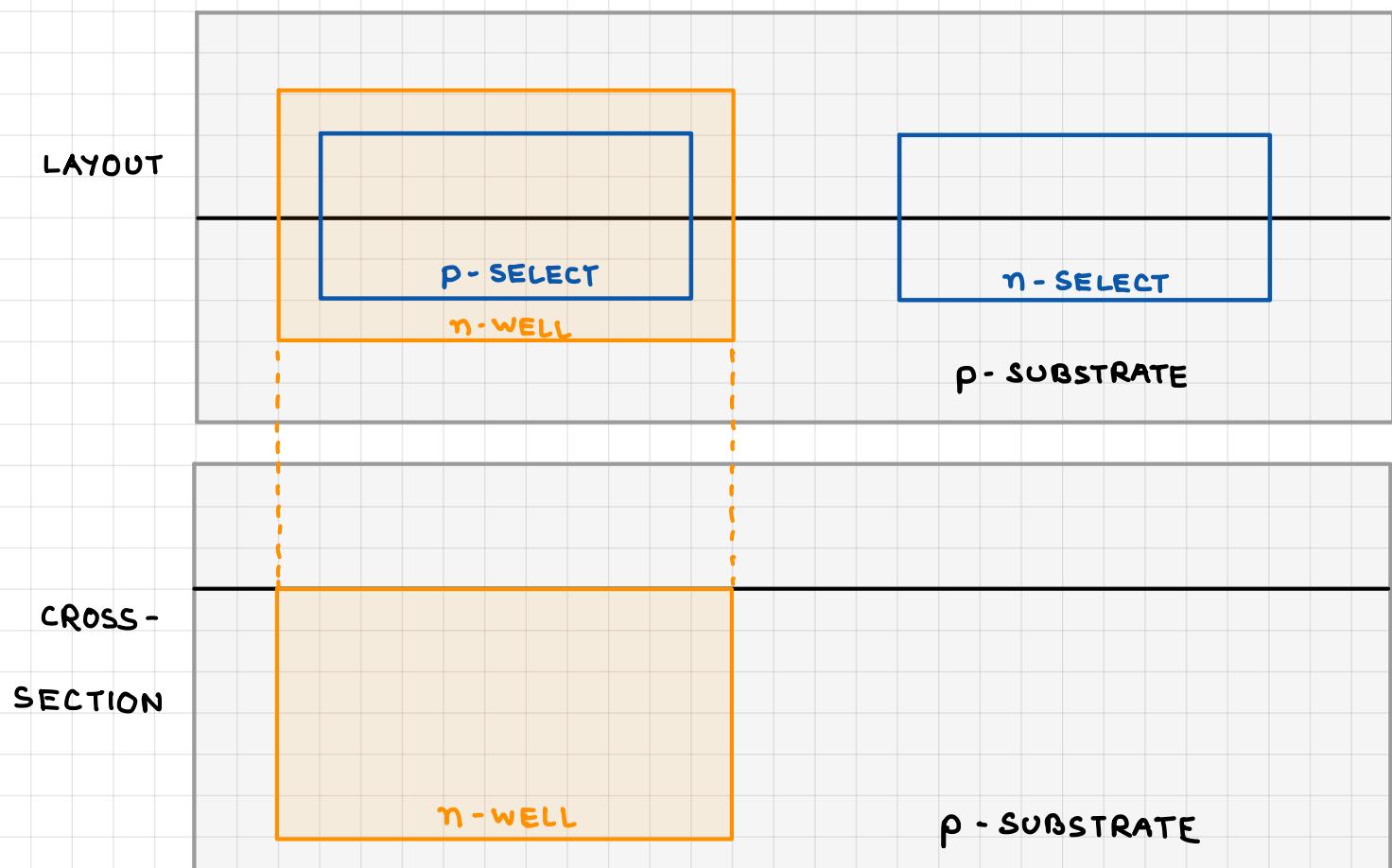


- ③ Next, we will draw the p-select layer and the n-select layer.

For the pMOS on the left, we will draw a p-select layer and for the nMOS on the right, we will draw an

$n$ -select layer. So, the  $p$ -select layer is drawn within the  $n$ -well and the  $n$ -select layer is drawn in the  $p$ -substrate.

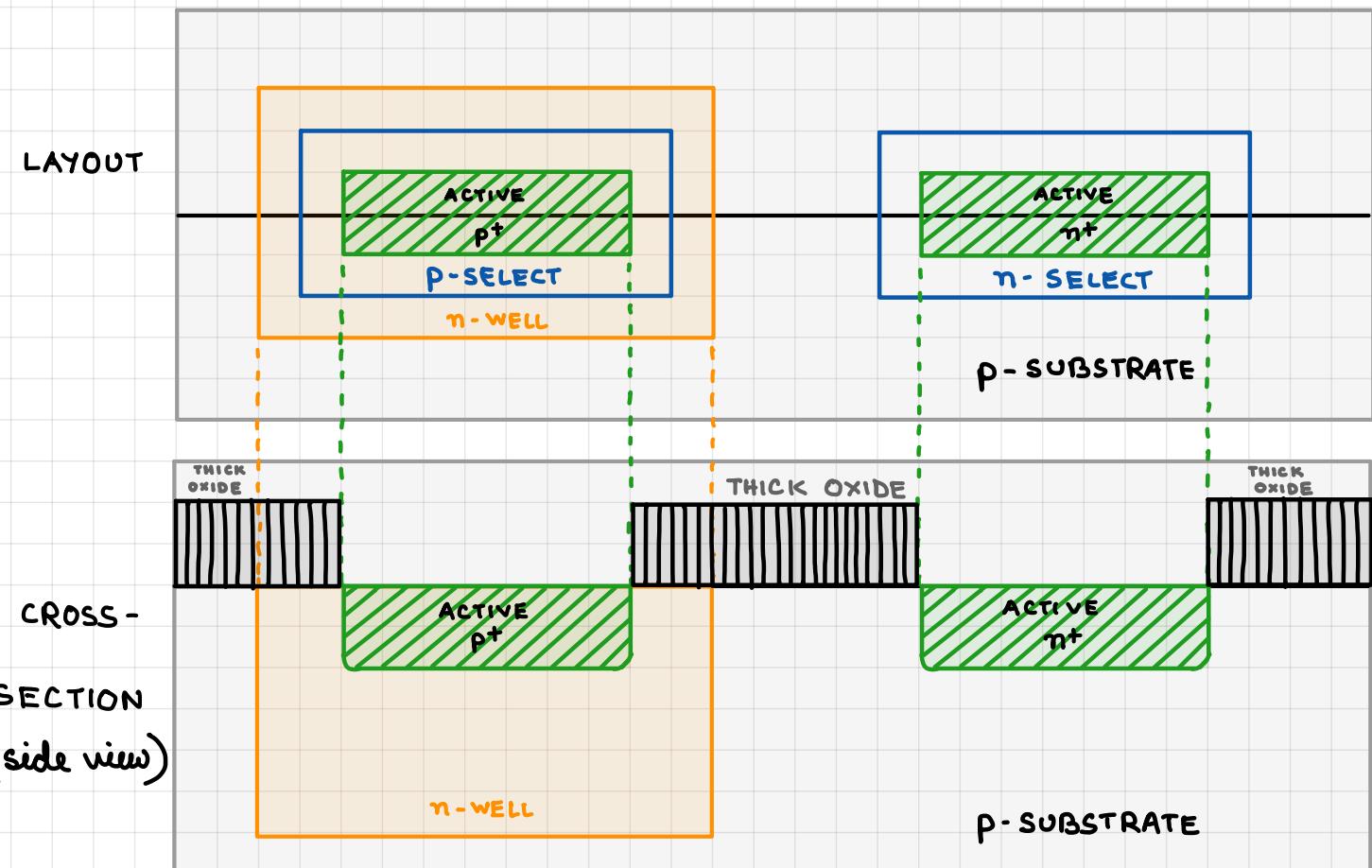
The select layers enclose the active layers and these two layers together define the  $n^+$  and  $p^+$  regions.



④ Next we will draw the ACTIVE LAYER within the select layers. And like we have seen before that the active layers along with the select layers are going to define the pMOS and the nMOS.

The active layers drawn here look identical but realize that in the pMOS, the active layer is  $p^+$  and in the nMOS, the active layer is  $n^+$ .

Wherever we do not have any active layer, we have THICK OXIDES (isolation layer that provides electrical isolation between the different contacts → gate, source, drain etc.)



- ⑤ The next layer which we are going to draw is the polysilicon layer.

Wherever an ACTIVE LAYER crosses the POLYSILICON LAYER, we have a TRANSISTOR.

We are not going to go into the details of how the channel is formed in this course. We will just learn how this structure looks like.

**NOTE :-** Here we are following the steps that are followed when drawing layouts. In actual device fabrication the gate is deposited first and then the  $n^+$ / $p^+$  diffusion regions are defined to

create SOURCE / DRAIN regions.

We have seen that the regions between the active layers will have THICK OXIDE (isolation oxides)

However, WITHIN the ACTIVE LAYERS, we will have the THIN OXIDE (Gate oxide)

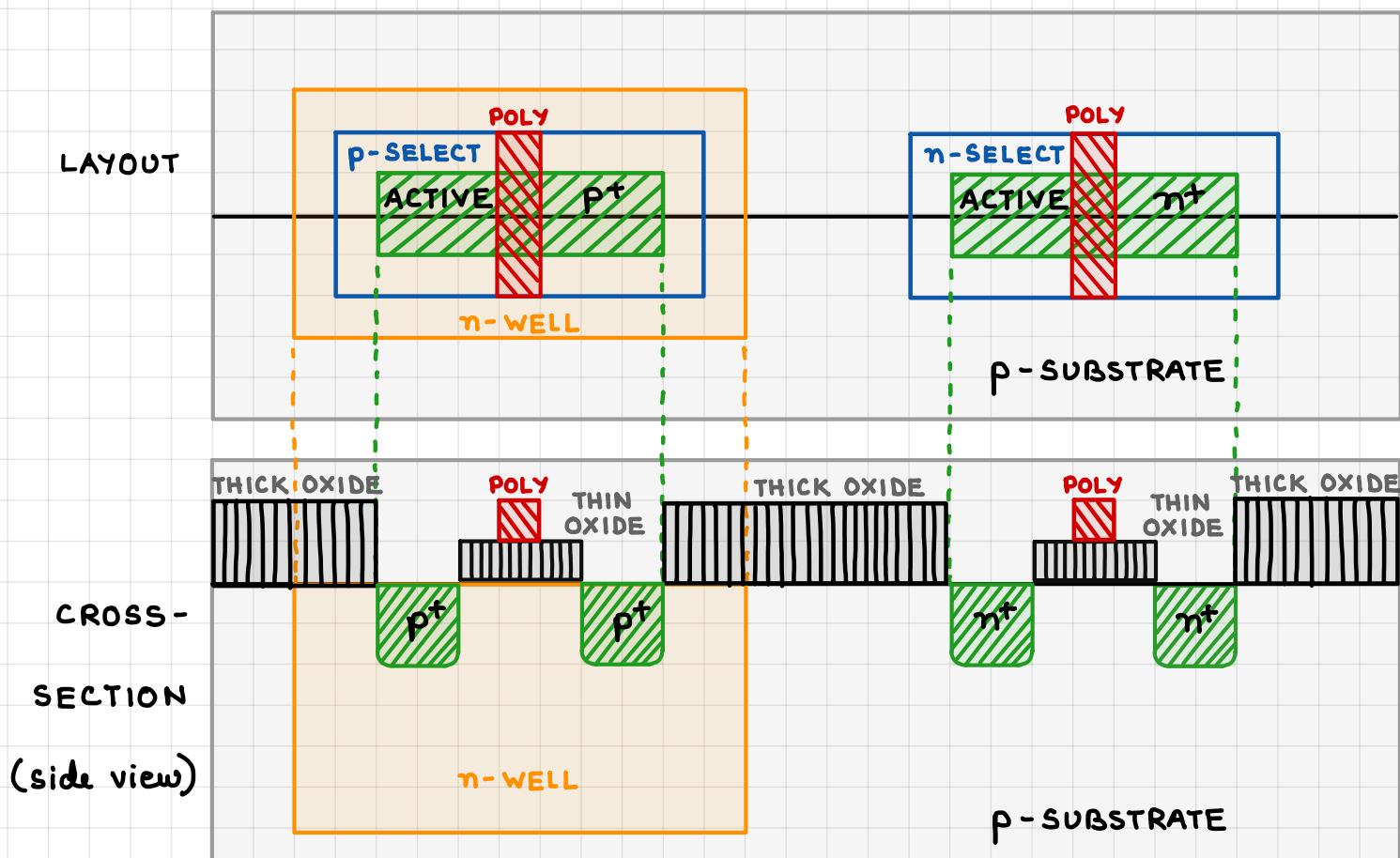
Why is this oxide not THICK OXIDE too?

If the thickness of the gate oxide increases, then

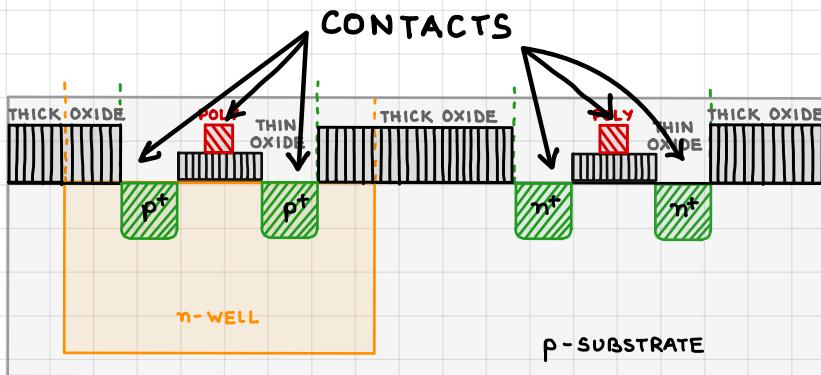
$C_{ox} = \frac{E_{ox}}{t_{ox}}$  decreases. We know that the current is proportional to  $C_{ox}$ . Hence, the current will also decrease, which is NOT what we want.

Thus, the gate oxide is THIN OXIDE.

In the cross-sectional view below, we can see that the polysilicon layer sits on top of this thin oxide layer, where we have the gate.



Now, we can see all the layers in the top-view  
(LAYOUT)



Now we will need  
to have CONTACTS for  
the GATES, SOURCES  
and DRAINS in the

places shown in the figure above. For this, we will need  
to look at wiring and contact layout next.

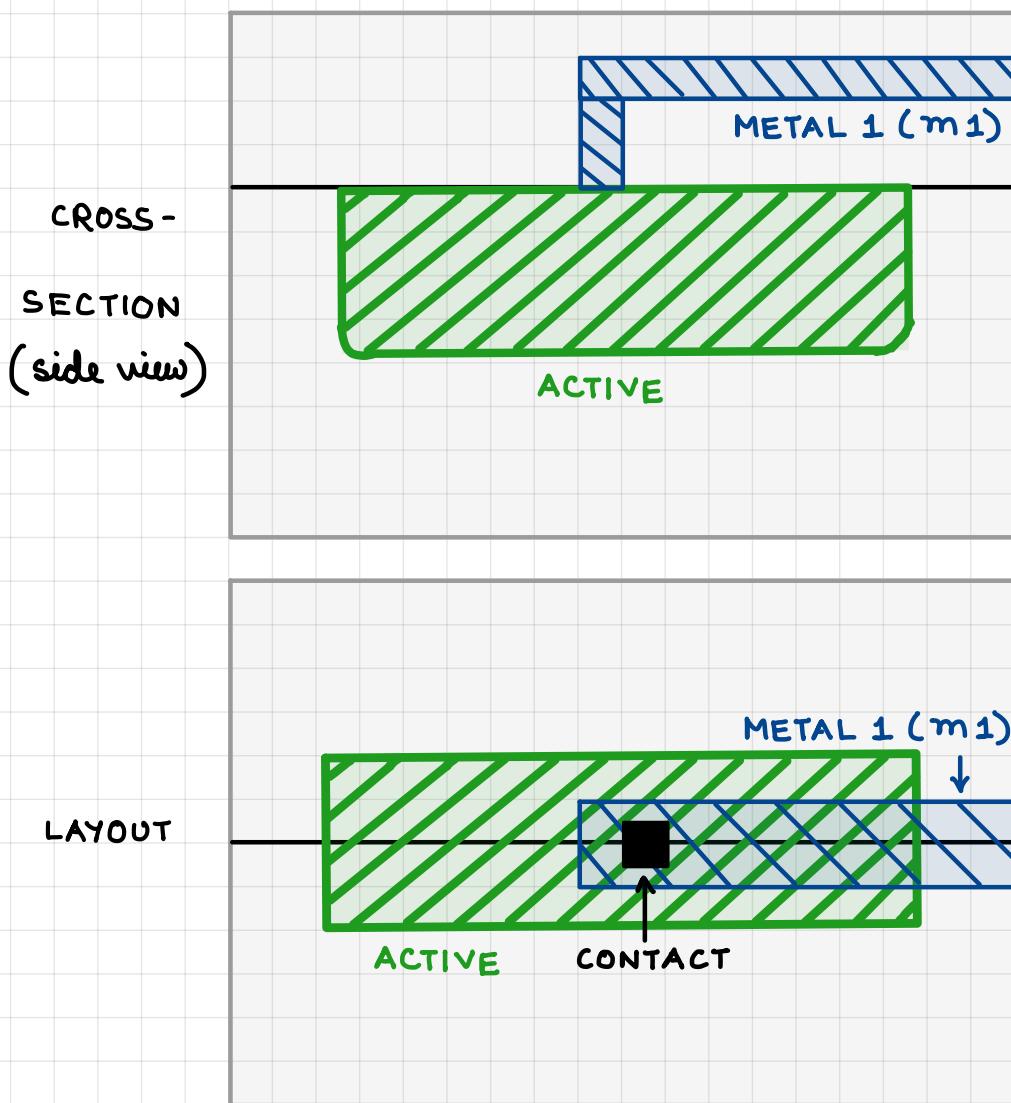
## ⑥ WIRING AND CONTACT LAYOUT :-

### ⓐ DIFFUSION CONTACTS or, ACTIVE-CUT LAYER or, ACTIVE CONTACT →

This layer connects the diffusion or active layer to the metal 1 layer. (Also called contact layer or source/drain contact layer or, via 0)

NOTE :- Here, we are going to draw the cross-section  
on top and use dotted lines to project this and draw  
the layout at the bottom.

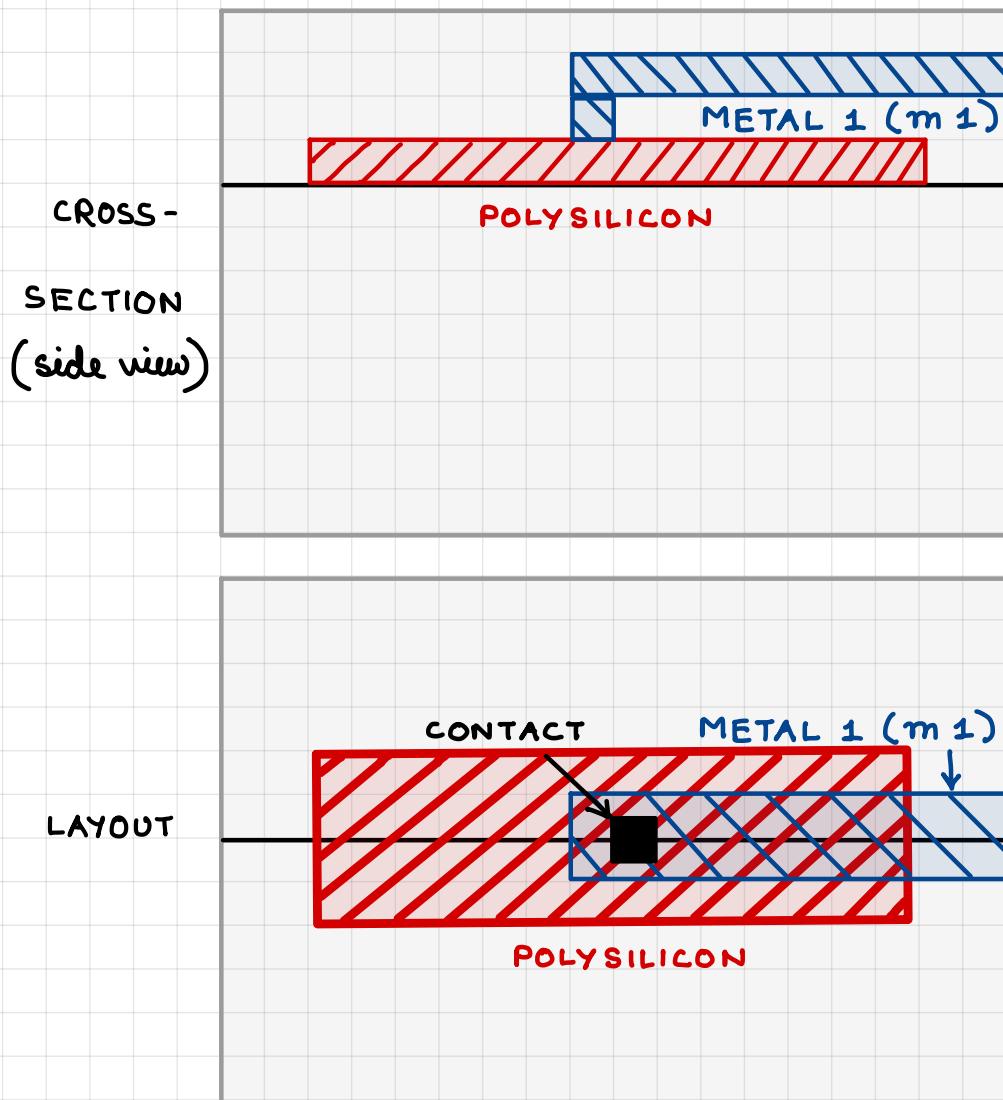
Please note that it is not enough if we draw a metal 1 ( $m_1$ )  
layer on top of the active layer to indicate that there is a  
CONTACT. We will indicate a contact between two layers  
by drawing a black square/rectangle between the  
two layers that we want to connect. ■ or ✕



(b) POLY-CUT LAYER or POLY CONTACT →

This layer connects the polysilicon layer to the metal 1 layer. (Also called poly contact layer or via 0)

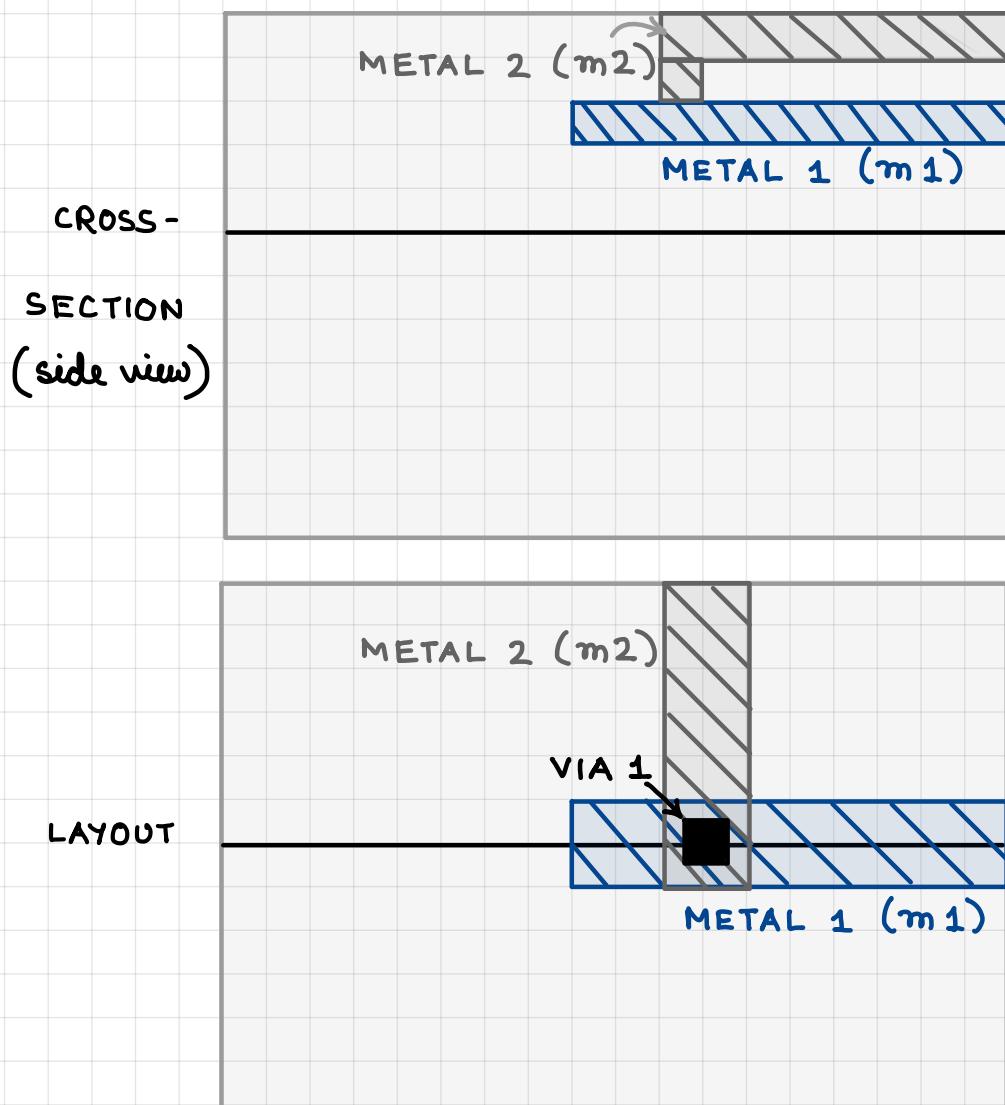
Here, too, we will indicate a contact between two layers by drawing a black square/rectangle between the two layers that we want to connect. ■ or ☒



### C) VIA LAYERS →

There are not enough available METAL 1 ( $m_1$ ) tracks to route all the signals. So we need to add more metal layers on top to be able to route all signals. Therefore, we have, VIA 1 connecting METAL 1 to METAL 2 and, VIA 2 connecting METAL 2 to METAL 3 and so on.

Here too, the contact (VIA 1) is represented by the black square ■ or ✕

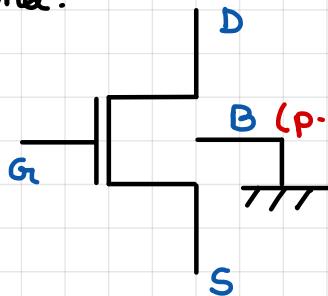


Now that we know how to connect the metal layers, the diffusion and the polysilicon, we can start thinking about building the entire transistor.

#### (d) TAPS / SUBSTRATE and WELL CONTACTS →

Whenever we design a transistor, we know that :-

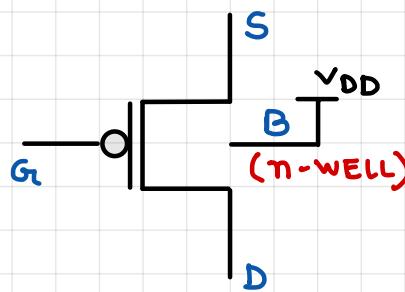
- For the nMOS, the Body needs to be connected to ground.



The Body of the nMOS  
is the p-SUBSTRATE.  
∴ The p-SUBSTRATE needs

to be connected to GND.

- For the pMOS, the Body needs to be connected to supply or  $V_{DD}$

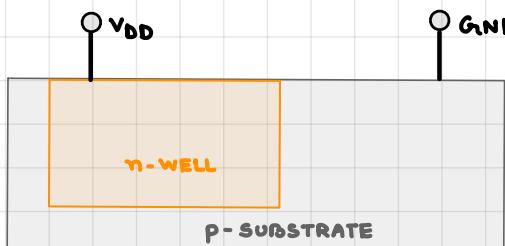


The Body of the pMOS

is the n-WELL.

∴ The n-WELL needs to be connected to  $V_{DD}$

Therefore, we need contacts that will let us connect the p-substrate to GND and the n-WELL to  $V_{DD}$ . These contacts to p-sub and n-WELL, are called SUBSTRATE and WELL CONTACTS OR, TAPS.



Now, we will look at some of the properties that these TAPS must have.

### WHY DO WE NEED TAPS?

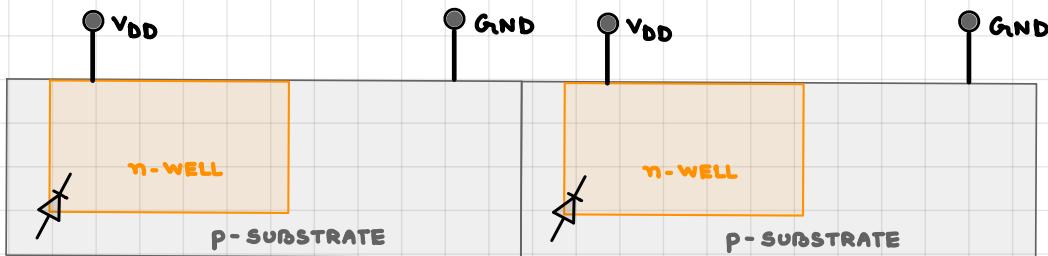
We set the n-well to  $V_{DD}$  and the substrate to GND. This is done for the following reasons :-

- So that we get good electrical properties of the MOSFET.  
(else the threshold voltage of the MOSFET will change. This is known as BODY EFFECT)
- So as to prevent the diodes (p-n junction) from being FORWARD BIASED.





If the p-n junction diodes are forward biased then current will flow from the p-substrate to the n-well and this causes unnecessary power consumption. So we want to reverse bias these diodes. These diodes are called PARASITIC DIODES.



Also, all of the n-wells MUST be connected to  $V_{DD}$ , as shown above to make sure that all of the parasitic diodes are reverse-biased.

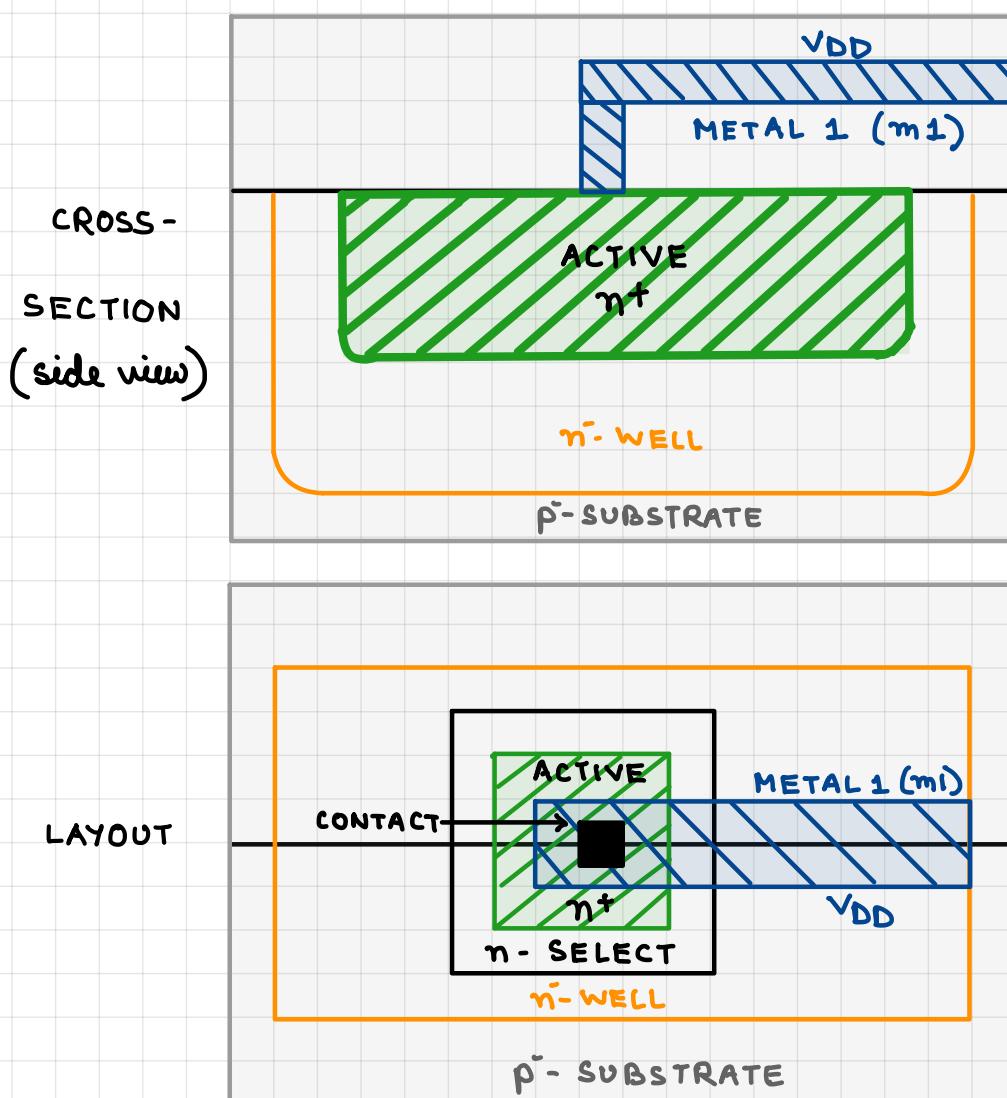
These TAPS should be placed at regular intervals (even for the substrate) so as to ensure a strong  $V_{DD}$  and GND connection for the n-wells and the substrate respectively (else there may be potential differences due to noise). Typically, TAPS are placed every few  $\mu\text{m}$ .

We have seen in Module 2 - Part B, that we cannot directly connect a metal line to a lightly doped region. So we need an  $n^+$  region within the n-well to prevent Schottky junctions.

Please note Schottky junctions are beyond the scope of our course and it is enough for us to know that it is a junction between a metal and a lightly doped semiconductor and it is highly resistive. Thus, to make a 'good connection', we need to connect a metal line to a heavily doped semiconductor.

Thus, to connect metal 1 to the n-well, we will need an additional n<sup>+</sup> region since the n-well is lightly doped. Whenever, we have a diffusion layer (in this case, n<sup>+</sup>), we will also need a select layer. Therefore, we will need a select layer on the n-well and the n<sup>+</sup> active layer on top of it. Now, we can connect the METAL 1 (connected to V<sub>DD</sub>) to the n<sup>+</sup> active layer with a CONTACT (block square) in between. This is shown below :-

### WELL TAP :-

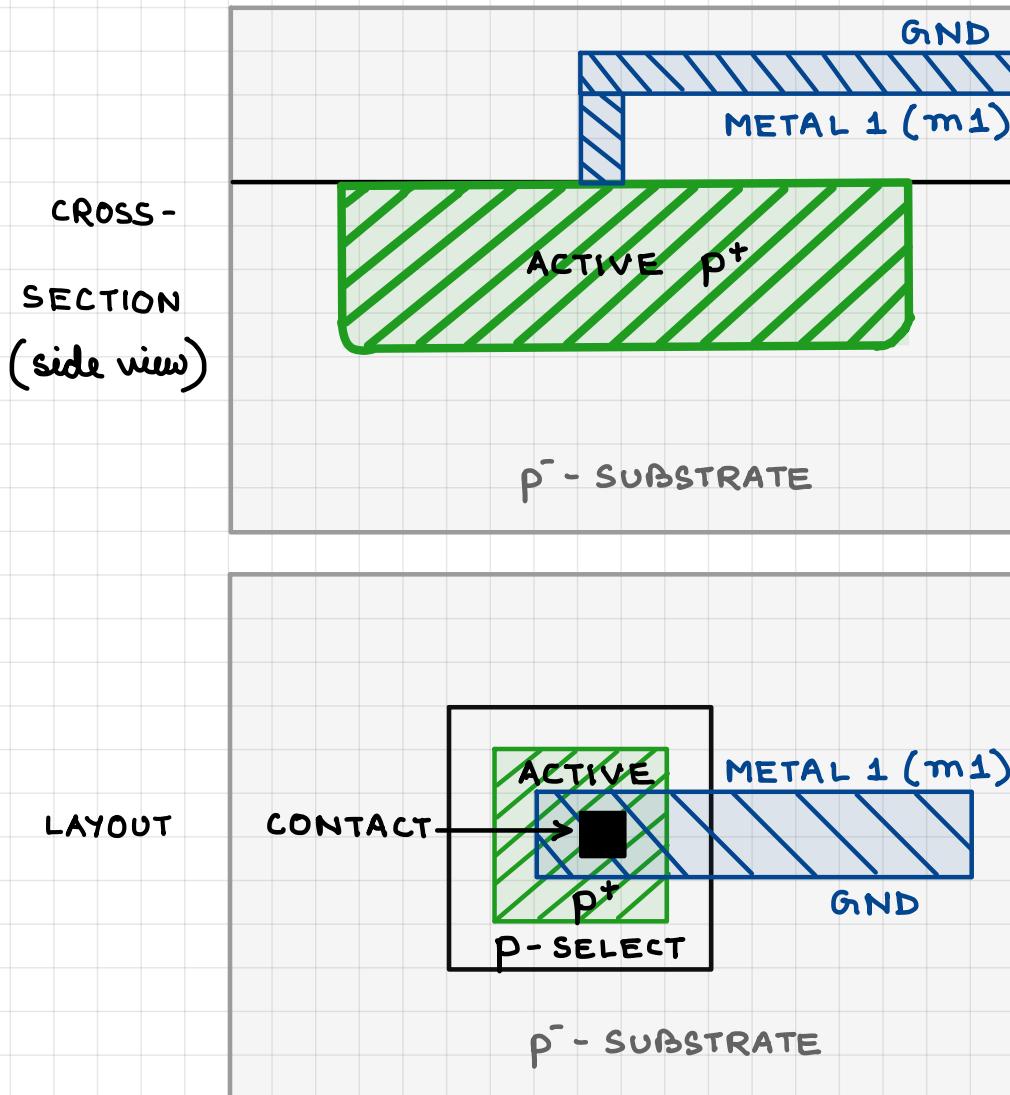


Similarly, we will have the SUBSTRATE TAP. Here too we cannot directly connect the metal line to the lightly doped p<sup>-</sup> region of the substrate. We will need a similar p-select

layer and a p+ active layer to make this connection.

We can draw this as below :-

### SUBSTRATE CONTACT :-



In your PROJECT, you will work with a particular technology node and you will see that some of these layers are named differently or there may be specific rules that you will need to follow. But these are the main layers that you will see whenever you are designing a LAYOUT from any SCHEMATIC.

Now that we have seen the different layers of a LAYOUT DESIGN, we will look at the DESIGN RULES associated with these layers. These are often known as DR. There are many design rules and with scaled process nodes the number of Design Rules have increased a lot. But here , we will talk about the BASIC DESIGN RULES.

These design rules allow us to fabricate our LAYOUT .

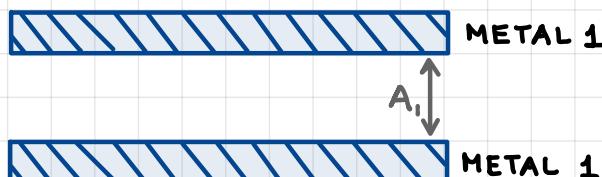
### DESIGN RULES :-

#### ① MINIMUM SEPARATION RULE →

These rules tell us how close a particular element can be to another . These may be :-

##### ⓐ INTRALAYER :- Which is within each layer .

For example , if we have two metal 1 lines , there should be a minimum distance of separation between these lines .

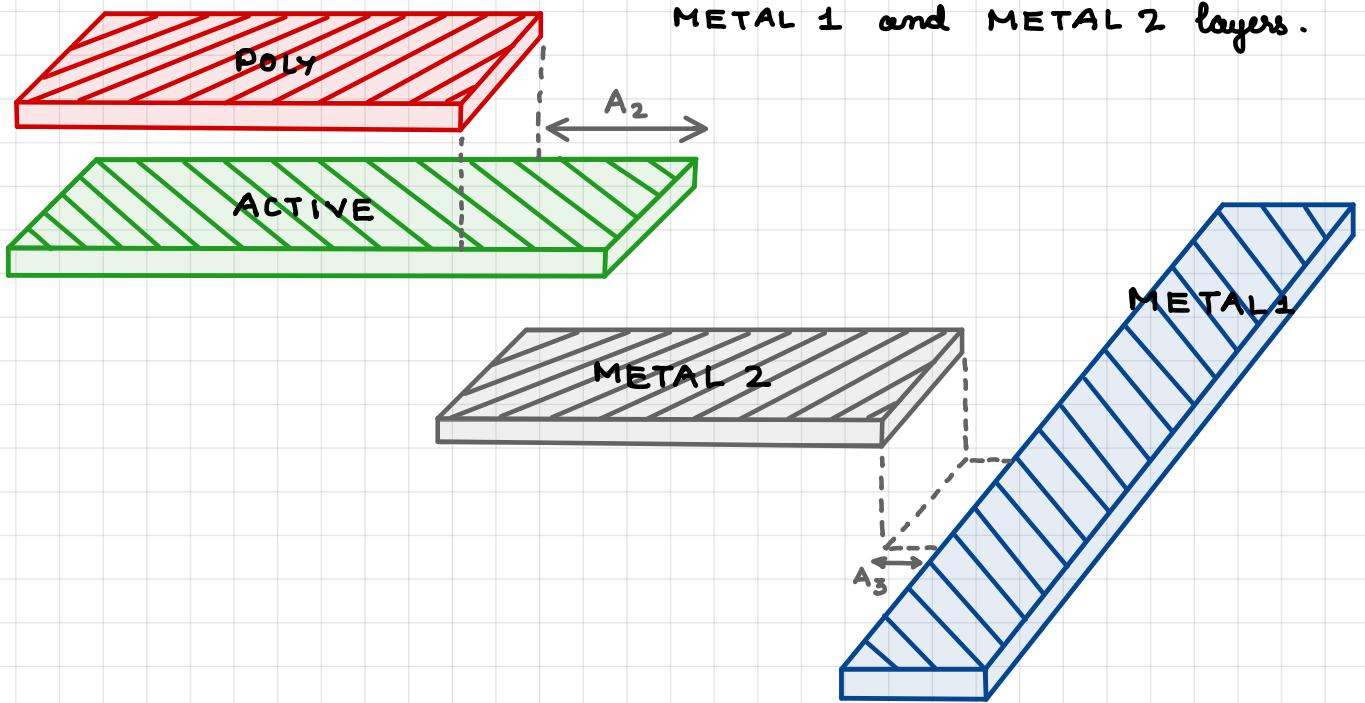


##### ⓑ INTERLAYER :- Which is from one layer to another .

We cannot have the edge of one layer very close to that of another layer. This is particularly true for the lower layers

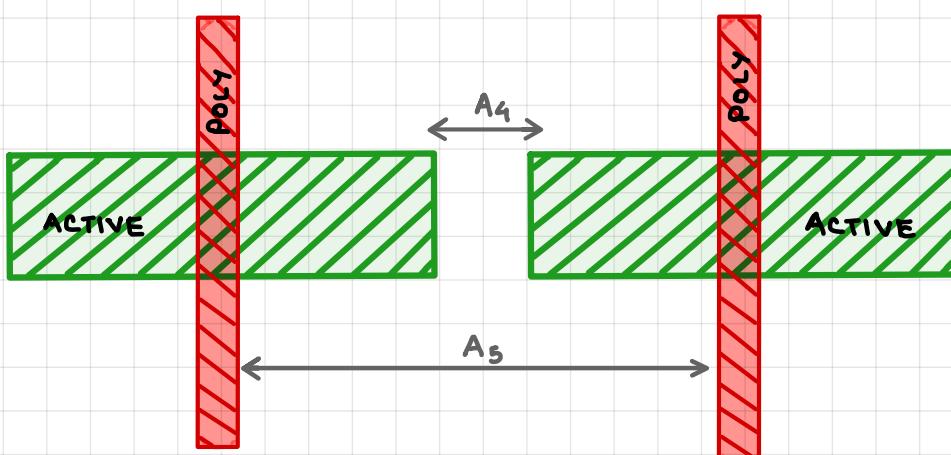
For example, we cannot have the edge of an active layer very close to the edge of a poly layer and so on .

Here we see that we should have a minimum distance of separation between the active and the poly layers and the METAL 1 and METAL 2 layers.



c) TRANSISTOR to TRANSISTOR :- Which is between one transistor and the next. We know that we have a transistor whenever a poly layer crosses an active layer.

There will be a minimum distance of separation between two transistors as shown below :-

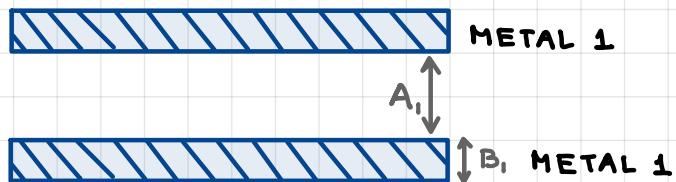


There are several such minimum distance of separation rules depending upon the process technology nodes. All of these rules must be followed in order for the LAYOUT DESIGN to pass the Design Rule Check or DRC.

## ② MINIMUM WIDTH RULE →

all layers have a minimum width. We cannot make the layers as narrow as we want to increase density (and as a result decrease the Area)

For example , if we have two METAL 1 layers , we cannot make these narrower than a certain given width ( here ,  $B_1$ ).

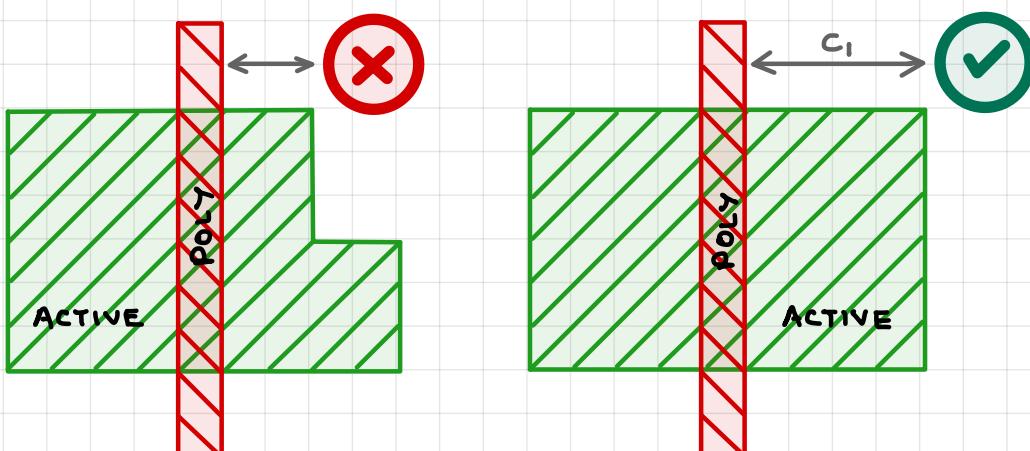


## ③ MINIMUM OVERLAP RULE →

If we have two layers that overlap , we need to have a minimum area of overlap between them.

### a) PAST A TRANSISTOR (ACTIVE - POLY) :-

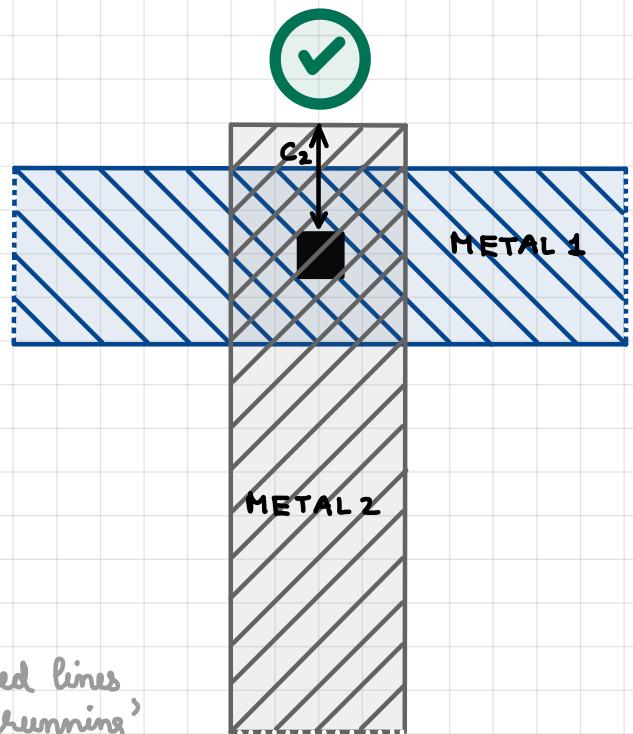
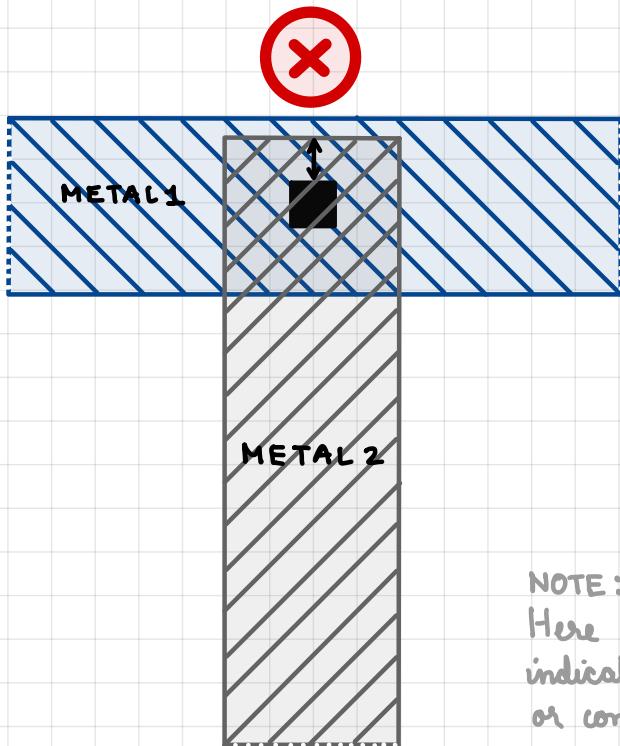
This is a classic example of the minimum overlap rule . We know that whenever poly crosses active , we have a transistor . But there should be a minimum overlap between the edge of the poly and that of the active as shown below :-



## (b) AROUND THE CONTACTS :-

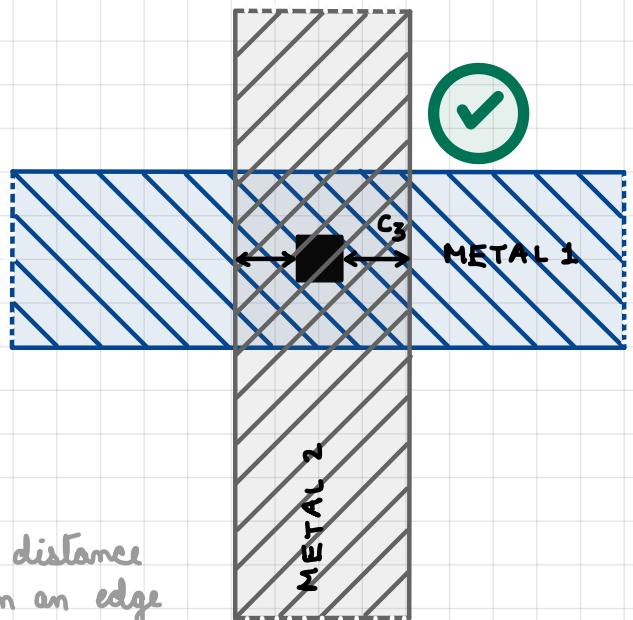
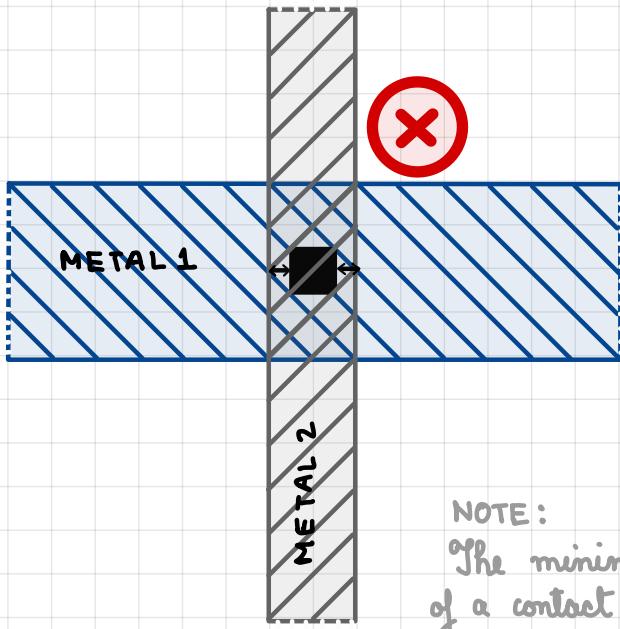
We need to have a minimum area of overlap between a contact and the layers that it is connecting.

See the examples below :-



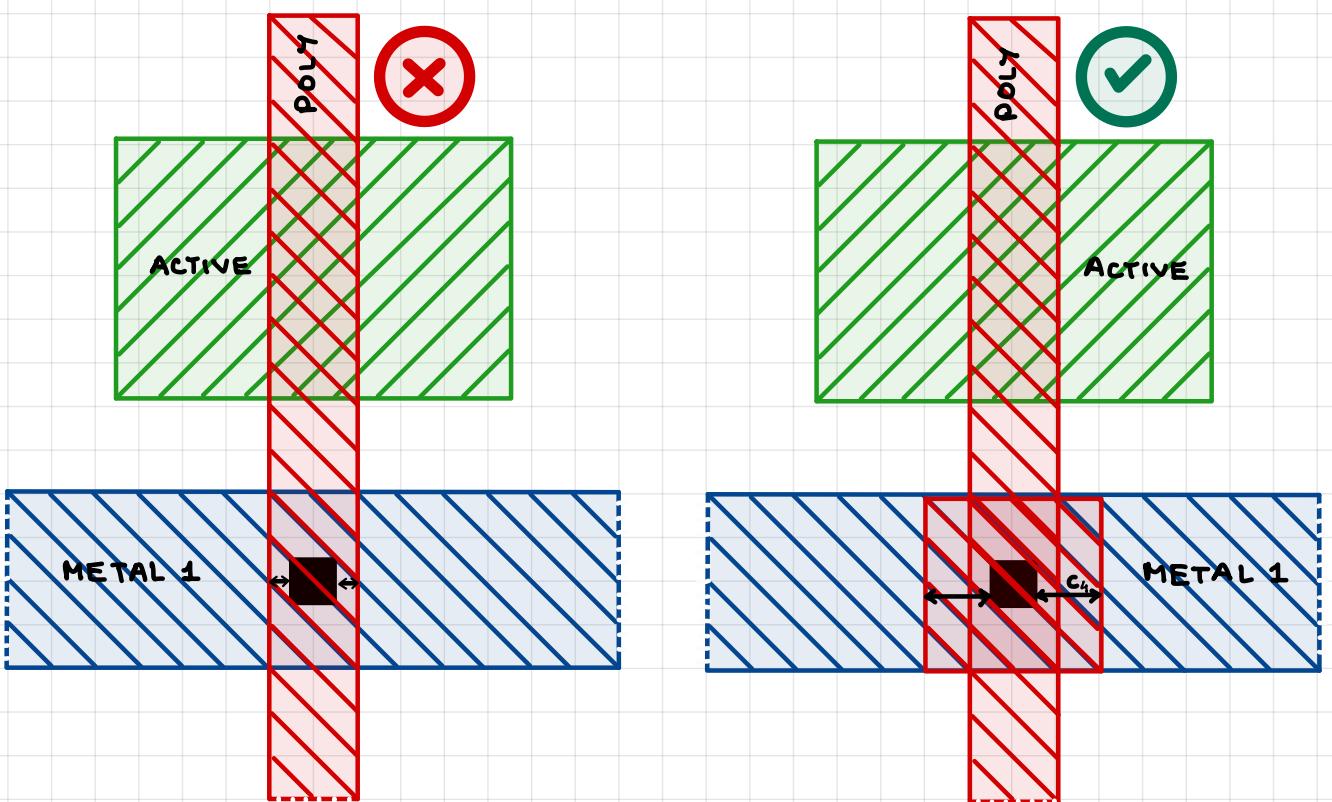
NOTE:

Here dotted lines indicate 'running' or continuous layers



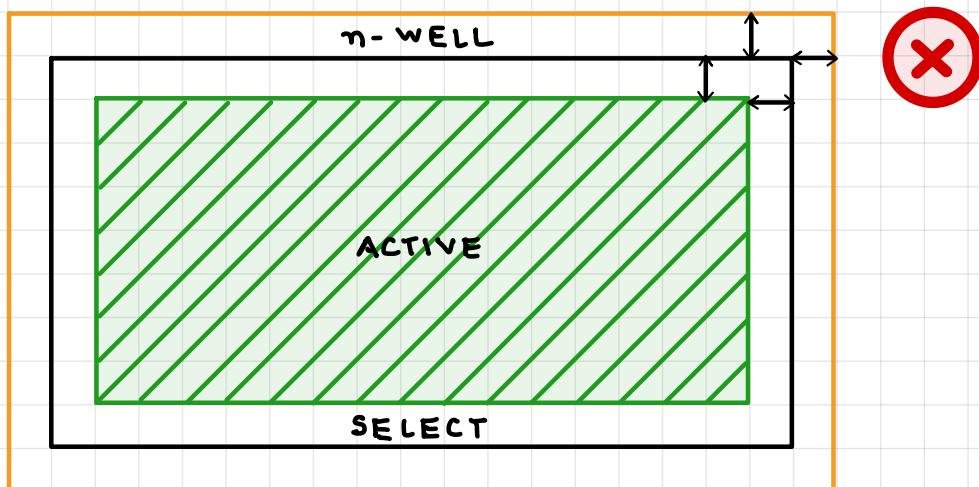
NOTE:

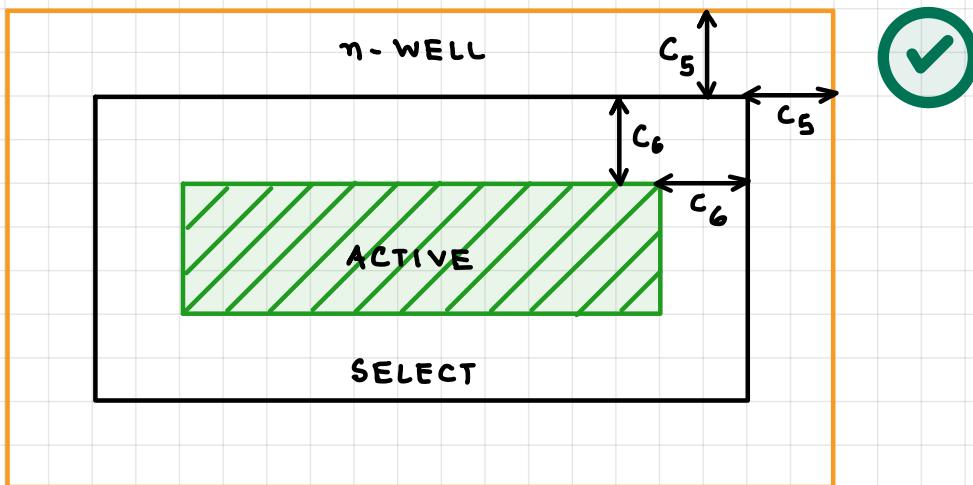
The minimum distance of a contact from an edge of layer A may not be the same as the minimum distance from the edge of layer B when the contact is connecting layer A and layer B.



### C AROUND ACTIVE LAYERS and WELLS :-

There needs to be a minimum distance between the edge of the ACTIVE LAYER and the SELECT LAYER as well as between the edges of the SELECT LAYER and the n-WELL LAYER. This is shown below :-



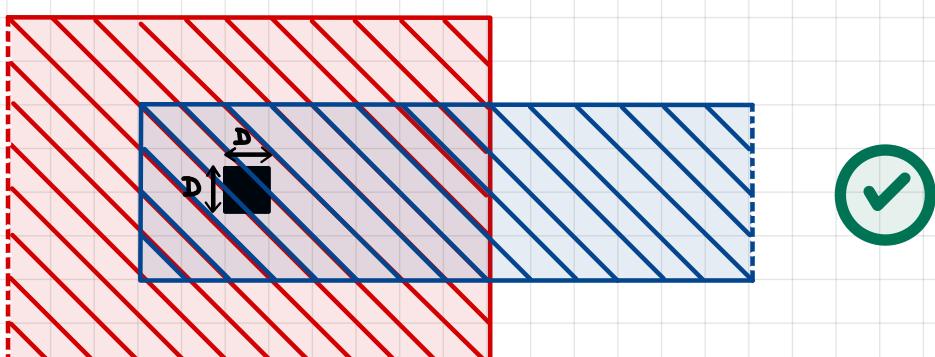
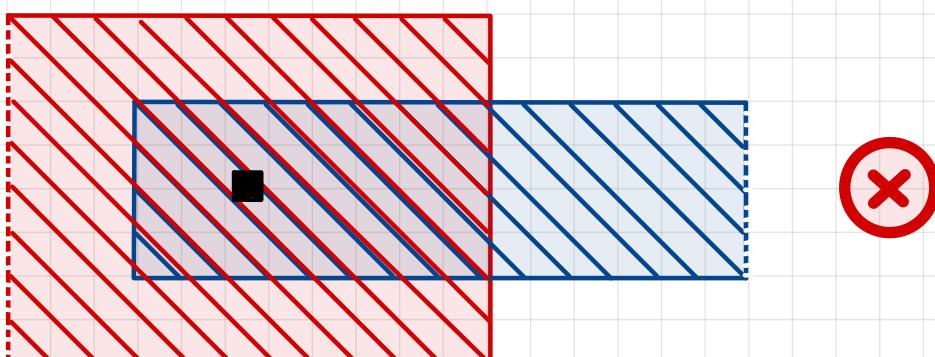


#### ④ EXACT SIZES or CUTS →

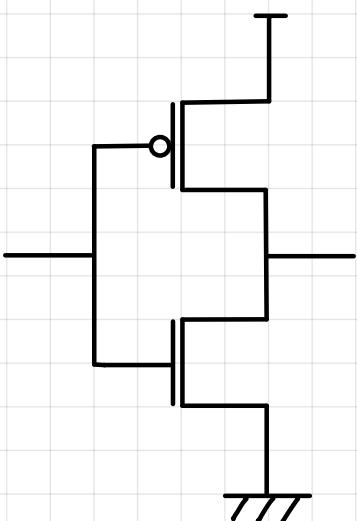
There are specific layers where only one particular size is allowed.

For example, a contact can only be of a certain length and width, and since it is usually a square, these lengths are equal (say,  $D$ )

This is shown below :-



Now that we have seen how this works, let us look at an example of the LAYOUT of a CMOS INVERTER.



In order to draw the LAYOUT of an INVERTER, we will follow the STEPS below. Later on, we will see how we can generalize this to draw the layout of a standard digital cell.

### STEP 1:

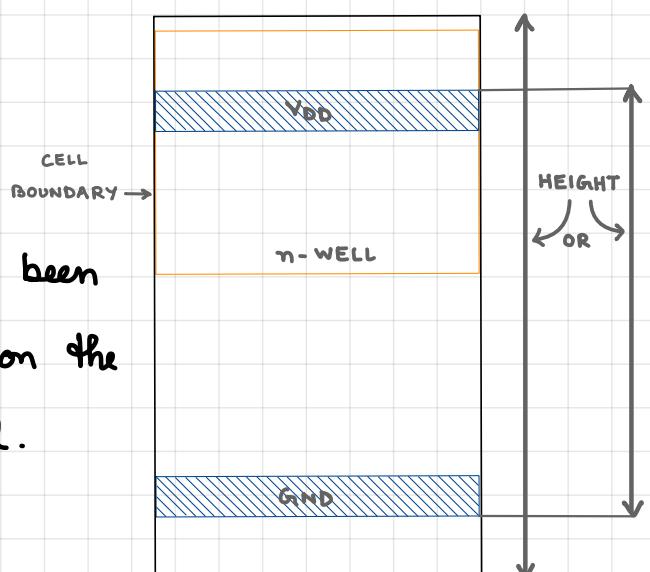
The first step is to set up the pitch of the cell. This is also the height of the cell, which in this case is an inverter. The cell height can either be from the top of the cell boundary to the bottom of the cell boundary. Sometimes it is also used to denote the height from the top of the  $V_{DD}$  power rail to the bottom of the GND power rail. (see layout below)

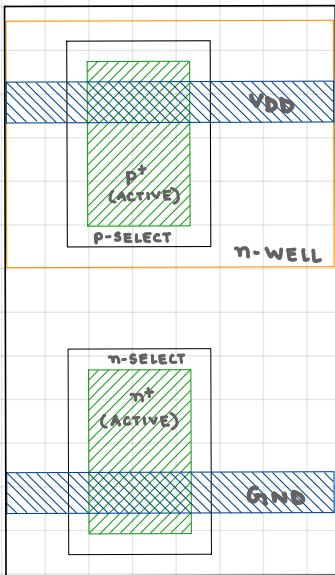
### STEP 2:

Along with defining the cell pitch, we will draw the  $V_{DD}$  and GND power rails that will provide the supply voltage to the inverter. We will see later on that all the digital cells will have the same height.

### STEP 3:

After the power and GND lines have been drawn, we will draw the n-WELL on the top half (typically top 50%) of the cell.





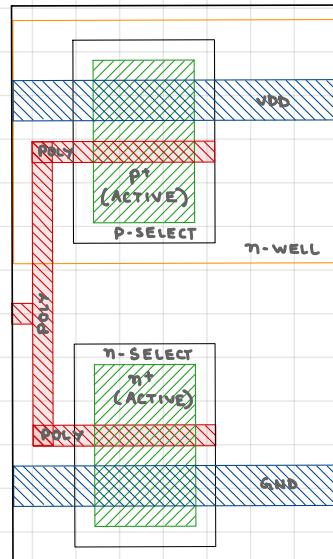
#### STEP 4 :

In this step, we will define the transistors. We will draw the n-select and the p-select regions followed by the n+ and p+ active regions. Please note

that although we draw the select regions with the same colors and the active regions with the same colors, they will be complementary for the n-MOS and the p-MOS.

#### STEP 5 :

The next step is to define the transistor using the polysilicon. Note that the gate of the pMOS and that of the nMOS are shorted. We use the polysilicon layer to make the connection as shown here.



#### STEP 6 :

Next the transistors need to be contacted. We define the diffusion cuts and use contacts to connect the transistor source/drain using metal lines and follow the connections from the schematic. At this point the transistors are defined

and properly connected as shown below :-

NOTE :-

The block boxes

are the contacts.

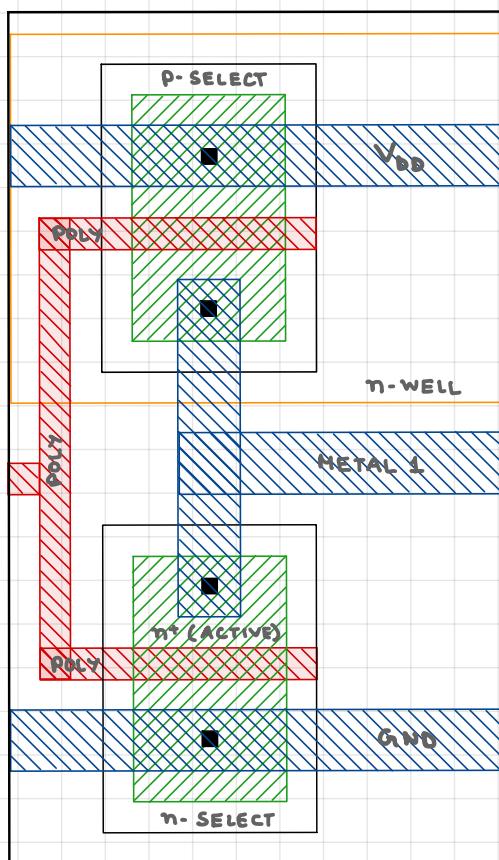
Also, the n-WELL

and the  $V_{DD}$  and

GND lines are

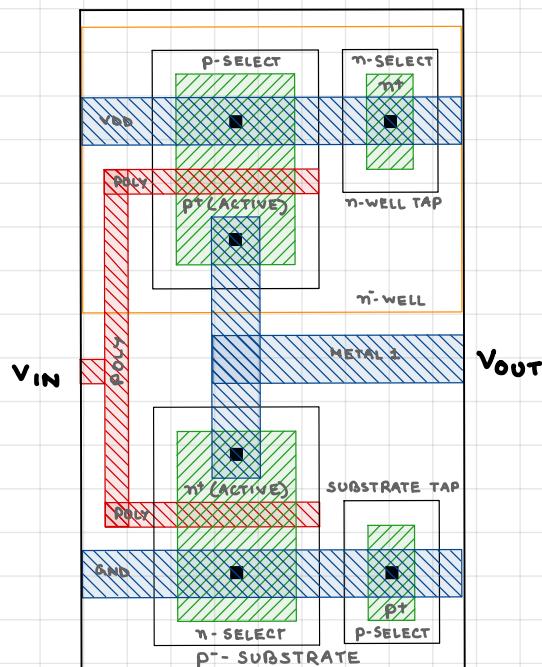
extended to the

cell boundary.



### STEP 7 :

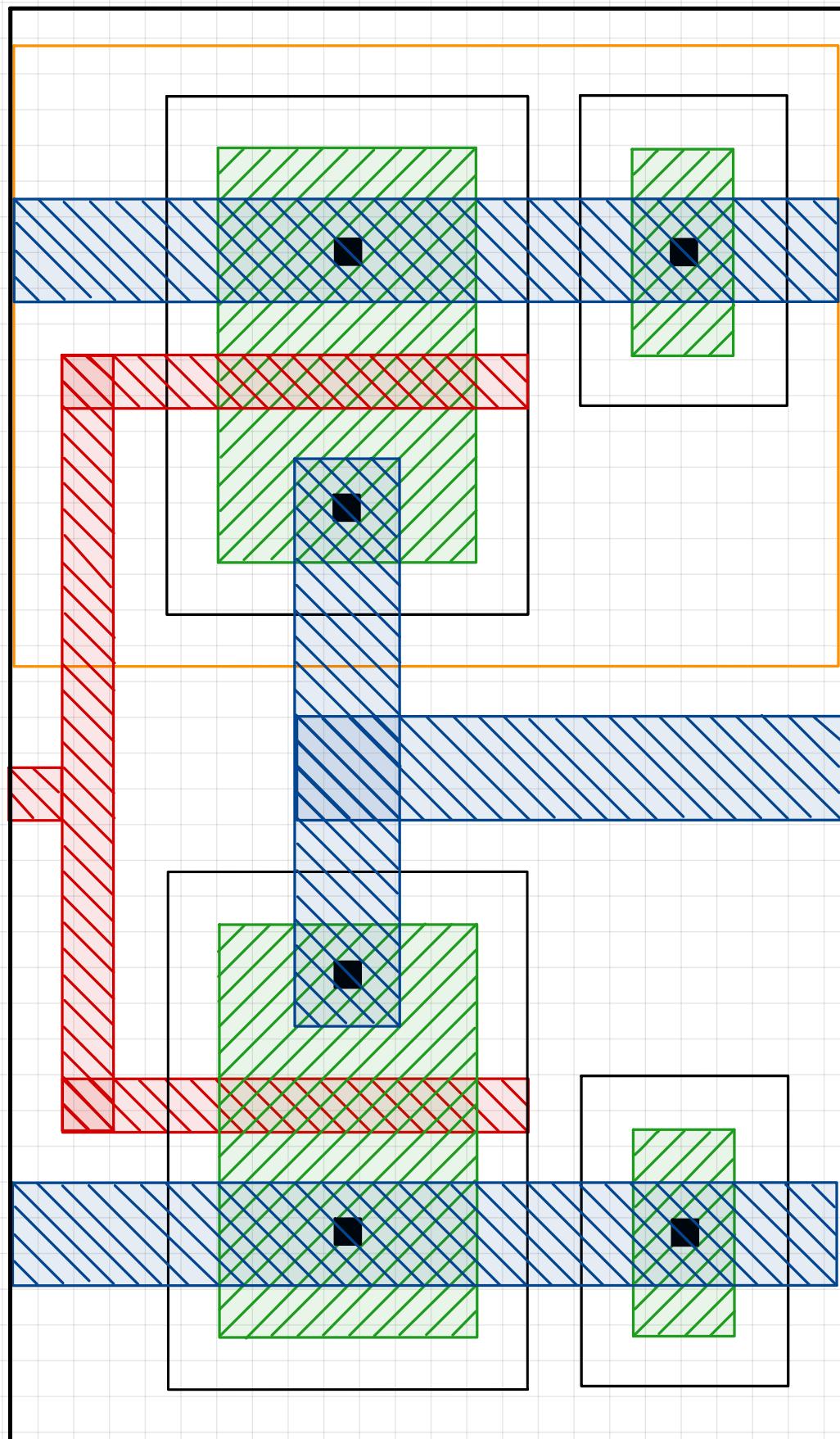
We have seen that the body of the transistors need to be connected to supply and GND for the pMOS and nMOS respectively. We use an n-WELL tap to connect the pMOS body to  $V_{DD}$  and a substrate tap to connect the nMOS body to GND.



## STEP 8 :

In this final step, we can connect the layout of the inverter to external circuits. In particular, we can connect  $V_{IN}$  and  $V_{OUT}$  to other digital logic cells. This is not shown here.

## FINAL LAYOUT :-



NOTE :-

Here, we have used polysilicon to connect the gates of the two transistors. We did not use poly cut to connect to metal 1 and then use metal 1 to connect the transistor gates. Polysilicon is resistive and cannot conduct as efficiently as the metal layers. However, the gate of the transistor has infinite input impedance, (we have seen this before) so it does not matter if the gate connection is made with polysilicon connections , as long as they are not too long . If the polysilicon is too long , it will affect the transient performance ( we will see this later ). The use of polysilicon for gate connections saves a lot of area in the inverter cell .