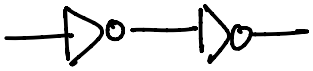
1. Consider a scenario where an inverter is driving an **identical** inverter. This means that the driver and the load inverters are exactly identical. Assume that the width of the PMOS to the width of the NMOS (for both the driver and the load inverter) is $\alpha$. Also assume that the wire capacitance is negligible and can be ignored. The output capacitance per unit width and the input gate capacitance per unit width is the same for both the NMOS and the PMOS. Both NMOS and PMOS have identical lengths, $C_{ox}$ and threshold voltages. We have seen that the propagation delay of the inverter can be written as:

$\frac{W_p}{W_n} = \frac{\alpha}{1}$ $\quad W_n = \alpha W_n$



$$t_p = \frac{C_L}{2V_{DD}}\left(\frac{1}{\beta_n} + \frac{1}{\beta_p}\right)$$

Prove that the optimal value of $\alpha$ so that the propagation delay is minimum, is given by:

$$\alpha_{optimal} = \sqrt{\frac{\mu_n}{\mu_p}}$$

**Hint**: Write down the propagation delay in terms of $\alpha$ and differentiate it with respect to $\alpha$ and set it to zero.

**Note:** The optimal $\alpha$ in this case is different from all the case that we have studied in the class where the optimal $\alpha$ for symmetric switching is just the ratio of the mobilities.

$$t = \frac{C_L}{2V_{DD}}\left[\frac{L}{\alpha \mu_p C_{ox}} + \frac{L}{\mu_n C_{ox}}\right]\frac{1}{W_n}$$

$$C_L = C_{out} + C_{in} = (1+\alpha)(\tilde{C}_{out} + \tilde{C}_{in})$$

$$t = \frac{(1+\alpha)(\tilde{C}_{out} + \tilde{C}_{in})L}{2V_{DD}(\alpha \mu_p C_{ox})W_n} + \frac{(1+\alpha)(\tilde{C}_{out} + \tilde{C}_{in})L}{2V_{DD}\mu_n C_{ox} W_n}$$

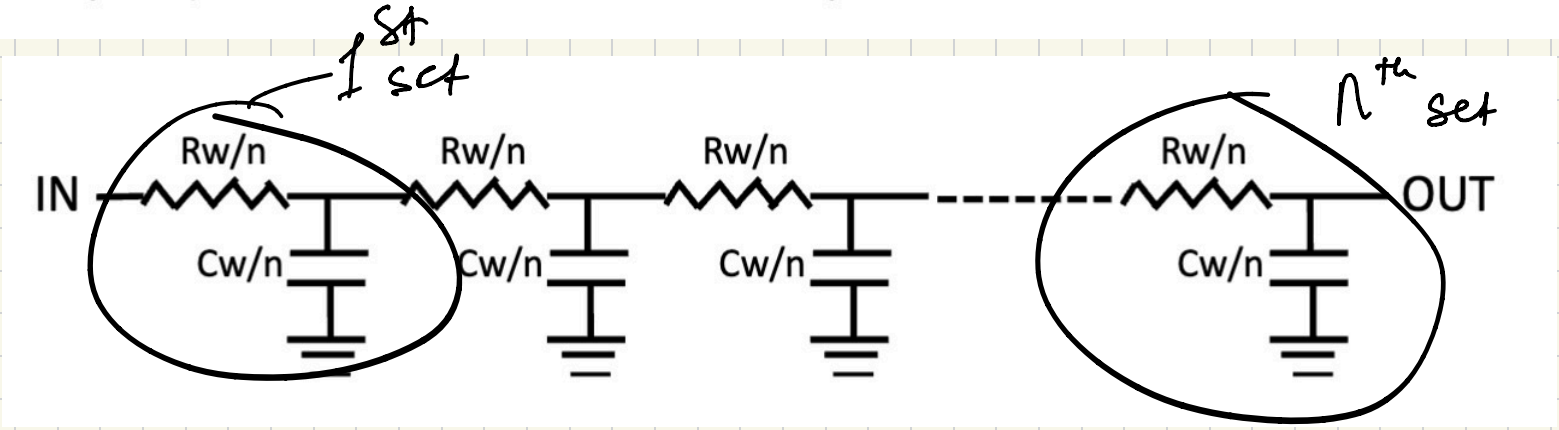
$$\left[\frac{(\tilde{C}_{out} + \tilde{C}_{in})L}{2V_{DD}\alpha\mu_p C_{ox}W_n} + \frac{\alpha(\tilde{C}_{out} + \tilde{C}_{in})L}{2V_{DD}\alpha\mu_p C_{ox}W_n} + \frac{(\tilde{C}_{out} + \tilde{C}_{in})L}{2V_{DD}\mu_n C_{ox}W_n} + \frac{\alpha(\tilde{C}_{out} + \tilde{C}_{in})L}{2V_{DD}\mu_n C_{ox}W_n}\right]\frac{d}{d\alpha}$$

$$-\frac{(\tilde{C}_{out} + \tilde{C}_{in})L}{2V_{DD}\mu_p C_{ox}W_n\alpha^2} + \frac{(\tilde{C}_{out} + \tilde{C}_{in})L}{2V_{DD}\mu_n C_{ox}W_n} = 0 \quad (2V_{DD}C_{ox}W_n)$$

$$+\frac{(\tilde{C}_{out} + \tilde{C}_{in})L}{\mu_p \alpha^2} = \frac{(\tilde{C}_{out} + \tilde{C}_{in})L}{\mu_n}$$

$$\Rightarrow \sqrt{\frac{\mu_n}{\mu_p}} = \alpha$$

2. An interconnect has a total resistance of *Rw* and a total capacitance of *Cw*. If this interconnect is broken down into *n* segments, in series (see picture below) where each individual segment has a resistance of *Rw/n* and a capacitance of *Cw/n*, find an expression for the total delay of the interconnect.
In the limit where *n* tends to infinity (i.e., the interconnect is divided into an infinite number of pieces) what is the effective interconnect delay?




$$T_n = \ln(2)\left[\frac{R_w}{n}\,\frac{C_w}{n}\right] \qquad T_t = T_1 + T_2 + T_3 + \ldots + T_{n-3} + T_{n-2} + T_{n-1}$$

$$T_{n-1} = \ln(2)\left[\frac{R_w}{n}\left(2\,\frac{C_w}{n}\right)\right]$$

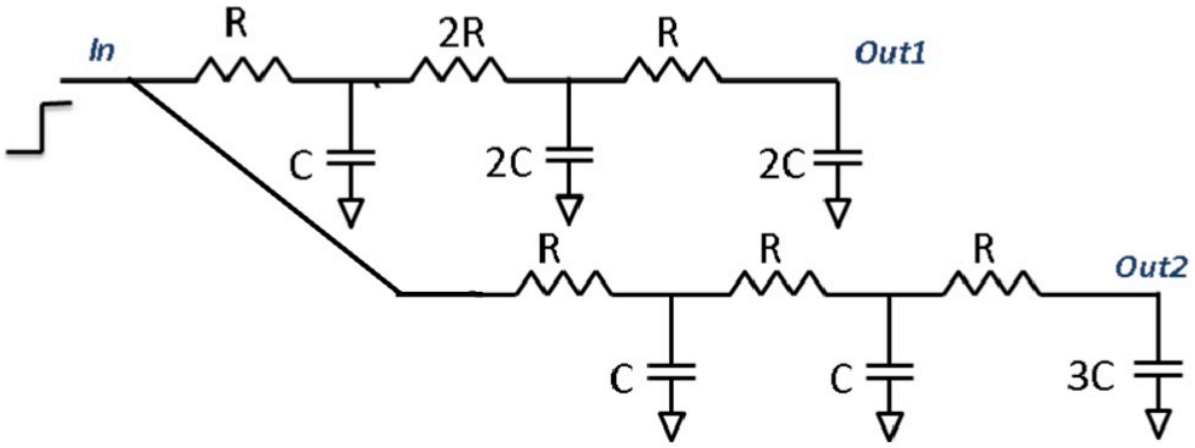
$$T_{n-2} = \ln(2)\left[\frac{R_w}{n}\left(3\,\frac{C_w}{n}\right)\right]$$

$$T_1 = \ln(2)\left(\frac{R_w}{n}\right)\left(\frac{C_w}{n}\right)(n)$$

$$T_t = \ln(2)\,\frac{R_w}{n}\,\frac{C_w}{n}\left(\frac{n(n+1)}{2}\right) \Rightarrow \ln(2)\,\frac{R_w C_w}{2}\left(\frac{n+1}{n}\right)$$

$$\lim_{n\to\infty}\left[\ln(2)\,\frac{R_w C_w}{2}\left(1+\frac{1}{n}\right)\right] \Rightarrow \boxed{t_t = \ln(2)\,\frac{R_w C_w}{2}}$$

3. Consider the RC circuit shown below:




Use the Elmore Delay model to determine the delay from *In* to *Out1* and from *In* to *Out2*.

The time Delay for the ith Node is

$$t_{PD} = \sum_i R_{is} C_i \Rightarrow \text{for out 1}$$

$$\ln(2)\left[RC + (R+2R)\cdot 2C + (R+2R+R)\cdot 2C\right] = RC + 6RC + 8RC \Rightarrow$$

$$\boxed{\ln(2)\cdot 15RC = 10.36RC}$$

$$\ln(2)\left[RC + 2RC + 9RC\right] = \boxed{\ln(2)\,12RC = 8.32RC}$$

4. What happens to the intrinsic delay (tpi) of in inverter when:
   a. The supply voltage is decreased
   b. The transistor widths are increased
   c. The load inverter is removed
   d. Transistor mobility is increased

   Explain each of your answers.

$t_{pi}$ is Given By $= \frac{\tilde{C}_{out}}{2 V_{DD} \tilde{\beta}}$

a) if Supply $V_{DD}$ is Decreased $\Rightarrow t_{pi} \uparrow$ Since

$t_{pi} \propto \frac{1}{V_{DD}}$

b) Since $\frac{1}{\tilde{\beta}} = \frac{w_d}{\beta_p} + \frac{w_d}{\beta_n}$

$t_{pi} \propto \frac{1}{\tilde{\beta}}$ $\quad \beta_p = \frac{\alpha w_d}{L} \nu_p C_{ox} \Rightarrow \frac{L}{\alpha w_d \nu_p C_{ox}} = \frac{1}{\beta_p}$

$\beta_n = \frac{w_d}{L} \nu_n C_{ox} \Rightarrow \frac{L}{w_d \nu_n C_{ox}} = \frac{1}{\beta_n}$

$\Rightarrow \frac{1}{\tilde{\beta}} = \frac{L}{\alpha w_p C_{ox}} + \frac{L}{\nu_n C_{ox}}$ $\Rightarrow$ Since $\tilde{\beta}$ has No dependence on $w_d \Rightarrow t_{pi} \Rightarrow$ NO change for $w_d \uparrow$

c) Since the loaded inverter is independent of $t_{pi}$

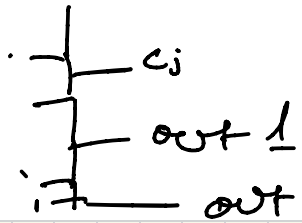
$\Rightarrow t_{pi}$ Does Not Change.

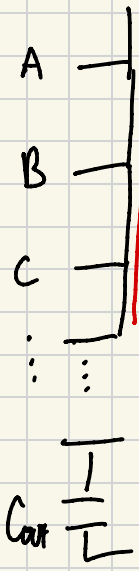
d) If $\nu_n$ or $\nu_p \uparrow \Rightarrow t_{pi} \downarrow$ Since $t_{pi} \propto \frac{1}{\tilde{\beta}} \propto \frac{1}{\nu_n}$

5. The total charging delay of an N input NOR Gate in terms of Rp (resistance of each PMOS transistor), $C_L$ (load capacitance at VOUT), and $C_J$ (total junction capacitance at each junction) can be expressed as:

$$T = 0.69\ (N.R_p.C_{OUT} + R_p.C_J\ f(N))$$

where f(N) is a function of N. Determine f(N).




if $T = \ln(2)\left[N \cdot R_p \cdot C_{out} + R_p \cdot C_j\, f(N)\right]$

$$f(N) = \sum_{i=1}^{N} i = \frac{N(N-1)}{2}$$

since for each successive device we add the $R_p$ and $C_j$

$\Rightarrow$ Elmore Delay Principle