**ECE 3030: Physical Foundations of Computer Engineering**
Fall 2021
Homework 6—Total points 100
Due on Saturday 11/20/2021 at 11.59am. In case of a late submission, you will be penalized by 50 points for each day after the submission deadline has passed. You will receive no score if you submit after the solution has been posted.

Q1 According to the scaling model proposed by Dennard *et al.*, in every subsequent generation, all three physical dimensions ($W$, $L$, $t_{ox}$), the power supply voltage $V_{DD}$ and the threshold voltage, $V_t$ are downscaled by factor of $x$ ($x$ >1). Show that in this scenario, the clock frequency can be increased by a factor of $x$ while keeping the chip power density (in W/cm$^2$) keeping the same. [40 pts]

**Solution to Q1:**

Total Area of the microprocessor chip=A

Area of a transistor in n-th generation=WL
# of transistors in n-th generation, $N_n$=A/WL

Area of a transistor in n+1-th generation=WL/x$^2$
# of transistors in n+1-th generation, $N_{n+1}$=A/WL=$N_n$x$^2$

Load capacitance in n-th generation $C_{L,n} = \frac{\epsilon_o \epsilon_{ox} WL}{t_{ox}}$

Load capacitance in n+1-th generation $C_{L,n+1} = \frac{\epsilon_o \epsilon_{ox} (\frac{W}{x})(\frac{L}{x})}{\frac{t_{ox}}{x}} = \frac{C_{L,n}}{x}$

On current in n-th generation $I_{on,n} = \mu C_{ox,n} \frac{W}{2L} (V_{DD} - V_{t,n})^2$

On current in n+1-th generation $I_{on,n+1} = \mu C_{ox,n} x \frac{\frac{W}{x}}{\frac{L}{x}} (\frac{V_{DD}}{x} - \frac{V_{t,n}}{x})^2 = \frac{I_{on,n}}{x}$

Delay in n-th generation $t_n = \frac{C_{L,n} V_{DD}}{I_{on,n}}$

Delay in n-th generation $t_{n+1} = \frac{\frac{C_{L,n} V_{DD}}{x \quad x}}{\frac{I_{on,n}}{x}} = \frac{t_n}{x}$

Power dissipated in a logic gate in n-th generation $P_n = C_L V_{DD}^2 f$

Power dissipated in a logic gate in n+1-th generation $P_{n+1} = \frac{C_L}{x} \frac{V_{DD}^2}{x^2} fx = \frac{P_n}{x^2}$

Total Area of the microprocessor chip=A

Area of a transistor in n-th generation=WL
# of transistors in n-th generation, $N_n$=A/WL

Area of a transistor in n+1-th generation=WL/x$^2$
# of transistors in n+1-th generation, $N_{n+1}$=A/WL=$N_n$x$^2$

Total Power dissipated in a microprocessor chip in n-th generation $P_{total,n} = P_n N_n$

Total Power dissipated in a microprocessor chip in n+1-th generation $P_{total,n+1} = \frac{P_n}{x^2} N_n x^2 = P_{total,n}$

Q2 In the scenario where, in each subsequent generation, you could downscale only the three physical dimensions ($W$, $L$, $t_{ox}$) by a factor of $x$ but had to keep $V_{DD}$ and $V_t$ fixed, how would you have changed the clock frequency? [30 pts]

**Solution to Q2:**
With $W$, $L$, $t_{ox}$ scaling by a factor of $x$, $C_{L,n+1} = C_{L,n}/x$.

Power dissipated in an inverter in n-th generation $P_n = C_L V_{DD}^2 f_n$.

With $V_{DD}$ not scaling, power dissipated in an inverter in n+1 generation, $P_{n+1} = C_{L,n+1} V_{DD}^2 f_{n+1} = C_{L,n} V_{DD}^2 f_{n+1} \frac{1}{x} = P_n \frac{f_{n+1}}{f_n} \frac{1}{x}$.

Total number of inverters in n+1-th generation, $N_{n+1} = \frac{A}{WL} = N_n x^2$.

Total power dissipated in the chip in n+1-th generation, $P_{total,n+1} = P_{n+1} N_{n+1} = P_n N_n \frac{f_{n+1}}{f_n} x = P_{total,n} \frac{f_{n+1}}{f_n} x$.

Ideally, you want to keep the total power (in W) or the power density (in W/cm$^2$) in the chip to constant in every generation–*i.e.*, $P_{total,n+1} = P_{total,n}$.

Hence, $\frac{f_{n+1}}{f_n} x = 1 \Rightarrow f_{n+1} = f_n / x$. In other words, you will have to reduce the clock frequency if you cant scale down $V_D D$ in successive generations to keep the power density the same.

Q3 Consider an inverter with its input voltage $V_i = 0$. Why would the inverter dissipate power even in this case? [20 pts]

**Solution to Q3:**
When $V_i$=0, the NMOSFET is off ($V_{GS,n} = 0 < V_{t,n}$). So to the first approximation, there current $I_D$ flowing through the inverter is zero. Hence power=$V_{DD} I_D$=0.

However, there is always an off-state leakage current that flows in a MOSFET since a MOSFET is not an ideal switch. When $V_i$=0, the current flowing through the NMOSFET is $I_{off}$ (=$I_{D,n}(V_{GS,n} = 0, V_{DS,n} = V_{DD})$.

You need understand why the NMOSFET current is equal to $I_{D,n}(V_{GS,n} = 0, V_{DS,n} = V_{DD})$ when $V_i$=0).

As such, at $V_i$=0, the power dissipated in the inverter =$V_{DD} I_{off}$.

Q4 In the first generation, assume delay is 20ns and a chip consumed 1.3W. After 20 generations with scaling of x=2 at each generation, what should be a chip's gate delay and power consumption? [10 pts]

**Solution to Q4:**
As per Dennard scling, if the feature size scales down by a factor of x, the time delay and power scales from $n^{th}$ generation to $(n+1)^{th}$ generation as follows:
t(n+1) = t(n)/x
P(n+1) = P(n)/$x^2$
therefore, delay and power for $n^{th}$ generation given the $1^{st}$ generation values are

t(n) = t(1)/$x^{(n-1)}$
P(n) = P(1)/$x^{2(n-1)}$
substitue t(1) as 20ns, P(1) as 1.3W, x as 2 and n as 20
t(20) = 1ns/$2^{19}$ = $1.907 \times 10^{-15} s$
P(20) = 1.3W/$2^{38}$ $\approx 4.55 \times 10^{-12} W$