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Lab 01 Report
ECE 2031 L10
01 September 2024

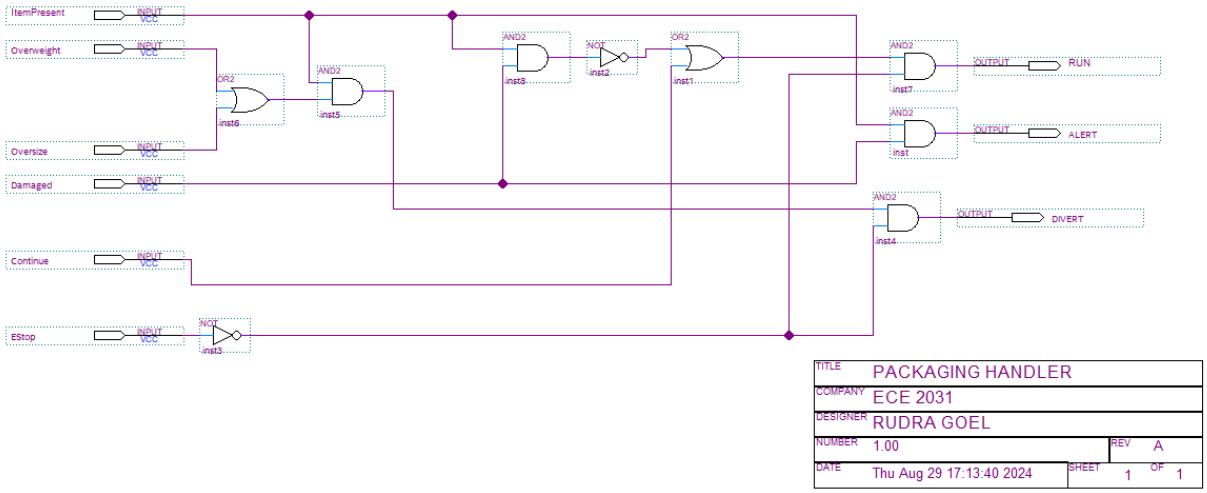

Figure 1: Schematic for package handling system. The outputs are dictated by the following boolean functions: $Run = \overline{EStop} \cdot Continue + \overline{(Damaged \cdot ItemPresent)}$. $Alert = ItemPresent \cdot Damaged$. $Divert = \overline{EStop} \cdot (ItemPresent \cdot (Overweight + Oversize))$.

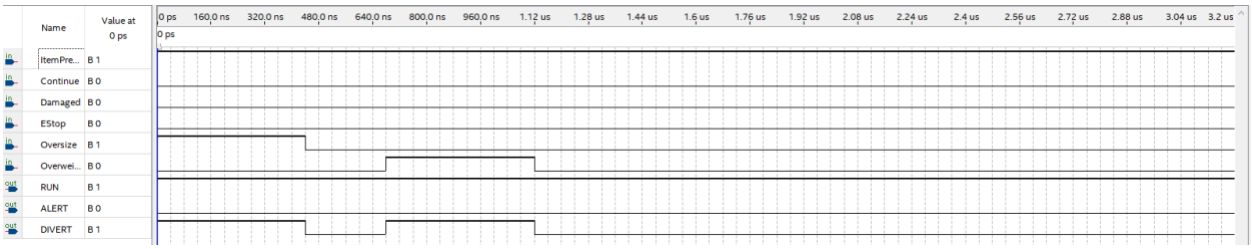

Figure 2: Simple waveform to ensure Quartus simulator working correctly. This also asserts "Divert" is active when "ItemPresent" and either "Oversize" or "Overweight" are active. "Alert" and "Run" remain inactive and active, respectively, as intended for this input.

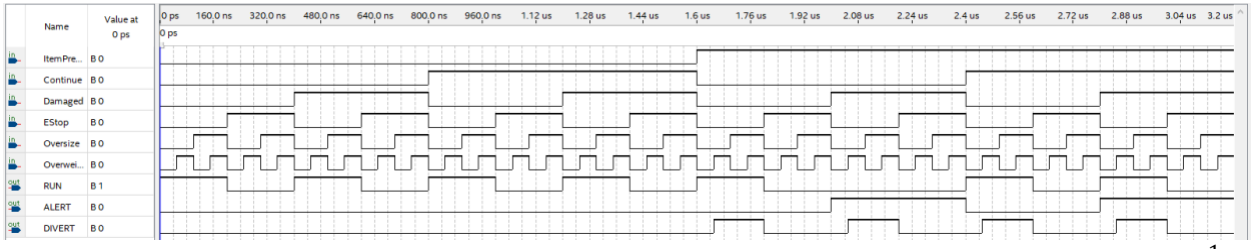

Figure 3: Complete waveform testing all possible inputs by cutting each subsequent input's period by $\frac{1}{2}$ within 3.2 μs frame. Asserts each output's result adheres to its intended boolean expression outlined in Figure 1.

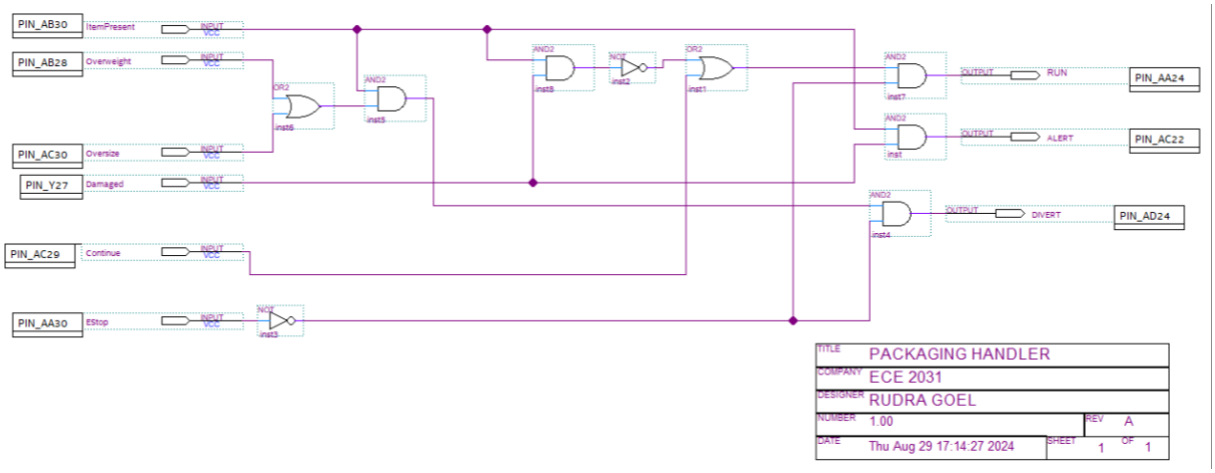

Figure 4: Package handler schematic with pin assignments for Cyclone 5 5CSXFC6D6F31C6N FPGA. Each output adheres to the boolean expressions outlined in Figure 1.