

MODULE 3 - PART C

DC CHARACTERISTICS OF CMOS GATES

In the last part (Part B) of Module 3, we had looked at the Voltage Transfer Characteristics of a typical inverter.

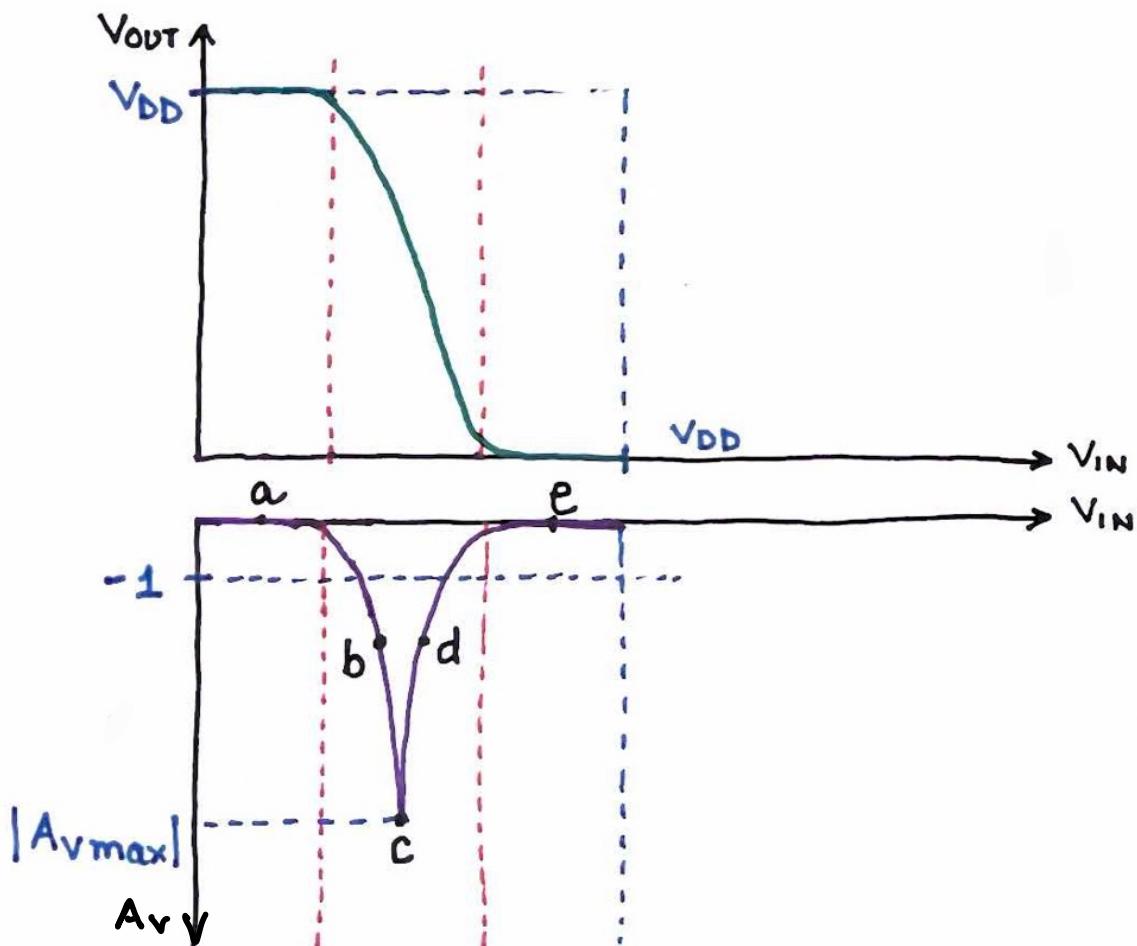
Here, we will look at some of the KEY FEATURES of the VTC.

① VOLTAGE GAIN OF THE INVERTER (A_v)

The voltage gain A_v is defined as,

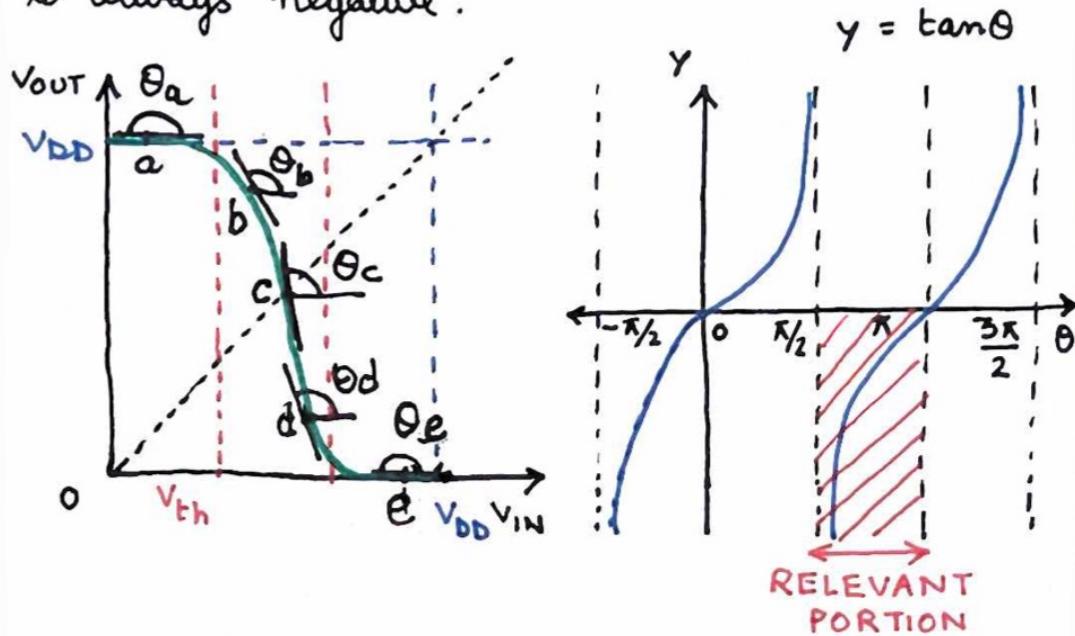
$$A_v = \frac{dV_{OUT}}{dV_{IN}}$$

It is measured by the slope of the VTC. At every point on the VTC, we calculate the $\tan \theta$ where θ is the angle that the VTC makes with the x-axis (V_{IN})



Characteristics of the GAIN PLOT :-

Since V_{OUT} decreases with V_{IN} , the gain is always negative.



Let us look at the various points on the VTC and the corresponding gain A_v .

- ① At point a, θ_a is almost $180^\circ (\pi)$ and thus $\tan \theta$ or $|A_v|$ is close to 0
(See the plot for $\tan \theta$)
- ② At point b, θ_b decreases and is between π and $\pi/2$. Thus, $|A_v|$ increases.
- ③ At point c, θ_c decreases further and is close to $\pi/2$ (lowest value of θ) and thus, $|A_v|$ is very high and is the maximum possible value of $|A_{vmax}|$.
- ④ At point d, θ_d increases again and is between $\pi/2$ and π and thus, $|A_v|$ decreases from $|A_{vmax}|$
- ⑤ Finally, at point e, θ_e is almost π and thus, $|A_v|$ is again close to 0.
Typically, $|A_{vmax}|$ is between 5 and 10

② TRIP POINT OR SWITCHING THRESHOLD OF THE INVERTER (V_M)

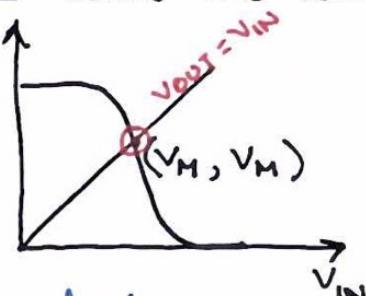
The switching threshold or the trip point of the inverter is defined as the input voltage V_M such that, the output voltage V_{OUT} is also equal to V_M .

\therefore At the trip point $V_{IN} = V_{OUT} = V_M$

If $V_{IN} < V_M$, then $V_{OUT} > V_{IN}$ and when $V_{IN} > V_M$, then $V_{OUT} < V_{IN}$. Hence, it is called the switching threshold.

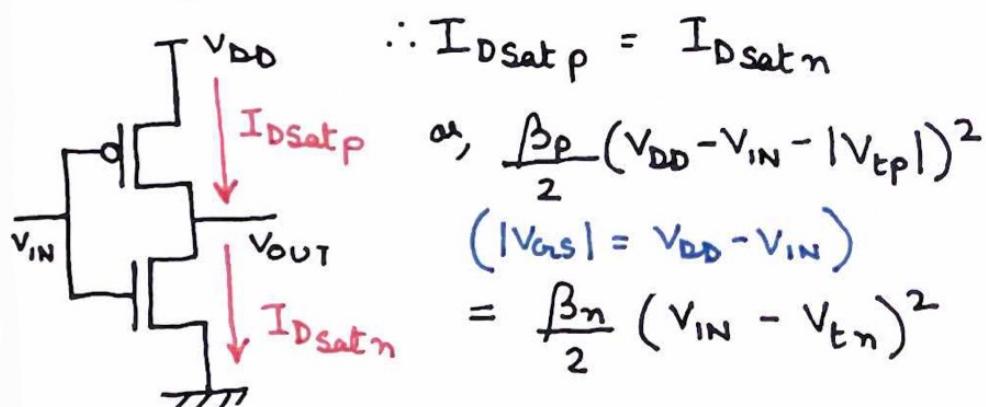
The point V_M is obtained at the intersection of the VTC and the line $V_{OUT} = V_{IN}$ ($y = x$)

Expression for the switching threshold :-



At V_M , in most inverter designs, both the transistors are in saturation (REGION 3). Therefore, $V_{IN} = V_{OUT} = V_M$

Here, the nMOS and the pMOS currents are equal.



At, $V_{IN} = V_{OUT} = V_M$,

$$\frac{\beta_p}{2} (V_{DD} - V_M - |V_{tp}|)^2 = \frac{\beta_n}{2} (V_M - V_{tn})^2$$

(taking square root on both sides, we have)

$$V_{DD} - V_M - |V_{tp}| = \sqrt{\frac{\beta_n}{\beta_p}} (V_M - V_{tn})$$

$$\text{or, } V_M = \frac{V_{DD} - |V_{tp}| + \sqrt{\frac{\beta_n}{\beta_p}} V_{tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

In an ideal inverter, $V_M = \frac{1}{2} V_{DD}$

and the nMOS and pMOS are also symmetric i.e. $|V_{tp}| = V_{tn}$

Now, assuming $V_M = \alpha V_{DD}$ ($\alpha = \frac{1}{2}$ for ideal inverter)

We can write,

$$\alpha V_{DD} = \frac{V_{DD} - |V_{tp}| + \sqrt{\frac{\beta_n}{\beta_p}} V_{tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

$$\text{or, } \alpha V_{DD} + \alpha \sqrt{\frac{\beta_n}{\beta_p}} V_{DD} = V_{DD} - |V_{tp}| + \sqrt{\frac{\beta_n}{\beta_p}} V_{tn}$$

Assuming, $\sqrt{\frac{\beta_n}{\beta_p}} = x$, we have,

$$\alpha V_{DD} + \alpha x V_{DD} = V_{DD} - |V_{tp}| + x V_{tn}$$

$$\alpha x V_{DD} - x V_{tn} = V_{DD} - \alpha V_{DD} - |V_{tp}|$$

$$\text{or, } x (\alpha V_{DD} - V_{tn}) = (1 - \alpha) V_{DD} - |V_{tp}|$$

$$\text{or, } x = \frac{(1 - \alpha) V_{DD} - |V_{tp}|}{\alpha V_{DD} - V_{tn}}$$

$$\text{or, } \sqrt{\frac{\beta_n}{\beta_p}} = \frac{(1 - \alpha) V_{DD} - |V_{tp}|}{\alpha V_{DD} - V_{tn}}$$

For ideal inverters, with symmetric nMOS and pMOS, we can write,

$$|V_{tp}| = V_{tn} = V_t \text{ (say)}$$

$$\sqrt{\frac{\beta_n}{\beta_p}} = \frac{(1-\alpha) V_{DD} - V_T}{\alpha V_{DD} - V_T}$$

Also, $\alpha = 1/2$

$$\therefore \sqrt{\frac{\beta_n}{\beta_p}} = \frac{1/2 V_{DD} - V_T}{1/2 V_{DD} - V_T} \text{ or, } \sqrt{\frac{\beta_n}{\beta_p}} = 1$$

$\alpha, \boxed{\beta_n = \beta_p}$

$$\text{or, } \mu_n C_{oxn} \left(\frac{W_n}{L_n} \right) = \mu_p C_{oxp} \left(\frac{W_p}{L_p} \right)$$

Typically, $C_{oxn} = C_{oxp}$.

$$\text{or, } \mu_n \left(\frac{W_n}{L_n} \right) = \mu_p \left(\frac{W_p}{L_p} \right)$$

$$\text{or, } \frac{\mu_n}{\mu_p} = \frac{(W_p/L_p)}{(W_n/L_n)}$$

If $\mu_n = 2\mu_p$ (since typically e⁻ mobility is 2 to 3 times higher than h⁺ mobility)

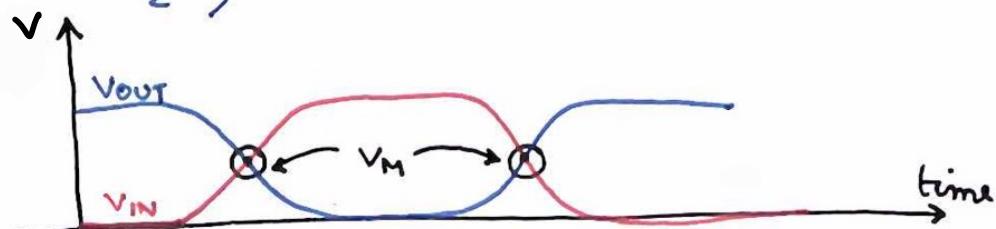
$$\therefore (W_p/L_p) = 2(W_n/L_n)$$

If, $L_p = L_n$ (typically, for modern processes)

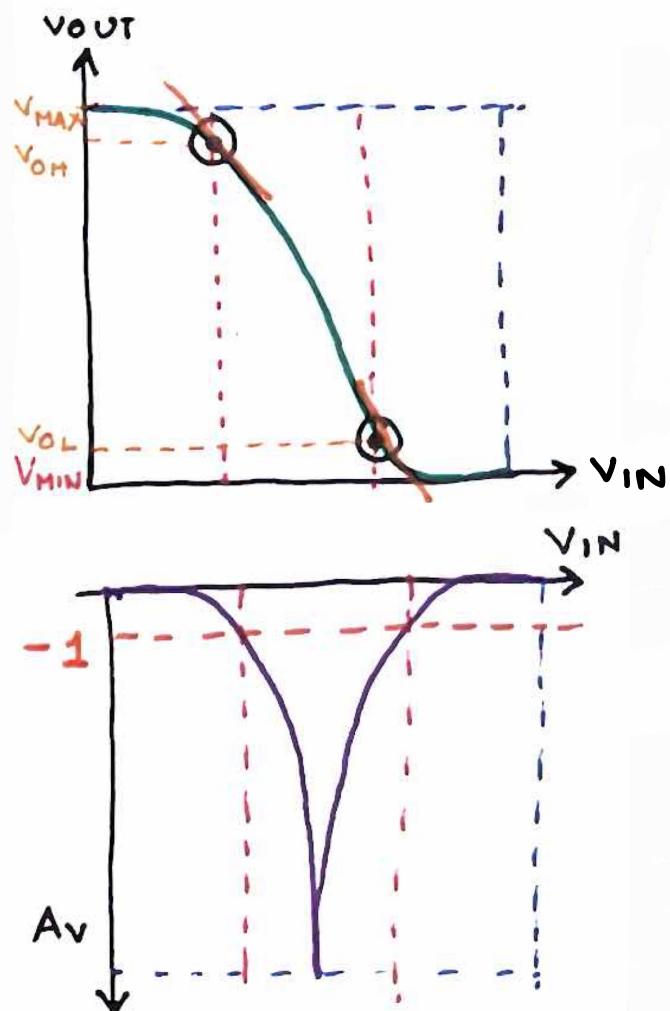
$$\therefore \boxed{\frac{W_p}{W_n} = 2}$$

In general $\frac{W_p}{W_n}$ is $\frac{\mu_n}{\mu_p}$. This is a very important result because it allows circuit designers to design INVERTERS with symmetric switching characteristics (i.e.

$$V_M = \frac{V_{DD}}{2}$$



③ INPUT LEVELS, OUTPUT LEVELS and NOISE MARGIN



et well designed inverter provides well defined logical outputs (0 and V_{DD}) even in the presence of noise.

The valid logic levels are :-

① LOGIC '0' $\rightarrow V_{MIN}$ (minimum output voltage) This is very close to '0' (not exactly 0 due to leakage current)

$V_{OL} \rightarrow$ output low. This is defined as the smallest output voltage where $A_v = -1$

$$\text{or, } \frac{dV_{OUT}}{dV_{IN}} = -1 \text{ or, } \tan\theta = -1 \text{ or } \theta = 135^\circ$$

$$(\pi/2 \leq \theta \leq \pi)$$

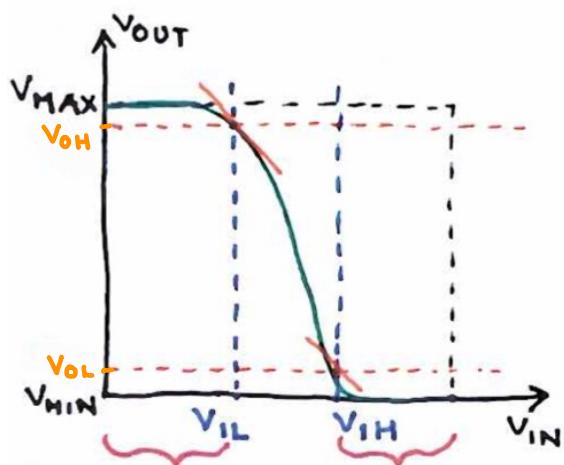
② LOGIC '1' $\rightarrow V_{MAX}$ (maximum output voltage)

When $V_{IN} = 0$. This is very close to V_{DD} (not exactly V_{DD} due to leakage current)

$V_{OH} \rightarrow$ output high. This is defined as the largest output voltage where

$$A_v = -1 \text{ or } \frac{dV_{OUT}}{dV_{IN}} = -1 \text{ or } \tan\theta = -1$$

$$\text{or } \theta = 135^\circ$$



Range of input values that produce output level of 1

Range of input values that produce output level of 0

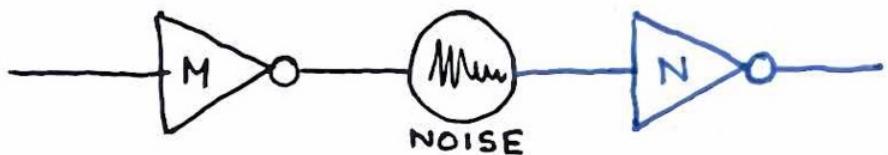
Two more voltage points are important in characterizing an INVERTER.

These are V_{IL} and V_{IH}

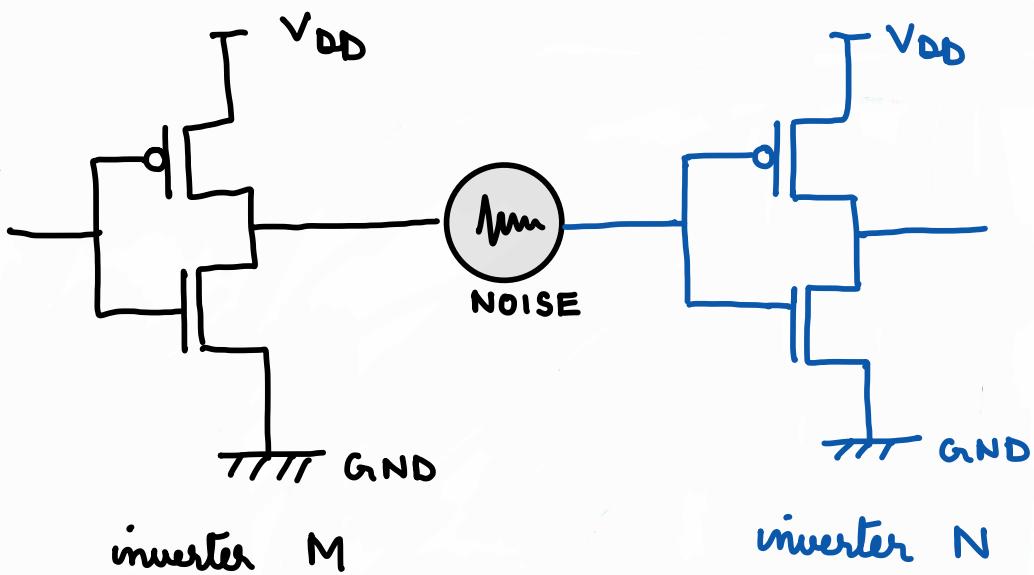
③ $V_{IL} \rightarrow$ input low. It is defined as the smallest input voltage where the slope is -1 (i.e. $A_v = -1$)

④ $V_{IH} \rightarrow$ input high. It is defined as the highest input voltage where the slope is -1 (i.e. $A_v = -1$)
(see figure for V_{IL} and V_{IH})

V_{OL} , V_{OH} , V_{IL} and V_{IH} are important parameters in defining the NOISE IMMUNITY of an INVERTER.



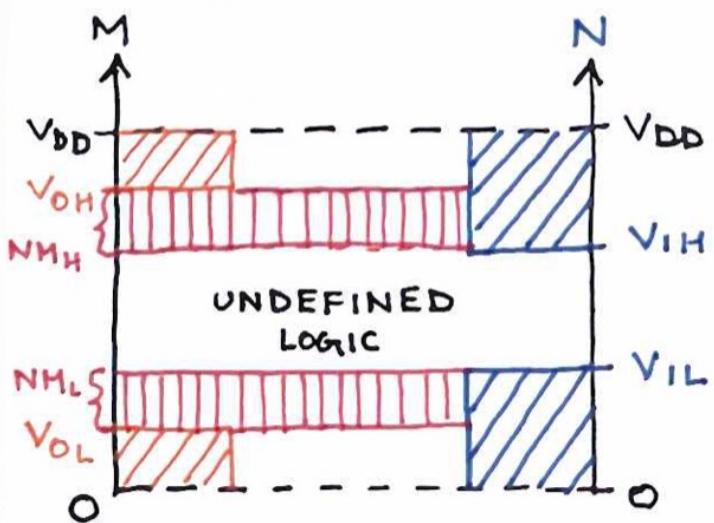
Consider an inverter M , driving another inverter N . Ideally, inverter N should return WELL-DEFINED LOGIC OUTPUTS, 0 and V_{DD} . However, in the real world there can be considerable NOISE (from voltage spikes, coupling, crosstalk etc.)



A well-designed INVERTER, should be able to tolerate this noise and provide, well defined logic outputs, even in the presence of noise. This is qualitatively called the **NOISE IMMUNITY** of the INVERTER and quantified by its' NOISE MARGINS.

⑤ NOISE MARGIN →

Let us look at the diagram below which shows us the voltage levels at the output of the first inverter M and the input of the second inverter N (see figure above)



In this diagram we can see :-

- ① The output inverter M, produces a voltage between V_{OH} and V_{DD} for LOGIC LEVEL '1'.
- ② The input inverter N, on the other hand recognizes any voltage between V_{IH} and V_{DD} as input LOGIC LEVEL '1'.

This shows that if a noise of maximum magnitude $V_{OH} - V_{IH}$ is injected at the output of M, then the inverter N will still be able to resolve the input level as 1 and produce the correct output.

This is called NOISE MARGIN HIGH

$$\text{or } NM_H ; NM_H = V_{OH} - V_{IH}$$

We can also see from the diagram,

③ The output inverter M, produces a voltage between 0 and V_{OL} for LOGIC LEVEL '0'

④ The input inverter N, on the other hand, recognizes any voltage between 0 and V_{IL} as input LOGIC LEVEL '0'

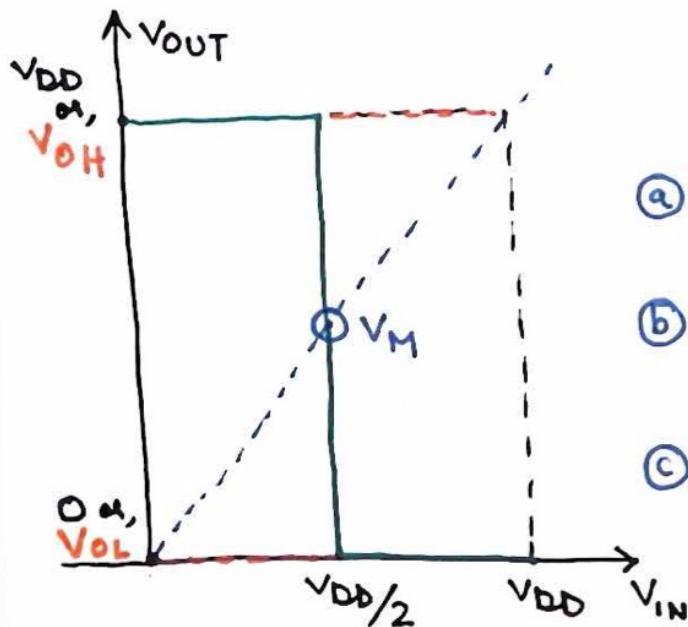
This shows that, if a noise of maximum magnitude $V_{IL} - V_{OL}$ is injected at the output of M, then the inverter N, will still be able to resolve the input level as '0' and produce the correct output.

This is called the NOISE MARGIN LOW or, NML

$$\therefore NML = V_{IL} - V_{OL}$$

The region between V_{IL} and V_{IH} is the region of UNDEFINED LOGIC. And if the output at N, produces a value that falls in this region, then it may produce a LOGIC ERROR.

Now let us look at the VTC of an IDEAL INVERTER.



For,

$$\textcircled{a} \quad V_M < \frac{V_{DD}}{2}; \text{ Slope } (A_v) = 0$$

$$\textcircled{b} \quad V_M = \frac{V_{DD}}{2}; \text{ Slope } (A_v) = -\infty$$

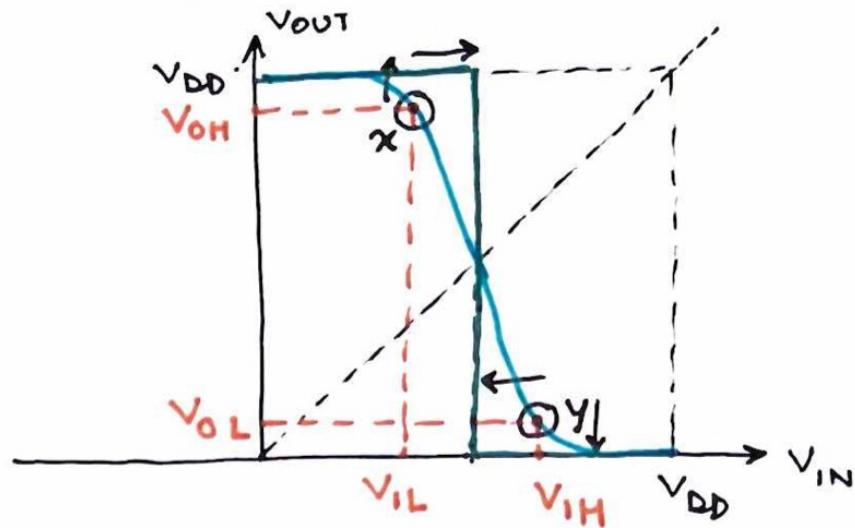
$$\textcircled{c} \quad V_M > \frac{V_{DD}}{2}; \text{ Slope } (A_v) = 0$$

For an IDEAL INVERTER, the switching threshold V_M is at $V_{DD}/2$. (TRIP POINT)

We can see from the VTC, that, here :-

- ① $V_{MAX} = V_{DD}$ and $V_{MIN} = 0$
- ② Also, V_{OH} which is the largest output voltage where the slope is -1 is V_{DD} or V_{MAX} .
- ③ Also, V_{OL} which is the smallest output voltage where the slope is -1 is 0 or V_{MIN} .

If we compare this VTC to that of a well-designed inverter, we have :-

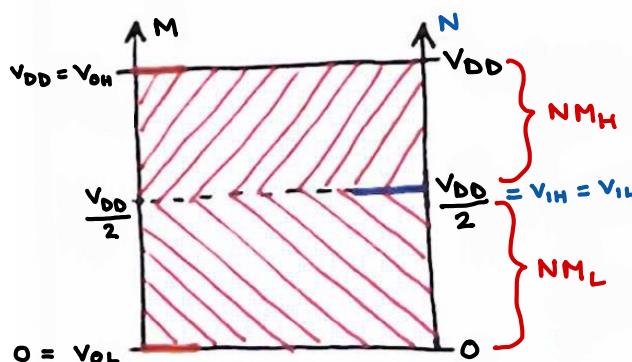


From the diagram above, we can see that as we go from the VTC of a well-designed inverter to the VTC of an IDEAL inverter, the point 'x' (V_{IL}, V_{OH}) moves right and up to coincide with $(\frac{V_{DD}}{2}, V_{DD})$ and the point 'y' (V_{IH}, V_{OL}) moves left and down to coincide with $(\frac{V_{DD}}{2}, 0)$

④ $V_{IH} = V_{IL}$ in this case and

$$V_{IH} = V_{IL} = \frac{V_{DD}}{2}$$

⑤ Let us see what the NOISE MARGINS will be in this case.



$$NM_H = V_{OH} - V_{IH}$$

$$\text{or, } NM_H = V_{DD} - \frac{V_{DD}}{2}$$

$$\text{or, } NM_H = \frac{V_{DD}}{2}$$

$$NM_L = V_{IL} - V_{OL}$$

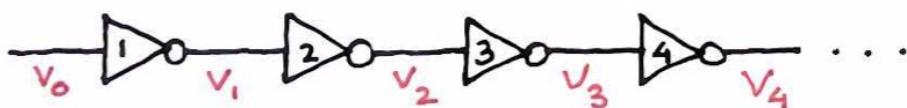
$$\text{or, } NM_L = \frac{V_{DD}}{2} - 0$$

$$\text{or, } NM_L = \frac{V_{DD}}{2}$$

REGENERATIVE PROPERTY OF CMOS INVERTERS

Previously, we have seen that a well-designed inverter of gain $|Av| > 1$ in the transition region provides immunity against noise. Here, we will see, if a chain of inverters (in general, all CMOS gates) can handle a significant amount of noise and regenerate correct logic outputs from noisy inputs.

Let us assume that we have a chain of inverters as shown below :-



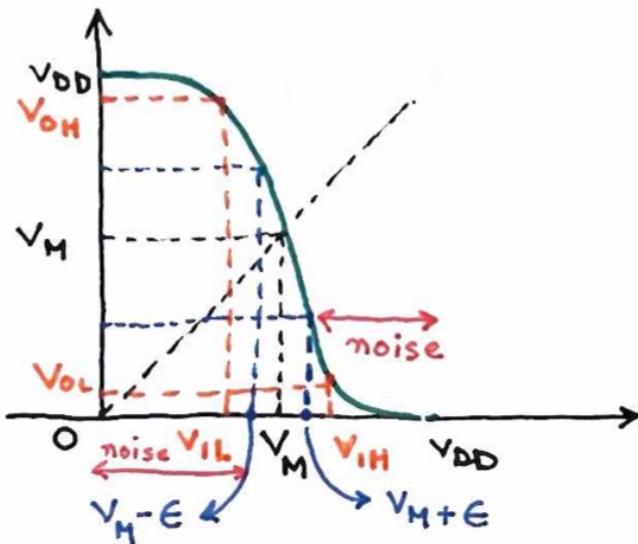
Let the input voltage of inverter 1 be V_0 ,
the output voltage of inverter 1 be V_1 ,
the input voltage of inverter 2 be V_1 ,
the output voltage of inverter 2 be V_2 ,
the input voltage of inverter 3 be V_2 ,
the output voltage of inverter 3 be V_3 ,
the input voltage of inverter 4 be V_3 ,
the output voltage of inverter 4 be V_4 ,
and so on...

We typically know that if
 V_0 is 0,
 V_1 is 1,
 V_2 is 0,
 V_3 is 1
 V_4 is 0 and
so on.

Can this chain of inverters suppress any noise?

Typically V_o will be either 0 or V_{DD}

But in a noisy environment we will assume that V_o is not exactly 0 or V_{DD}



Say,
 V_o in a noisy environment is given by,
$$V_o = V_M - \epsilon$$
 and this

represents $V_o = 0$ and $V_o = V_M + \epsilon$
and this represents $V_o = 1$ (see figure)

We can see that both $V_M - \epsilon$ and $V_M + \epsilon$ lies in the UNDEFINED LOGIC region (V_{IH} to V_{IL})

Our aim here is to be able to move $V_M - \epsilon$ further and further to the left so that the final output lies between V_{OH} and V_{DD} and similarly, move $V_M + \epsilon$ further and further to the right so that the final output lies between 0 and V_{OL} .

ϵ is a very small quantity.

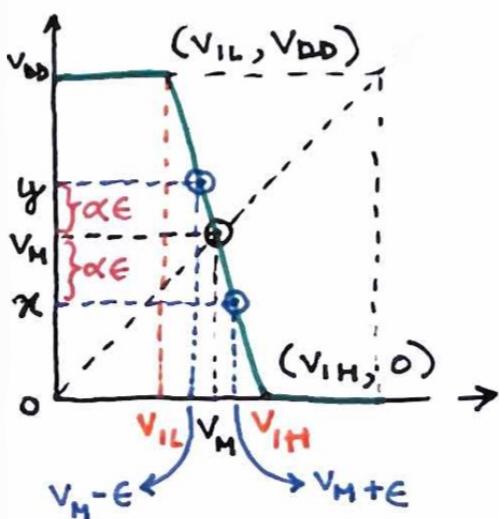
The question we are trying to answer here is since there is a gain in CMOS gates, will the voltages ($V_M + \epsilon$) and ($V_M - \epsilon$) get amplified as the signal propagates through the inverter chain?

Let us consider the following VTC for an inverter. Here our approximation is that :-

$$① V_{OH} = V_{DD} \quad \text{and} \quad ② V_{OL} = 0$$

③ the slope between the points (V_{IL}, V_{DD}) and $(V_{IH}, 0)$ is $-\alpha$ (alpha) i.e this slope is constant.

In reality every point on the curve between these points has a different slope. We are trying to simplify our problem by assuming this curve to be piece-wise linear.

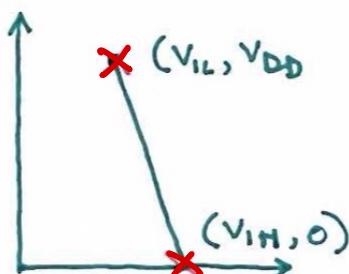


In this VTC plot,

$$\begin{aligned} V_{OUT} &= V_{DD} \text{ when, } V_{IN} < V_{IL} \\ &= \frac{V_{IH} - V_{IN}}{V_{IH} - V_{IL}} \cdot V_{DD}, \quad V_{IL} \leq V_{IN} \leq V_{IH} \\ &= 0 \text{ when, } V_{IN} > V_{IH} \end{aligned}$$

How do we get $V_{OUT} = \frac{V_{IH} - V_{IN}}{V_{IH} - V_{IL}} \cdot V_{DD}$ when, $V_{IL} \leq V_{IN} \leq V_{IH}$?

You can find this using the 2 points (V_{IL}, V_{DD}) and $(V_{IH}, 0) \rightarrow$ slope of a line when 2 points on it are given \rightarrow from Analytic Geometry



Find the slope $-\alpha$

$$-\alpha = \frac{y_2 - y_1}{x_2 - x_1}$$

$$\alpha, -\alpha = \frac{0 - V_{DD}}{V_{IH} - V_{IL}} = \frac{-V_{DD}}{V_{IH} - V_{IL}}$$

Now that we know the slope of this line, we can find the equation of the line too.

$$y - y_1 = m(x - x_1)$$

$$\text{or, } V_{\text{OUT}} - V_{\text{DD}} = \frac{-V_{\text{DD}}}{V_{\text{IH}} - V_{\text{IL}}} (V_{\text{IN}} - V_{\text{IL}})$$

$$\text{or, } V_{\text{OUT}} = V_{\text{DD}} \left[\frac{\frac{V_{\text{IL}} - V_{\text{IN}} + V_{\text{IH}} - V_{\text{IL}}}{V_{\text{IH}} - V_{\text{IL}}}}{1} \right]$$

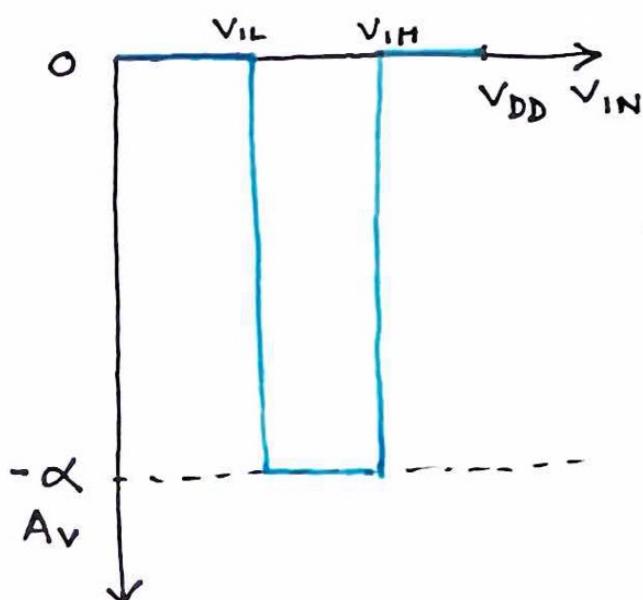
$$\text{or, } V_{\text{OUT}} = \left[\frac{V_{\text{IH}} - V_{\text{IN}}}{V_{\text{IH}} - V_{\text{IL}}} \right] \cdot V_{\text{DD}}$$

which is what we have written before.

Now, we can write the gain in this case as :-

$$\text{GAIN : } \frac{dV_{\text{OUT}}}{dV_{\text{IN}}} = \begin{cases} 0 & \text{when } V_{\text{IN}} < V_{\text{IL}} \\ \frac{-V_{\text{DD}}}{V_{\text{IH}} - V_{\text{IL}}} = -\alpha & \text{when } V_{\text{IL}} \leq V_{\text{IN}} < V_{\text{IH}} \\ 0 & \text{when } V_{\text{IN}} > V_{\text{IH}} \end{cases}$$

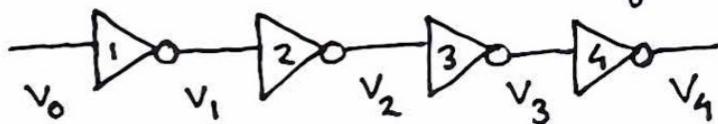
We can draw this as below :-



Let the output of the noisy input $V_M + \epsilon$ be x and the output of the noisy input $V_M - \epsilon$ be y (see figure)

x should ideally be equal to 0 and y should ideally be equal to V_{DD} .

\therefore If we have a chain of inverters



then, if $V_0 = V_M + \epsilon$ (noisy input)

$$\text{then, } V_1 = \left[\frac{V_{IH} - V_{IN}}{V_{IH} - V_{IL}} \right] \cdot V_{DD} \dots (i)$$

since, $V_0 = V_{IN}$ lies between $V_{IL} \leq V_{IN} \leq V_{IH}$

Also, we know that,

$$\text{when } V_{IN} = V_M, V_{OUT} = V_M$$

$$\text{and } V_{IL} \leq V_M \leq V_{IH}.$$

\therefore We can write,

$$V_M = \left[\frac{V_{IH} - V_M}{V_{IH} - V_{IL}} \right] \cdot V_{DD} \dots (ii)$$

From (i), we can write,

$$V_1 = \left[\frac{V_{IH} - V_0}{V_{IH} - V_{IL}} \right] \cdot V_{DD}$$

$$\text{or, } V_1 = \left[\frac{V_{IH} - (V_M + \epsilon)}{V_{IH} - V_{IL}} \right] \cdot V_{DD}$$

$$\text{or, } V_1 = \left[\frac{V_{IH} - V_M}{V_{IH} - V_{IL}} - \frac{\epsilon}{V_{IH} - V_{IL}} \right] \cdot V_{DD}$$

$$\text{or, } V_1 = V_M - \epsilon \left[\frac{V_{DD}}{V_{IH} - V_{IL}} \right]$$

or,

$$V_1 = V_M - \alpha E$$

$\therefore x$ is $V_M - \alpha E$ (see figure)

Similarly, we can show that,

$$y = V_M + \alpha E \text{ (see figure)}$$

$$\therefore \text{if } V_0 = V_M + E,$$

$$V_1 = V_M - \alpha E$$

$$V_2 = V_M + \alpha^2 E$$

$$V_3 = V_M - \alpha^3 E$$

$$V_4 = V_M + \alpha^4 E \text{ and so on.}$$

$$\text{And, if } V_0 = V_M - E,$$

$$V_1 = V_M + \alpha E,$$

$$V_2 = V_M - \alpha^2 E$$

$$V_3 = V_M + \alpha^3 E$$

$$V_4 = V_M - \alpha^4 E \text{ and so on.}$$

\therefore The initial input voltage V_0 is amplified more and more and finally will be $V_n = V_M + \alpha^n E$ or $V_M - \alpha^n E$

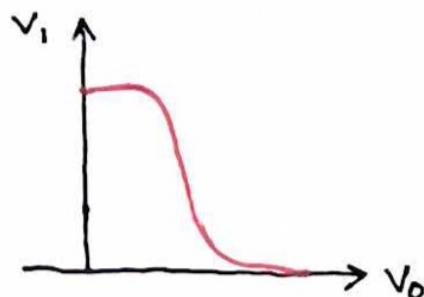
depending on whether n is even or odd and if V_0 is $V_M + E$ (Logic 1) or $V_M - E$ (Logic 0)

\therefore The output voltages eventually will increase and will be very close to V_{DD} or will decrease and be very close to 0.

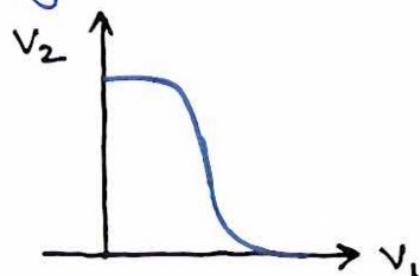
Now let us look at this graphically.
Let us first consider 2 inverters in cascade.



Let us draw the VTC of the 1st inverter.



The VTC of the 2nd inverter will similarly be :-

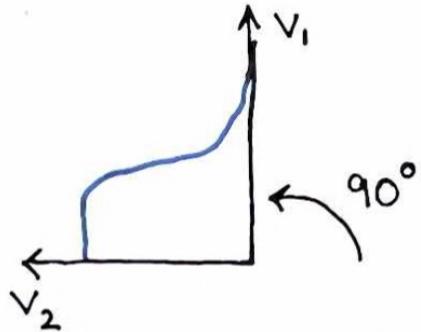


Now, we know that the input of the 2nd inverter, v_1 , is actually the output of the first inverter.

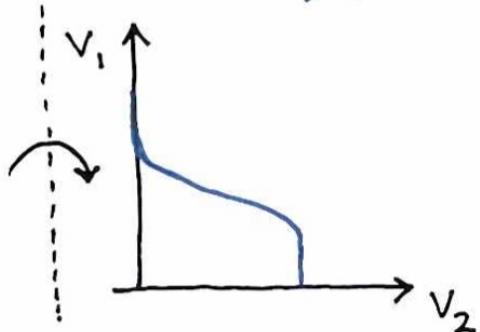
∴ We can map v_1 to the same axis and draw a combined graph.

This is known as the BUTTERFLY CURVE.

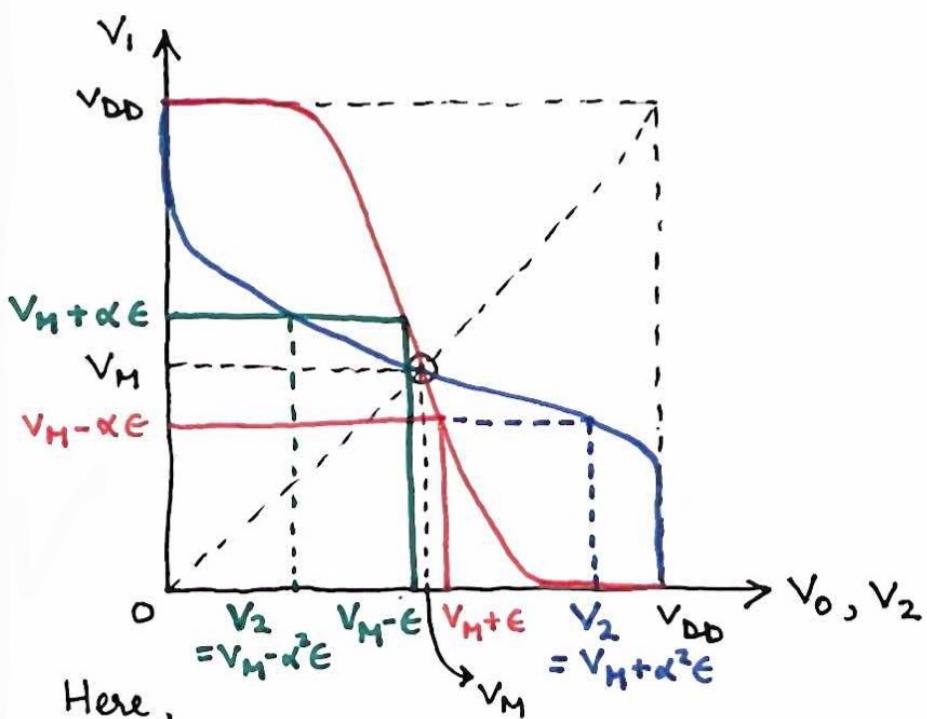
What we are trying to do here is that, we will draw the first VTC as normal and then rotate the 2nd VTC by 90° anti-clockwise



and then flip it along the y-axis.



Now we will overlay this on the 1st VTC to get our final BUTTERFLY CURVE as shown below :-



Here,

- ① V_0 and V_2 are along the x-axis
- ② V_1 is along the y-axis
- ③ If everything is symmetric then the point V_M will be as shown, i.e. at the intersection of the 2 curves.

$$(V_M = \frac{V_{DD}}{2} \text{ and } V_{tn} = |V_{tp}| \text{ etc.})$$

④ Now let us consider $V_0 = V_M + \epsilon$ as the noisy input of the 1st inverter and see what happens if we go through the chain of 2 inverters.

The output V_1 of this $V_0 = V_M + \epsilon$ will be $V_1 = V_M - \alpha \epsilon$ as shown, along the y-axis.

This $V_1 = V_M - \alpha \epsilon$ is now the input of the 2nd inverter. Therefore, we will extend this all the way to the 2nd VTC (blue curve) and now, the corresponding x-axis value will be the output of the 2nd inverter, i.e. $V_2 = V_M + \alpha^2 \epsilon$

We see that V_2 is much closer to V_{DD} , than $V_1 = V_M - \alpha \epsilon$ was to 0.

As we continue this process by including more and more inverters, the output will get closer and closer to V_{DD} or 0, depending on if we have an even number of inverters or odd.

⑤ Similarly, if $V_0 = V_M - \epsilon$ of the 1st inverter, we will see that

$V_2 = V_M - \alpha^2 \epsilon$ will be much closer to 0, than $V_1 = V_M + \alpha \epsilon$ is to V_{DD} .

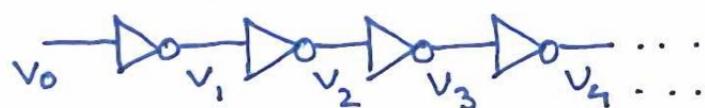
Here, too as we continue this process and add more inverters, the output will get closer and closer to 0 or V_{DD} depending on whether we have an

even number of inverters or odd.

∴ Because of the inherent gain of the inverters, the LOGIC will be corrected after an appropriate number of inverters connected in cascade. Thus, a chain of inverters can handle a significant amount of NOISE and regenerate correct LOGIC outputs from noisy inputs.

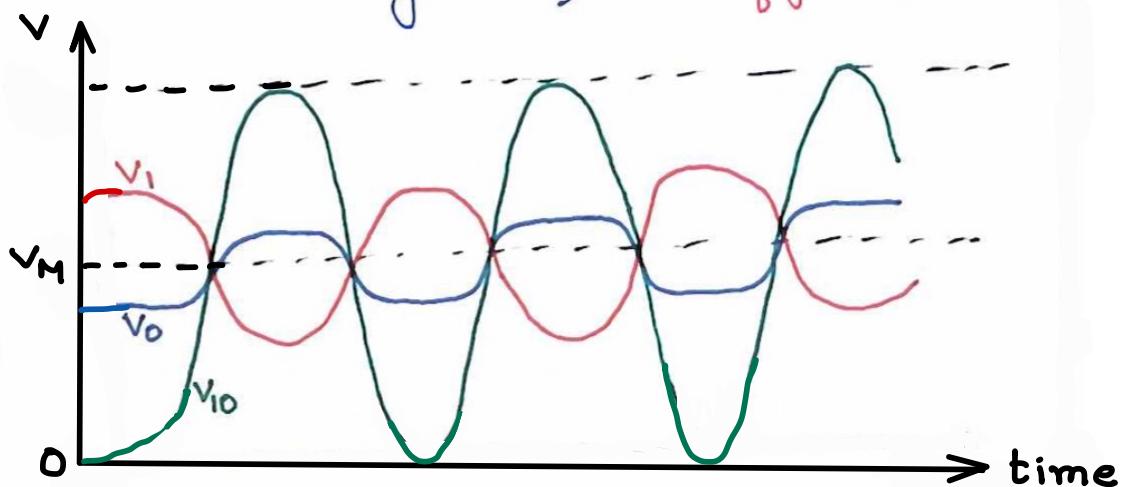
∴ As we go through more and more logic stages, signals get regenerated and the noise is suppressed, because the inverters have a gain $|Av| > 1$.

∴ If we have a chain of inverters as below:-



If we draw the voltage signal v_0 and it has a small swing, then in the 2nd stage when we have v_1 , the swing has already increased a little bit. Then, say after 10 stages when $v_0 + v_{10}$ will have the same polarity, we will see that the

voltage V_{10} has a full swing and goes from V_{DD} to 0. (V_{10} is of course just chosen arbitrarily here) (see figure)



Here we have assumed that :-

- ① All the inverters are symmetric and thus the voltage waveforms swing around V_M .
- ② There is no DELAY between the signals

Finally, we can write down the CHARACTERISTICS of a GOOD INVERTER from the 'DC characteristics' point of view since the DC Characteristics allow us to understand how well the inverter is designed.

- ① $V_M = \frac{V_{DD}}{2}$ (symmetric)
- ② A very high gain (steep VTC)



③ Noise Margin as high as possible

In an IDEAL inverter,

$$NM_{H} = NM_L = \frac{V_{DD}}{2}$$

④ The circuit designer can set

the V_M by controlling the width of the nMOS and the pMOS.

For $V_M = V_{DD}$, $\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}$

and if $\mu_n = 2\mu_p$, then,

$$\frac{W_p}{W_n} = 2$$

In this Module, we have studied the DC characteristics of the inverter.

The same concepts of voltage swing, trip point, noise margin and gain can be extended to other CMOS logic gates after accounting for the multiple inputs of these gates (NAND, NOR, etc.) You will study these in advanced courses.

In Modules 5 & 6, we will next look at the ac characteristics of the inverter with respect to DELAY and POWER.