

1. Draw the stick diagrams for the following Boolean functions and CMOS logic gates by ordering the transistor inputs in the optimal order. You will need to use the concept of Euler paths to reduce the number of breaks in the diffusion. You can assume that both the variables and their inversions are available as inputs.

$$x_{pu} = \{AC + BD\} \cdot (E+F) - P_{news}^D$$

$$b) F = AB + E + CD$$

b) $F = AB + E + CD$

c) The Boolean Function is determined as the output of the following gate

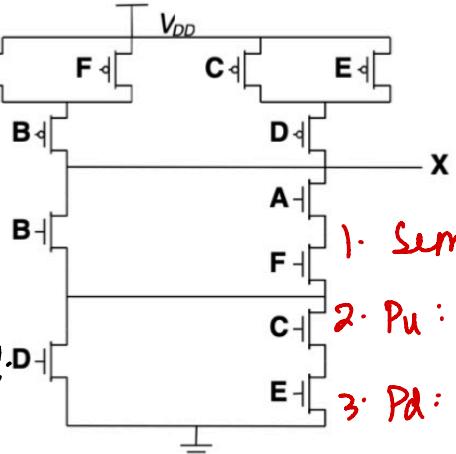
$$X = \overline{(A+C)(B+D)} \cdot \overline{EF}$$

$$= (\overline{A+D} + \overline{B+D}) \cdot (\overline{E+F})^A$$

$$= \{ \bar{A}\bar{C} + \bar{B}\bar{D} \} \cdot (\bar{E} + \bar{F})$$

Py: x w inv unts

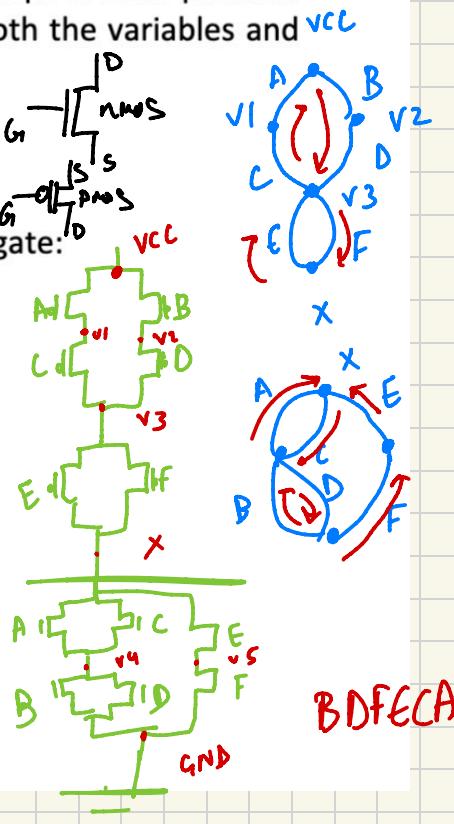
DD = x dual w \sin^w input^{D+}



1. Simplify x

2. Pu : flip inf

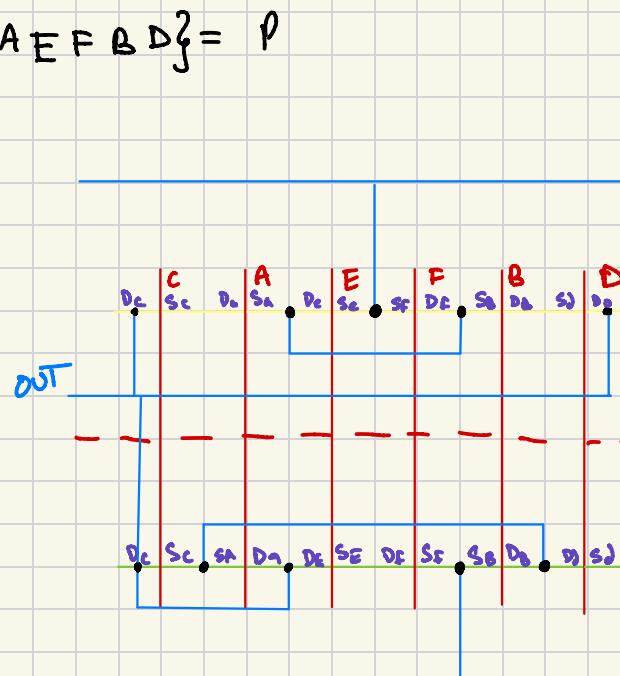
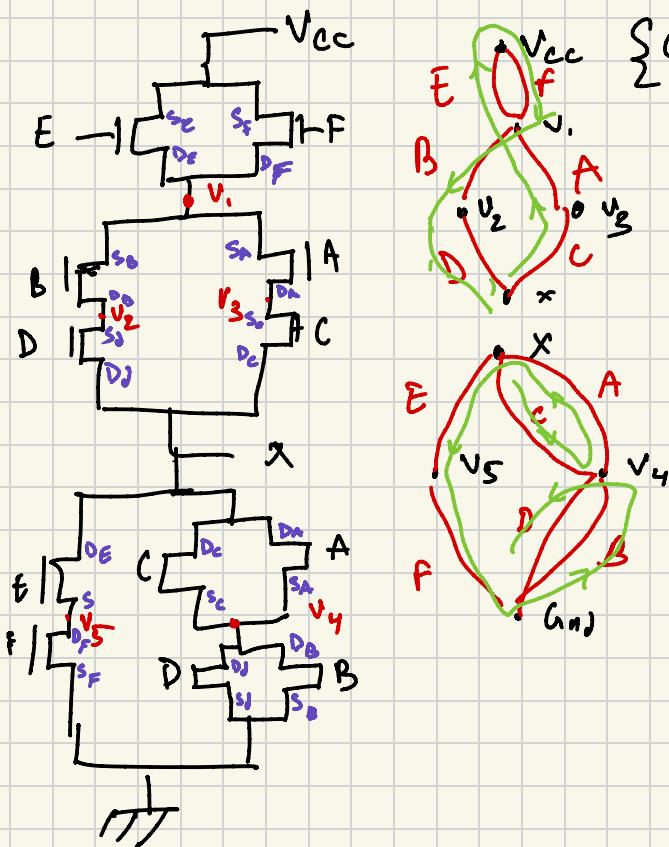
3. Pd: dual Py



a) x for

$$\left[\overline{AC} + \overline{BD} \right] \cdot \left(\overline{E} + \overline{F} \right) \rightarrow \text{pull } \underline{\text{up}} \quad \text{Network}$$

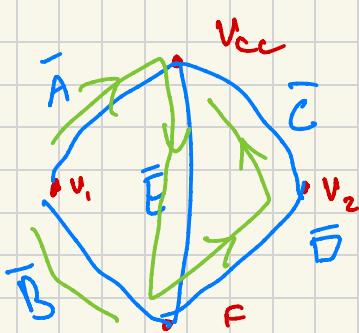
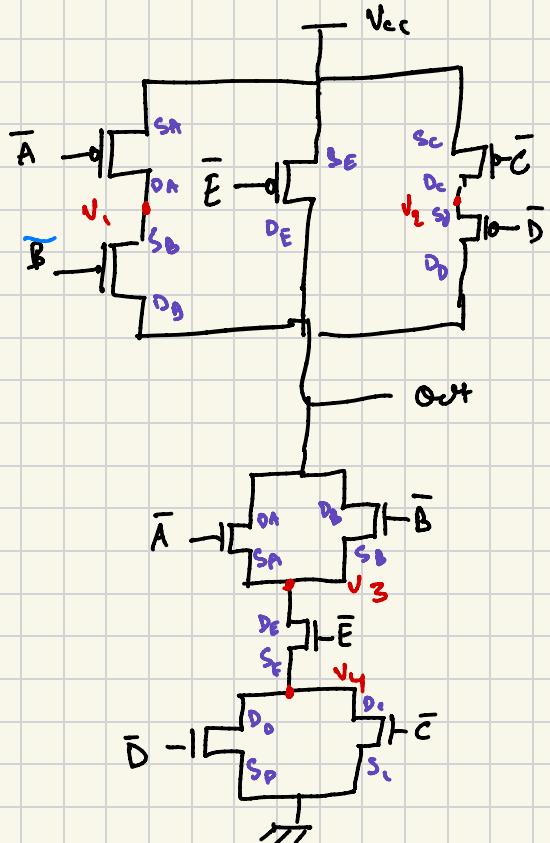
$(A+C)(B+D) + EF \rightarrow$ Pull Down Network



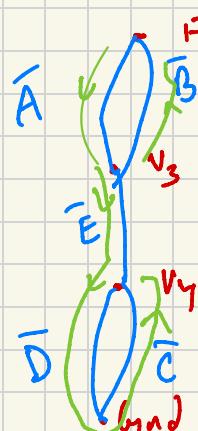
$$b) F = AB + E + CD$$

$$\text{PU: } \bar{A}\bar{B} + \bar{E} + \bar{C}\bar{D}$$

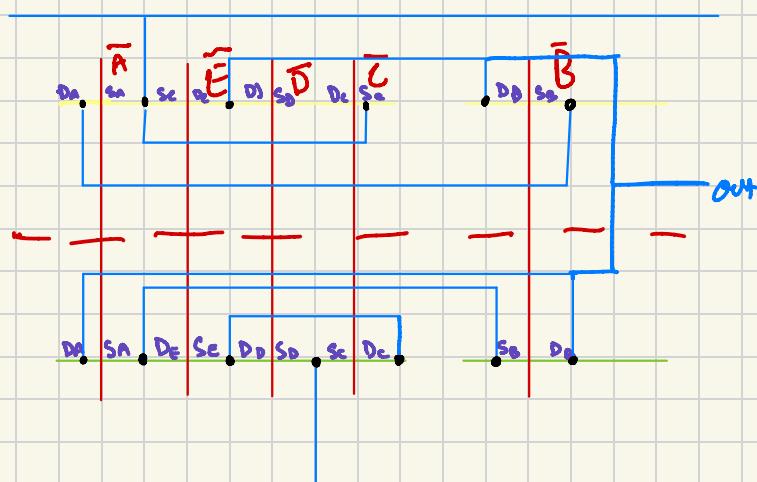
$$\text{PD: } (\bar{A} + \bar{B})(\bar{E})(\bar{C} + \bar{D})$$



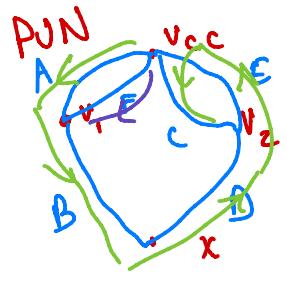
$$P = \{\bar{A}\bar{E}\bar{D}\bar{C}\} \cup \{\bar{B}\bar{D}\}$$



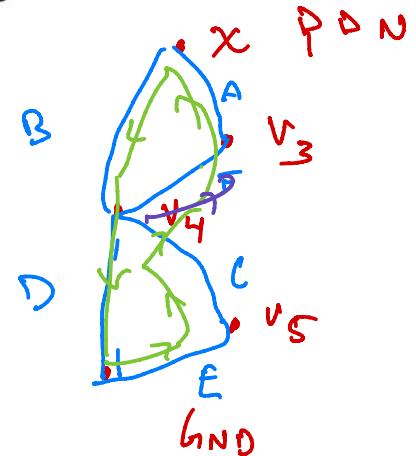
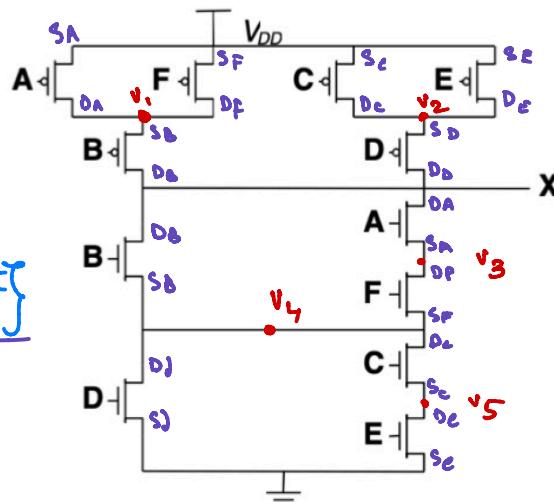
$$P = \{\bar{A}\bar{E}\bar{D}\bar{C}\} \cup \{\bar{B}\bar{D}\}$$



c) The Boolean Function is determined as the output of the following gate:

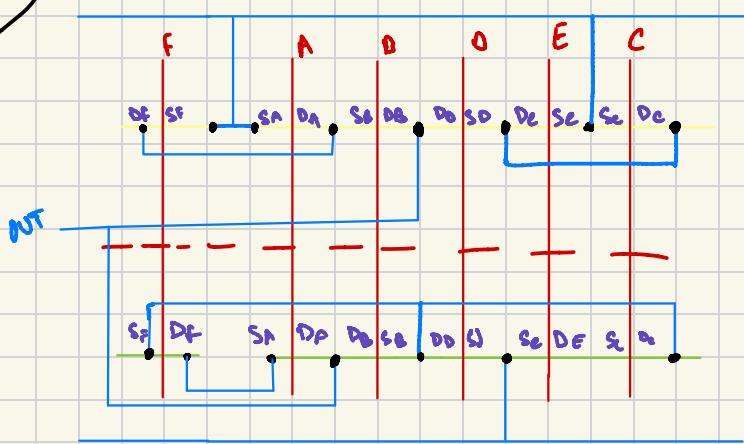


$$P = \sum \{ A B D E C \} \cup \sum \{ F \}$$



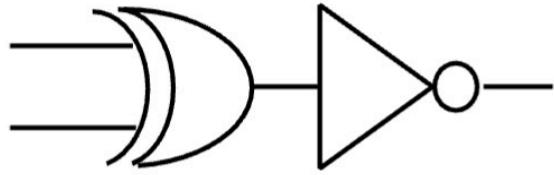
$$P = \sum \{ A B D E C \} \cup \sum \{ F \}$$

C



d) $F = \overline{YZ} + PR(Q + X)$

e) A composition of two logic gates:



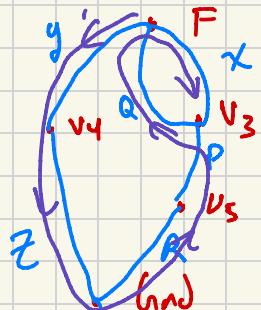
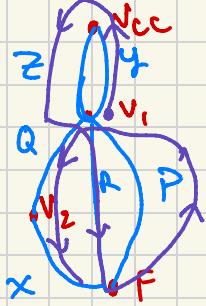
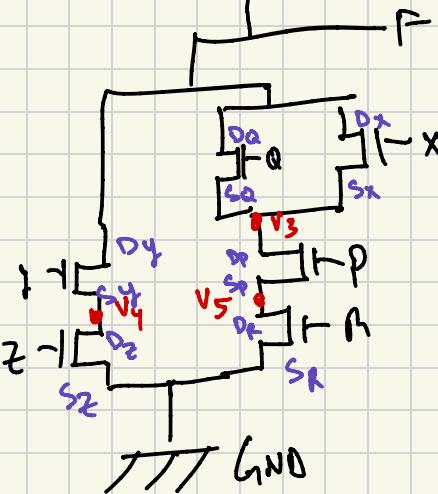
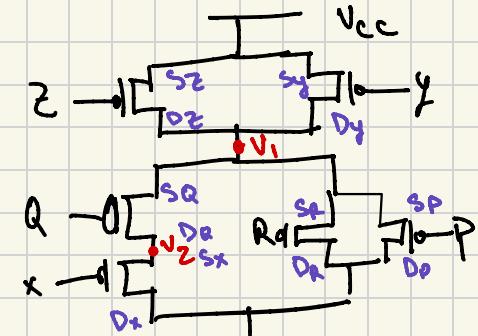
For the two gates cascaded here, there will be a break in the diffusion (diffusion for XOR and diffusion for the inverter). Follow the traditional layout design rules where the two cells can abut. You do not need to insert an substrate tap.

$$D) F = \overline{\{Y+Z\}} \cdot \overline{\{PR\}} \cdot \overline{\{Q+X\}}$$

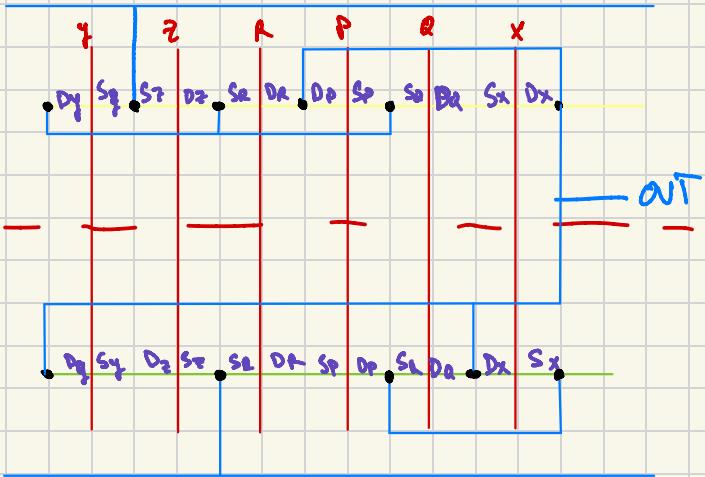
$$\{ \overline{Y} + \overline{Z} \} \cdot \{ (\overline{P} + \overline{R}) + (\overline{Q} \overline{X}) \}$$

$$PUN: (Y+Z)((P+R) + (QX))$$

$$PDN: (Y\bar{Z}) + ((P\bar{R})(Q+\bar{X}))$$

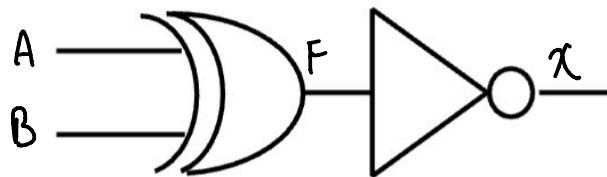


$$P = \{Y\bar{Z}R\bar{P}QX\}$$



d) $F = \overline{YZ} + PR(Q + X)$

e) A composition of two logic gates:



For the two gates cascaded here, there will be a break in the diffusion (diffusion for XOR and diffusion for the inverter). Follow the traditional layout design rules where the two cells can abut. You do not need to insert in substrate tap.

$$F = \overline{A}\overline{B} + A\overline{B}$$

$$\text{PUN: } A\overline{B} + \overline{A}B$$

$$\text{PDN: } (A+B)(\overline{A}+\overline{B})$$

$$X = \overline{F}$$

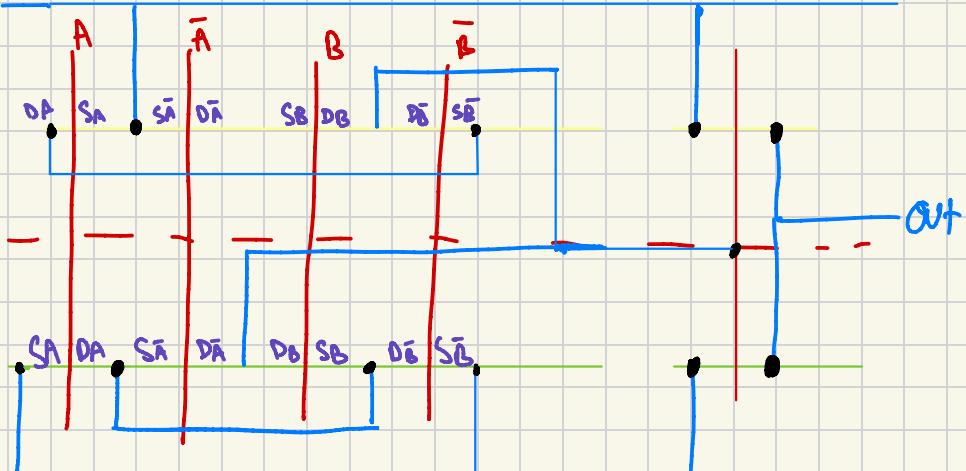
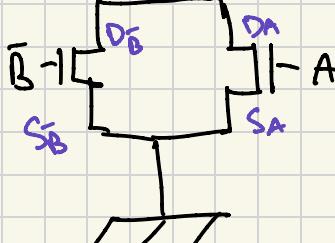
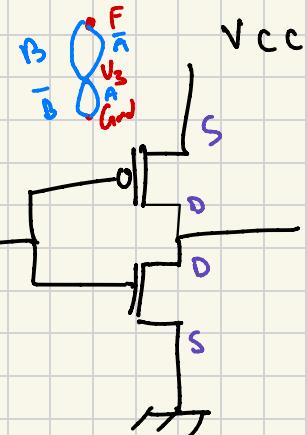
$$\text{PUN: } F$$

$$\text{PDN: } F$$

E)

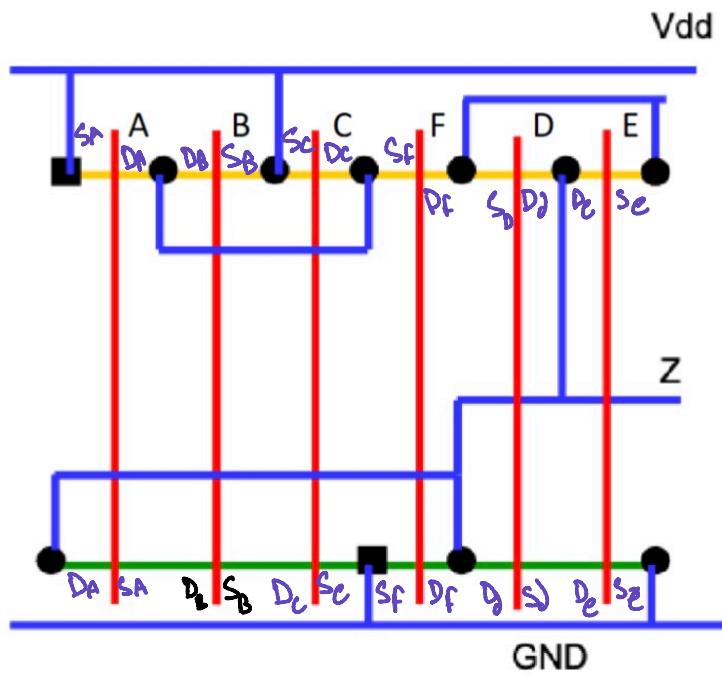


$$P = \{A, \overline{A}, B, \overline{B}\}$$

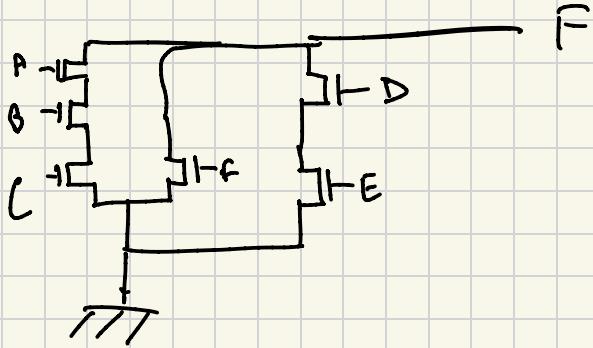


2. Write down the Boolean expression corresponding to the stick diagrams shown below:

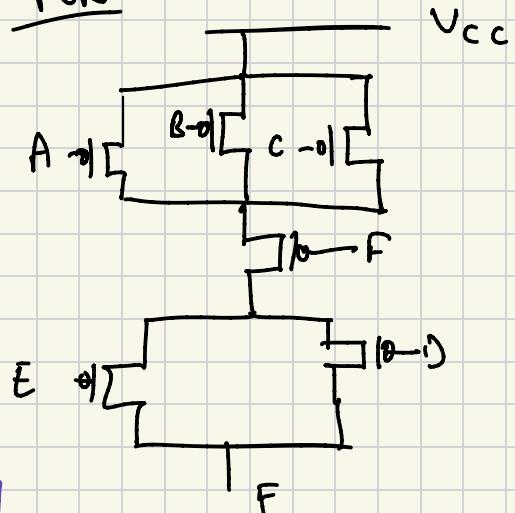
a)



PON

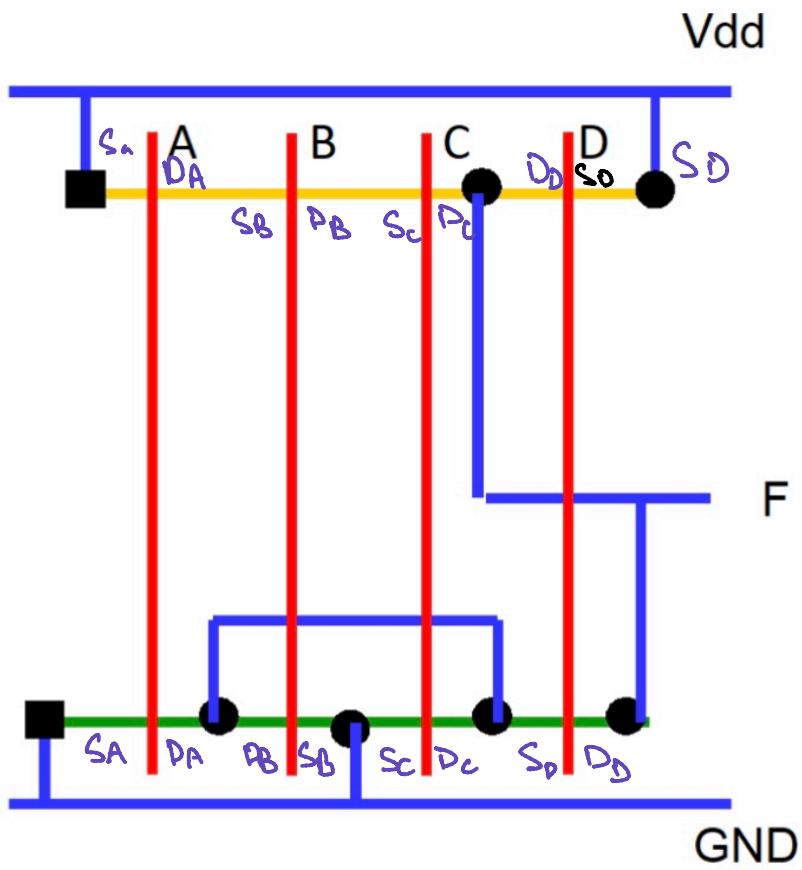


PUN



$$F = (\bar{A} + \bar{B} + \bar{C})(\bar{F})(\bar{E} + \bar{D})$$

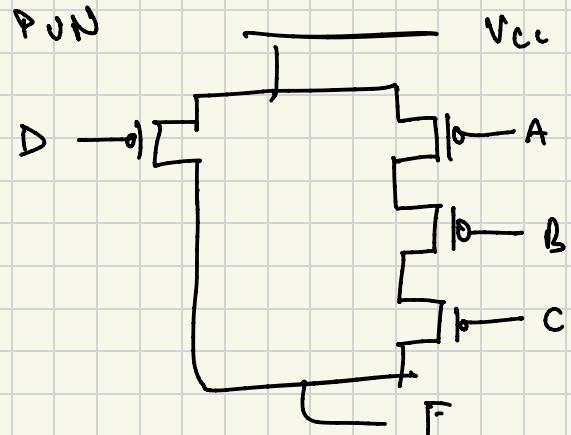
b)



PDN



PUN



$$\overline{F} = (\bar{A}\bar{B}\bar{C}) + (\bar{D})$$