

MODULE 3 - PART B

DC CHARACTERISTICS OF CMOS GATES

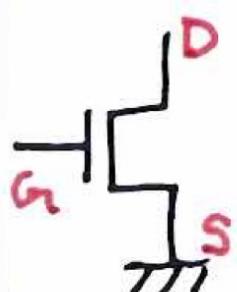
In the first part of M3 we had started looking at the CMOS inverter. We were looking at the DC characteristics of the CMOS inverter and were trying to draw its Voltage Transfer Characteristics (VTC).

To be able to draw the VTC, we had looked at some background information

- ① We have seen how the OUTPUT characteristics and TRANSFER characteristics of the pMOS looks like.

② We have seen that :-

a) For an nMOS in the **ON** state →

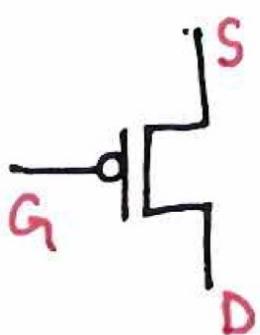


As V_D goes from V_{DD} to 0,

the nMOS goes from the **SATURATION** to **LINEAR** region

b) For a pMOS in the

ON state →

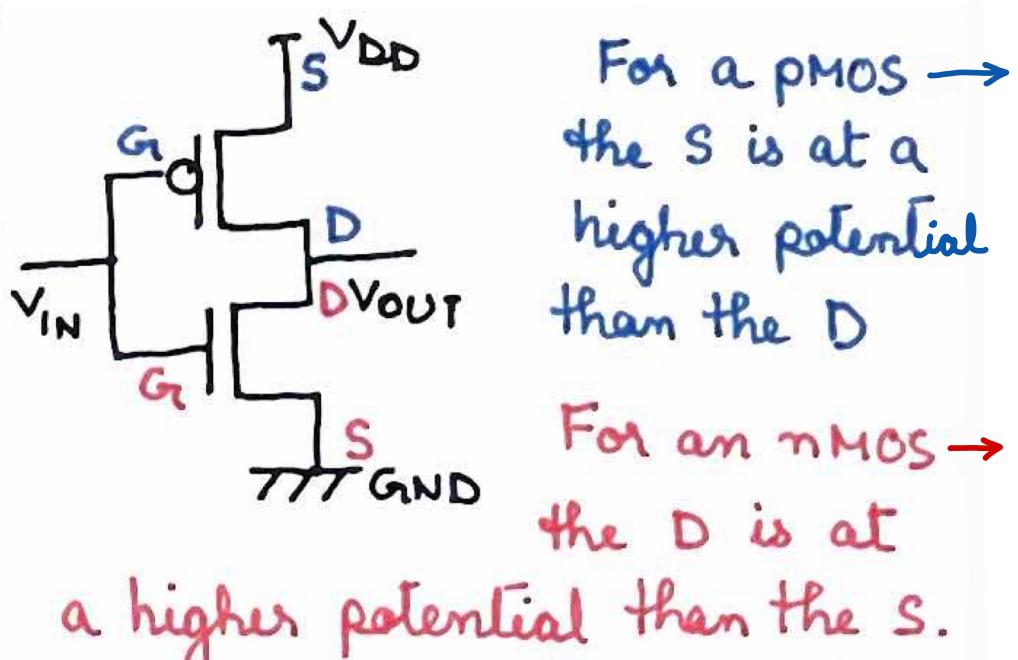


As V_D goes from V_{DD} to 0, the

pMOS goes from

the **LINEAR** to **SATURATION** region.

To proceed further, we will also need the following equations for a CMOS inverter.



nMOS :-

$$\textcircled{a} \quad V_{GS} = V_G - V_S$$

$$\text{or, } V_{GS} = V_{IN} - 0$$

$$\text{or, } V_{GS} = V_{IN}$$

$$\textcircled{b} \quad V_{DS} = V_D - V_S$$

$$\text{or, } V_{DS} = V_{OUT} - 0$$

$$\text{or, } V_{DS} = V_{OUT}$$

pMOS :-

$$\textcircled{a} \quad V_{GS} = V_G - V_S$$

$$\text{or, } V_{GS} = V_{IN} - V_{DD}$$

$$\text{or, } |V_{GS}| = V_{DD} - V_{IN}$$

$$\textcircled{b} \quad V_{DS} = V_D - V_S$$

$$\text{or, } V_{DS} = V_{OUT} - V_{DD}$$

$$\text{or, } |V_{DS}| = V_{DD} - V_{OUT}$$

We have already seen that when $V_{IN} = 0$; $V_{OUT} = V_{DD}$ and when, $V_{IN} = V_{DD}$; $V_{OUT} = 0$.

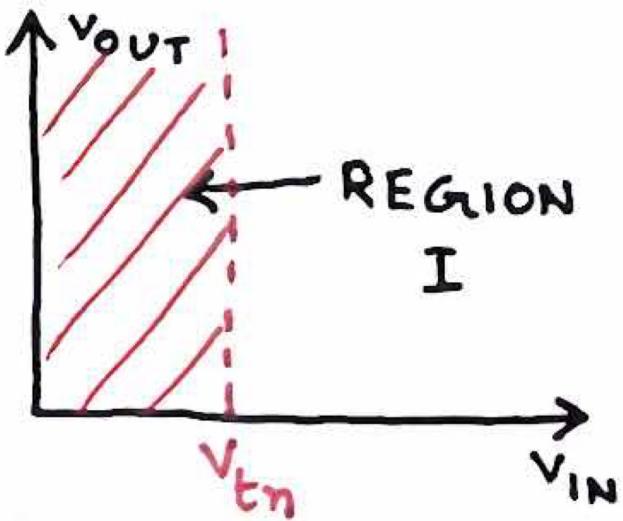
$\therefore (0, V_{DD})$ and $(V_{DD}, 0)$ are points on this plot.

Now, we will look at how to join these 2 points in our plot. For this, we will divide the plot into 5 REGIONS, starting with $V_{IN} = 0$ and we will move along the x-axis.

REGION I :

Here, we have, $V_{IN} < V_{TN}$

We can draw this region as shown below :-



In this region,

① nMOS :-

a) $V_{GS} = V_{IN}$ (we know)

and $V_{IN} < V_{tn}$

$$\therefore V_{GS} < V_{tn}$$

\therefore the nMOS is in the
CUT-OFF REGION.

\therefore nMOS is **OFF**

② pMOS :-

a) $|V_{GS}| = V_{DD} - V_{IN} \dots (i)$

(we know)

and,

$$V_{IN} < V_{tn} \dots (ii)$$

From (i), we can write,

$$|V_{GS}| = V_{DD} - V_{IN}$$

$$\text{or, } V_{IN} = V_{DD} - |V_{GS}|$$

$$\text{or, } V_{DD} - |V_{GS}| < V_{tn}$$

(from (ii))

$$\text{or, } |V_{GS}| > V_{DD} - V_{tn} \dots (\text{iii})$$

For typical CMOS circuits,
we know,

$$V_{DD} > V_{tn} + |V_{tp}|$$

(typically, $3V_{tn} = V_{DD}$)

$$\text{or, } V_{DD} - V_{tn} > |V_{tp}| \dots (\text{iv})$$

From (iii) and (iv), we have,

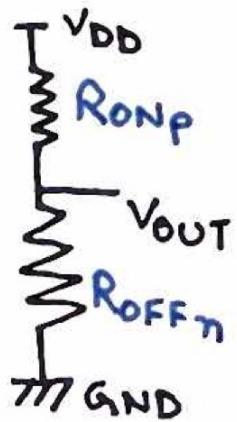
$$|V_{GS}| > V_{DD} - V_{tn} > |V_{tp}|$$

$$\therefore |V_{GS}| > |V_{tp}|$$

\therefore pMOS is **ON**

b) Now that we know
the pMOS is ON, we
have to find which
region it is in.

Let us look at the resistor
divider diagram.



From Voltage Division, we can write,

$$V_{OUT} = \frac{1}{1 + \frac{R_{ONP}}{R_{OFFn}}} \cdot V_{DD}$$

We know, $\frac{R_{ON}}{R_{OFF}} \approx 10^{-3}$ or 10^{-4}

$$\therefore V_{OUT} = V_{DD} - \Delta$$

where Δ is a very small quantity

$$\text{Also, } V_{OUT} = V_{D_{PMOS}}$$

\therefore The Drain of the pMOS is almost equal to V_{DD}
 $(V_{DD} - \Delta)$

The Source of the pMOS is V_{DD} .

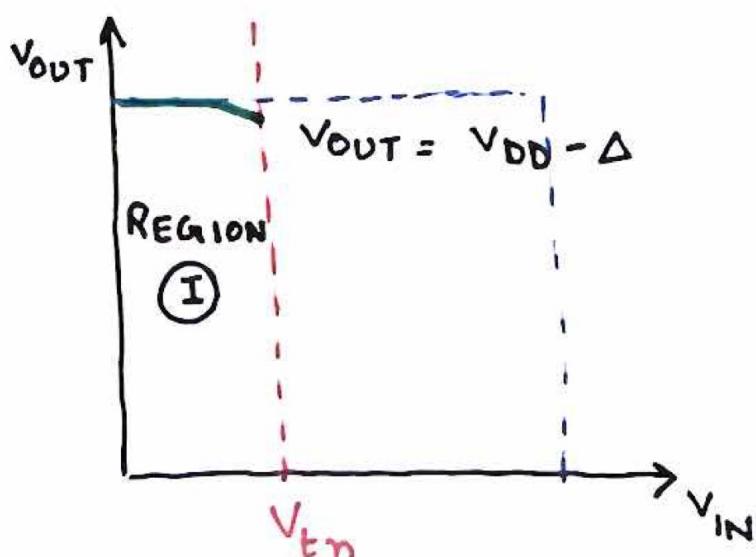
$\therefore |V_{DS}|$ of the pMOS is very small.

\therefore pMOS is in the LINEAR REGION.

\therefore REGION I:

- ① nMOS \rightarrow OFF
- ② pMOS \rightarrow ON
LINEAR

\therefore We can draw the plot in REGION I as below:-



The plot will be mostly flat. There will be a slight dip in the curve as V_{IN} approaches V_{tn} due to increase in the leakage current, but we will not consider this in our course.

REGION II :-

Here, we have,

$$V_{IN} \geq V_{TN} \text{ but,}$$

$$V_{IN} < V_{OUT} - |V_{TP}|$$

$$\text{or, } V_{OUT} > V_{IN} + |V_{TP}|$$

∴ This will be the $y=x$ line, but shifted by $-|V_{TP}|$
where, $V_{OUT} = y$; $V_{IN} = x$

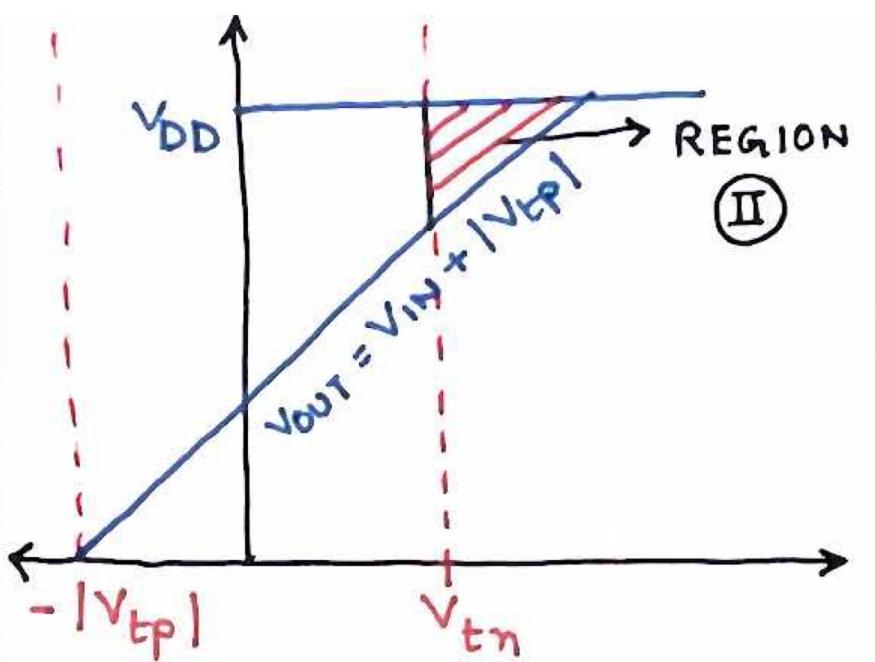
V_{OUT} will be greater than
the region bound by this
line and the x -axis.

Also, note, that,

$$V_{OUT} \leq V_{DD}, \text{ since,}$$

V_{DD} is the supply voltage
and V_{OUT} can never be
greater than the supply.

∴ We can draw this
region as below :-



In this region,

① nMOS :-

ⓐ $V_{GS} = V_{IN}$ (we know)

and we have,

$$V_{IN} > V_{tn}$$

$$\therefore V_{GS} > V_{tn}$$

\therefore nMOS is **ON**

Now, we need to find which region is the nMOS in.

ⓑ $V_{DS} = V_{OUT}$ (we know)

and we have,

$$V_{OUT} > V_{IN} + |V_{tp}|$$

$$\therefore V_{DS} > V_{GS} + |V_{tp}|$$

as,
 $V_{DS} > V_{GS} - V_{tn}$

If $x > p + k$ then,
 $x > p - m$ if k and
 m are positive quantities

$\therefore nMOS$ is in the

SATURATION REGION

② pMOS :-

$$\textcircled{a} \quad |V_{GS}| = V_{DD} - V_{IN}$$

(we know)

and, we have here,

$$V_{IN} \geq V_{TN}$$

$$V_{IN} < V_{OUT} - |V_{TP}|$$

$$\text{or, } -V_{IN} > |V_{TP}| - V_{OUT}$$

$$\text{or, } V_{DD} - V_{IN} > |V_{TP}| - V_{OUT} \\ + V_{DD}$$

(adding V_{DD} to both sides)

$$\text{or, } |V_{GS}| > (V_{DD} - V_{OUT}) + |V_{TP}|$$

Since, V_{OUT} can never be greater than V_{DD} (supply),
 $\therefore (V_{DD} - V_{OUT})$ is always a positive quantity.

\therefore If, $|V_{GDS}| > |V_{TP}| +$
(positive no.)

then,

$$|V_{GDS}| > |V_{TP}|$$

\therefore pMOS is ON

Now we need to find the region of operation of the pMOS.

⑥ $|V_{GDS}| = V_{DD} - V_{OUT}$
(we know)

and, we have here,

$$V_{OUT} > V_{IN} + |V_{TP}|$$

or,
 $-V_{OUT} < -V_{IN} - |V_{TP}|$

$$\text{or, } V_{DD} - V_{OUT} < V_{DD} - V_{IN} - |V_{tp}|$$

(adding V_{DD} to both sides)

or,

$$|V_{DS}| < V_{DD} - V_{IN} - |V_{tp}|$$

(we know, $V_{DD} - V_{IN} = |V_{GS}|$)

or,

$$|V_{DS}| < |V_{GS}| - |V_{tp}|$$

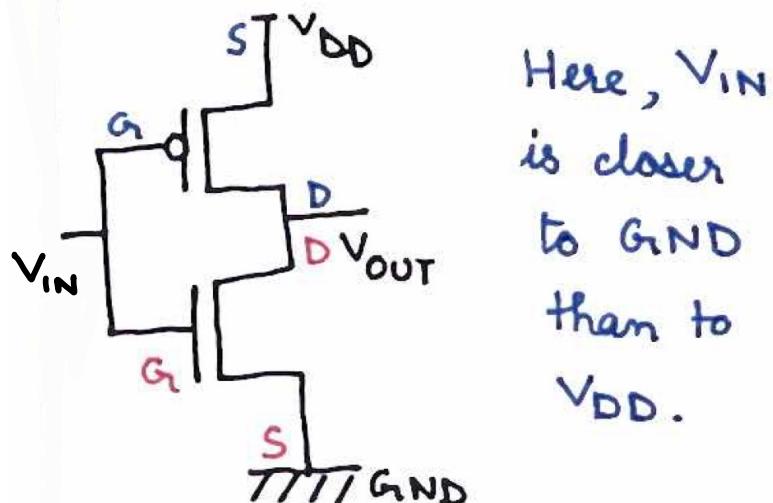
\therefore pMOS is in the
LINEAR REGION.

\therefore REGION II :-

① nMOS \rightarrow ON
SATURATION

② pMOS \rightarrow ON
LINEAR

Let us see what happens
in this region.



For the nMOS,
as V_{IN} increases,
 V_G increases.

$\therefore V_{GS}$ increases
($V_{GS} = V_G - V_S = V_G - 0$)

\therefore the nMOS is getting
stronger and more
conductive and the
 R_{ONn} is decreasing

For the pMOS,
as V_{IN} increases,
 V_G increases

$$\therefore V_{GS} = V_G - V_S = V_G - V_{DD}$$

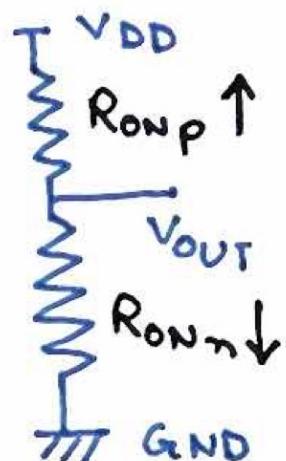
$$\text{or, } |V_{GS}| = V_{DD} - V_G$$

$\therefore |V_{GS}|$ decreases
 \therefore the pMOS is getting
weaker and less
conductive, and R_{ONp}
is increasing.

But still at this point,
 V_{IN} is closer to GND
than to V_{DD} .

$\therefore R_{ONP}$ is lesser
than R_{ONn} .

\therefore We can draw the
resistance diagram as,



Here,

$$V_{OUT} = \frac{1}{1 + \frac{R_{ONP}}{R_{ONn}}} \cdot V_{DD}$$

Now, $\frac{R_{ONP}}{R_{ONn}}$ although still

a small quantity,

(therefore V_{OUT} is closer to V_{DD})

is increasing rapidly due
to the double effect of

$R_{ONP} \uparrow$ and $R_{ONn} \downarrow$

$\therefore V_{OUT}$ will fall rapidly
from V_{DD} .

Also note that in this region, nMOS is in SATURATION.

∴ The current in the nMOS increases quadratically with V_{GS} .

∴ As the resistance is inversely proportional to the current, the resistance DECREASES quadratically.

∴ R_{ONn} decreases as power of 2.

In this region, the pMOS is in the LINEAR region.

∴ The current here is proportional to $|V_{GS}|$ and consequently, the resistance will increase linearly.

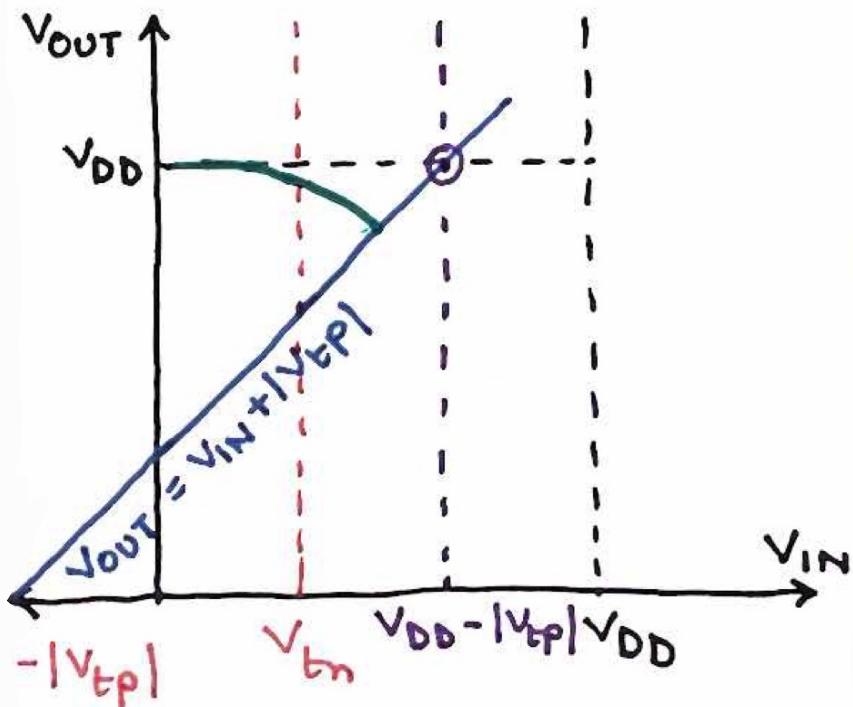
∴ R_{ONp} increases linearly

∴ $R_{ONp} \uparrow$ increases
 $R_{ONn} \downarrow$ RAPIDLY

because of this joint effect of the pMOS and the nMOS

V_{OUT} will fall from V_{DD} rapidly.

\therefore We can draw the plot in REGION II as below:-



Note that this region is also bounded by,

$$V_{OUT} \leq V_{DD}$$

\therefore When $V_{OUT} = V_{DD}$,

$$V_{IN} = V_{DD} - |V_{tp}|$$

(See plot)

Beyond this line, the pMOS will be OFF.

REGION III :-

Here, we have ,

$$V_{IN} \geq V_{OUT} - |V_{tp}|$$

and,

$$V_{IN} \leq V_{OUT} + V_{tn}$$

or $V_{OUT} \geq V_{IN} - V_{tn}$

Therefore, $V_{OUT} = V_{IN} - V_{tn}$

is the $y = x$ line, but
shifted by V_{tn} where,

$$V_{OUT} = y ; V_{IN} = x.$$

$\therefore V_{OUT}$ will be greater
than the region bounded
by this line and the
 x -axis .

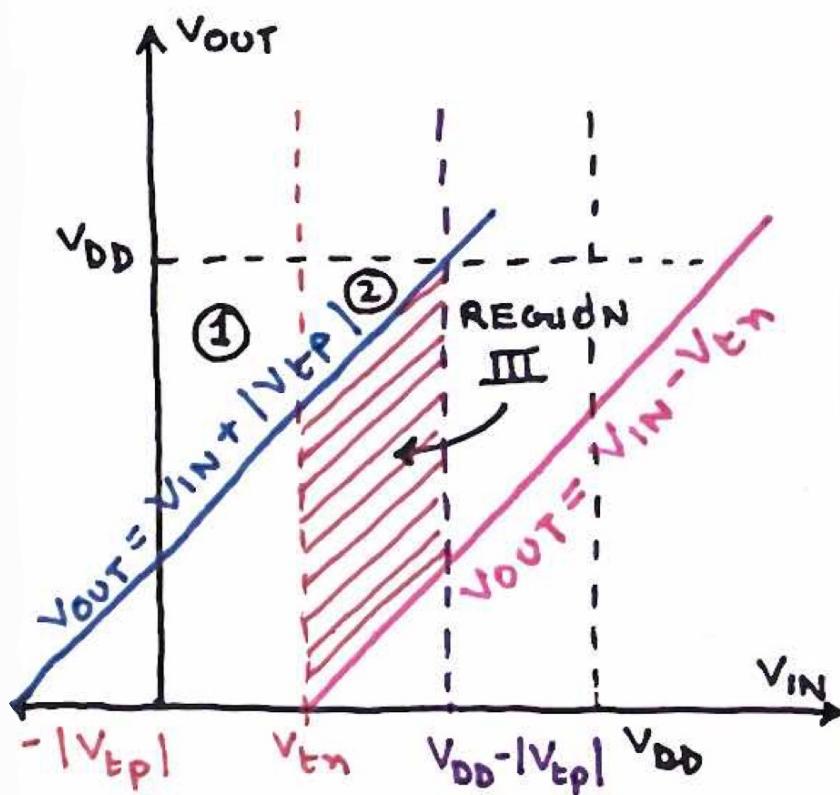
V_{OUT} will also be lesser
than the region bounded
by the line $V_{OUT} = V_{IN} +$
 $|V_{tp}|$.

V_{IN} will be greater than V_{tn} and less than $V_{DD} - |V_{tp}|$ as the pMOS will be OFF beyond this point (hard bound)

$$\therefore V_{IN} \leq V_{DD} - |V_{tp}|$$

$$\text{and } V_{IN} \geq V_{tn}$$

We can draw this region as below :-



In this region,

① nMOS :-

a) $V_{GS} = V_{IN}$ (we know)

We also have,

$$V_{IN} \geq V_{tn}$$

$$\therefore V_{GS} \geq V_{tn}$$

\therefore nMOS is **ON**

Now we have to find the region of operation of the nMOS.

b) $V_{DS} = V_{OUT}$ (we know)

and, here, we have,

$$V_{OUT} \geq V_{IN} - V_{tn}$$

$$\text{or, } V_{DS} \geq V_{GS} - V_{tn}$$

(since, $V_{IN} = V_{GS}$)

\therefore nMOS is in

SATURATION

② pMOS :-

③ $|V_{GS}| = V_{DD} - V_{IN}$
(we know)

and from here we have,

$$V_{IN} \leq V_{DD} - |V_{tp}|$$

from the HARD-BOUND condition. If V_{IN} increases any further, then the PMOS will turn OFF.

This is why we have this hard-bound condition.

$$\therefore V_{IN} \leq V_{DD} - |V_{tp}|$$

$$\text{or, } -V_{IN} \geq |V_{tp}| - V_{DD}$$

$$\text{or, } V_{DD} - V_{IN} \geq |V_{tp}|$$

(adding V_{DD} to both sides)

$$\text{or, } |V_{GS}| \geq |V_{tp}|$$

(since, $|V_{GS}| = V_{DD} - V_{IN}$)

\therefore pMOS is **ON**

Now, we need to find
the region of operation
of the pMOS.

(b) $|V_{DS}| = V_{DD} - V_{OUT}$
(we know)

and we have here,

$$V_{OUT} \leq V_{IN} + |V_{tp}|$$

$$\therefore -V_{OUT} \geq -V_{IN} - |V_{tp}|$$

$$\text{or, } V_{DD} - V_{OUT} \geq V_{DD} - V_{IN} \\ - |V_{tp}|$$

(adding V_{DD} to both sides)

$$\therefore |V_{DS}| \geq |V_{GS}| - |V_{tp}|$$

\therefore pMOS is in
SATURATION.

\therefore REGION III :-

① nMOS \rightarrow ON
SATURATION

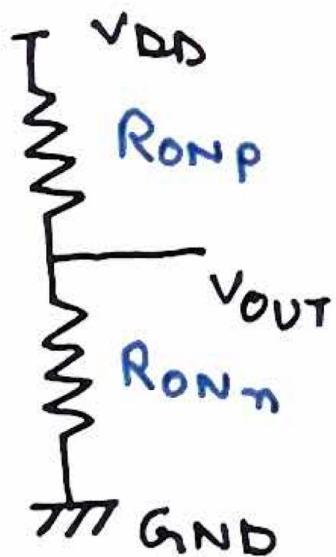
② pMOS \rightarrow ON
SATURATION

Let us see what happens in this region.

Here, too nMOS is getting stronger and the pMOS is getting weaker.

But, here V_{IN} is almost between GND and V_{DD}
 $\therefore R_{ONp}$ and R_{ONn} are almost equal.

\therefore We can draw the resistance diagrams as below:-



$$R_{ONp} \approx R_{ONn}$$

$$V_{OUT} = \frac{1}{1 + \frac{R_{ONp}}{R_{ONn}}} \cdot V_{DD}$$

Here too, R_{ONP} is increasing and R_{ONn} is decreasing, so this double effect will make V_{OUT} fall rapidly.

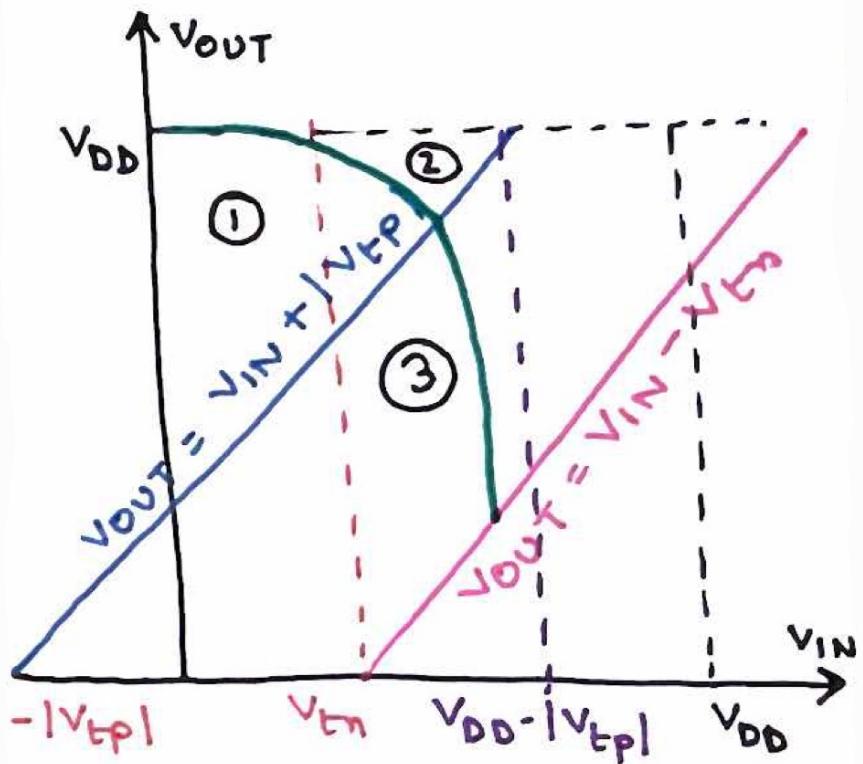
Also here both the nMOS and the pMOS are in SATURATION.

$\therefore R_{ONP}$ will increase quadratically and R_{ONn} will decrease quadratically.

$\therefore \frac{R_{ONP} \uparrow}{R_{ONn} \downarrow}$ will increase more rapidly than in REGION II.

$\therefore V_{OUT}$ will fall faster than in REGION II.

Now, we can draw the plot of REGION III as below :-



REGION IV :

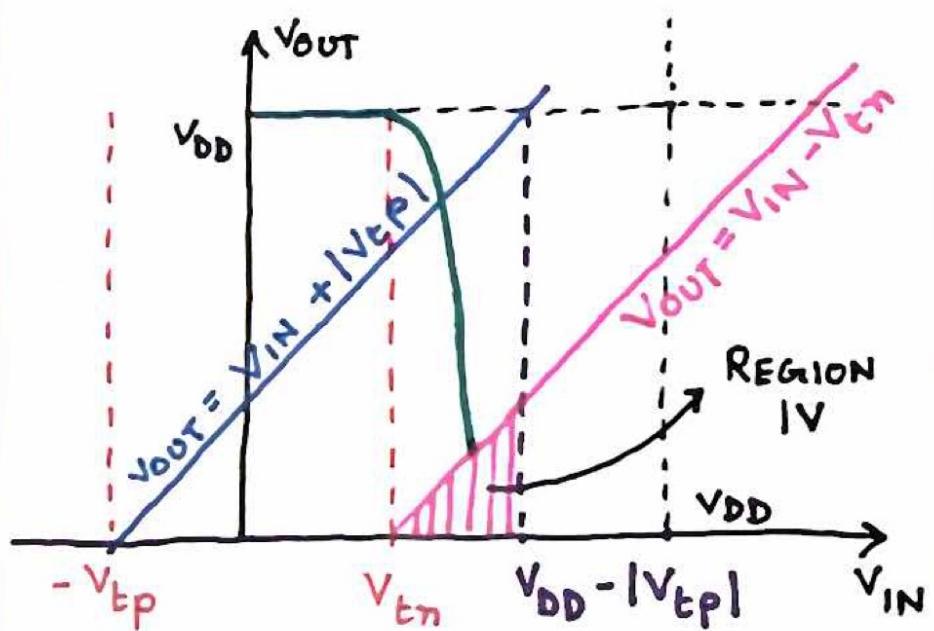
Here, we have,

$$V_{IN} > V_{OUT} + V_{tn}$$

and

$$V_{IN} \leq V_{DD} - |V_{tp}|$$

We can draw this region as :-



For REGION II, which is also a triangle, we had another bound.

$$\text{i.e. } V_{\text{OUT}} \leq V_{\text{DD}}$$

But here, in REGION IV, the triangle is bounded below by the x-axis.

$$\text{i.e. } V_{\text{OUT}} \geq 0$$

In this region,

① nMOS :-

$$V_{GS} = V_{IN} \quad (\text{for the nMOS})$$

and we know,

$$V_{IN} > V_{\text{OUT}} + V_{tn}$$

$$\therefore V_{IN} > V_{tn}$$

\therefore nMOS is **ON**

Also, $V_{DS} = V_{OUT}$ (for the nMOS)

and here,

$$V_{IN} > V_{OUT} + V_{tn}$$

$$\text{or, } V_{OUT} < V_{IN} - V_{tn}$$

(subtracting V_{tn} from both sides)

$$\text{or, } V_{DS} < V_{GS} - V_{tn}$$

(substituting $V_{OUT} = V_{DS}$ and
 $V_{IN} = V_{GS}$ for the nMOS)

which is the condition for
linear operating region of the
nMOS.

\therefore nMOS is in the
LINEAR REGION

② pMOS :-

$$|V_{GS}| = V_{DD} - V_{IN} \quad (\text{for the pMOS})$$

and we know,

$$V_{IN} \leq V_{DD} - |V_{tp}|$$

$$-V_{IN} \geq |V_{tp}| - V_{DD}$$

$$\text{or, } V_{DD} - V_{IN} \geq |V_{tp}|$$

(adding V_{DD} to both sides)

$$\text{or, } |V_{GS}| \geq |V_{tp}|$$

(since, $|V_{GS}| = V_{DD} - V_{IN}$)

that is, V_{GS} is more negative
than V_{tp} .

\therefore pMOS is ON

For the pMOS :-

We know,

$$\text{or, } |V_{DS}| = V_{DD} - V_{OUT} \dots (\text{i})$$

and,

$$\text{or, } |V_{G_S}| = V_{DD} - V_{IN} \dots (\text{ii})$$

We also have here,

$$V_{IN} > V_{OUT} + V_{t_n}$$

From (i), we have,

$$|V_{DS}| = V_{DD} - V_{OUT}$$

$$\text{or, } V_{OUT} = V_{DD} - |V_{DS}| \dots (\text{iii})$$

From (ii), we have,

$$|V_{G_S}| = V_{DD} - V_{IN}$$

$$\text{or, } V_{IN} = V_{DD} - |V_{G_S}| \dots (\text{iv})$$

Substituting the values of

V_{IN} and V_{OUT} from

equations (iii) and (iv) in

the inequality,

$$V_{IN} > V_{OUT} + V_{t_n},$$

we have,

$$V_{DD} - |V_{G_S}| > V_{DD} - |V_{DS}| + V_{t_n}$$

$$\text{or, } -|V_{G_S}| > -|V_{DS}| + V_{t_n}$$

(V_{DD} eliminated from both sides)

$$\text{or, } |V_{GS}| < |V_{DS}| - V_{TN}$$

(changing signs on both sides)

$$\text{or, } |V_{DS}| > |V_{GS}| + V_{TN}$$

(adding V_{TN} to both sides)

$$\therefore |V_{DS}| > |V_{GS}|$$

(since, if $|V_{DS}|$ is greater than $|V_{GS}|$ plus a '+'ve quantity, it will be greater than $|V_{GS}|$)

$$\text{or, } |V_{DS}| > |V_{GS}| - |V_{EP}|$$

($|V_{DS}|$ will also be greater than $|V_{GS}|$ minus a '+'ve quantity)

This is the condition of the saturation region for a pMOS.

\therefore pMOS is in the

SATURATION Region

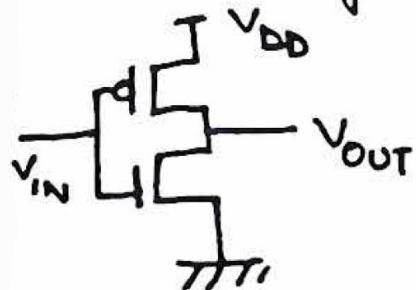
\therefore In REGION IV, we have :

REGION IV :-

① nMOS \rightarrow ON
LINEAR

② pMOS \rightarrow ON
SATURATION

Let us see what happens in this region.

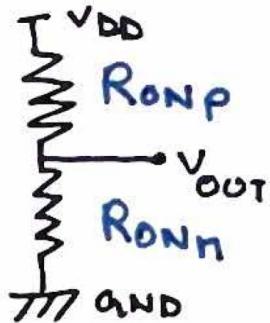


Here, V_{IN} is closer to V_{DD} than to GND.

nMOS is still getting stronger and R_{ONn} is decreasing.

pMOS is still getting weaker and R_{ONp} is increasing

∴ We can draw the resistance diagram as:



But since V_{IN} is closer to V_{DD} than to GND,

$$R_{ONN} < R_{ONP}$$

Here,

$$V_{OUT} = \frac{1}{1 + \frac{R_{ONP}}{R_{ONN}}} \cdot V_{DD}$$

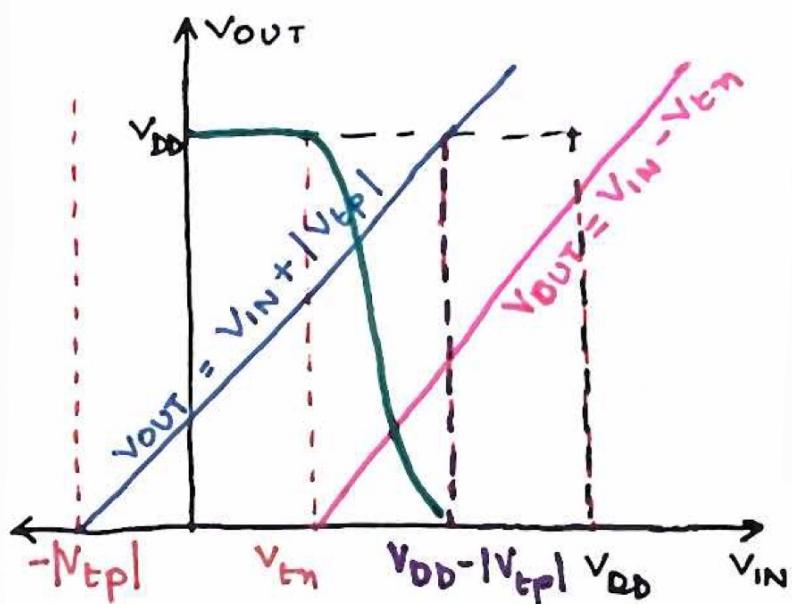
Now, V_{OUT} will fall rapidly due to the double effect of R_{ONP} increasing and R_{ONN} decreasing.

Also, the pMOS is in SATURATION here, so R_{ONP} increases quadratically and the nMOS is in

the LINEAR
region , so R_{ONN}
decreases linearly .

$\therefore \frac{R_{ONP} \uparrow}{R_{ONN} \downarrow}$ will increase
as rapidly as REGION II
but not as much as
REGION III where
both transistors were in
saturation .

\therefore We can draw the VTC
in REGION IV as below :-

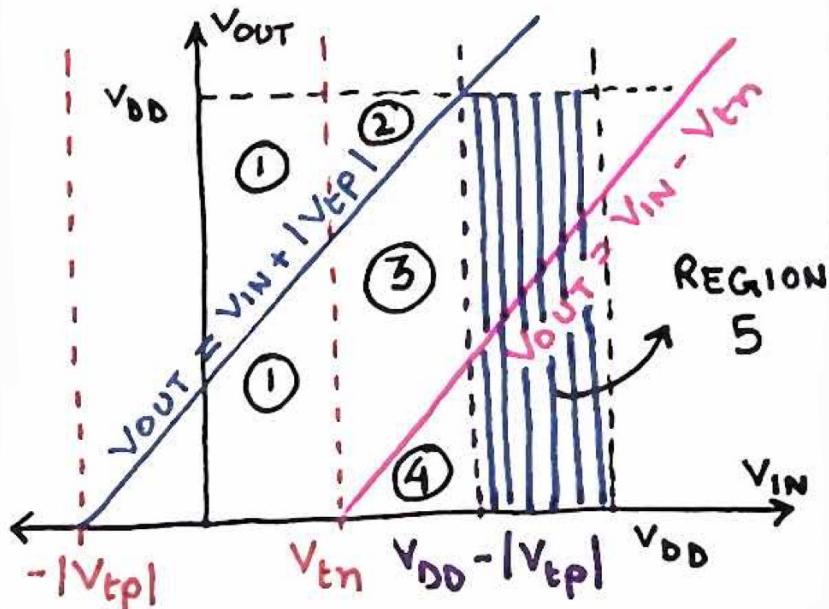


REGION V :-

Here we have ,

$$V_{DD} \geq V_{IN} > V_{DD} - |V_{tP}|$$

We can draw this region as below :-



In this region,

① pMOS :-

We know,

$$|V_{GSS}| = V_{DD} - V_{IN}$$

We also have,

$$V_{IN} > V_{DD} - |V_{tp}|$$

$$\text{or, } V_{IN} + |V_{tp}| > V_{DD}$$

(adding $|V_{tp}|$ to both sides)

$$\text{or, } |V_{tp}| > V_{DD} - V_{IN}$$

(subtracting V_{IN} from both sides)

$$\text{or, } |V_{tp}| > |V_{GSS}|$$

(since, for a pMOS,

$$|V_{GSS}| = V_{DD} - V_{IN}$$

\therefore the pMOS is **OFF**

② nMOS :-

$$V_{GS} = V_{IN} \text{ (we know)}$$

We also have,

$$V_{IN} > V_{DD} - |V_{tp}|$$

$$\text{or, } V_{GS} > V_{DD} - |V_{tp}| \dots (i)$$

$$\text{(since, } V_{GS} = V_{IN})$$

We have also seen that,

$$V_{DD} > V_{tn} + |V_{tp}| \quad (3V_{tn} = V_{DD})$$

$$\text{or, } V_{DD} - |V_{tp}| > V_{tn} \dots (ii)$$

(Subtracting $|V_{tp}|$ from
both sides)

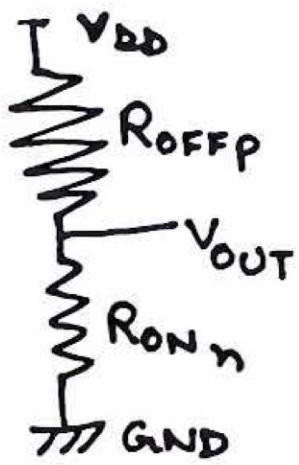
From (i) and (ii),

$$V_{tn} < V_{DD} - |V_{tp}| < V_{GS}$$

$$\text{or, } V_{GS} > V_{tn}$$

\therefore the nMOS is **ON**

Now, let us look at
the resistor divider
diagram :-



Here, V_{OUT} is given by :-

$$\frac{1}{1 + \frac{R_{OFFP}}{R_{ONn}}} \cdot V_{DD}$$

(voltage division)

We know that, $\frac{R_{ON}}{R_{OFF}}$ is

almost equal to 10^{-3} to 10^{-4}

$$\therefore \frac{R_{OFF}}{R_{ON}} \approx 10^3 \text{ to } 10^4$$

$$\therefore V_{OUT} = \frac{1}{\text{large quantity}} \times V_{DD}$$

$$\text{or, } V_{OUT} \approx 0$$

$\therefore V_{DS} = V_{OUT} \approx 0$ of the nMOS.

$$\therefore V_{DS} < V_{GS} - V_{tn} \quad (\text{very small})$$

\therefore nMOS is in the

LINEAR REGION

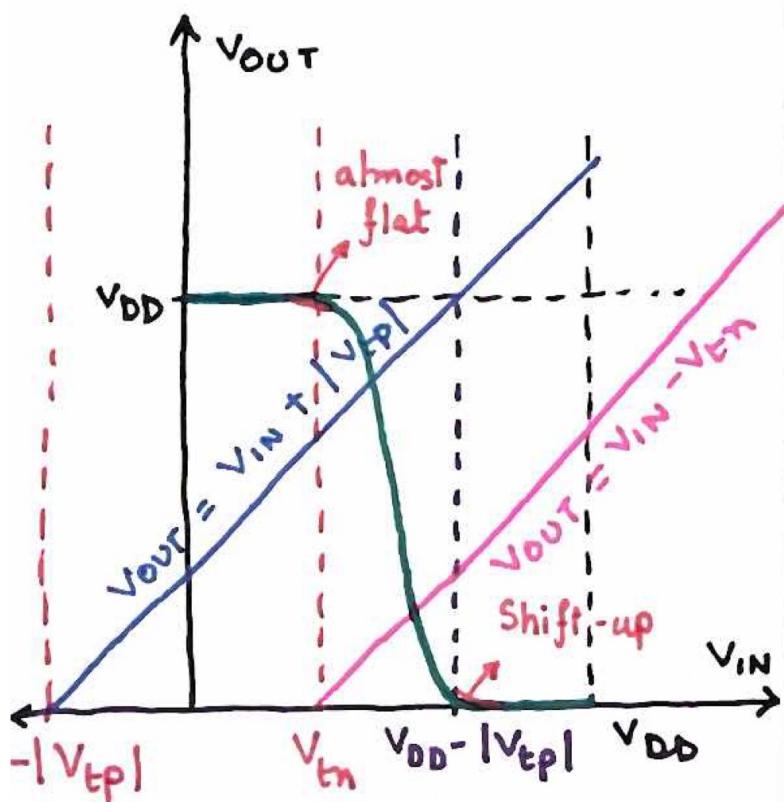
\therefore In REGION IV, we have :-

REGION IV :-

① nMOS \rightarrow ON
LINEAR

② pMOS \rightarrow OFF

Let us now draw the complete Voltage Transfer Characteristics (VTC) of the CMOS INVERTER :



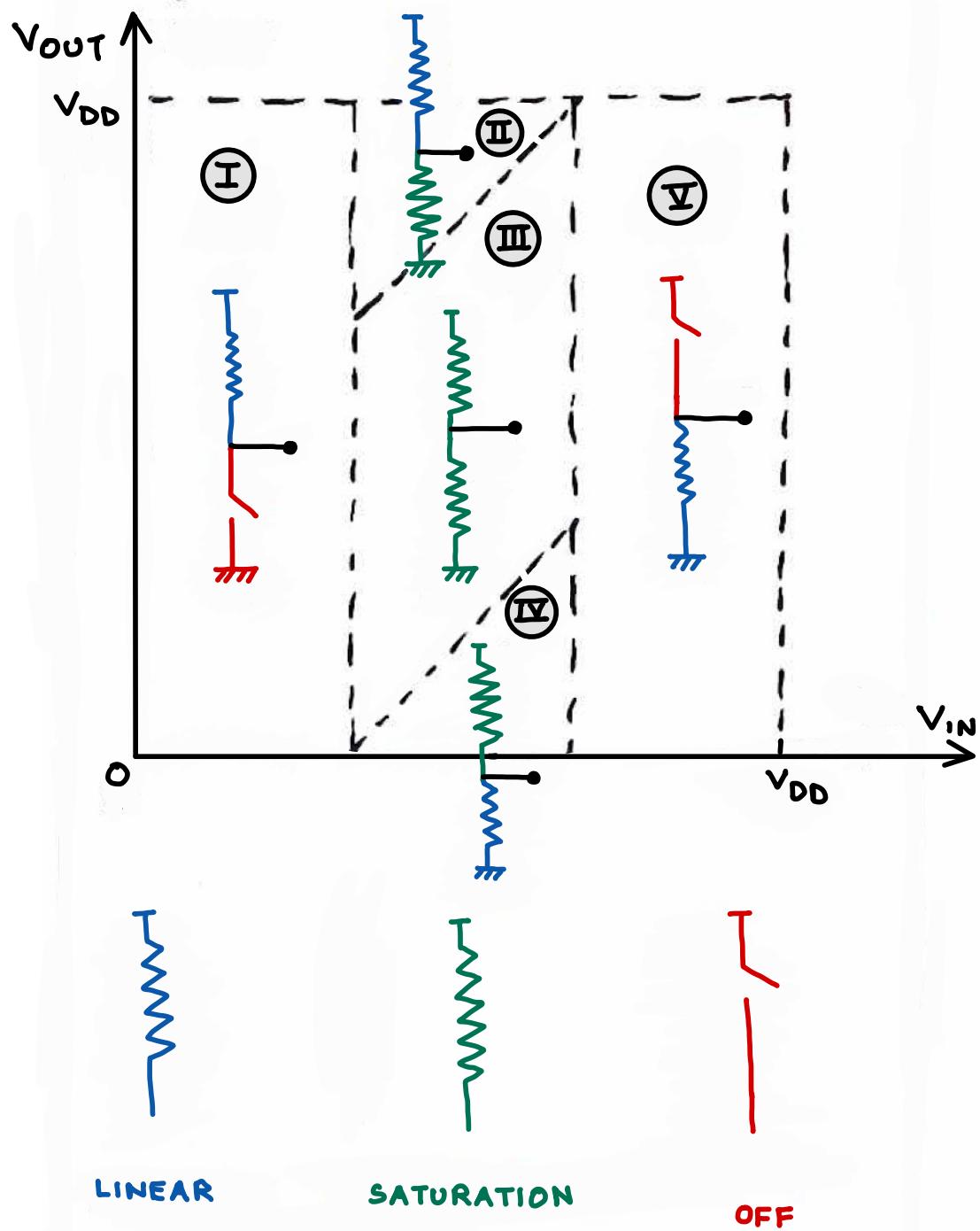
In this plot, we have assumed that V_{OUT} is flat and almost zero. In reality, when V_{IN} is closer to $V_{DD} - |V_{tp}|$, the R_{OFF} of the pMOS is lower due to leakage current.

$\therefore \frac{R_{OFFP}}{R_{ONn}}$ is also a little lower.

$\therefore V_{OUT}$ is a little higher than 0 when V_{IN} is closer to $V_{DD} - |V_{tp}|$.

So the plot in VTC is not absolutely flat but shifts up. But in our course we will ignore these second-order effects and assume that the curve is flat.

If we draw the resistance diagrams for the different regions, we will have :-



NOTE :- The colors of the resistances indicate the region of operation of the transistor and the size indicates the relative magnitude of the resistances.