JAYPEE UNIVERSITY OF ENGINEERING & TECHNOLOGY, GUNA
DEPARMENT OF COMPUTER SCIENCE & ENGINEERING
Course: Computer Organization & Architecture Lab
Course Code: CS208/18B17CI474
B. Tech. (CSE IV/VI Sem.)

Experiment # 5

Aim: Design of common bus, logic unit and shift unit.

Exercise#1: Design 4-bit common bus system using **in-built block of multiplexer** which shares data to the output from four sources as given in the table. Use inputs and outputs as individual bits and selection lines in the form of bus.

Design Steps:
- Find number of required multiplexer (=Number of bits).
- Identify size of required multiplexer (≥ Number of sources).
- Implement the common bus system.
- To verify the design, apply four 4-bit random inputs, vary the selection lines, and see the output if it is correct or not.

Select Lines	Micro operations
00	F ← A
01	F ← B
10	F ← C
11	F ← D

Exercise#2: Repeat **Exercise#1** using **in-built block of tri-state (controlled) buffers** and **decoder.**

Design Steps:
- Find number of required tri-state buffers (= Number of bits × Number of Sources).
- Identify size (no. of output lines) of required decoder (≥ Number of sources).
- Implement the common bus system.
- Verify the design as in Exercise#1.

Exercise#3: Design 4-bit logic unit using **in-built block of multiplexer** which performs four logical operations as given in the table. Use all inputs, outputs and selection lines in the form of bus.

Design Steps:
- Find number of required multiplexer (= Number of bits).
- Identify size of required multiplexer (≥ Number of operations).
- Implement the logic unit and verify it as in Exercise#1.

Select Lines	Micro operations
00	F ← $\bar{A}$
01	F ← A ∧ B
10	F ← A V B
11	F ← A ⊕ B

Exercise#4: Design 4-bit shift circuit in using **in-built block of multiplexer** which performs four shift operations as given in the table. Use all inputs, outputs and selection lines in the form of bus.

Design Steps:
- Find number of required multiplexer (= Number of bits).
- Identify of required multiplexer (≥ Number of operations).
- Implement the shift unit and verify it as in Exercise#1.

Select Lines	Micro operations
00	F ← Shl A
01	F ← Cir B
10	F ← Ashr A
11	F ← Cil B