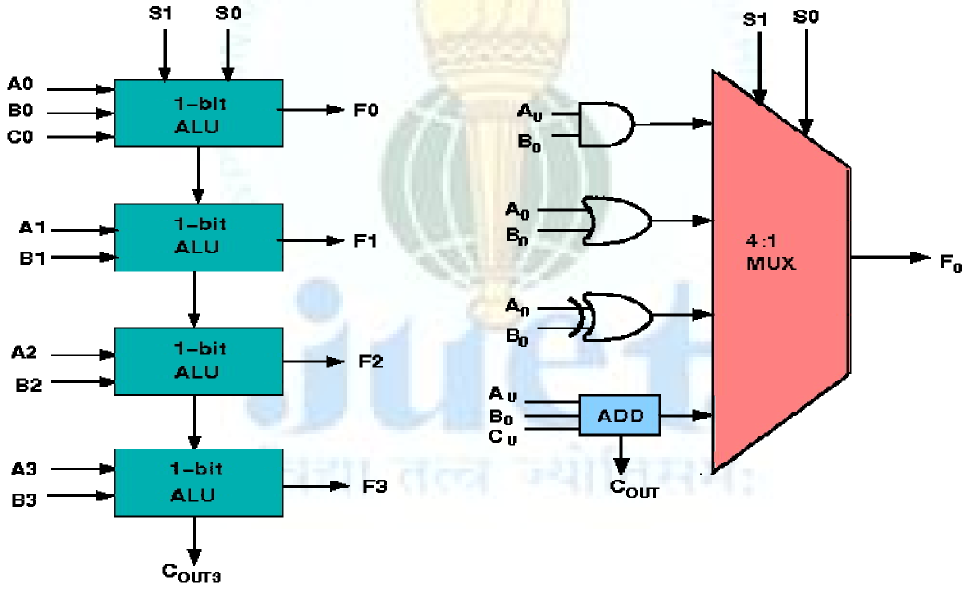
# JAYPEE UNIVERSITY OF ENGINEERING & TECHNOLOGY, GUNA
# DEPARMENT OF COMPUTER SCIENCE & ENGINEERING

## Course: Computer Organization & Architecture Lab
## Course Code: CS208/18B17CI474
## B. Tech. (CSE IV/VI Sem.)

## Experiment # 6

**Aim: Design of Arithmetic Logic Shift Unit and Multiplier.**

An arithmetic logic shift unit (generally known as ALU) is one of the important units of the central processing unit (CPU) of a computer system. It does all processes related to arithmetic and logic operations that need to be done on instruction words. In some microprocessor architectures, the ALU is divided into the arithmetic, logic and shift units. The design and implementation of the ALU is an important architecture design problem. Block diagrams of four operations ALU with two control (select) lines are shown here below:-



(a) (b)

Fig. 1: Block diagrams (a) 4-bit-4-operation ALU (b) 1-bit-4-operation ALU

**Exercise#1:** Design 4-bit, 8-operations (given in Table) Arithmetic Logic Shift Unit as shown in block diagram of figure-2 using initial carry ($C_{in}$) as LSB of the control lines of multiplexers. Use control signals and input/output signals in the form of **bus**.

| **Control Signals** | **Operations** |
|---|---|
| **$S_2S_1S_0$** | **Arithmetic Operations** |
| 000 | Transfer : $F = A$ |
| 001 | Subtract: $F = A - B$ |
| 010 | Addition: $F = A + B$ |
| 011 | Decrement: $F = A - 5$ |
| **Logical Operations** | |
| 100 | XOR: $F = A \oplus B$ |
| 101 | AND: $F = A \wedge B$ |
| **Shift Operations** | |
| 110 | Circular left shift of A: $F = cil\ A$ |
| 111 | Arithmetic shift of B: $F = Ashr\ B$ |

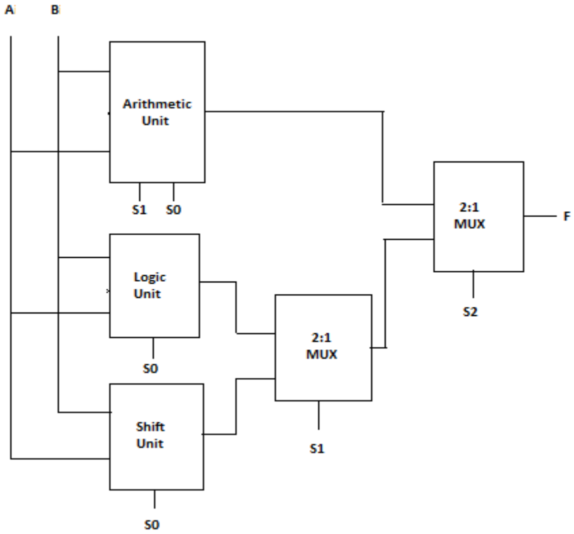


Figure-2: Block diagram of 4-bit, 8-operation ALU

**Design steps:**

- Use **4 bit bus in-built blocks** of multiplexers, shifters, full adder, gates required in the design.
- Design arithmetic, logic and shift units individually and use them as **sub-circuit** in the design of ALU using input/output signals in the form of **bus.**
- Implement the design of ALU.
- Add two hex displays at input and two hex displays at output (one with 4bit output and one with one bit end carry).
- To verify the ALU design, apply four 4-bit random inputs, vary the selection lines, and check the output if it is correct or not.

**Exercise#2:** Design 2-bit array multiplier using **in-built block** of half adder. Display both the inputs and output result in decimal format using suitable display devices.