JAYPEE UNIVERSITY OF ENGINEERING & TECHNOLOGY, GUNA
DEPARMENT OF COMPUTER SCIENCE & ENGINEERING
Course: Computer Organization & Architecture Lab
Course Code: CS208/18B17CI474
B. Tech. (CSE IV/VI Sem.)

Experiment # 7

Aim: Design of sequential logic circuits.

A sequential logic circuit is the digital system whose **output depends on its current combination of input values as well as previous values of the output**. All flip-flops, registers, counters are the examples of sequential circuits. Other important features of these circuits are as following:-

- Feedback connections in the circuits.
- Clock signal i.e. time dependent
- Memory elements in the circuit

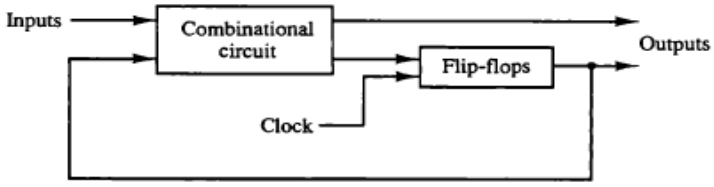
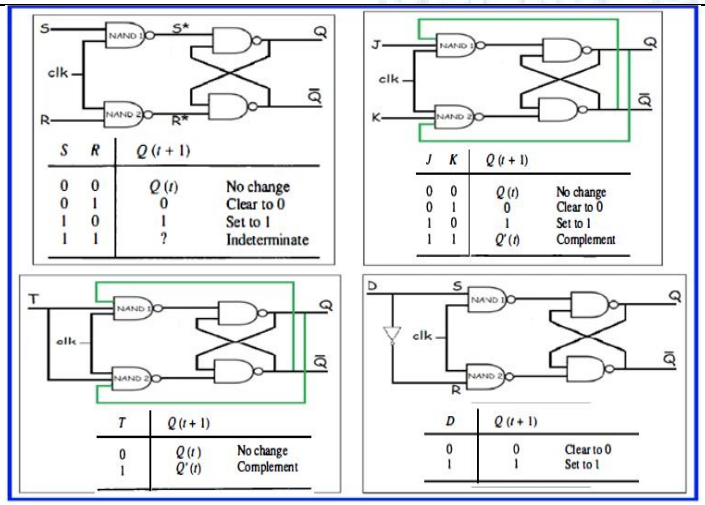


Figure 1: Block diagram of a typical sequential logic circuit

Flip-flops: These are the most elementary building blocks of sequential logic circuit which can store single bit binary data at a time. This name comes from the ability to 'flip' or 'flop' between two stable states either 1 or 0. There are four basic types of flip-flops i.e. SR, JK, T, and D. Out of these, D flip-flop is most commonly used in the design of various sequential circuits.

Flip-flops with their Truth Tables



Excitation Tables

SR flip-flop

Q(t)	Q(t + 1)	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

D flip-flop

Q(t)	Q(t + 1)	D
0	0	0
0	1	1
1	0	0
1	1	1

JK flip-flop

Q(t)	Q(t + 1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

T flip-flop

Q(t)	Q(t + 1)	T
0	0	0
0	1	1
1	0	1
1	1	0

Registers: These are the group of flip-flops. Its basic function is to hold and shift the information within a digital system so as to make it available to the logic units during the computing process. This sequential device loads the data present on its inputs and then moves or "shifts" it to its output once every clock cycle, hence the name **Shift Register**. Data bits may be fed in or out of a shift register serially (SISO: serial in serial out), that is one after the other from either the left or the right direction, or all together at the same time in a parallel configuration (PIPO: parallel in parallel out) as shown in Figure 2. A shift register basically consists of several single bit flip-flops, one for each data bit, connected together.

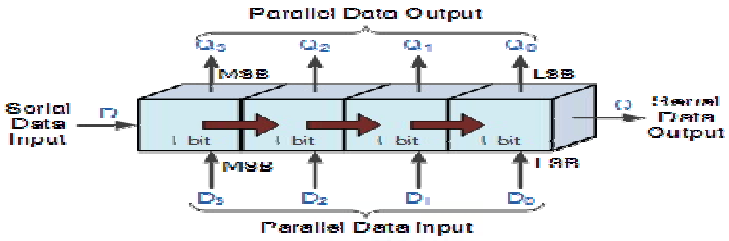
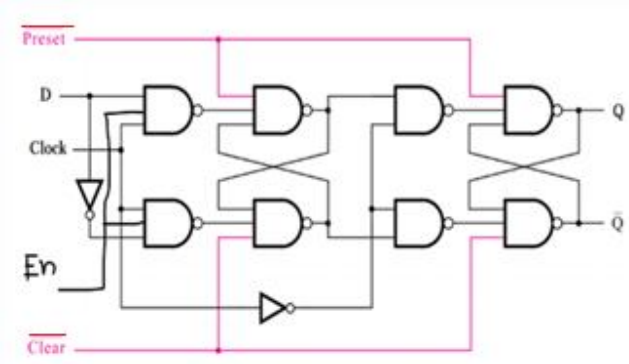


Figure 2: Four configurations (SISO, SIPO, PIPO, and PISO) of a shift register.

Counters: *Counters* are the (group of flip-flops) sequential *circuits* which "count" through a specific state of sequence. The number of flip-flops used and the way in which they are connected determine the number of states and also the specific sequence of states that the counter goes through during each complete cycle. Counters are classified according to the way they are clocked: **Asynchronous** (also called ripple counter) in which the first flip-flop is clocked by the external clock pulse and then each successive flip-flop is clocked by the output of the preceding flip-flop and **Synchronous** counter is one in which the flip-flops within the counter changes states at exactly the same time because they do have a common clock pulse to all flip-flops**.**

Exercise#1: Design D flip-flops with Enable, Clear and Preset control lines as shown in Fig.3. Verify the designs with given truth table and in-blocks of flip-flop.



En	Preset	Clear	Clock	D	Q
0	x	x	x	x	N.C.
1	1	0	x	x	1
1	0	1	x	x	0
1	0	0	0	0	N.C
1	0	0	0	1	N.C
1	0	0	1	1	1
1	0	0	1	0	0

N.C. = No Change; X = don't care

Figure 3: Logic diagram of D Flip flop

Exercise#2: Design and verify 4-bit SISO shift register (without in-built block) as using D flip-flops as sub-circuit. Also use preset and enable control lines in the design. [**Note:** Replace **clock signal** with **input pin** before using D flip flop as sub-circuit in the design]

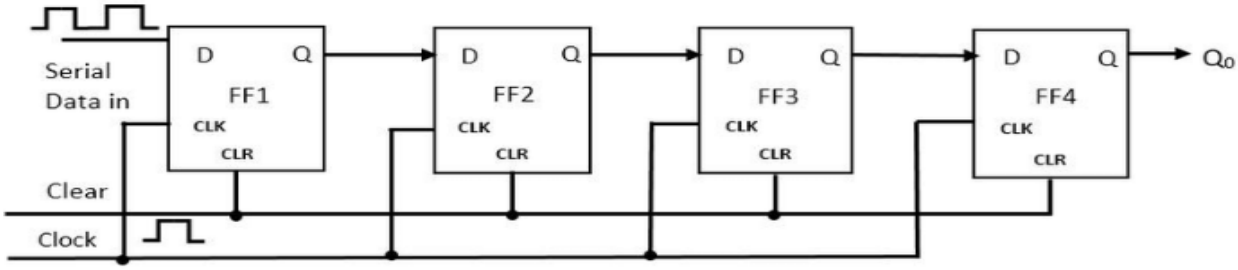


Figure 4: Block diagram of 4-bit SISO register

Exercise#3: Design and verify MOD-6 binary counter as shown in Figure-5 using in-built block of D-flip-flop. Display counting using Hex display. Consider Q_A and Q_C as LSB and MSB respectively.

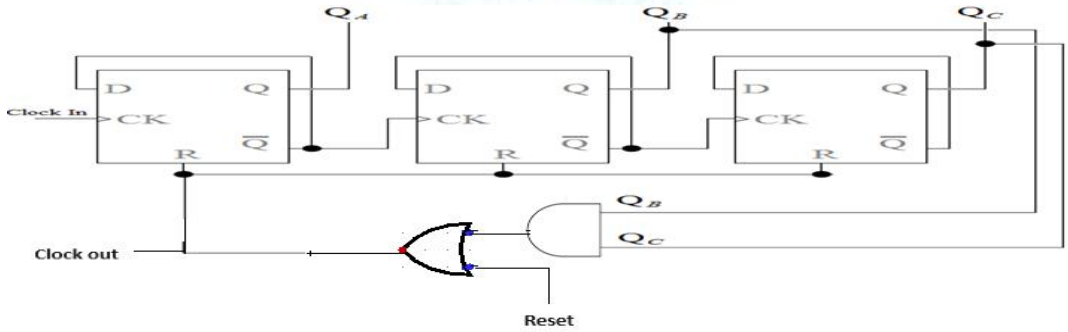


Figure 5: Block diagram of MOD-6 counter

Exercise#4: Design 24/12 hour format digital clock as shown in Figure-6.

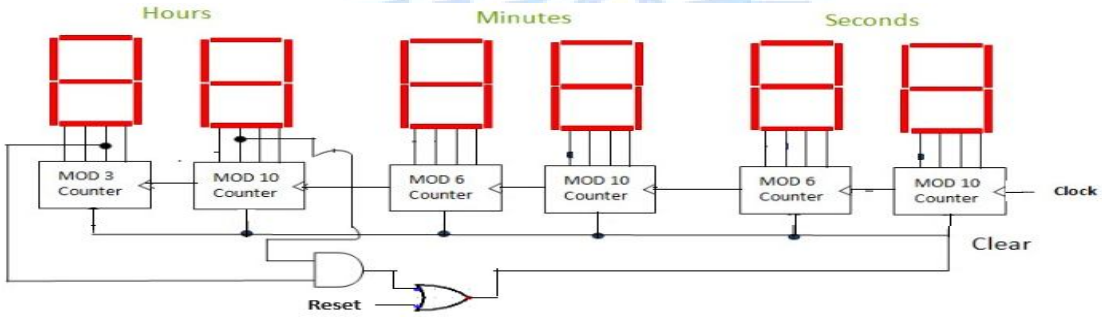


Figure 6: Block diagram of digital clock

Design steps:

- Design MOD-3, MOD-6, and MOD-10 counters individually and use them as **sub-circuit** in the design of digital clock.
- Replace **clock signal** with **input pin** before using individual counters in cascaded form in the design.
- Design a logic circuit to include **format** control line for changing the format of the clock (24 hour to 12 hour and vice-versa).
- Press **Ctrl+K** for auto toggling of the clock.
- Clock frequency can be varied by changing the number of ticks in the low/high duration.