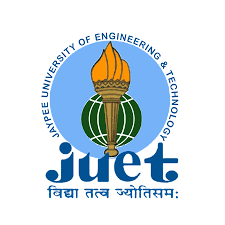
**JAYPEE UNIVERSITY OF ENGINEERING & TECHNOLOGY, GUNA**

**DEPARTMENT OF Computer science & engineering**



**A PRACTICAL WORK BOOK**

**of**

**COMPUTER ORGANIZATION & Architecture LAB**

**(COURSE CODE: CS208)**

**SUBMITTED**

**TO**

**Type FaCulTy Name**

**Name of student\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_ENRL NO.\_\_\_\_\_\_\_\_**

**Class\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ BATCH\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**BRANCH\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_SESSION\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

***INDEX***

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**EXPERIMENT#1**

**Aim: Designing of basic digital circuits using logic gates.**

**Exercise#1:** Design two inputs and five outputs All-in-One logic gate circuit shown in Fig.1 using Logisim simulator with (i) data width 1 (ii) data width 4.

|  |  |
| --- | --- |
| **Boolean Expressions** | **Logic Diagram** |
| C = not A  D = A.B  E = A+B  F = ~(A.B)  G = AB |  |
| **Truth Table** or **Karnaugh (K) Map** |
|  |

* Use above format to prepare your lab record.
* Use given cover page in your file and write your information (name, enrl. etc) by pen.
* Use given index format in the file and write the information after the completion of each experiment by pen.
* Use minimum number of pages for the text of each experiment.
* Don’t leave space in the pages unnecessarily.
* Edit the contents carefully for better appearance of the file..
* Use optimal size of figures. Text in figures should be visible clearly but figure should not be unnecessarily too big.
* Each page of file must have **your name and enrolment number** at the bottom of page (can be used footer). File must not be a copy and paste.
* Save all files at your personnel space, preferably in N-drive, by creating a folder named as ‘COA Lab’.