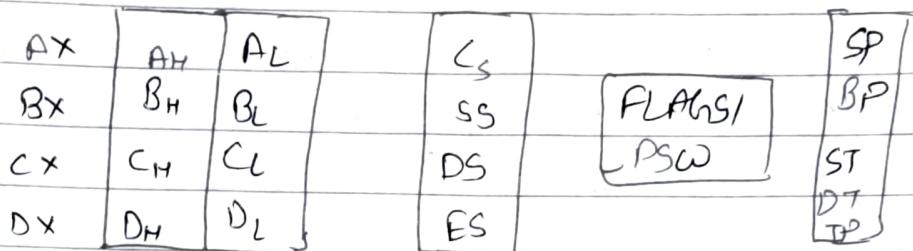


(A)

MAP ASSIGNMENT

- ① Explain Register Organization of 8086 with the help of block diagram

→



General data Segment Pointers & index  
register registers register

→ 8086 registers are classified into :

- ① General data Registers
- ② Segment Registers
- ③ Pointers & Index Registers
- ④ Flag Register.

→ ① General data Registers

→ AX, BX, CX & DX are general purpose 16-bit registers

→ All data registers can be used as either 16 bit or 8 bit

→ AX is

→ AX is used as 16 bit accumulator  
AL is designated lower 8-bit  
while AH is higher 8-bit used for  
8 bit operation.

→ ② Segment Register  
⇒ a

→ 4 segment register.

- (A) code segment Register
- (B) Data segment Register
- (C) Extra segment Register
- (D) stack segment Register

→ CS:-

Used for addressing memory location in the code segment of the memory

→ DS :- point to the  
Point to the data segment of the memory where the data is stored

→ ES :-

Also refer to a segment in the memory which is another data segment in the memory

→ SS :-

Used for addressing stack segment of the memory.

③ PSW) Flags:-

→ content indicate the results of computation in the ALU It also

Some flag bit to control the CPU operation

#### (A) Pointer & Index register

(A) IP (Instruction pointer):

store memory location of next instruction to be executed

(B) BP (Base pointer):

contains offset within the data segment

(C) SI (Source index):

To store the offset of source data in data segment

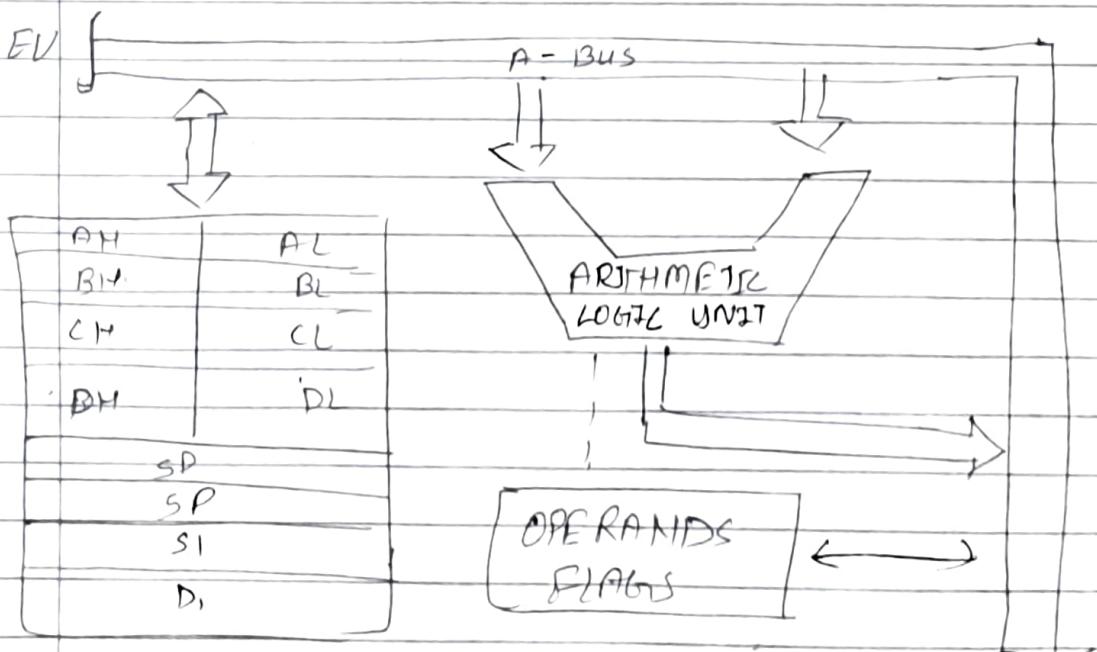
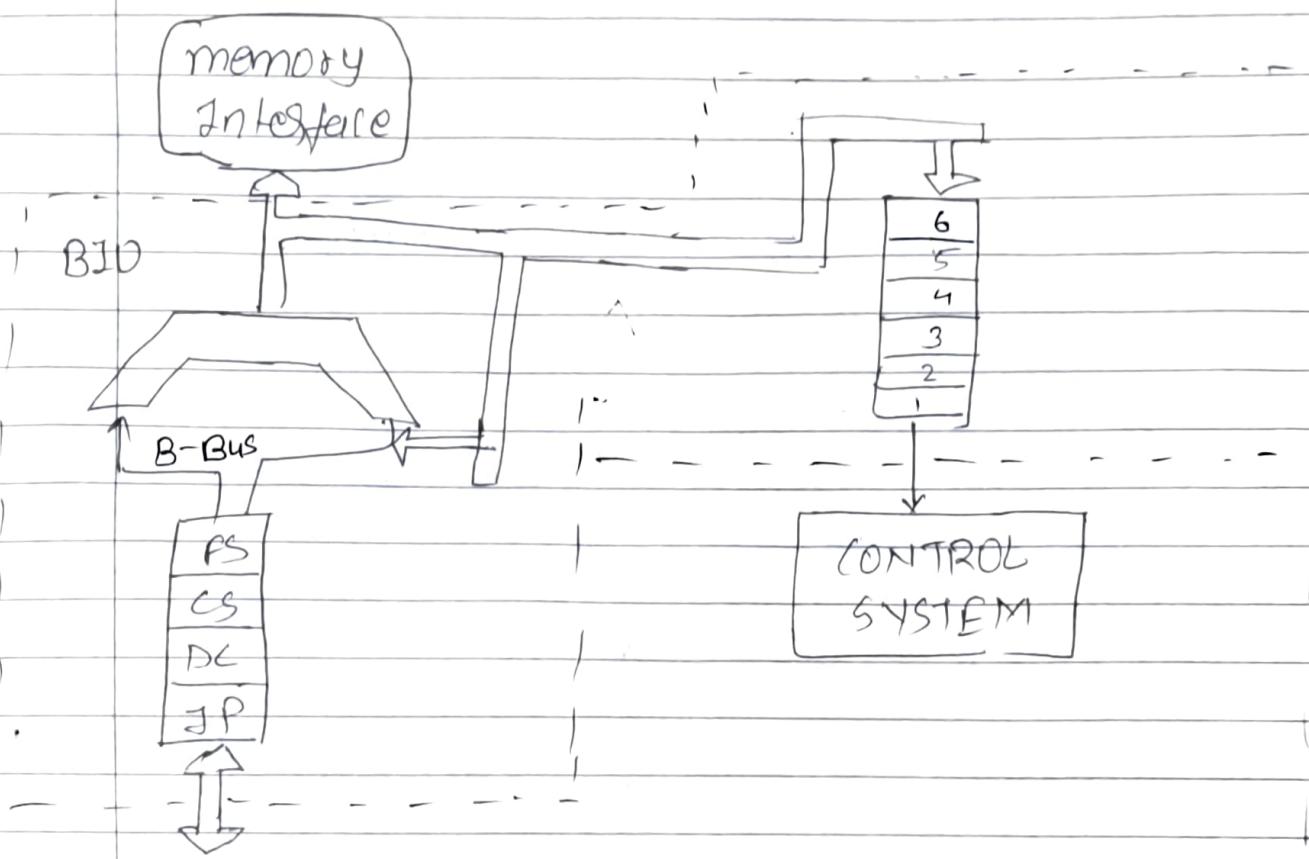
(D) SP (Stack pointer):

contains offset within stack segment

(E) DI (Destination index)

Used to store offset of destination in data or extra segment

Q Q Draw and Explain Architecture of 8086 Micro processor.



→ Divided into two independent functional parts

- Bus Interface unit (BIU)

- Execution unit (EU)

→ A) BIU :-

→ It sends out address, fetches instruction from memory, reads data from ports

→ It handles all transfers of data and addresses on the buses for the execution unit

→ B) EU :-

→ Tells the BIU where to fetch instruction or data from decoder  
Instruction & executes instruction

→ Contains control circuitry which directs internal operations

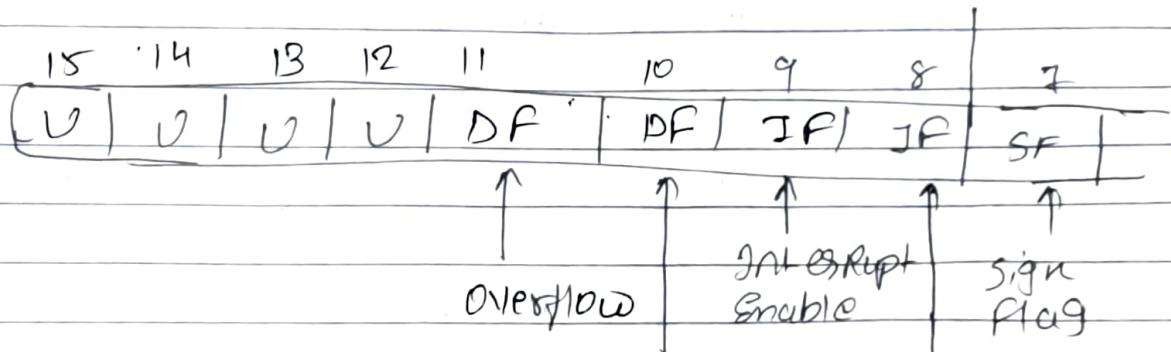
→ Also has a 16-bit ALU which can ADD, SUB, AND, OR, XOR, OR INCREMENT etc:-

Q. ③ Explain flags of 8086 microprocessor

→ 16 bit flag divided into two parts

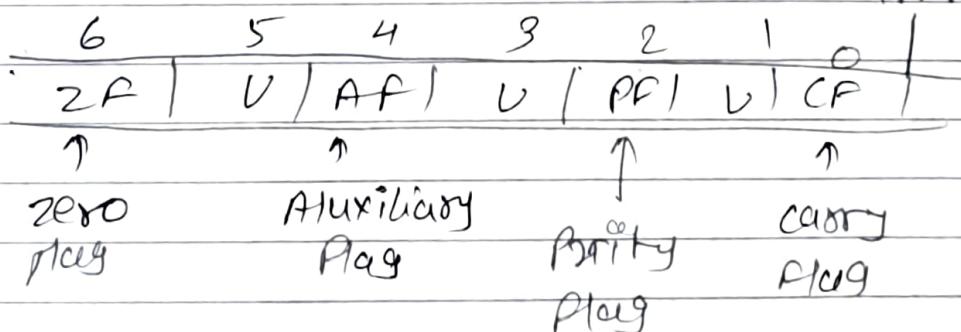
- Condition code or status flags

- Machine control flags



STRIKETHROUGH  
DIRECT

single  
step  
TRAP



→ SF - SIGN FLAG :- Result of any computation is Negative

→ ZF - ZERO FLAG :- If is set if result is zero

- PF Parity Flag : - It is set to 1, if lower byte is even
- CF CARRY FLAG : It is set when carry out in case of borrow
- AF - Auxiliary carry Flag :- It is set if carry is lowest nibble
- OF - overflow Flag :- It is set when overflow occurs
- D - Direction Flag ! - Used by string manipulation instruction.

Q (4) Explain all signal of 8086 micro processor

→ Three signals :-

- (A) Control Signal
- (B) Interrupt signal
- (C) DMA Interface signal

⇒ (A) control signals :-

→ They control function such as when the bus is to carry a valid address in which direction data are to be transferred.

→ Ready Signal

→ It is used to insert wait state into the bus cycle

(B) Interrupt Signals

→ The key interrupt signals are interrupt request (INTR) and interrupt acknowledge (INTA)

→ INTR represent an active interrupt request on it  
it indicate the fact to external circuit with pulse to logic 0 at the INTA output

(C) DMA Interface Signals

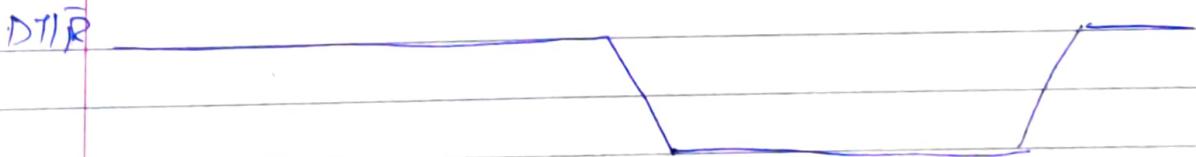
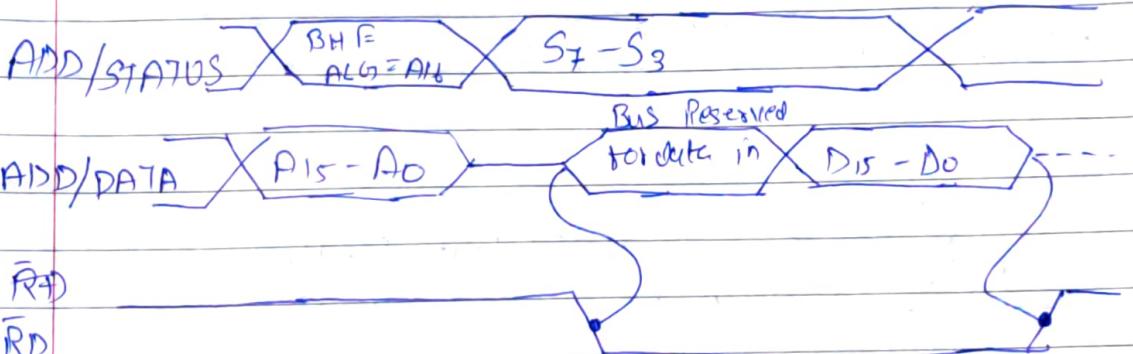
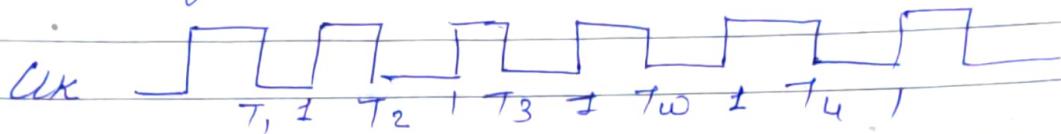
→ The direct memory access DMA interface of the 8086 minimum mode consist of the HOLD and HLDA signals

→ When an external device wants to take control of the system bus it signal to the 8086

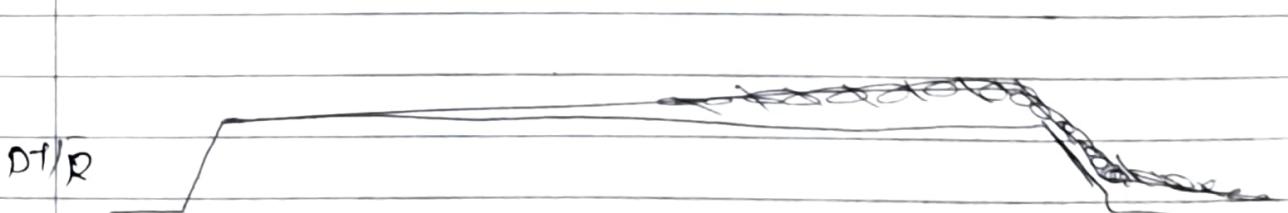
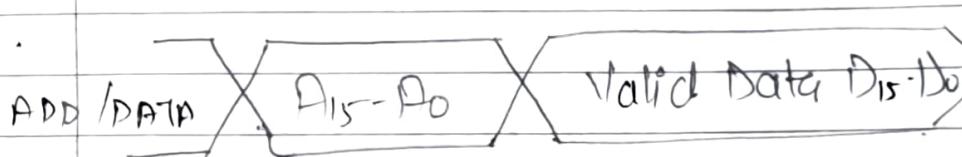
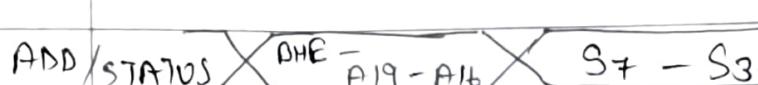
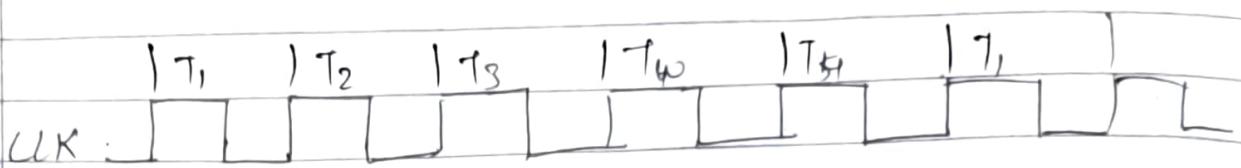
→ The 8086 signal external device that it is in the state by sufficing its HLDA output to logic 1 level

Q5 Draw timing diagrams of memory Read & memory write operation

① Memory Read Bus cycle

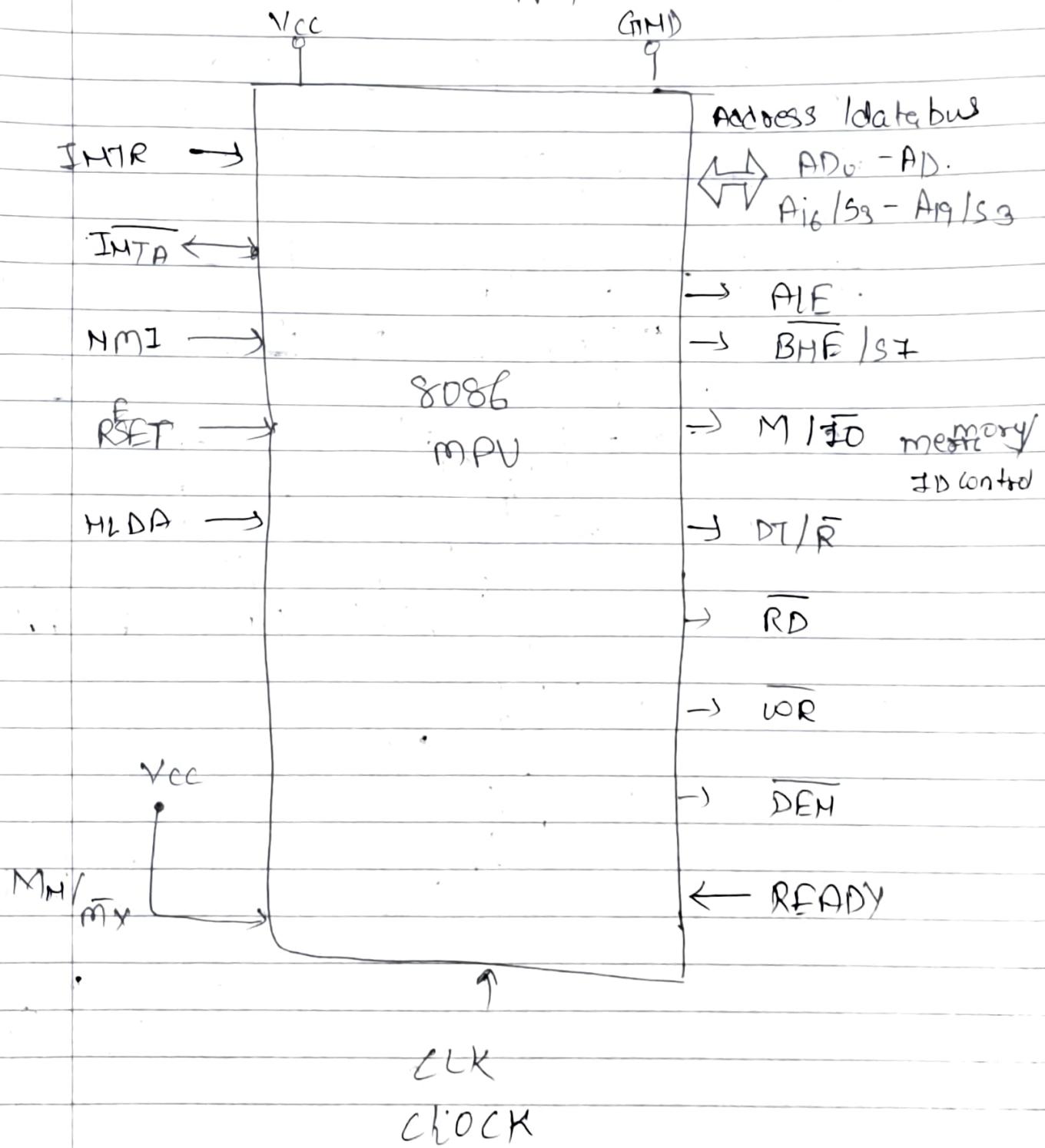


(2) Memory write Bus cycle :-

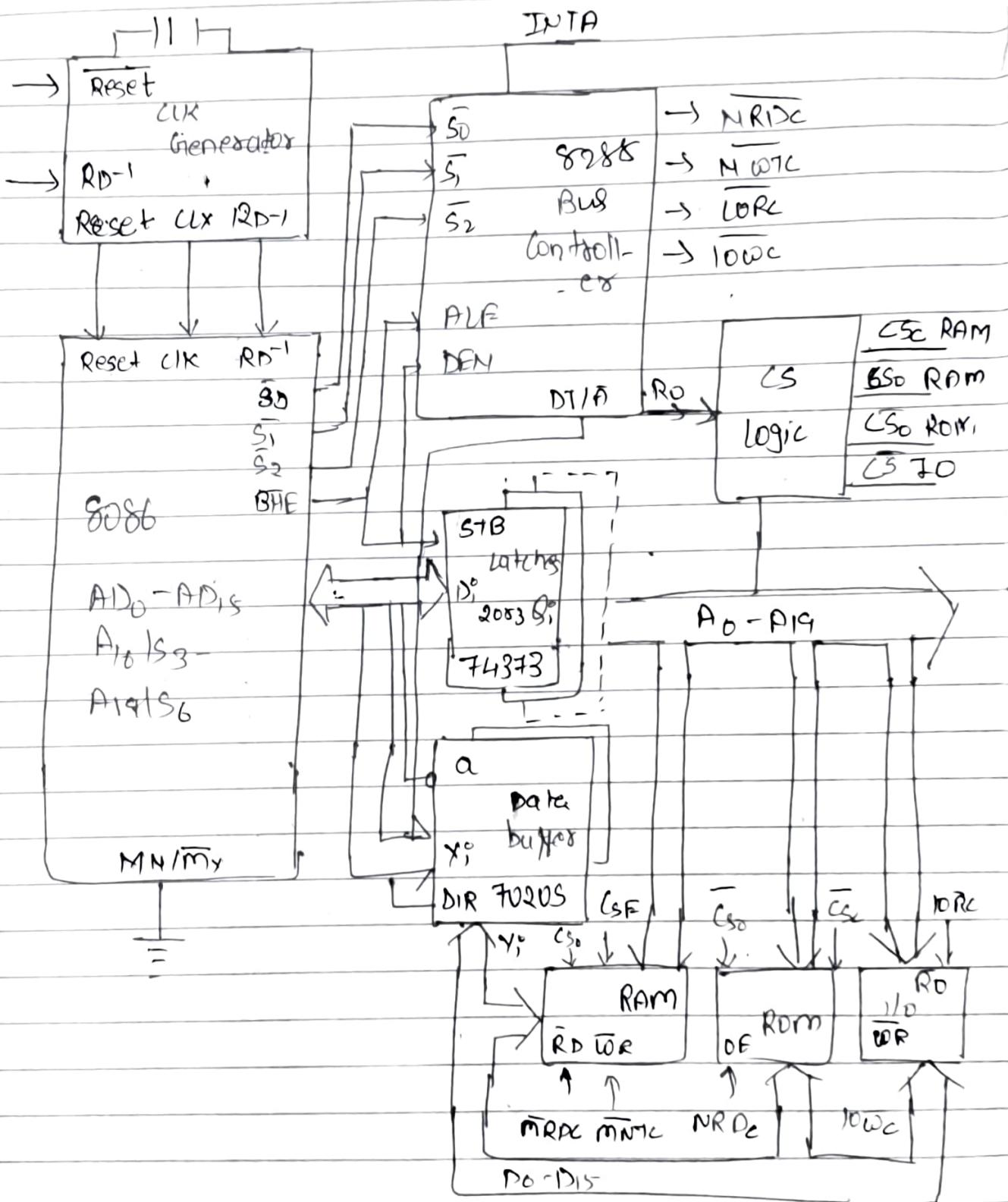


Q(6) Draw block diagram of minimum mode of 8086 microprocessor.

### Power Supply



Q ⑦ Draw block diagram of 8086 microprocessor  
maximum mode

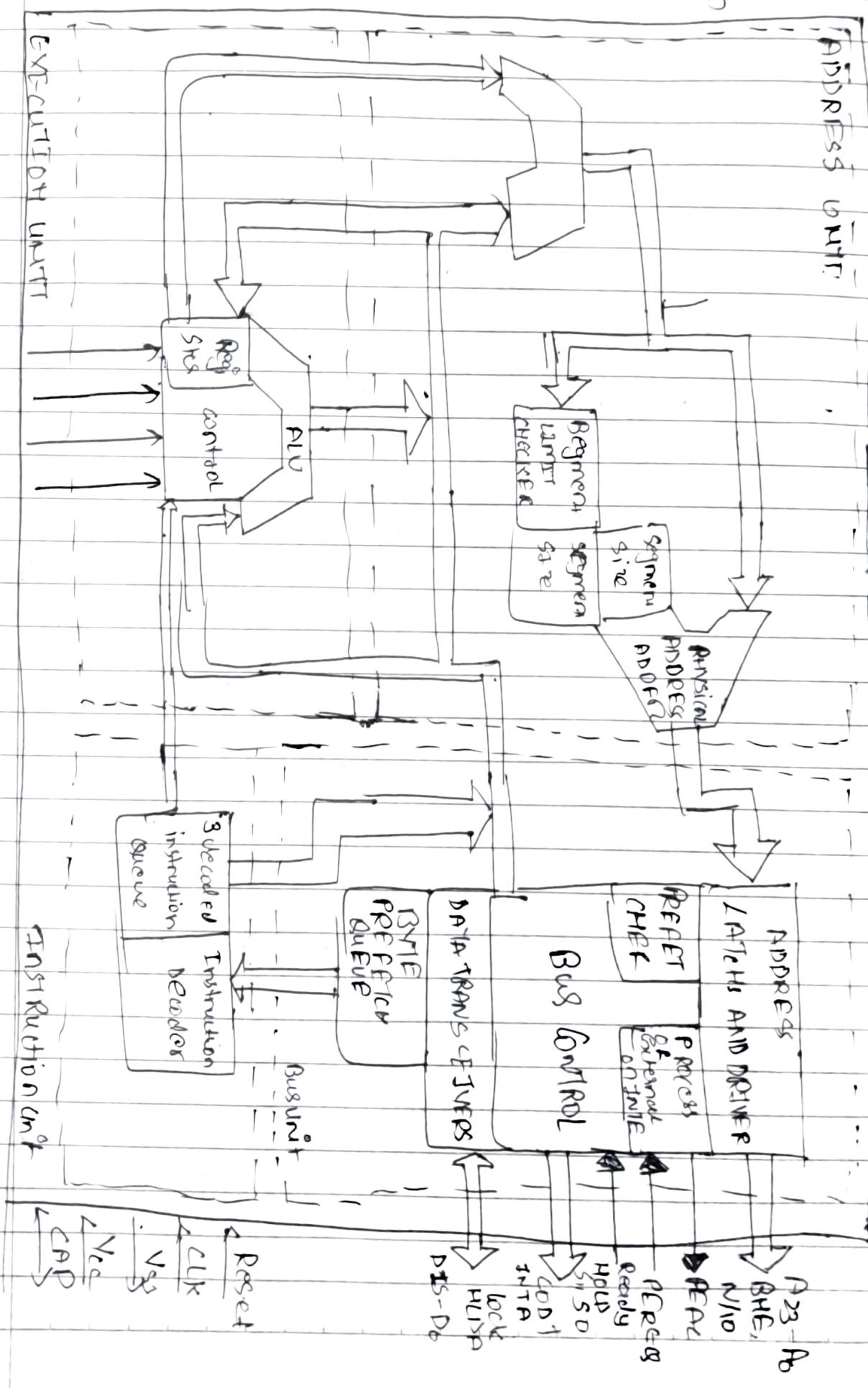


Q(8)

Write difference between 8085 & 8086 microprocessor

Property	8085	8086
→ Data Bus size	8-bit	16-bit
→ Address Bus size	16-bit	20-bit
→ clock speed	3 MHz	Varies in range 5-8-10 MHz
→ Duty cycle for clock	50%	33%
→ Flag	5 flags	9 flag
→ Memory size	64 KB	1 MB

Q. (a) Draw and explain 80286 block diagram.



- The CPU may be viewed to contain four functional parts viz
- (a) Address Unit (AU)  
(b) Bus Unit (BU)  
(c) Instruction Set (ISU)  
(d) Execution Unit (EU)
- The address unit is responsible for calculating the physical address of instruction and date that CPU wants to access.
- This physical address computed by the address unit is handed over to the bus unit (BU) of the CPU
- The address latches and drivers in the bus unit transmit the physical address thus formed over the address bus A<sub>0</sub>-A<sub>23</sub>
- One of the major function of the bus unit is to fetch instruction bytes from the memory
- The instruction unit accepts instructions from the prefetch queue & an instruction decoder them one by one.

(Q10) what is real address mode and protected virtual address mode of 80286?

→ (1) Real address mode

- Act as a fast 8086
- Instruction Set is upwardly compatible
- It address only 1M byte of Physical memory using A0 - A19

→ (2) Protected virtual address mode

→ It is the first processor to support the concept of virtual memory & memory management

→ It is able to address 1G byte (2<sup>30</sup> bytes) of virtual memory per task

→ It can also permit system software feature such as virtual memory, paging and safe multi-tasking.

Q.11 What are the salient features of 80286?

- It is a high performance 16 bit microprocessor
- It has been specially designed for multiuser & multi-tasking system
- Various versions of 80286 are available that run on 12.5 MHz, 10 MHz and 8 MHz clock frequencies
- It is upwardly compatible with 8086 in terms of instruction set
- It is the first CPU to incorporate the integrated memory management unit
- It has 4 level memory protection and support for virtual memory & OS
- It has 24 address lines and 16 data lines
- There are 2 OS
  - real address mode
  - protected virtual memory address.

(Q12)

write in short 80826 Signer

→ CLK :-

It is the System clock input pin

→ D<sub>15</sub>-D<sub>0</sub> : These are sixteen bi-directional data bus lines

→ A<sub>23</sub>-A<sub>0</sub> :-

These are the physical address output lines used to address memory or I/O devices

→ BHE :-

It indicates that active low status of output signal which indicate initiation of a bus cycle & with M1# & C01 / INTA

→ LOCK : It is active - low output pin used to prevent the masters from gaining the control of the bus for the current and the following bus cycle

- V<sub>SS</sub> :-

System ground pin

→ Ready →

It is active low input pin used to pinset wait state in a bus cycle for interfacing low speed peripherals

→ V<sub>CC</sub> → Used to apply +5V power supply voltage to internal circuit

→ CAP :- A 0047 12V capacitor between input pin & ground to filter.

Part

(B)

- ① Find maximum number from the array of 15 numbers

→ Data Segment

Arr DS 5, 3, 7, 1, 9, 2, 6, 8, 4, 0, 17, 10, 11  
↓ 12, 22

Data ends

Code Segment

Assume DS: DATA CS: CODE

Start:

MOV AX, DATA  
MOV DS, AX  
LEA SI, ARR  
MOV AL, ARR[SI]  
MOV MAX, AL

MOV AH, 4CH  
INT 21H  
CODE ENDS  
ENDS START

CHECK MAX:

CMP MAX, AL  
JG DONE  
MOV MAX, AL

DONE

INC SI  
LOOP REPEAT

(2) Sort array of 20 numbers in ascending order.

→ org 100h

mov cx, 3000

mov ds, ax

mov dl, 10h

mov si, 500h

mov di, 500h

mov al, dl

L0 : mov al, [si]

    mov cl, dl

L1 : inc si

    mov bl, [si]

    cmp dl, bl

    jg next

    jc next

    xchg al, bl

    mov [si], bl

next: loop L1

    mov bh, al

    mov [di], bh

    inc di

    mov si, di

    dec di, di

    pn 2 L2

    ret

③ Count even numbers & odd numbers from the list

→ org 100h

mov ax, 3000h

mov ds, ax

mov cx, 0Ah

mov dh, 00h

mov dl, 00h

clr mov bh, [si]

shl bh, 1

JC Odd

Inc Even

odd : inc dh

inc si

dec cx

Jnz a

hlt

Even : inc dl

inc si

dec cx

Jnz a

hlt

ret

④ Write to get carry flag & parity flag without affecting other flags

→

mov al, 9Ch

mov dh, 64H

add al, dh

AL	1001	110D
+ DH	0110	010D

1	[ 0000 0000 ]
---	---------------

CF = 1