Rudrajyoti Roy

Ann Arbor, MI, 48105 | rudraroy@umich.edu | rudrajyotiroy@gmail.com | (+1)734-596-4864

linkedin.com/in/rudrajyoti-roy-9a9417187 | github.com/rudrajyotiroy | rudrajyotiroy.github.io | G-Scholar

Education

University of Michigan, Ann-Arbor, MI, USA Aug 2024 – May 2026

- **MS in Computer Science and Engineering** (Current GPA: 4.0/4.0), Advisor : **Satish Narayanasamy**
- **Research:** Exploring ways to ensure EULA compliance of on-premise AI and HPC chips remotely through hardware-enforced workload intent authorization and performance regulation (*why is this useful?*)
- **Coursework:** Adv Computer Architecture, Adv Compilers, Scalable Systems for GenAI, Privacy-Enhancing Tech

Indian Institute of Technology (IIT), Kharagpur, WB, India Aug 2018 – May 2022

- **B.Tech Major in Electronics & Elec. Comm. Eng.** GPA : 9.26/10 (3.9/4.0 US equivalent)
- **Minor** in Computer Science and Engineering, **Micro-specialisation** in Embedded Software Modelling & Design
- **Major Coursework:** Adv VLSI, Digital Design, Embedded System, Digital Signal Processing, Control Theory
- **Minor Coursework:** Algorithms, AI, Computer Architecture, CUDA/OpenMP Programming, Hardware Security

Work Experience

Graduate Student Instructor (GSI), EECS183, University of Michigan – Ann Arbor, MI Aug 2025 – Present

- Managed a class of 805 students (35 students per GSI) learning introduction to programming in C++, Python.
- Conducted weekly labs, office hours, prepared and graded exams and actively contributed to holistic curriculum development, student experience and staff productivity improvement. (Average Student Rating: **4.5 out of 1-5**)

HW System Modeling Engineer, Qualcomm – Bengaluru, India Dec 2023 – Aug 2024

- Single-handedly developed and verified a functional **co-simulation model** of High-Performance Audio Engine in C++ and integrated with QEMU Virtual Platform to enable **RTL-agnostic audio driver testing**.
- Facilitated full register set programmability with functionality and timing accurate modelling, enabling fast prototyping and **expediting SW driver development by 6 months** ahead of RTL maturity.
- **Individually recognized by VP** (Audio Systems, Toronto), for pioneering first-of-its-kind execution.

Associate HW Verification Engineer, Qualcomm – Bengaluru, India Jul 2022 – Nov 2023

- Proposed and **published** a segregable, scalable, fault-tolerant hierarchical **ML framework** for **early detection, termination and intelligent triaging of deadlocks** encountered during long-running HW simulations.
- Integrated the proposed framework with CI/CD pipeline for automated deployment across projects. Achieved **40%** reduction in early-stage debugging time and significantly minimised cluster resource wastage.
- Developed an automated assertion generation and binding flow for in-situ monitoring of post-reset memory reads and flagging incorrect POR values, improved power-aware GLS sign-off TAT by 25%.
- Took ownership of fixing testbench and writing testcases for **two IP blocks** within audio core across projects.

HW Engineering Intern, Qualcomm – Bengaluru, India May 2021 – Jul 2021

- **Developed a secondary UVM monitor** to detect bus stalls by passively tracking bus read/write transactions.
- Automated it's integration with AXI/AHB, achieving up to **80% bus stall detection** with <5% false positives.

Publications

[1] **Scheduling & Routing Strategies for Executing Task Graphs on AdHoc Networks** Nov 3, 2025

Chhavi Chaudhury; ***Rudrajyoti Roy***; Rajesh Devaraj; Arnab Sarkar

Ad Hoc Networks Journal (Elsevier) DOI: 10.1016/j.adhoc.2025.104084

[2] **Harnessing Machine Learning in DTM in CPU-GPU Embedded Platforms** Jan 10, 2025

Srijeeta Maity; Anirban Majumder; ***Rudrajyoti Roy***; Soumyajit Dey; Ashish R. Hota
ACM Transactions on Design Automation of Electronic Systems DOI: 10.1145/3708890 (***EDITOR'S PICK***)

[3] **ML Based Scalable Plug-and-Play Framework for Early Hang Detection** May 8 - 9, 2024
Rudrajyoti Roy; Anshul Sengar, Ronak Shah Bengaluru, India
Qualcomm Global SoC Conference, IP-Cores track (***BEST PAPER AWARD***)

[4] **Future aware Dynamic Thermal Management in CPU-GPU Embedded Platforms** Dec 5 - 8, 2022
Srijeeta Maity*, ***Rudrajyoti Roy****; Anirban Majumder; Soumyajit Dey; Ashish R Hota Houston, TX
IEEE Real-Time Systems Symposium (RTSS) DOI: 10.1109/RTSS55097.2022.00041

[5] **Selective detection of multiple VOCs employing ZnO nanorods and PCA** Oct 2-4, 2020
Avik Sett; Tanisha Rana; ***Rudrajyoti Roy***; Tufan Saha; Tarun Kanti Bhattacharyya Kolkata, India
Intl Conference on Electronics & Materials Engineering DOI: 10.1109/IEMENTech51367.2020.9270117

Projects

Attention As You Need It Sept 2025 - Present

- Proposed automated rewriting framework to dynamically generate tiled and **fused attention kernel** variants (like FlexAttention) tailored to maximize performance under various **LLM inference** deployment scenarios.
- Currently developing a framework to translate PyTorch kernels into compute graphs, followed by cost-constrained exploratory state-space search to **optimise compute and memory bottlenecks**.

MirrorMaze: Compiler-guided control-flow obfuscation to prevent timing attacks Jan 2025 - Apr 2025

- Developed an **LLVM extension** that automatically detects secret-dependent control flow divergence (taint analysis) and intelligently inserts minimal dummy operations to make all branches computationally equivalent.
- Achieved **4-5% performance boost** over state-of-the-art obfuscation method without compromising security.

Contention Aware Task Scheduling on Arbitrarily Networked Execution Platforms July 2021 - July 2023

- Developed a framework for task-graph generation and scheduling on arbitrarily distributed execution platform.
- Proposed two novel heuristics towards scheduling computation and communication for minimizing total makespan while adhering to contention constraints. Conducted extensive Monte-Carlo simulations to evaluate.

Future-Aware Dynamic Thermal Management in Heterogenous MPSoC Platforms Mar 2021 - June 2022

- Designed and implemented a Future-Aware Supervisory Control Framework for real-time resource configuration for dynamically arriving OpenCL kernels on embedded platforms, that minimizes **peak platform temperature**.
- Formulated and trained Newtonian thermal model and analytical performance model for discretized MPC.
- Leveraged a thermal axiom as a heuristic upperbound to reduce an exponential state-space search into linear-time beam search, enabling real-time deployment and outperforming SOTA by 14% on average.

Efficient GPGPU Parallelization of RCNN pipeline for Real-time Object Detection Feb 2021 - Apr 2021

- Constructed efficient CUDA convolution kernels by formulating as multiplication (GEMM) in fourier domain.
- Achieved 100x speedup over naive approach by leveraging cuFFT/cuBLAS support and fine-tuning using GPU optimization techniques like Im2Col flattening, tiling, fusion and memory access coalescing.

Skills

Languages: C, C++, Embedded C, CUDA, OpenCL, Python, Systemverilog, SystemC, MATLAB, Shell, LLVM
Tools: UVM, Synopsis VCS, Verdi, gem5, SniperSim, gpgpuSim, Hexagon SDK, PyTorch, Docker, Git, ClearCase

Extra-curricular Activities

Robotics: SWARM UG research group; Runner-up for JLR(**Inter-IIT Tech Meet**) and Tessaract (as Team Leader)
Sports and Cultural: Chess, Table-Tennis, Badminton, Whitewater Kayaking, Music (Vocal and Keyboard)
Mentoring: SWG Peer Mentor for UG Students, tutored underprivileged school children as **NSS volunteer**