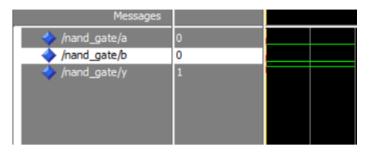
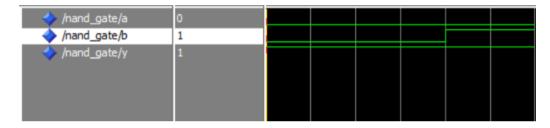
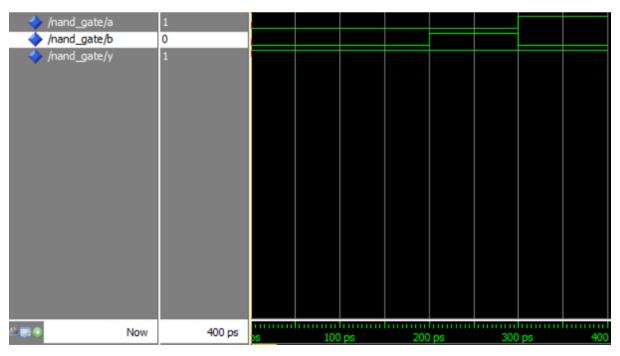
NAND GATE

CASE 1



CASE 2





CASE 4

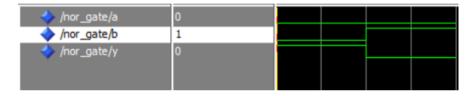
<pre>/nand_gate/a</pre>	1					
<pre>/nand_gate/b //nand_gate/y</pre>	1					
/nand_gate/y	0					

NOR GATE

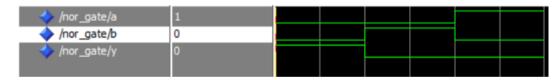
CASE 1

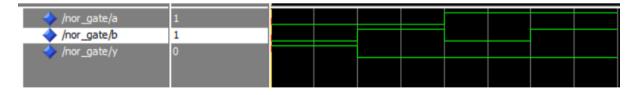
<pre>/nor_gate/a</pre>	0		
<pre>/nor_gate/b</pre>	0		
/nor_gate/y	1		

CASE 2



CASE 3





EXOR GATE

CASE 1

/exor_gate/a	0	
<pre>/exor_gate/b</pre>	0	
/exor_gate/y	0	
*		

CASE 2

/exor_gate/a	0		
<pre>/exor_gate/b</pre>	1		
<pre>/exor_gate/y</pre>	1		

CASE 3

/exor_gate/a	1			
<pre>/exor_gate/b</pre>	0			
<pre>/exor_gate/y</pre>	1			

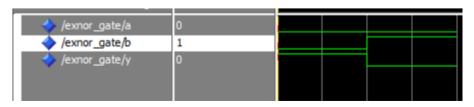
CASE 4

/exor_gate/a	1				
/exor_gate/b	1				
/exor_gate/y	0				

EXNOR GATE

CASE 1

/exnor_gate/a	0	
/exnor_gate/b	0	
<pre>/exnor_gate/y</pre>	1	



CASE 3

→ /exnor_gate/a	1			
<pre>/exnor_gate/b</pre>	0			
/exnor_gate/y	0			

/exnor_gate/a	1				
<pre>/exnor_gate/b</pre>	1				
<pre>/exnor_gate/y</pre>	1				