Lab2

- **Brief introduction about the overall system**

這次 lab 中建立兩個 fir 的 ip，分別是使用 AXI master 跟 AXI stream 來傳輸資料

- **What is observed & learned**

1. 使用 GUI 設定 directive 時，有時會發生沒有成功寫入 tcl 檔的情況
2. 學習如何使用 AXI master 跟 AXI stream 及設定 DMA 來傳送資料

- **Screen dump**

FIRN11MAXI

- Performance

```
================================================================
== Performance Estimates
================================================================
+ Timing:
    * Summary:
    +--------+----------+----------+------------+
    |  Clock |  Target  | Estimated| Uncertainty|
    +--------+----------+----------+------------+
    |ap_clk  |  10.00 ns|  7.300 ns|     2.70 ns|
    +--------+----------+----------+------------+

+ Latency:
    * Summary:
    +---------+---------+----------+----------+-----+-----+---------+
    |  Latency (cycles) |  Latency (absolute) |  Interval | Pipeline|
    |   min   |   max   |    min   |    max   | min | max |   Type  |
    +---------+---------+----------+----------+-----+-----+---------+
    |        ?|        ?|         ?|         ?|    ?|    ?|       no|
    +---------+---------+----------+----------+-----+-----+---------+

    + Detail:
        * Instance:
        +-----------------------------------------------+--------------------------------+---------+---------+----------+----------+-----+-----+---------+
        |                                               |                                |  Latency (cycles) |  Latency (absolute) |  Interval | Pipeline|
        |                   Instance                    |             Module             |   min   |   max   |    min   |    max   | min | max |   Type  |
        +-----------------------------------------------+--------------------------------+---------+---------+----------+----------+-----+-----+---------+
        |grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_242     |fir_n11_maxi_Pipeline_XFER_LOOP |        ?|        ?|         ?|         ?|    ?|    ?|       no|
        +-----------------------------------------------+--------------------------------+---------+---------+----------+----------+-----+-----+---------+

        * Loop:
        N/A
```

- Utilization

```
================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+-----+--------+-------+-----+
|       Name      | BRAM_18K| DSP |   FF   |  LUT  | URAM|
+-----------------+---------+-----+--------+-------+-----+
|DSP              |        -|    -|       -|      -|    -|
|Expression       |        -|    -|       0|     40|    -|
|FIFO             |        -|    -|       -|      -|    -|
|Instance         |        0|   33|    3806|   2838|    -|
|Memory           |        -|    -|       -|      -|    -|
|Multiplexer      |        -|    -|       -|    175|    -|
|Register         |        -|    -|     650|      -|    -|
+-----------------+---------+-----+--------+-------+-----+
|Total            |        0|   33|    4456|   3053|    0|
+-----------------+---------+-----+--------+-------+-----+
|Available        |      280|  220|  106400|  53200|    0|
+-----------------+---------+-----+--------+-------+-----+
|Utilization (%)  |        0|   15|       4|      5|    0|
+-----------------+---------+-----+--------+-------+-----+

+ Detail:
    * Instance:
    +-----------------------------------------------+--------------------------------+---------+-----+------+------+-----+
    |                    Instance                   |             Module             | BRAM_18K| DSP |  FF  |  LUT | URAM|
    +-----------------------------------------------+--------------------------------+---------+-----+------+------+-----+
    |control_s_axi_U                                |control_s_axi                   |        0|    0|   294|   436|    0|
    |grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_242     |fir_n11_maxi_Pipeline_XFER_LOOP |        0|   33|  2794|  1084|    0|
    |gmem_m_axi_U                                   |gmem_m_axi                      |        0|    0|   718|  1318|    0|
    +-----------------------------------------------+--------------------------------+---------+-----+------+------+-----+
    |Total                                          |                                |        0|   33|  3806|  2838|    0|
    +-----------------------------------------------+--------------------------------+---------+-----+------+------+-----+

    * DSP:
    N/A

    * Memory:
    N/A

    * FIFO:
```

```
+-----------------------------------------+-------------------------------+--------+---+-----+------+-----+
|Total                                    |                               |       0|  33|  3806|  2838|    0|
+-----------------------------------------+-------------------------------+--------+---+-----+------+-----+

* DSP:
N/A

* Memory:
N/A

* FIFO:
N/A

* Expression:
+----------------------+----------+---+---+----+------------+------------+
|    Variable Name     | Operation| DSP| FF| LUT| Bitwidth P0| Bitwidth P1|
+----------------------+----------+---+---+----+------------+------------+
|add_ln16_fu_289_p2    |         +|   0|  0|  40|          33|           2|
+----------------------+----------+---+---+----+------------+------------+
|Total                 |          |   0|  0|  40|          33|           2|
+----------------------+----------+---+---+----+------------+------------+

* Multiplexer:
+------------------+----+------------+----+------------+
|       Name       | LUT| Input Size| Bits| Total Bits|
+------------------+----+------------+----+------------+
|an32Coef_address0 |  65|          12|    4|          48|
|ap_NS_fsm         |  65|          15|    1|          15|
|gmem_ARVALID      |   9|           2|    1|           2|
|gmem_AWVALID      |   9|           2|    1|           2|
|gmem_BREADY       |   9|           2|    1|           2|
|gmem_RREADY       |   9|           2|    1|           2|
|gmem_WVALID       |   9|           2|    1|           2|
+------------------+----+------------+----+------------+
|Total             | 175|          37|   10|          73|
+------------------+----+------------+----+------------+

* Register:
+-------------------------------------------------------+---+---+----+-----------+
|                          Name                         | FF | LUT| Bits| Const Bits|
+-------------------------------------------------------+---+---+----+-----------+
```

* Register:

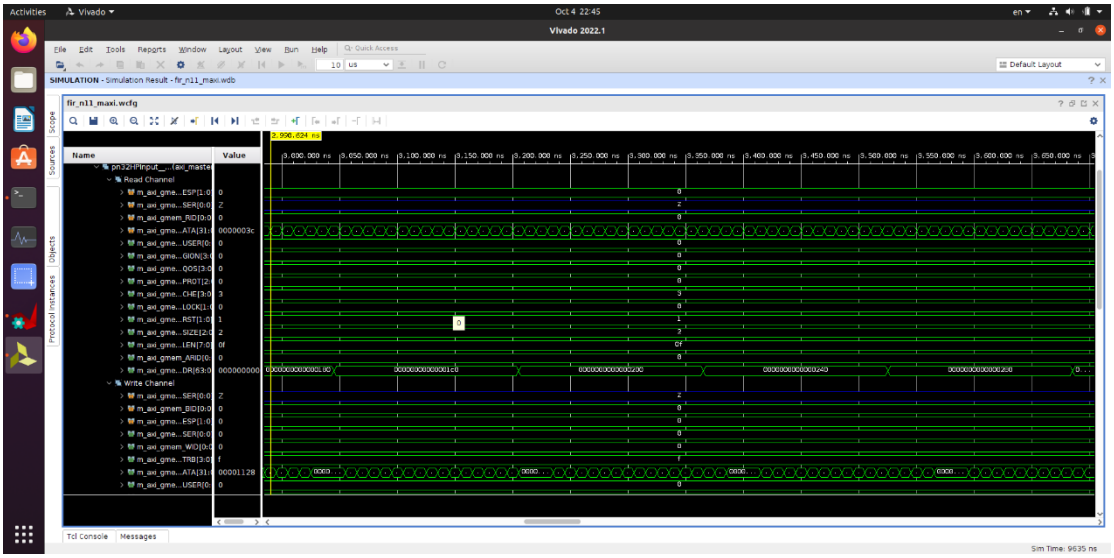
Name	FF	LUT	Bits	Const Bits
an32Coef_load_10_reg_446	32	0	32	0
an32Coef_load_1_reg_340	32	0	32	0
an32Coef_load_2_reg_350	32	0	32	0
an32Coef_load_3_reg_360	32	0	32	0
an32Coef_load_4_reg_370	32	0	32	0
an32Coef_load_5_reg_380	32	0	32	0
an32Coef_load_6_reg_390	32	0	32	0
an32Coef_load_7_reg_400	32	0	32	0
an32Coef_load_8_reg_410	32	0	32	0
an32Coef_load_9_reg_420	32	0	32	0
an32Coef_load_reg_330	32	0	32	0
ap_CS_fsm	14	0	14	0
grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_242_ap_start_reg	1	0	1	0
lshr_ln16_cast_reg_440	31	0	31	0
pn32HPInput_read_reg_435	64	0	64	0
pn32HPOutput_read_reg_430	64	0	64	0
trunc_ln18_1_reg_451	62	0	62	0
trunc_ln30_1_reg_456	62	0	62	0
Total	650	0	650	0

- Interface

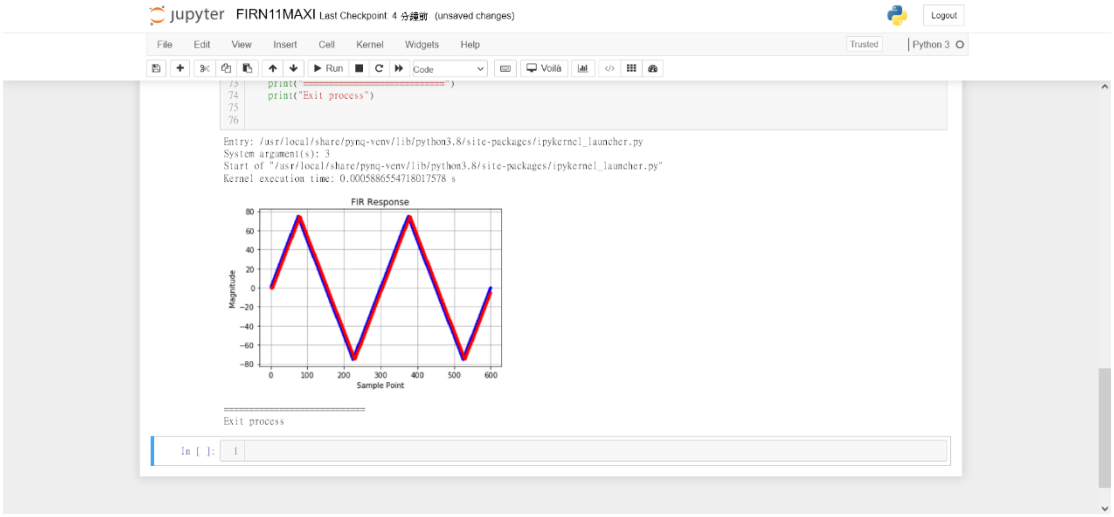
```
================================================================
== Interface
================================================================
* Summary:
```

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
s_axi_control_AWVALID	in	1	s_axi	control	array
s_axi_control_AWREADY	out	1	s_axi	control	array
s_axi_control_AWADDR	in	7	s_axi	control	array
s_axi_control_WVALID	in	1	s_axi	control	array
s_axi_control_WREADY	out	1	s_axi	control	array
s_axi_control_WDATA	in	32	s_axi	control	array
s_axi_control_WSTRB	in	4	s_axi	control	array
s_axi_control_ARVALID	in	1	s_axi	control	array
s_axi_control_ARREADY	out	1	s_axi	control	array
s_axi_control_ARADDR	in	7	s_axi	control	array
s_axi_control_RVALID	out	1	s_axi	control	array
s_axi_control_RREADY	in	1	s_axi	control	array
s_axi_control_RDATA	out	32	s_axi	control	array
s_axi_control_RRESP	out	2	s_axi	control	array
s_axi_control_BVALID	out	1	s_axi	control	array
s_axi_control_BREADY	in	1	s_axi	control	array
s_axi_control_BRESP	out	2	s_axi	control	array
ap_clk	in	1	ap_ctrl_hs	fir_n11_maxi	return value
ap_rst_n	in	1	ap_ctrl_hs	fir_n11_maxi	return value
interrupt	out	1	ap_ctrl_hs	fir_n11_maxi	return value
m_axi_gmem_AWVALID	out	1	m_axi	gmem	pointer
m_axi_gmem_AWREADY	in	1	m_axi	gmem	pointer
m_axi_gmem_AWADDR	out	64	m_axi	gmem	pointer
m_axi_gmem_AWID	out	1	m_axi	gmem	pointer
m_axi_gmem_AWLEN	out	8	m_axi	gmem	pointer
m_axi_gmem_AWSIZE	out	3	m_axi	gmem	pointer
m_axi_gmem_AWBURST	out	2	m_axi	gmem	pointer
m_axi_gmem_AWLOCK	out	2	m_axi	gmem	pointer
m_axi_gmem_AWCACHE	out	4	m_axi	gmem	pointer
m_axi_gmem_AWPROT	out	3	m_axi	gmem	pointer
m_axi_gmem_AWQOS	out	4	m_axi	gmem	pointer
m_axi_gmem_AWREGION	out	4	m_axi	gmem	pointer
m_axi_gmem_AWUSER	out	1	m_axi	gmem	pointer
m_axi_gmem_WVALID	out	1	m_axi	gmem	pointer
m_axi_gmem_WREADY	in	1	m_axi	gmem	pointer
m_axi_gmem_WDATA	out	32	m_axi	gmem	pointer
m_axi_gmem_WSTRB	out	4	m_axi	gmem	pointer
m_axi_gmem_WLAST	out	1	m_axi	gmem	pointer
m_axi_gmem_WID	out	1	m_axi	gmem	pointer
m_axi_gmem_WUSER	out	1	m_axi	gmem	pointer
m_axi_gmem_ARVALID	out	1	m_axi	gmem	pointer
m_axi_gmem_ARREADY	in	1	m_axi	gmem	pointer
m_axi_gmem_ARADDR	out	64	m_axi	gmem	pointer
m_axi_gmem_ARID	out	1	m_axi	gmem	pointer
m_axi_gmem_ARLEN	out	8	m_axi	gmem	pointer
m_axi_gmem_ARSIZE	out	3	m_axi	gmem	pointer
m_axi_gmem_ARBURST	out	2	m_axi	gmem	pointer
m_axi_gmem_ARLOCK	out	2	m_axi	gmem	pointer
m_axi_gmem_ARCACHE	out	4	m_axi	gmem	pointer
m_axi_gmem_ARPROT	out	3	m_axi	gmem	pointer
m_axi_gmem_ARQOS	out	4	m_axi	gmem	pointer
m_axi_gmem_ARREGION	out	4	m_axi	gmem	pointer
m_axi_gmem_ARUSER	out	1	m_axi	gmem	pointer
m_axi_gmem_RVALID	in	1	m_axi	gmem	pointer
m_axi_gmem_RREADY	out	1	m_axi	gmem	pointer
m_axi_gmem_RDATA	in	32	m_axi	gmem	pointer
m_axi_gmem_RLAST	in	1	m_axi	gmem	pointer
m_axi_gmem_RID	in	1	m_axi	gmem	pointer
m_axi_gmem_RUSER	in	1	m_axi	gmem	pointer
m_axi_gmem_RRESP	in	2	m_axi	gmem	pointer
m_axi_gmem_BVALID	in	1	m_axi	gmem	pointer
m_axi_gmem_BREADY	out	1	m_axi	gmem	pointer
m_axi_gmem_BRESP	in	2	m_axi	gmem	pointer
m_axi_gmem_BID	in	1	m_axi	gmem	pointer
m_axi_gmem_BUSER	in	1	m_axi	gmem	pointer

- Co-simulation transcript/waveform



- Jupyter Notebook execution results



FIRN11Stream

- Performance

```
================================================================
== Performance Estimates
================================================================
+ Timing:
    * Summary:
    +--------+----------+----------+------------+
    |  Clock |  Target  | Estimated| Uncertainty|
    +--------+----------+----------+------------+
    |ap_clk  |  10.00 ns|  6.923 ns|     2.70 ns|
    +--------+----------+----------+------------+

+ Latency:
    * Summary:
    +---------+---------+----------+----------+-----+-----+---------+
    |  Latency (cycles) |  Latency (absolute) |  Interval | Pipeline|
    |   min   |   max   |    min   |    max   | min | max |   Type  |
    +---------+---------+----------+----------+-----+-----+---------+
    |        ?|        ?|         ?|         ?|    ?|    ?|       no|
    +---------+---------+----------+----------+-----+-----+---------+

    + Detail:
        * Instance:
        +-----------------------------------------------+-------------------------------+---------+---------+----------+----------+-----+-----+---------+
        |                                               |                               |  Latency (cycles) |  Latency (absolute) |  Interval | Pipeline|
        |                Instance                       |             Module            |   min   |   max   |    min   |    max   | min | max |   Type  |
        +-----------------------------------------------+-------------------------------+---------+---------+----------+----------+-----+-----+---------+
        |grp_fir_n11_strm_Pipeline_XPER_LOOP_fu_112     |fir_n11_strm_Pipeline_XPER_LOOP|        ?|        ?|         ?|         ?|    ?|    ?|       no|
        +-----------------------------------------------+-------------------------------+---------+---------+----------+----------+-----+-----+---------+

        * Loop:
        N/A
```

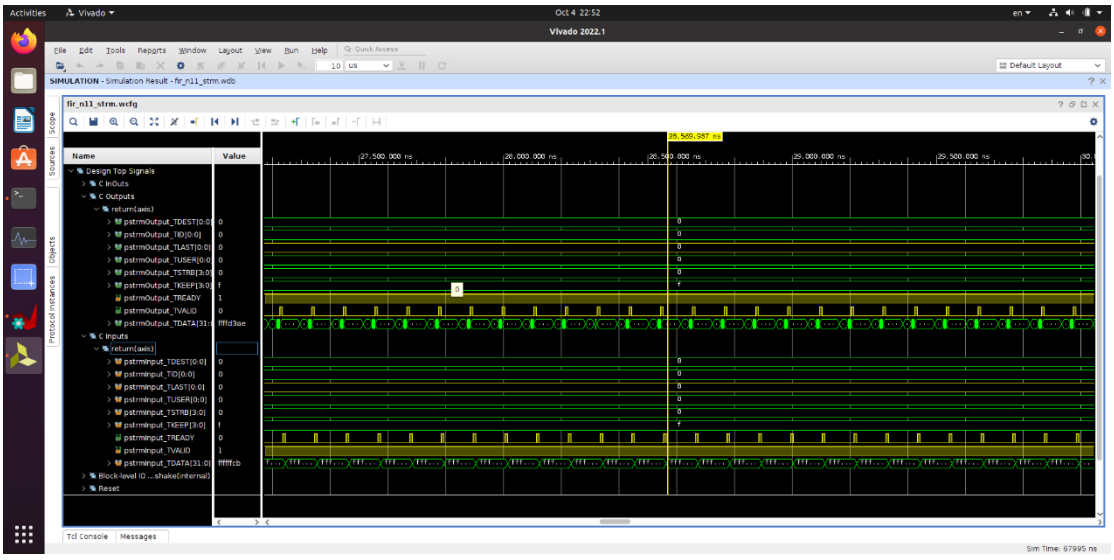
- Utilization

```
================================================================
== Utilization Estimates
================================================================
* Summary:
+---------------+---------+-----+--------+-------+-----+
|      Name     | BRAM_18K| DSP |   FF   |  LUT  | URAM|
+---------------+---------+-----+--------+-------+-----+
|DSP            |        -|    -|       -|      -|    -|
|Expression     |        -|    -|       0|     42|    -|
|FIFO           |        -|    -|       -|      -|    -|
|Instance       |        0|   33|    2988|   1333|    -|
|Memory         |        -|    -|       -|      -|    -|
|Multiplexer    |        -|    -|       -|     34|    -|
|Register       |        -|    -|      36|      -|    -|
+---------------+---------+-----+--------+-------+-----+
|Total          |        0|   33|    3024|   1409|    0|
+---------------+---------+-----+--------+-------+-----+
|Available      |      280|  220|  106400|  53200|    0|
+---------------+---------+-----+--------+-------+-----+
|Utilization (%)|        0|   15|       2|      2|    0|
+---------------+---------+-----+--------+-------+-----+

+ Detail:
    * Instance:
    +-----------------------------------------+-------------------------------+---------+---+----+-----+-----+
    |                 Instance                |             Module            | BRAM_18K| DSP|  FF  |  LUT | URAM|
    +-----------------------------------------+-------------------------------+---------+---+----+-----+-----+
    |control_s_axi_U                          |control_s_axi                  |        0|  0|   154|   180|    0|
    |grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112  |fir_n11_strm_Pipeline_XFER_LOOP  |        0|  33|  2834|  1153|    0|
    +-----------------------------------------+-------------------------------+---------+---+----+-----+-----+
    |Total                                    |                               |        0|  33|  2988|  1333|    0|
    +-----------------------------------------+-------------------------------+---------+---+----+-----+-----+

    * DSP:
    N/A

    * Memory:
    N/A

    * FIFO:
    N/A

    * Expression:
    +-----------------------------------------------------------------+----------+---+---+----+------------+------------+
    |                          Variable Name                          | Operation| DSP| FF| LUT| Bitwidth P0| Bitwidth P1|
    +-----------------------------------------------------------------+----------+---+---+----+------------+------------+
    |ret_V_fu_171_p2                                                  |         +|   0|  0|  40|          33|           2|
    |grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112_pstrmOutput_TREADY  |       and|   0|  0|   2|           1|           1|
    +-----------------------------------------------------------------+----------+---+---+----+------------+------------+
    |Total                                                            |          |   0|  0|  42|          34|           3|
    +-----------------------------------------------------------------+----------+---+---+----+------------+------------+

    * Multiplexer:
    +-------------------------------+----+-----------+-----+-----------+
    |              Name             | LUT| Input Size| Bits| Total Bits|
    +-------------------------------+----+-----------+-----+-----------+
    |ap_NS_fsm                      |  25|          5|    1|          5|
    |pstrm_TREADY_int_regslice  |   9|          2|    1|          2|
    +-------------------------------+----+-----------+-----+-----------+
    |Total                          |  34|          7|    2|          7|
    +-------------------------------+----+-----------+-----+-----------+

    * Register:
    +-----------------------------------------------------+---+---+----+-----------+
    |                         Name                        | FF| LUT| Bits| Const Bits|
    +-----------------------------------------------------+---+---+----+-----------+
    |ap_CS_fsm                                            |  4|  0|   4|          0|
    |grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112_ap_start_reg |  1|  0|   1|          0|
    |tmp_reg_187                                          | 31|  0|  31|          0|
    +-----------------------------------------------------+---+---+----+-----------+
    |Total                                                | 36|  0|  36|          0|
    +-----------------------------------------------------+---+---+----+-----------+
```

- Interface

```
================================================================
== Interface
================================================================
* Summary:
+-----------------------+-----+-----+------------+---------------------+--------------+
|       RTL Ports       | Dir | Bits|  Protocol  |    Source Object    |    C Type    |
+-----------------------+-----+-----+------------+---------------------+--------------+
|s_axi_control_AWVALID  |   in|    1|       s_axi|              control|         array|
|s_axi_control_AWREADY  |  out|    1|       s_axi|              control|         array|
|s_axi_control_AWADDR   |   in|    7|       s_axi|              control|         array|
|s_axi_control_WVALID   |   in|    1|       s_axi|              control|         array|
|s_axi_control_WREADY   |  out|    1|       s_axi|              control|         array|
|s_axi_control_WDATA    |   in|   32|       s_axi|              control|         array|
|s_axi_control_WSTRB    |   in|    4|       s_axi|              control|         array|
|s_axi_control_ARVALID  |   in|    1|       s_axi|              control|         array|
|s_axi_control_ARREADY  |  out|    1|       s_axi|              control|         array|
|s_axi_control_ARADDR   |   in|    7|       s_axi|              control|         array|
|s_axi_control_RVALID   |  out|    1|       s_axi|              control|         array|
|s_axi_control_RREADY   |   in|    1|       s_axi|              control|         array|
|s_axi_control_RDATA    |  out|   32|       s_axi|              control|         array|
|s_axi_control_RRESP    |  out|    2|       s_axi|              control|         array|
|s_axi_control_BVALID   |  out|    1|       s_axi|              control|         array|
|s_axi_control_BREADY   |   in|    1|       s_axi|              control|         array|
|s_axi_control_BRESP    |  out|    2|       s_axi|              control|         array|
|ap_clk                 |   in|    1|  ap_ctrl_hs|       fir_n11_strm|  return value|
|ap_rst_n               |   in|    1|  ap_ctrl_hs|       fir_n11_strm|  return value|
|interrupt              |  out|    1|  ap_ctrl_hs|       fir_n11_strm|  return value|
|pstrmInput_TDATA       |   in|   32|        axis|  pstrmInput_V_data_V|       pointer|
|pstrmInput_TVALID      |   in|    1|        axis|  pstrmInput_V_dest_V|       pointer|
|pstrmInput_TREADY      |  out|    1|        axis|  pstrmInput_V_dest_V|       pointer|
|pstrmInput_TDEST       |   in|    1|        axis|  pstrmInput_V_dest_V|       pointer|
|pstrmInput_TKEEP       |   in|    4|        axis|  pstrmInput_V_keep_V|       pointer|
|pstrmInput_TSTRB       |   in|    4|        axis|  pstrmInput_V_strb_V|       pointer|
|pstrmInput_TUSER       |   in|    1|        axis|  pstrmInput_V_user_V|       pointer|
|pstrmInput_TLAST       |   in|    1|        axis|  pstrmInput_V_last_V|       pointer|
|pstrmInput_TID         |   in|    1|        axis|    pstrmInput_V_id_V|       pointer|
|pstrmOutput_TDATA      |  out|   32|        axis| pstrmOutput_V_data_V|       pointer|
|pstrmOutput_TVALID     |  out|    1|        axis| pstrmOutput_V_dest_V|       pointer|
|pstrmOutput_TREADY     |   in|    1|        axis| pstrmOutput_V_dest_V|       pointer|
|pstrmOutput_TDEST      |  out|    1|        axis| pstrmOutput_V_dest_V|       pointer|
|pstrmOutput_TKEEP      |  out|    4|        axis| pstrmOutput_V_keep_V|       pointer|
|pstrmOutput_TSTRB      |  out|    4|        axis| pstrmOutput_V_strb_V|       pointer|
|pstrmOutput_TUSER      |  out|    1|        axis| pstrmOutput_V_user_V|       pointer|
|pstrmOutput_TLAST      |  out|    1|        axis| pstrmOutput_V_last_V|       pointer|
|pstrmOutput_TID        |  out|    1|        axis|   pstrmOutput_V_id_V|       pointer|
+-----------------------+-----+-----+------------+---------------------+--------------+
```

- Co-simulation transcript/waveform



- Jupyter Notebook execution results

jupyter FIRN11Stream Last Checkpoint: 現秒前 (unsaved changes)

Logout

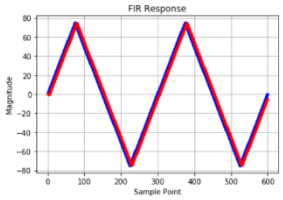
File Edit View Insert Cell Kernel Widgets Help

Trusted Python 3

Run Code Voilà

```
    plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0, 'r.')
else:
    plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0 / m32DCGain, 'r.')
plt.grid(True)
plt.show() # In Jupyter, press Tab + Shift keys to show plot then redo run

print("========================")
print("Exit process")
```

```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py"
Kernel execution time: 0.0016939640045166016 s
```




```
========================
Exit process
```