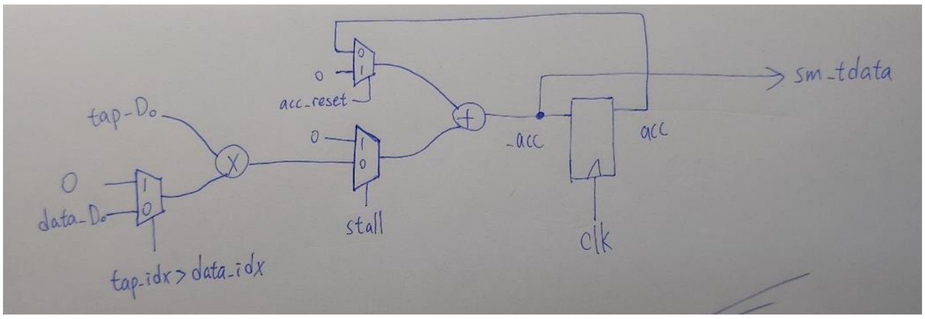
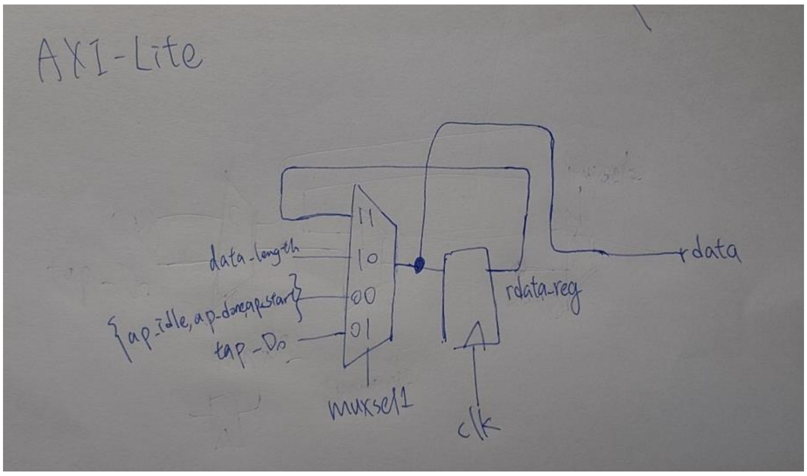
Soc design lab3-fir

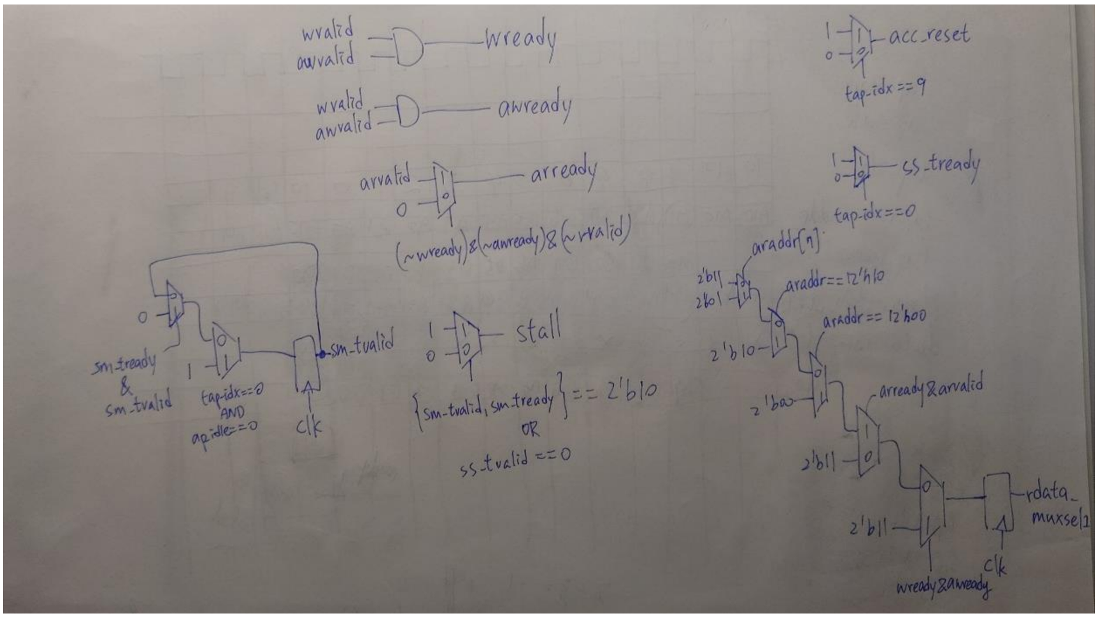
Block Diagram

- **Datapath–dataflow**



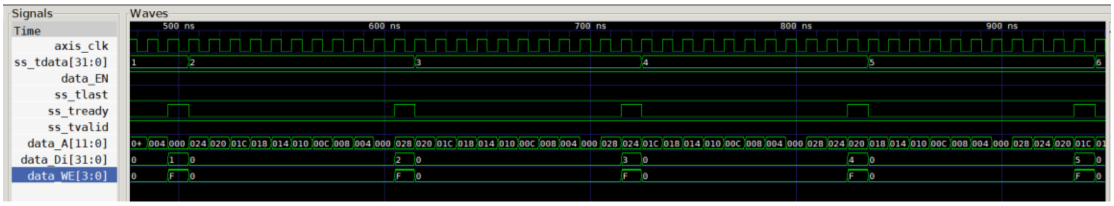


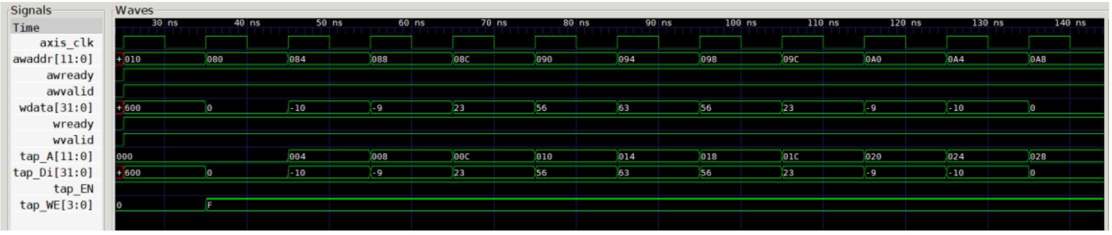
- **Control signals**



Describe operation

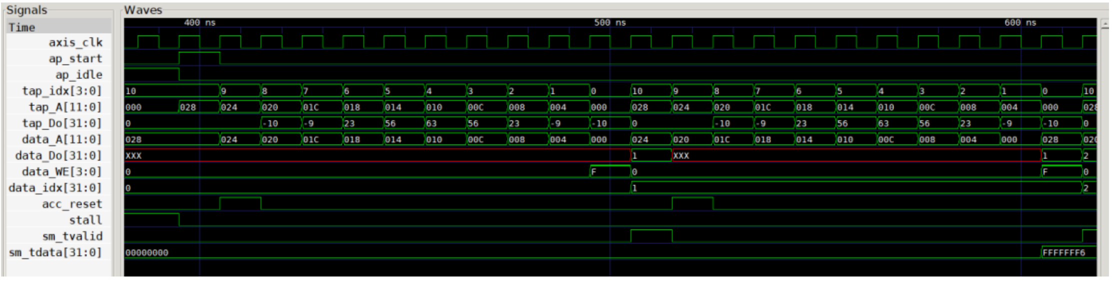
- **How to receive data-in and tap parameters and place into SRAM**





fir 在讀入資料的同時會直接將資料寫入 SRAM

- **How to access shiftram and tapRAM to do computation**



為了能增加 performance，不直接 shift SRAM 裡面的資料，而是移動每次開始讀取 data ram 的位置。而且在需要進行計算的前一個 cycle 就先將所需資料的位置給 SRAM，到下一個 cycle 時，除了對 SRAM 傳來的資料進行計算外，也將下一 cycle 所需資料的位置給 SRAM，如此可以充分利用資源。

- **How each output y is computed.**

計算一個 y 需要 11 個 clock cycle，tap_idx 從 9 到 10。

9: 計算 tap10。開始計算一個新的 y，acc_reset=1，重新累加

8~1: 計算 tap9~2

0: 計算 tap1。讀入一個 input x，並將其寫到 data ram

10: 計算 tap0。輸出 y，sm_tvalid=1

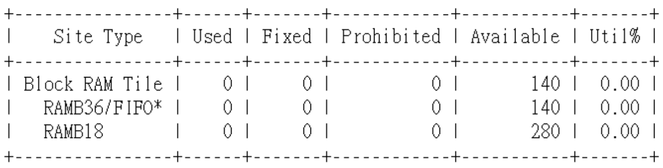
對於前 11 個 y，因為 data ram 中的數值並未經過初始化，tap_idx>data_idx 來判斷要從 data ram 中讀取數值，還是直接用 0 進行計算

- **How ap_done is generated.**

當最後一筆輸出被 fir_tb 接收後將 ap_done 設為 1

Resource usage: including FF, LUT, BRAM

```
+-------------------------+------+-------+------------+-----------+-------+
|        Site Type        | Used | Fixed | Prohibited | Available | Util% |
+-------------------------+------+-------+------------+-----------+-------+
| Slice LUTs*             |  303 |     0 |          0 |     53200 |  0.57 |
|   LUT as Logic          |  303 |     0 |          0 |     53200 |  0.57 |
|   LUT as Memory         |    0 |     0 |          0 |     17400 |  0.00 |
| Slice Registers         |  145 |     0 |          0 |    106400 |  0.14 |
|   Register as Flip Flop |  145 |     0 |          0 |    106400 |  0.14 |
|   Register as Latch     |    0 |     0 |          0 |    106400 |  0.00 |
| F7 Muxes                |    0 |     0 |          0 |     26600 |  0.00 |
| F8 Muxes                |    0 |     0 |          0 |     13300 |  0.00 |
+-------------------------+------+-------+------------+-----------+-------+
```

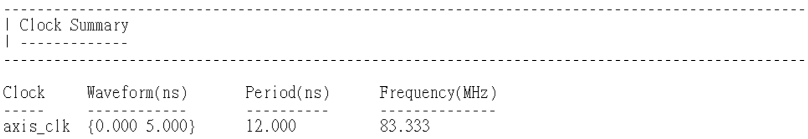


```
+----------------+------+-------+------------+-----------+-------+
|    Site Type   | Used | Fixed | Prohibited | Available | Util% |
+----------------+------+-------+------------+-----------+-------+
| Block RAM Tile |    0 |     0 |          0 |       140 |  0.00 |
|   RAMB36/FIFO* |    0 |     0 |          0 |       140 |  0.00 |
|   RAMB18       |    0 |     0 |          0 |       280 |  0.00 |
+----------------+------+-------+------------+-----------+-------+
```

從合成報告截圖中可以看出此設計並未使用 BRAM

Timing Report

- **Try to synthesize the design with maximum frequency**

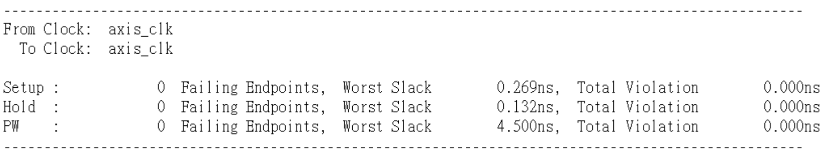


```
------------------------------------------------------------------------------------------------
| Clock Summary
| -------------
------------------------------------------------------------------------------------------------

Clock     Waveform(ns)       Period(ns)      Frequency(MHz)
-----     ------------       ----------      --------------
axis_clk  {0.000 5.000}      12.000          83.333
```

經過測試最短週期設為 12ns

- **Report timing on longest path, slack**



```
----------------------------------------------------------------------------------------------------
From Clock:  axis_clk
  To Clock:  axis_clk

Setup :            0  Failing Endpoints,  Worst Slack        0.269ns,  Total Violation        0.000ns
Hold  :            0  Failing Endpoints,  Worst Slack        0.132ns,  Total Violation        0.000ns
PW    :            0  Failing Endpoints,  Worst Slack        4.500ns,  Total Violation        0.000ns
----------------------------------------------------------------------------------------------------
```

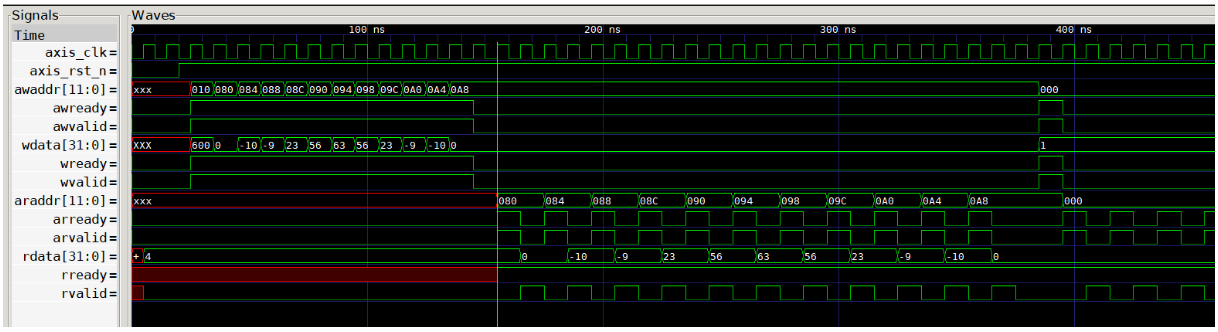
```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             0.269ns  (required time - arrival time)
  Source:                 mul_data_in_sel_reg/C
                            (rising edge-triggered cell FDRE clocked by axis_clk  {rise@0.000ns fall@5.000ns period=12.000ns})
  Destination:            acc_reg[29]/D
                            (rising edge-triggered cell FDRE clocked by axis_clk  {rise@0.000ns fall@5.000ns period=12.000ns})
  Path Group:             axis_clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            12.000ns  (axis_clk rise@12.000ns - axis_clk rise@0.000ns)
  Data Path Delay:        11.626ns  (logic 8.472ns (72.868%)  route 3.154ns (27.132%))
  Logic Levels:           10  (CARRY4=5 DSP48E1=2 LUT2=2 LUT4=1)
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 14.128 - 12.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock axis_clk rise edge)
                                                      0.000     0.000 r  
                                                      0.000     0.000 r  axis_clk (IN)
                         net (fo=0)                   0.000     0.000    axis_clk
                                                                      r  axis_clk_IBUF_inst/I
                         IBUF (Prop_ibuf_I_O)         0.972     0.972 r  axis_clk_IBUF_inst/O
                         net (fo=1, unplaced)         0.800     1.771    axis_clk_IBUF
                                                                      r  axis_clk_IBUF_BUFG_inst/I
                         BUFG (Prop_bufg_I_O)         0.101     1.872 r  axis_clk_IBUF_BUFG_inst/O
                         net (fo=145, unplaced)       0.584     2.456    axis_clk_IBUF_BUFG
                         FDRE                                         r  mul_data_in_sel_reg/C
  -------------------------------------------------------------------    -------------------
                         FDRE (Prop_fdre_C_Q)         0.478     2.934 f  mul_data_in_sel_reg/Q
                         net (fo=32, unplaced)        0.382     3.316    mul_data_in_sel
                                                                      f  acc2__0_i_1/I1
                         LUT2 (Prop_lut2_I1_O)        0.295     3.611 r  acc2__0_i_1/O
                         net (fo=1, unplaced)         0.800     4.411    acc3[16]
                                                                      r  acc2__0/A[16]
                         DSP48E1 (Prop_dsp48e1_A[16]_PCOUT[47])
                                                      4.036     8.447 r  acc2__0/PCOUT[47]
                         net (fo=1, unplaced)         0.055     8.502    acc2__0_n_106
                                                                      r  acc2__1/PCIN[47]
                         DSP48E1 (Prop_dsp48e1_PCIN[47]_P[0])
                                                      1.518    10.020 r  acc2__1/P[0]
                         net (fo=2, unplaced)         0.800    10.820    acc2__1_n_105
                                                                      r  sm_tdata_OBUF[19]_inst_i_13/I0
                         LUT2 (Prop_lut2_I0_O)        0.124    10.944 r  sm_tdata_OBUF[19]_inst_i_13/O
                         net (fo=1, unplaced)         0.000    10.944    sm_tdata_OBUF[19]_inst_i_13_n_0
                                                                      r  sm_tdata_OBUF[19]_inst_i_10/S[1]
                         CARRY4 (Prop_carry4_S[1]_CO[3])
                                                      0.533    11.477 r  sm_tdata_OBUF[19]_inst_i_10/CO[3]
                         net (fo=1, unplaced)         0.009    11.486    sm_tdata_OBUF[19]_inst_i_10_n_0
                                                                      r  sm_tdata_OBUF[23]_inst_i_10/CI
                         CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117    11.603 r  sm_tdata_OBUF[23]_inst_i_10/CO[3]
                         net (fo=1, unplaced)         0.000    11.603    sm_tdata_OBUF[23]_inst_i_10_n_0
                                                                      r  sm_tdata_OBUF[27]_inst_i_10/CI
                         CARRY4 (Prop_carry4_CI_O[3])
                                                      0.331    11.934 r  sm_tdata_OBUF[27]_inst_i_10/O[3]
                         net (fo=3, unplaced)         0.636    12.570    sm_tdata_OBUF[27]_inst_i_10_n_4
                                                                      r  acc[24]_i_2/I0
                         LUT4 (Prop_lut4_I0_O)        0.307    12.877 r  acc[24]_i_2/O
                         net (fo=1, unplaced)         0.473    13.350    in[27]
                                                                      r  acc_reg[24]_i_1/DI[3]
                         CARRY4 (Prop_carry4_DI[3]_CO[3])
                                                      0.396    13.746 r  acc_reg[24]_i_1/CO[3]
                         net (fo=1, unplaced)         0.000    13.746    acc_reg[24]_i_1_n_0
                                                                      r  acc_reg[28]_i_1/CI
                         CARRY4 (Prop_carry4_CI_O[1])
                                                      0.337    14.083 r  acc_reg[28]_i_1/O[1]
                         net (fo=1, unplaced)         0.000    14.083    acc_reg[28]_i_1_n_6
                         FDRE                                         r  acc_reg[29]/D
  -------------------------------------------------------------------    -------------------

                         (clock axis_clk rise edge)
                                                     12.000    12.000 r  
                                                      0.000    12.000 r  axis_clk (IN)
                         net (fo=0)                   0.000    12.000    axis_clk
                                                                      r  axis_clk_IBUF_inst/I
                         IBUF (Prop_ibuf_I_O)         0.838    12.838 r  axis_clk_IBUF_inst/O
                         net (fo=1, unplaced)         0.760    13.598    axis_clk_IBUF
                                                                      r  axis_clk_IBUF_BUFG_inst/I
                         BUFG (Prop_bufg_I_O)         0.091    13.689 r  axis_clk_IBUF_BUFG_inst/O
                         net (fo=145, unplaced)       0.439    14.128    axis_clk_IBUF_BUFG
                         FDRE                                         r  acc_reg[29]/C
                         clock pessimism              0.184    14.311    
                         clock uncertainty           -0.035    14.276    
                         FDRE (Setup_fdre_C_D)        0.076    14.352    acc_reg[29]
  -------------------------------------------------------------------
                         required time                         14.352    
                         arrival time                         -14.083    
  -------------------------------------------------------------------
                         slack                                  0.269    
```

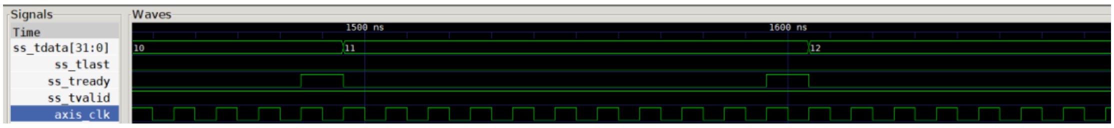
Simulation Waveform:

- **Coefficient program, and read back**



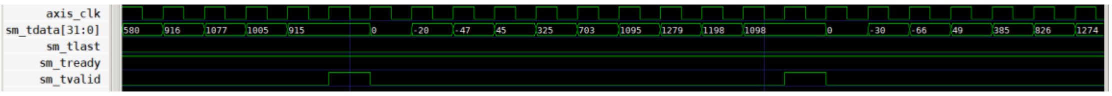
從波形圖可以看到先對 fir 設定 data length 跟 coefficient，然後再把 coefficient 讀出來。接著 program ap_start，fir 開始計算之後 fir_tb 會持續 polling ap_done。

- **Data-in stream-in**



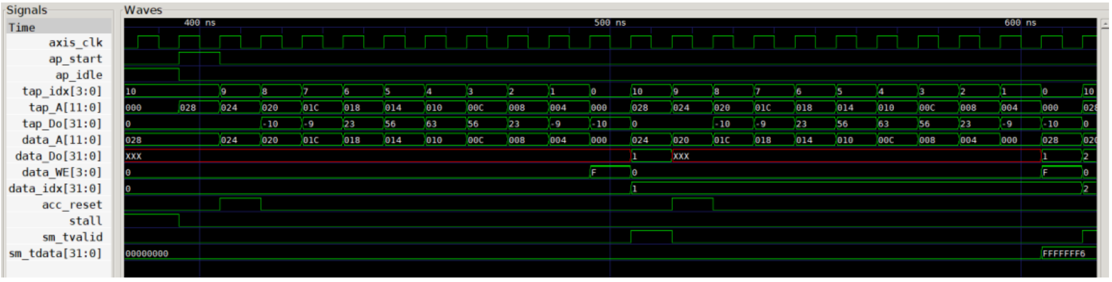
可以看到 fir 每 11 個週期會讀入 1 筆資料

- **Data-out stream-out**



可以看到 fir 每 11 個週期會輸出 1 筆資料

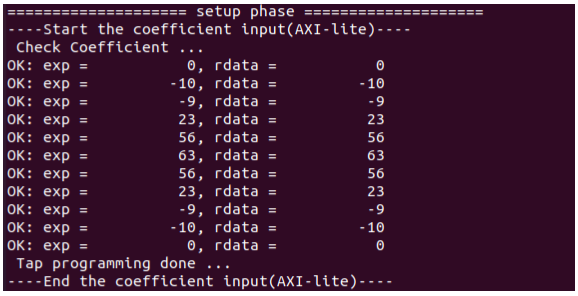
- **RAM access control**



- **FSM**

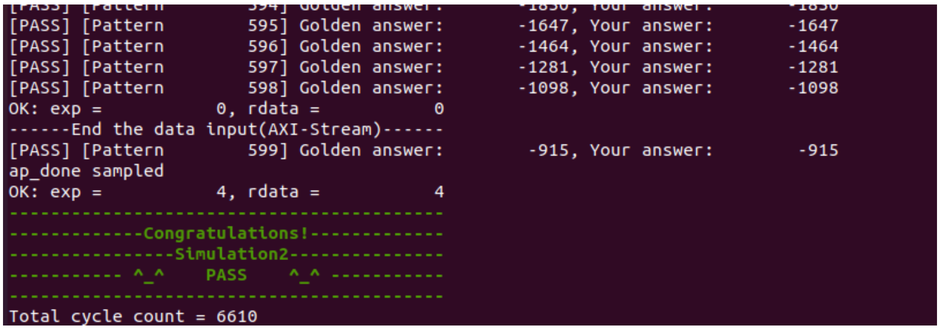
無 FSM

Simulation result



```
=================== setup phase ===================
----Start the coefficient input(AXI-lite)----
 Check Coefficient ...
OK: exp =          0, rdata =          0
OK: exp =        -10, rdata =        -10
OK: exp =         -9, rdata =         -9
OK: exp =         23, rdata =         23
OK: exp =         56, rdata =         56
OK: exp =         63, rdata =         63
OK: exp =         56, rdata =         56
OK: exp =         23, rdata =         23
OK: exp =         -9, rdata =         -9
OK: exp =        -10, rdata =        -10
OK: exp =          0, rdata =          0
 Tap programming done ...
----End the coefficient input(AXI-lite)----
```

所有係數都正確



```
[PASS] [Pattern        594] Golden answer:       -1830, Your answer:       -1830
[PASS] [Pattern        595] Golden answer:       -1647, Your answer:       -1647
[PASS] [Pattern        596] Golden answer:       -1464, Your answer:       -1464
[PASS] [Pattern        597] Golden answer:       -1281, Your answer:       -1281
[PASS] [Pattern        598] Golden answer:       -1098, Your answer:       -1098
OK: exp =          0, rdata =          0
------End the data input(AXI-Stream)------
[PASS] [Pattern        599] Golden answer:        -915, Your answer:        -915
ap_done sampled
OK: exp =          4, rdata =          4
------------------------------------------
-------------Congratulations!-------------
----------------Simulation2---------------
---------- ^_^    PASS    ^_^ ----------
------------------------------------------
Total cycle count = 6610
```

所有 output 跟 golden 相同

計算 600 筆資料共花費 6610 個 clock cycle