phyCORE – A5D2x

Hardware Manual

Document No. : RB-HWSM-001-A0

Edition – April, 2019

A Product Of Rugged Board – An open source Hardware Platform

Revision History

Date	Change Note	Revision No.
12 April 2019	Beta Release	001-A0

Contents

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Conventions, Abbreviations and Acronyms

This hardware manual describes the phyCore-A5D2x, the following is referred to as Industrial ruggedBOARD. The manual specifies the Industrial ruggedBOARD's design and function. Precise specifications for the Texas Instruments A5D2x microcontrollers can be found in the Texas Instrument's A5D2x Data Sheet and Technical Reference Manual.

SIP	System-In-Package
SOM	System On Module
DDR2-SDRAM	Double Data Rate 2 Synchronous Dynamic Random-Access Memory
DSC	Direct Solder Connection
ESD	Electrostatic discharge
Mbit	Megabit
EMI/EMC	Electromagnetic Interference/Electromagnetic Compatibility
DDR	Double Data Rate
BGA	Ball Grid Array
RTC	Real-Time Clock
USB	Universal Serial Bus
TFT-LCD	Thin Film Transistor - Liquid Crystal Display.
ADC	Analog-to-Digital Converter
PWM	Pulse width Modulation
QSPI	Queued Serial Peripheral Interface
UART	universal asynchronous receiver-transmitter
IIC	Inter-Integrated Circuit
eMMC	embedded Multi-Media Controller"
PCB	Printed Circuit Board
PMIC	Power Management IC
POR	Power On reset
GPIO	General Purpose Input/output

Note: The BSP delivered with the phyCORE-A5D2x usually includes drivers and/or software for controlling all components such as interfaces, memory, etc. Therefore, programming close to hardware at register level is not necessary in most cases. For this reason, this manual contains no detailed description of the controller's registers, or information relevant for software development. Please refer to the A5D2x *Reference Manual*, if such information need to connect customer designed applications.

Ordering Information

The part numbering of the phyCORE-A5D2x has the following structure:

CHECK AND ORDER ONLINE!!

www.ruggedboard.com

Product Specific Information and Technical Support

In order to receive product specific information on changes and updates in the best way also in the future, we recommend to register at:

http://www.ruggedboard.com/ or
https://ruggedboard.wixsite.com/ruggedboard/forum

Contact Information	
Address	**PHYTEC Embedded Pvt. Ltd.** **27th Main, HSR Layout, Bengaluru 560102**
Phone Number	**+91-9741652770**
E-Mail	**info@ruggedboard.com**
Technical Support	**https://ruggedboard.wixsite.com/rugged-board/forum**
Website	**www.ruggedboard.com**

Assembly options include choice of Controller; RAM (Size/Type); Size of NOR Flash, etc.; Interfaces available; Vanishing; Temperature Range; and other features. Please contact our sales team to get more information on the ordering options available.

Declaration of Electro Magnetic Conformity of the ruggedBOARD [To Be Decided]

phyCORE-A5D2x: RuggedBOARD System on Module (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution!

RuggedBOARD products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products.

RuggedBOARD products fulfil the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Note:

Implementation of RuggedBOARD into target devices, as well as user modifications and extensions of RuggedBOARD products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

Products EMI/EMC standards test Specifications and qualified for CE

- IEC/EN 61000-4-6 (RE conducted susceptibility test) : 1G to 3G
- IEC/EN 61000-4-2 (Electro Static Discharge immunity test)
- IEC/EN 61000-4--5 (Surge immunity test)
- IEC /EN** Vibration Test (Shockproof with Multiple drops from 5' (1.5 m) (TBD)

ESD Warning:

Electronic components and circuits are sensitive to Electrostatic Discharge (ESD). When handling any circuit board assemblies including Pico Computer carrier assemblies, it is recommended that ESD safety precautions be observed. ESD safe best practices include, but are not limited to:

- Leaving circuit boards in their antistatic packaging until they are ready to be installed.
- Using a grounded wrist strap when handling circuit boards, at a minimum you should touch a grounded metal object to dissipate any static charge that may be present on you.
- Only handling circuit boards in ESD safe areas, which may include ESD floor and table mats, wrist strap stations and ESD safe lab coats.
- Avoiding handling circuit boards in carpeted areas.
- Try to handle the board by the edges, avoiding contact with components

Power Supply Warning:

Hardware Power Supply Limitation: Powering the board with voltages higher than **3.3V ± 5%** may damage the module. We recommend Supply voltage to SOM module from Carrier Board is **3.3V ± 5%.**

In addition, for proper operation of the module into the target application also requires connecting all GND pins common.

1 Introduction

PhyCORE-A5D2x-SOM is a compact form-factor multi-layer (6-layer PCB Board) with 35x35mm dimension with 0.8mm Pitch with Edge Cartelization/ Edge Plated Holes based on the high-performance SAMA5D2 SIP series ultra-low-power 289 Pin BGA Module.

Fig 1

PhyCORE-A5D2x-SOM available in three different variants with same footprint pin-to-pin compatibility;

SOM Variants	A5D2x-SOM-"**Premium**"	A5D2x-SOM- "**Professional**"	A5D2x-SOM-"**Standard**"
SIP Module	ATSAMA5D27C-D5M-CU	ATSAMA5D27C-D1G-CU	ATSAMA5D28C-D1G-CU
Architecture	ARM Cortex-A5 CPU	ARM Cortex-A5 CPU	ARM Cortex-A5 CPU
Clock Frequency	500 MHz	500 MHz	500 MHz
DDR2-SDRAM (Part of SIP)	512Mbit (64MByte)	1Gbit (128MByte)	1Gbit (128MByte)
Flash Memory (NOR Type 32Mbit or 64Mbit)	SST26VF032B-104I/SM or SST26VF064BT-104I/SM	SST26VF064BT-104I/SM	SST26VF064BT-104I/SM
EEPROM memory with EUI-48™ Node Identity	24AA02E48T-I/OT	24AA02E48T-I/OT	24AA02E48T-I/OT
PMIC IC	MIC2800-G1JJYML	MIC2800-G1JJYML	MIC2800-G1JJYML
Ethernet PHY	KSZ8081RNAIA-TR	KSZ8081RNAIA-TR	KSZ8081RNAIA-TR
Operating voltage:	**3.3V ± 5%**	**3.3V ± 5%**	**3.3V ± 5%**
Temperature Grade /Range	Industrial Grade (-40°C ~ 85°C)	Industrial Grade (-40°C ~ 85°C)	- Industrial Grade (-40°C ~ 85°C)
Board thickness	1.2mm, Standard FR4	1.2mm, Standard FR4	1.2mm, Standard FR4
Package	QFN 160 Pins + 20 EPAD (GND): :Half Edge Plated Holes	QFN 160 Pins + 20 EPAD (GND): :Half Edge Plated Holes	QFN 160 Pins + 20 EPAD (GND): :Half Edge Plated Holes
Module Pitch	0.8mm Pitch	0.8mm Pitch	0.8mm Pitch
Dimension	35x35mm QFN, DSC	35x35mm QFN, DSC	35x35mm QFN, DSC
Variant Code	PhyCORE-PICM-A0_001	PhyCORE-PICM-A0_002	PhyCORE-PICM-A0_002

Table 1

The **PhyCORE-A5D2x-SOM** offers an extensive peripheral set, including High-speed USB Host and Device, HSIC Interface, 10Base-T/100Base-TX Ethernet Interface, system control and up to 100+ I/O's featuring with 3.3V IO level:

- Up to 4 UARTS
- Up to 4 Flexcoms
- Up to 6 Capacitive Touch lines for up to 9 touch buttons
- Up to 4 ADC Inputs
- Up to 2 CAN
- Up to 7 Tamper Pins
- Serial Interfaces such as SPI, TWI, QSPI, SSC and I²S
- SD/MMC, eMMC, SDIO Interfaces
- Up to 24-bit LCD RGB Interface
- CMOS Camera Interface
- Mono PDMIC and Full-Bridge Class-D Stereo
- Up to 6 Capacitive Touch Lines

Note:

Each I/O of the **PhyCORE-A5D2x-SOM** is configurable, as either a general-purpose I/O line only, or as an I/O line multiplexed with up to *six peripheral I/O's*. As the multiplexing is hardware defined, the hardware designer and programmer must carefully determine the configuration of the PIO Controllers required by their application.

1.1 PhyCORE- A5D2x SOM Architecture

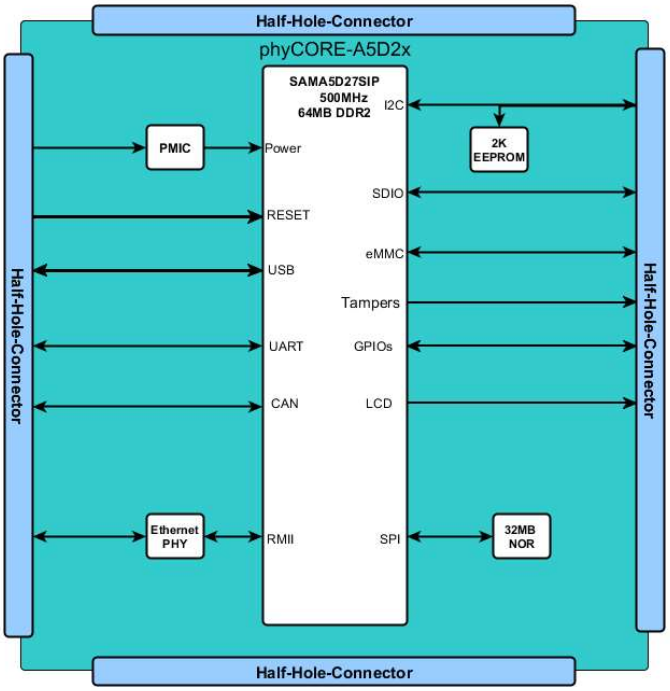


Fig 2

1.2 PhyCORE- A5D2x Components Placement Diagram

(Assembly Top with Silk)

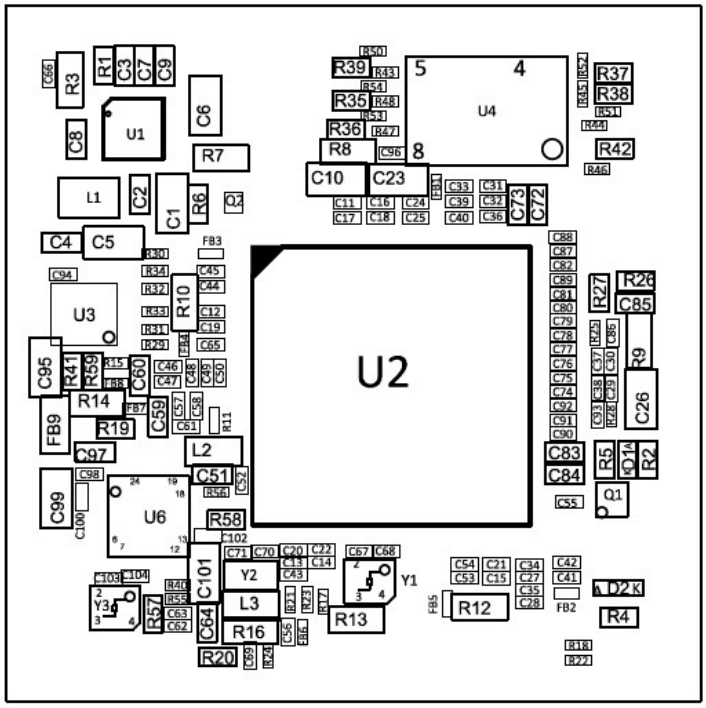


Fig 3

1.3 PhyCORE_A5D2x SOM QFN Package Pin Outs:

The following table describes the PhyCORE_A5D2x SOM QFN pin-out details with IO 3.3V Voltage levels.

Please note that all module connections are not to exceed their expressed maximum voltage or current.

Important:

Microchip SAMA5D2 SIP devices are not pin-to-pin compatible with SAMA5D2 devices

1.3.1 PhyCORE_A5D2x Port –A "PIO" 3.3V Levels

Pin#	PIO	Power Rail	PIO Feature	Type	SIP-289-BGA
67	PA00	VDDSDMMC	SDMMC0_CK/QSPIO0_SLK/D0	IO	U13
66	PA01	VDDSDMMC	SDMMC0_CMD/QSPI0_CS/D1	IO	N7
68	PA02	VDDSDMMC	SDMMC0_DAT0/QSPI0_IO0/D2	IO	U14
69	PA03	VDDSDMMC	SDMMC0_DAT1/QSPI0_IO1/D3	IO	T13
70	PA04	VDDSDMMC	SDMMC0_DAT2/QSPI0_IO2/D4	IO	U15
71	PA05	VDDSDMMC	SDMMC0_DAT3/QSPI0_IO3/D5	IO	U16

72	PA06	VDDSDMMC	SDMMC0_DAT4/TIOA5/FLEXCOM2_IO0/D6	IO	U17
65	PA07	VDDSDMMC	SDMMC0_DAT5/TIOB5/FLEXCOM2_IO1/D7	IO	R11
64	PA08	VDDSDMMC	SDMMC0_DAT6/TCLK5/FLEXCOM2_IO2/NWE/NANDWE	IO	R9
63	PA09	VDDSDMMC	SDMMC0_DAT7/TIOA4/FLEXCOM2_IO3/NCS3	IO	P8
62	PA10	VDDSDMMC	SDMMC0_RSTN/TIOB4/FLEXCOM2_IO4/A21/NANDALE	IO	R10
73	PA11	VDDIN_3V3	SDMMC0_VDDSEL/TCLK4/A22/NANDCLE	IO	P15
77	PA12	VDDIN_3V3	SDMMC0_WP/IRQ/NRD/NANDOE	IO	N17
76	PA13	VDDIN_3V3	SDMMC0_CD/FLEXCOM3_IO1/D8	IO	P16
97	PA14	VDDIN_3V3	SPI0_SPCK/TK1/QSPI0_SCK/I2SMCK1/FLEXCOM3_IO2/D9	IO	M17
95	PA15	VDDIN_3V3	SPI0_MOSI/TF1/QSPI0_CS/I2SCK1/FLEXCOM3_IO0/D10	IO	N16
98	PA16	VDDIN_3V3	SPI0_MISO/TD1/QSPI0_IO0/I2SWS1/FLEXCOM3_IO3/D11	IO	M11
94	PA17	VDDIN_3V3	SPI0_NPCS0/RD1/QSPI0_IO1/I2SDI1/FLEXCOM3_IO4/D12	IO	N14
92	PA18	VDDIN_3V3	SPI0_NPCS1/RK1/QSPI0_IO2/I2SDO1/SDMMC1_DAT0/D13	IO	T16
89	PA19	VDDIN_3V3	SPI0_NPCS2/RF1/QSPI0_IO3/TIOA0/SDMMC1_DAT1/D14	IO	T15
91	PA20	VDDIN_3V3	SPI0_NPCS3/TIOB0/SDMMC1_DAT2/D15	IO	P9
88	PA21	VDDIN_3V3	PCK2/IRQ/TCLK0/SDMMC1_DAT3/NANDRDY	IO	P10
93	PA22	VDDIN_3V3	FLEXCOM1_IO2/SPI1_SPCK/SDMMC1_CK/QSPI0_SCK	IO	T17
90	PA23	VDDIN_3V3	FLEXCOM1_IO1/SPI1_MOSI/QSPI0_CS	IO	T14
86	PA24	VDDIN_3V3	FLEXCOM1_IO0/SPI1_MISO/QSPI0_IO0	IO	R17
85	PA25	VDDIN_3V3	FLEXCOM1_IO3/SPI1_NPCS0/QSPI0_IO1	IO	R16
87	PA26	VDDIN_3V3	FLEXCOM1_IO4/SPI1_NPCS1/QSPI0_IO2	IO	P17
75	PA27	VDDIN_3V3	TIOA1/D5/SPI0_NPCS2/SPI1_NPCS2/SDMMC1_RSTN/QSPI0_IO3	IO	R15
83	PA28	VDDIN_3V3	TIOB1/SPI0_NPCS3/SPI1_NPCS3/SDMMC1_CMD/CLASSD_L0	IO	R14
84	PA29	VDDIN_3V3	TCLK1/SPI0_NPCS1/SDMMC1_WP/CLASSD_L1	IO	P14
82	PA30	VDDIN_3V3	SPI0_NPCS0/PWMH0/SDMMC1_CD/CLASSD_L2	IO	R13
78	PA31	VDDIN_3V3	SPI0_MISO/PWML0/CLASSD_L3	IO	P13

Table 2

1.3.2 PhyCORE_A5D2x Port – B "PIO" 3.3V Levels

Pin#	PIO	Power Rail	PIO Feature	Type	SIP-289-BGA
105	PB00	VDDIN_3V3	SPI0_MOSI/PWMH1	IO	F5
108	PB01	VDDIN_3V3	SPI0_SPCK/PWML1/CLASSD_R0	IO	C8
110	PB02	VDDIN_3V3	PWMFI0/CLASSD_R1	IO	C7
109	PB03	VDDIN_3V3	URXD4/IRQ/PWMEXTRG0/CLASSD_R2	IO	B8
111	PB04	VDDIN_3V3	UTXD4/FIQ/CLASSD_R3	IO	B7
114	PB05	VDDIN_3V3	TCLK2/PWMH2/QSPI1_SCK	IO	A10
SOM	PB06	VDDIN_3V3	QSPI_CS_PB06 [Internally Used at SOM Module]	IO	A9
115	PB07	VDDIN_3V3	TIOB2/PWMH3/QSPI1_IO0	IO	D5
112	PB08	VDDIN_3V3	TCLK3/PWML3/QSPI1_IO1	IO	E5
116	PB09	VDDIN_3V3	TIOA3/PWMFI1/QSPI1_IO2	IO	C6
113	PB10	VDDIN_3V3	TIOB3/PWMEXTRG1/QSPI1_IO3	IO	A8
133	PB11	VDDIN_3V3	LCDDAT0/URXD3/PDMDAT0	IO	A7
135	PB12	VDDIN_3V3	LCDDAT1/UTXD3/PDMCLK0	IO	B6
143	PB13	VDDIN_3V3	LCDDAT2/PCK1	IO	C5
134	PB14	VDDIN_3V3	LCDDAT3/TK1/I2SMCK1	IO	A6
147	PB15	VDDIN_3V3	LCDDAT4/TF1/I2SCK1	IO	E4
137	PB16	VDDIN_3V3	LCDDAT5/TD1/I2SWS1	IO	B5
144	PB17	VDDIN_3V3	LCDDAT6/RD1/I2SDI1	IO	C4
136	PB18	VDDIN_3V3	LCDDAT7/RK1/I2SDO1	IO	A5
139	PB19	VDDIN_3V3	LCDDAT8/RF1/TIOA3	IO	B4
138	PB20	VDDIN_3V3	LCDDAT9/TK0/TIOB3/PCK1	IO	A4
149	PB21	VDDIN_3V3	LCDDAT10/TF0/TCLK3/FLEXCOM3_IO2	IO	D3
145	PB22	VDDIN_3V3	LCDDAT11/TD0/TIOA2/FLEXCOM3_IO1	IO	C3
146	PB23	VDDIN_3V3	LCDDAT12/RD0/TIOB2/FLEXCOM3_IO0	IO	B3
153	PB24	VDDIN_3V3	LCDDAT13/RK0/TCLK2/FLEXCOM3_IO3	IO	E2
140	PB25	VDDIN_3V3	LCDDAT14/RF0/FLEXCOM3_IO4	IO	A3
154	PB26	VDDIN_3V3	LCDDAT15/URXD0	IO	G3
148	PB27	VDDIN_3V3	LCDDAT16/UTXD0	IO	F4
152	PB28	VDDIN_3V3	LCDDAT17/FLEXCOM0_IO0/TIOA5	IO	D2
131	PB29	VDDIN_3V3	LCDDAT18/FLEXCOM0_IO1/TIOB5	IO	G8
151	PB30	VDDIN_3V3	LCDDAT19/FLEXCOM0_IO2/TCLK5	IO	C2
130	PB31	VDDIN_3V3	LCDDAT20/FLEXCOM0_IO3	IO	G7

Table 3

1.3.3 PhyCORE_A5D2x Port – C "PIO" 3.3V Levels

Pin#	PIO	Power Rail	PIO Feature	Type	SIP-289-BGA
129	PC00	VDDIN_3V3	LCDDAT21/FLEXCOM0_IO4	IO	N10
127	PC01	VDDIN_3V3	LCDDAT22/CANTX0/SPI1_SPCK/I2SCK0	IO	N11
132	PC02	VDDIN_3V3	LCDDAT23/CANRX0/SPI1_MOSI/I2SMCK0	IO	N9
128	PC03	VDDIN_3V3	LCDPWM/TIOA1/SPI1_MISO/I2SWS0	IO	M10

122	PC04	VDDIN_3V3	LCDDISP/TIOB1/SPI1_NPCS0/I2SDI0	IO	N15
123	PC05	VDDIN_3V3	LCDVSYNC/TCLK1/SPI1_NPCS1/I2SDO0	IO	M16
126	PC06	VDDIN_3V3	LCDHSYNC/TWD1/SPI1_NPCS2	IO	L11
125	PC07	VDDIN_3V3	LCDPCK/TWCK1/SPI1_NPCS3/URXD1	IO	M15
124	PC08	VDDIN_3V3	LCDDEN/FIQ/PCK0/UTXD1	IO	M13
156	PC09	VDDISC	FIQ/ISI_D0/TIOA4	IO	B2
12	PC10	VDDISC	ISI_D1/TIOB4/CANTX0	IO	G4
150	PC11	VDDISC	ISI_D2/TCLK4/CANRX0/A0/NBS0	IO	A2
6	PC12	VDDISC	ISI_D3/URXD3/TK0/A1	IO	A1
7	PC13	VDDISC	ISI_D4/UTXD3/TF0/A2	IO	B1
11	PC14	VDDISC	ISI_D5/TD0/A3	IO	G5
14	PC15	VDDISC	ISI_D6/RD0/A4	IO	G2
117	PC16	VDDISC	ISI_D7/RK0/A5	IO	G6
8	PC17	VDDISC	ISI_D8/RF0/A6	IO	C1
142	PC18	VDDISC	ISI_D9/FLEXCOM3_IO2/A7	IO	G9
9	PC19	VDDISC	ISI_D10/FLEXCOM3_IO1/A8	IO	D1
16	PC20	VDDISC	ISI_D11/FLEXCOM3_IO0/A9	IO	H4
10	PC21	VDDISC	ISI_PCK/FLEXCOM3_IO3/A10	IO	E1
13	PC22	VDDISC	ISI_VSYNC/FLEXCOM3_IO4/A11	IO	F1
141	PC23	VDDISC	ISI_HSYNC/A12	IO	H9
15	PC24	VDDISC	ISI_MCK/A13	IO	G1
155	PC25	VDDISC	ISI_FIELD/A14	IO	H8
101	PC26	VDDIN_3V3	CANTX1/A15	IO	F7
100	PC27	VDDIN_3V3	PCK1/CANRX1/A16	IO	B10
103	PC28	VDDIN_3V3	FLEXCOM4_IO0/PCK2/A17	IO	F6
104	PC29	VDDIN_3V3	FLEXCOM4_IO1/A18	IO	B9
106	PC30	VDDIN_3V3	FLEXCOM4_IO2/A19	IO	E6
102	PC31	VDDIN_3V3	FLEXCOM4_IO3/URXD3/A20	IO	A11

Table 4

1.3.4 PhyCORE_A5D2x Port – D "PIO" 3.3V Levels

Pin#	PIO	Power Rail	PIO Feature	Type	SIP-289-BGA
107	PD00	VDDIN_3V3	FLEXCOM4_IO4/UTXD3/A23	IO	E7
99	PD01	VDDIN_3V3	A24	IO	C9
22	PD02	VDDIN_3V3	URXD1/A25	IO	D8
21	PD03	VDDANA	UTXD1/FIQ/NWAIT/PTCROW0	IO	J1
24	PD04	VDDANA	TWD1/NCS0/PTCROW1	IO	H7
19	PD05	VDDANA	TWCK1/NCS1/PTCROW2	IO	H1
20	PD06	VDDANA	PCK1/NCS2/PTCROW3	IO	J2
23	PD07	VDDANA	NWR1/NBS1/PTCROW4	IO	H6
25	PD08	VDDANA	NANDRDY/PTCROW5	IO	K3
SOM	PD09	VDDANA	Used Internal : RMII interface with Ethernet PHY		

SOM	PD10	VDDANA	Used Internal : RMII interface with Ethernet PHY		
SOM	PD11	VDDANA	Used Internal : RMII interface with Ethernet PHY		
SOM	PD12	VDDANA	Used Internal : RMII interface with Ethernet PHY		
SOM	PD13	VDDANA	Used Internal : RMII interface with Ethernet PHY		
SOM	PD14	VDDANA	Used Internal : RMII interface with Ethernet PHY		
SOM	PD15	VDDANA	Used Internal : RMII interface with Ethernet PHY		
SOM	PD16	VDDANA	Used Internal : RMII interface with Ethernet PHY		
SOM	PD17	VDDANA	Used Internal : RMII interface with Ethernet PHY		
SOM	PD18	VDDANA	Used Internal : RMII interface with Ethernet PHY		
48	PD19	VDDANA	PCK0/TWD1/AD0	IO	L8
47	PD20	VDDANA	TIOA2/TWCK1/AD1	IO	L2
17	PD21	VDDANA	EEPROM_TWD_PD21	IO	P1
18	PD22	VDDANA	EEPROM_TWCK_PD22	IO	L6
27	PD23	VDDANA	PD23/DBGU_RXD	IO	T1
26	PD24	VDDANA	PD24/DBGU_TXD	IO	L4
96	PD25	VDDANA	AD6	IO	L5
30	PD26	VDDANA	AD7	IO	R1
45	PD27	VDDANA	JTAG_TCK	IO	L7
43	PD28	VDDANA	JTAG_TDI	IO	L3
44	PD29	VDDANA	JTAG_TDO	IO	M2
46	PD30	VDDANA	JTAG_TMS	IO	M9
SOM Internal Use	PD31	VDDANA	Used Internal : RMII interface with Ethernet PHY	INPT	M8

Table 5

1.3.5 PhyCORE_A5D2x SOM IO's levels (3.3V)

Pin#	PIO	Power Rail	PIO Feature	Type	SIP-289-BGA
52	CLK_AUDIO	VDDIN_3V3	Audio clock	Output	T8
50	COMPN	VDDBU	External analog comparator input	Input	U7
51	COMPP	VDDBU	External analog comparator input	Input	U6
54	USBA_M/ HHSDMA	VDDIN_3V3	USB Device High Speed Data -	-	T10

55	USBA_P/ HHSDPA	VDDIN_3V3	USB Device High Speed Data +	-	U10
58	USBB_M	VDDIN_3V3	USB Host Port B High Speed Data -	-	T11
57	USBB_P	VDDIN_3V3	USB Host Port B High Speed Data +	-	U11
61	DATA	VDDHSIC	USB High-Speed Inter-Chip Data		T12
60	STROBE	VDDHSIC	USB High-Speed Inter-Chip Strobe		U12
42	nRST	VDDIN_3V3	Microprocessor reset input (Active low)	Input	T7
29	PIOBU1	VDDBU	Tamper or Wakeup input	Input	M3
38	PIOBU2	VDDBU	Tamper or Wakeup input	Input	P2
39	PIOBU3	VDDBU	Tamper or Wakeup input	Input	P4
40	PIOBU4	VDDBU	Tamper or Wakeup input	Input	N4
74	PIOBU5	VDDBU	Tamper or Wakeup input	Input	M5
49	PIOBU6	VDDBU	Tamper or Wakeup input	Input	N5
5	PIOBU7	VDDBU	Tamper or Wakeup input	Input	N3
28	RXD	VDDBU	Low Power Asynchronous Receiver	Input	N2
79	SHDN	VDDBU	Shutdown Control	**Output** /Tripad with WKUP	T2
79	WKUP	VDDBU	Wakeup	**Input Tripad Option with SHDN**	R2
31	ETH_LED0	VDDIN_3V3	Status LED control for Ethernet ports	Output	ETH
32	ETH_RXM	**± 2.5V**	Physical receive or transmit signal (differential 100 Ohm Impedance)	IO	ETH
33	ETH_RXP	**± 2.5V**	Physical receive or transmit signal (differential 100 Ohm Impedance)	IO	ETH
35	ETH_TXM	**± 2.5V**	Physical receive or transmit signal (differential 100 Ohm Impedance)	IO	ETH
36	ETH_TXP	**± 2.5V**	Physical receive or transmit signal	IO	ETH

			(differential 100 Ohm Impedance)		

Table 6

1.4 PhyCORE_A5D2x SOM: Power Sources Types

Pin#	PIO	Power Rail	PIO Feature	Type
1,2,159,160	VDDIN_3V3 (3V3_IN)	Main-power input Signal to SOM	Main 3.3V Supply inputs. Used for Peripheral I/O lines and MIC2800 supplies.	Power
158	VDDBU	Power to internal RTC	Input supply for Slow Clock Oscillator, internal 32 kHz RC Oscillator and a part of the System Controller	Power
3V3	VDDSDHC	Power to SD Card	SDMMC I/O lines supply input (N8 SOM BGA)	Power
3,4	VDDISC	Power to Sensors	Image Sensor I/O lines supply input	Power
34,37,41,80,81,118-121,157,161-180	GND	Ground	Ground connections (Must be connected together)	Power

Table 7

Important Note:

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger
2. Refer to the DDR2-SDRAM datasheet for DDRM_VDDQ and DDRM_VDDL definitions. DDRM_VDDQ/DDRM_VDDL = 1.8V ±0.1V.

1.4.1 Types of Signals

Different types of signals are brought out at the phyCore SOM. The following table lists the abbreviations used to specify the type of signals

Signal Type	Description	Abbreviation
Power	Main Supply Input Voltage	3V3_IN
Power	RTC backup Supply Voltage	VDDBU
Power	Image Sensor I/O lines supply input	VDDISC
Power	SDMMC I/O lines supply input	VDDSDHC
Input	Digital Input	I
Output	Digital Output	O
IO	Bidirectional Input/Output	IO
Ethernet Signals	Differential pair 100 ohm impedance	ETH

Table 8

2 Functional Description

2.1 SAMA5D2x System-In-Package

The SAMA5D2x System-In-Package (SIP) integrates the ARM Cortex-A5 processor-based SAMA5D2 MPU with upto 1 Gbit DDR2-SDRAM in a single package.

By combining the high-performance, ultra-low-power SAMA5D2 with DDR2-SDRAM in a single package, PCB routing complexity, area and number of layers is reduced. This makes board design easier and lowers the overall cost of bill of materials.

The SAMA5D27C-D1G-CU is available in a 289-ball TFBGA package.

For more information about the SIP, see "Reference Documents". This section lists the sole reference documents for product information on the SAMA5D2 and the DDR2-SDRAM memory.

DDR2-SDRAM Features

- Power Supply: VDD, VDDQ = 1.8 V ±0.1 V
- Double Data Rate architecture: two data transfers per clock cycle
- CAS Latency: 3
- Burst Length: 8
- Bi-directional, differential data strobes (DQS and DQSN) are transmitted/received with data
- Edge-aligned with Read data and center-aligned with Write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CLK and CLKN)
- Data masks (DM) for write data
- Commands entered on each positive CLK edge, data and data mask are referenced to both edges of DQS
- Auto-refresh and Self-refresh modes
- Precharged Power down and Active Power down
- Write Data Mask
- Write Latency = Read Latency - 1 (WL = RL - 1)

- Interface: SSTL_18

2.2 PhyCORE_A5D2x Primary “System Power (VDD_3V3)”

The PhyCORE_A5D2x SOM is supplied by an external 3.3V, ~2A rated current and generates its own internal supplies by interfacing with the Microchip MIC2800-G1JJYML -TR power management unit.

The MIC2800 is a high-performance power management IC (PMIC), providing three output voltages with maximum efficiency and is optimized to respect the MPU power up and down cycles Integrating a 2 MHz DC/DC converter with an LDO post regulator, the MIC2800 gives two high-efficiency outputs with a second, 300mA LDO for maximum flexibility. The DC-to-DC converter uses small values of L and C to reduce board space while still retaining efficiency over 90% at load currents up to 600mA.

The three outputs supply the following internal nodes:

- **DCDC set @ 1.8V** supplies PhyCORE_A5D2x DDR2 pads and device.
- **LDO1 set @ 1.25V** supplies PhyCORE_A5D2x Core.
- **LDO2 set @ 2.5V** supplies PhyCORE_A5D2x VDDFUSE pad.

The MIC2800 is a µCap design, operating with very small ceramic output capacitors and inductors for stability.

It is available in fixed output voltages in the 16-QFN (3x3) ® lead-less package. For more information, see datasheet at "Reference Documents”

2.2.1 Backup Power Supply

The SAMA5D2x requires a power source in order to permanently power the backup part of the SAMA5D2x device (refer to SAMA5D2x Series datasheet). The super capacitor / VRTC sustains such permanent power to VDDBU when all system power sources are off “VDDBU”.

For Proper operation of the PhyCORE-A5D2x SOM module must be supplied with a voltage source of **3.3V ± 5%** at the VCC pins of the SOM QFN pads.

Connect all **3.3V** VCC input pins to your power supply and at least the matching number of GND pins and some of the GND pins located underneath of Module.

2.3 PhyCORE_A5D2x SOM Current Consumption Table

[Actual Value to be Monitored Update Table)

<<Evaluate with PicoBoard and compare with Microchip EVK ….>> and Refer below Doc for Power Optimization Process

SL#	Scenarios	Mean current	Peak Current	SOM Power IN Voltage	Mean power Consumption
1	During Boot-Bare Box		120mA	3.3V	
2	Idle Mode in Linux without ETH		TB Test	3.3V	
3	Idle Mode in Linux with ETH		TB Test	3.3V	
4	Idle with following with 100% CPU load without ETH		TB Test	3.3V	
5	100% CPU load without ETH,		TB Test	3.3V	
6	100% CPU load with ETH		TB Test	3.3V	
7	Full load with several tasks		TB Test	3.3V	
8	Suspend Memory without ETH		TB Test	3.3V	
9	Suspend Memory with ETH		TB Test	3.3V	
10	Suspend standby with ETH		TB Test	3.3V	
11	Suspend freeze with ETH		TB Test	3.3V	
12	All Expansion GPIO High/Toggle		TB Test	3.3V	

Table 9

On Board Indications list:

- Power On LED Indication “D2” (Red Color Constant Always)
- CPU health Status LED Indication “D1“ (Green Color SW GPIO/PWM Controlled LED)
-

Refer -> SAMA5D2 Low-Power Modes Implementation Process:

http://ww1.microchip.com/downloads/en/AppNotes/SAMA5D2-Low-Power-Modes-Implementation-Application-Note-DS00002896A.pdf

<<< Hardware Power Budget; Follow UL/ other SOM refer and capture actual current consumption at 3.3V input

Different states of the hardware w.r.t to the software enable/Running Mode>>>>>

The above values in table are to be seen as an orientation for dimensioning the power supply of the SOM. In Order to ensure proper functionality of the SOM we recommend that the power supply is design to provide approximately 20 % Higher current. We also recommend that the final application is revalidated in regards of adequate current supply using application specific use case scenarios.

Warning:

As a General design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry. For Maximum EMI performance all GND pins should be connected to al Solid Ground Plane...!

<<<Prepare a Test SOM Zig board pluggable with Lock /Spring contac/ Other Simple Mechanism>>>

2.4 System Control

The PhyCORE_A5D2x SOM provides global system Reset (NRST) and Shutdown (SHDN) pins to the application board.

• The NRST pin is an **output** pin generated by the internal Power Management Unit (MIC2800-G1JJYML) in respect with power sequence timing. It can be forced externally in case of a system crash and must be connected as described in the example schematic below.

• The SHDN pin is an output pin and is managed by the software application. It switches the Main 3.3V Supply ON or OFF.

2.5 Ethernet PHY (10BASE-T/100BASE-TX)

The Microchip PhyCORE_A5D2x SOM embeds a single-supply 10BASE-T/100BASE-TX Ethernet physical layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ8081RNAIA is a highly-integrated PHY solution. The KSZ8081RNAIA offers the Reduced Media Independent Interface (RMII) for direct connection to RMII-compliant MACs in Ethernet processors. The

board supports RMII interface modes. The Ethernet interface consists of two pairs of low-voltage

differential pair signals. These signals can be used to connect to a 10/100 Base-T RJ45 connector integrated on the Carrier Board.

Additionally, for monitoring and control purposes, LED functionality is carried on the RJ45 connectors to indicate activity, link, and speed status information.

For more information about the Ethernet controller device, refer to the Microchip KSZ8081RNAIA controller

Datasheet at "Reference Documents"

2.6 QSPI Memory

The PhyCORE_A5D2x SOM embeds the SST26VF064BT-104I/MF, a 64Mbit Serial Quad I/O Flash memory. The SST26VF032B-104I/SM (32Mbit) SQI features a six-wire, 4-bit I/O interface that allows for low-power, high-performance operation in a low pin-count package.

The SST26VF032B-104I/SM is available in 8-SOIC (0.209", 5.30mm Width) package.

For more information, see datasheet at "Reference Documents".

Tip: The QSPI interface can be shared with another external device. To do so, the QSPI_CS# node must stay at "High" level at SOM Module internally

Replace with Macronix with Higher Flash Memory:

MX25L25645G
MX25L25673G
MX25L51245GMI-10G

2.7 EEPROM Memory

The PhyCORE_A5D2x SOM embeds the 24AA02E48T-I/OT, a 1Kb Serial EEPROM with pre-programmed EUI-48 MAC address.

The device is organized as one block of 128 x 8-bit memory with a 2-wire serial interface. The second block is reserved for MAC Address storage.

The 24AA02E48T-I/OT also has a page write capability for up to 8 bytes of data.

The 24AA02E48T-I/OT is available in the standard 5-lead SOT-23 package. For more information, see datasheet at "Reference Documents".

Important: If the 2-Wire serial interface is used externally, the device connected must have a different I^2C address than the embedded EEPROM. For more details, refer to the device datasheet and more no of slave devices connected long distance means route I2C signals via a I2C buffer IC.

3 Power Supply Connections and Timing Sequences:

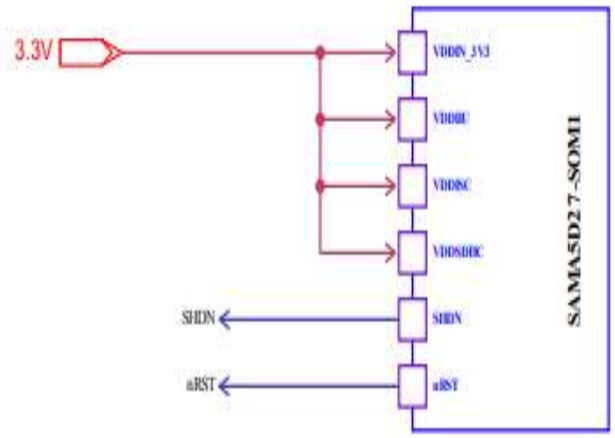
The PhyCORE_A5D2x SOM can be supplied in different ways depending on application needs.

Four power domains must be supplied and can be connected differently. The four different power connections are described below:

• Power Configuration #1: All supplies are connected to the Main 3.3V Supply.

• Power Configuration #2: Backup domain is connected to a coin-cell and the rest to the Main 3.3V Supply.

3.1 Power Configuration #1



In this configuration mode, the two following timing sequences are applied.

Figure 6-2. Power-On Sequence Timing Diagram

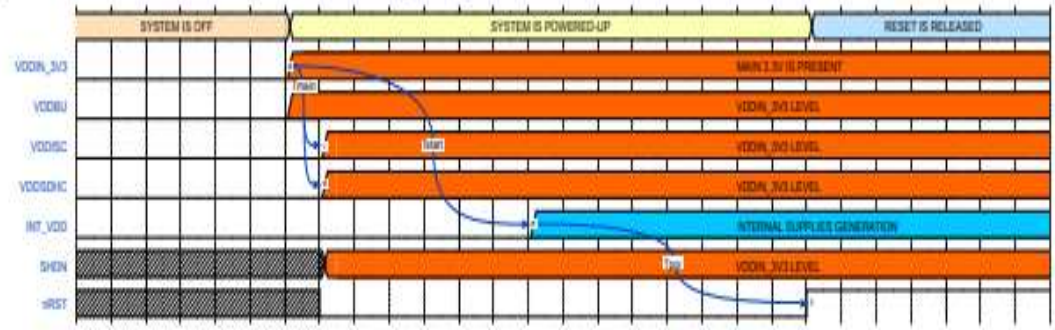


Fig 4

Figure 6-3. Power-Off Sequence Timing Diagram

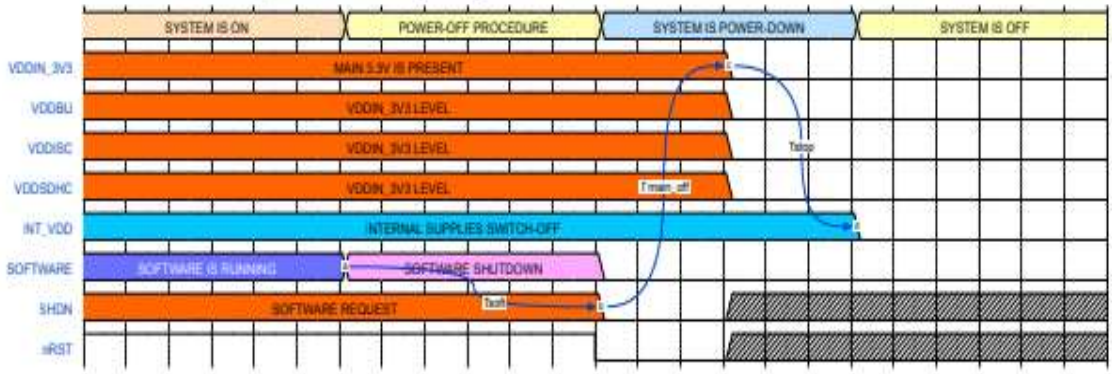


Fig 5

Table 6-1. Timing Values

Symbol	Description	Min.	Typ.	Max.	Unit
t_{main} (1)	Main 3.3V Startup Time	–	–	1	ms
t_{start}	Internal Delay before starting System Core Supplies	1	–	3	ms
t_{por}	Power-On Reset Delay	–	10	11	ms
t_{soft}	Software Shutdown Time	Depending on system off time			ms
t_{main_off}	Main 3.3V Power-off Time	–	–	1	ms
t_{stop}	Internal Delay before switching off System Core Supplies	1	–	3	ms

Note:

1. The three supplies VDDIN_3V3, VDDISC and VDDSDHC must be applied at the same time. If a delay is implemented, it must be lower than 800µs. VDDBU must be applied at the same time as VDDIN_3V3 or just before. It is forbidden to apply VDDBU after VDDIN_3V3.

3.2 Power Supply Configuration #2

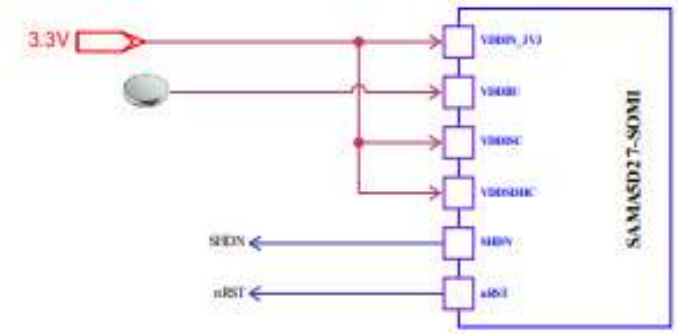
The SAMA5D27 SOM1 is supplied by different power supplies.

- Backup domain is connected to a coin-cell (~3V)
- The rest of the power inputs are connected to the main 3.3V supply.

In this configuration, the following PIOs have VDDBU Power Rail as reference.

All other PIO have VDDIN_3V3 Power Rail as reference.

- COMPP and COMPN
- PIOBU1 to PIOBU7
- RXD, SHDN and WKUP



In this configuration, the two following timing sequences are applied.

Figure 6-5. Power-On Sequence Timing Diagram

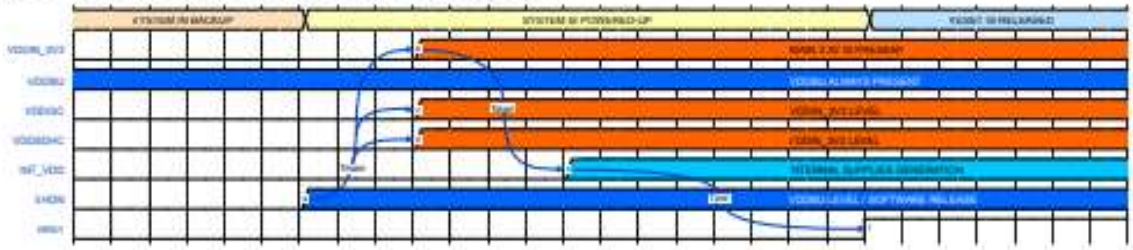


Figure 6-6. Power-Off Sequence Timing Diagram

Fig 6

Table 6-2. Timing Values

Symbol	Description	Min.	Typ.	Max.	Unit
t_{main} (1)	Main 3.3V Startup Time	–	–	1	ms
t_{start}	Internal Delay before starting System Core Supplies	1	–	3	ms
t_{por}	Power-On Reset Delay	–	10	11	ms
t_{soft}	Software Shutdown Time	Depending on system off time			ms
t_{main_off}	Main 3.3V Power-off Time	–	–	1	ms
t_{stop}	Internal Delay before switching-off System Core Supplies	1	–	3	ms

Note:

1. The three supplies VDDIN_3V3, VDDISC and VDDSDHC must be applied at the same time. If a delay is implemented, it must be lower than tstart

<<In final doc above highlighted will be removed>>

3.3 Electrical Characteristics

This section provides an overview of the electrical characteristics of the PhyCORE-A5D2x SOM module. Absolute maximum ratings for the PhyCORE-A5D2x SOM module are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the module at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

Table 9-1. Absolute Maximum Ratings

Parameter	Conditions	Min.	Max.
Storage Temperature	–	-60°C	+150°C
Maximum Operating Temperature	–	-40°C	+85°C
Voltage on Inputs Pins	With respect to ground	-0.3V	+4.0V
Maximum Voltage	On VDDIN_3V3 Pads	–	+4.0V
	On VDDBU Pad	–	+4.0V
	On VDDSDHC Pad	–	+4.0V
	On VDDISC Pad	–	+4.0V

Important: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the

device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operational Characteristics

The following characteristics are applicable to the operating temperature range T_A = -40°C to +85°C, unless otherwise specified.

Table 9-2. Table 7. Power Supplies Operating Conditions

Pad	Parameters	Conditions	Min.	Typ.	Max.
VDDIN_3V3	DC Supply	–	3.0V	3.3V	3.6V
	Maximum Input Current	–	–	–	450mA
VDDBU	DC Supply	Must be established first or at the same time as VDDIN_3V3.	1.65V	3.3V	3.6V

Pad	Parameters	Conditions	Min.	Typ.	Max.
	Maximum Input Current	–	–	–	0.1 mA
VDDSDHC	DC Supply	SDHC I/Os Lines	1.65V	3.3V	3.6V
	Maximum Input Current	–	–	–	30mA
VDDISC	DC Supply	ISC I/Os Lines	1.65V	3.3V	3.6V
	Maximum Input Current	–	–	–	30mA

<< In final doc above highlighted will be removed in final Doc/After SOM Power/Current consumption Validation>>

3.3.1 PhyCORE-A5D2x SOM PCB Footprint Dimensions (Top View)

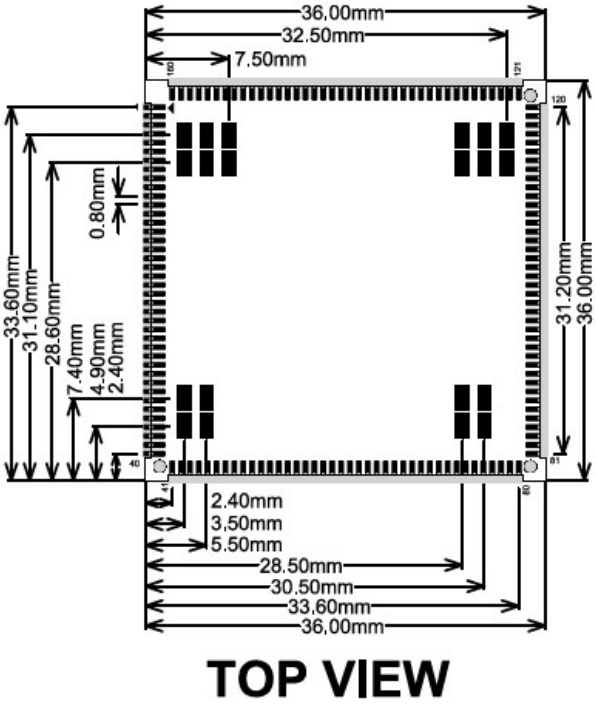


Fig 7

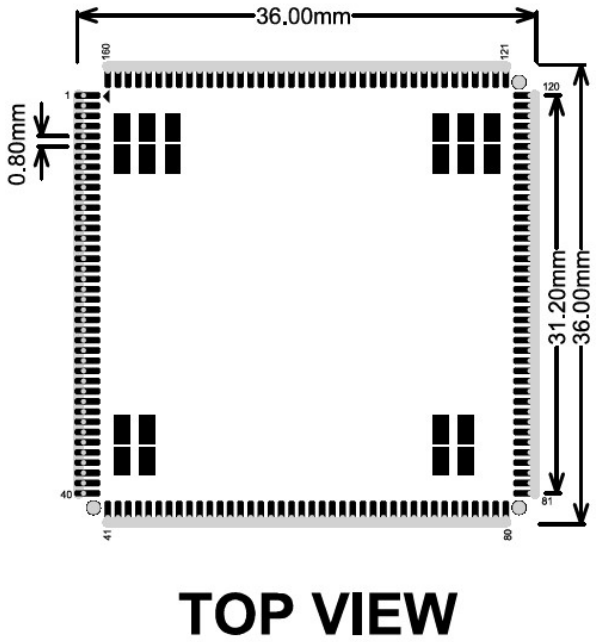


Fig 8

Additional specifications:

Dimensions:	36 mm x 36 mm
Weight:	approx. 6.2g
Storage temperature:	-60°C +150°C
Operatingtemperature:	-40 °C to + 85 °C
Operating voltage:	VCC 3.3 V +/- 5 %
Power consumption:	Linux prompt only: typical 0.5 W Fullload: typical 1W

Technical Specifications

Table 10

PhyCORE-SOM Dimensions with 3D View

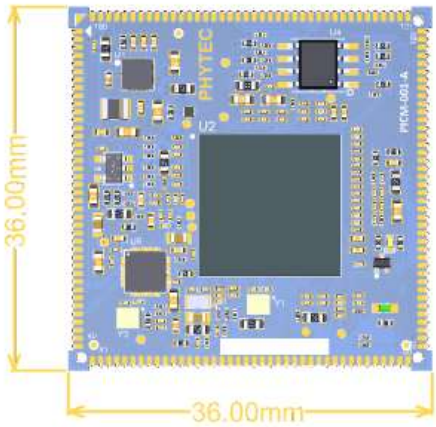


Fig 9

Note:

To facilitate the integration of the PhyCORE-A5D2x SOM Into your custom Board design, the Altium Schematic Symbol and Altium Layout PCB Footprint of the PhyCORE-A5D2x SOM is available for download online:

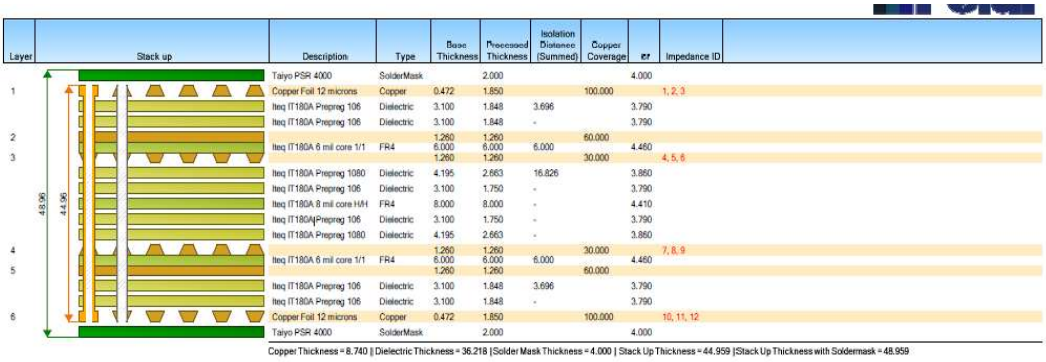
WWW.ruggedboard.com/Downloads/PhyCORE-A5D2x-SOM Altium Footprints

3.3.2 PhyCORE-A5D2x SOM Module Land Pattern on Custom Carrier Board

The PhyCORE-A5D2x SOM Module has the following recommended Land Pattern characteristics.

<<Raghu To be update Landing pattern on CB with Dimensions & Pin# Silk>>

PCB Stack Info; 6 layer with Impedance Controlled Board (HiQ India)



Layer	Stack up	Description	Type	Base Thickness	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	er	Impedance ID
		Taiyo PSR 4000	SolderMask		2.000			4.000	
1		Copper Foil 12 microns	Copper	0.472	1.850		100.000		1, 2, 3
		Iteq IT180A Prepreg 106	Dielectric	3.100	1.848	3.696		3.790	
		Iteq IT180A Prepreg 106	Dielectric	3.100	1.848	-		3.790	
2				1.260	1.260		60.000		
3		Iteq IT180A 6 mil core 1/1	FR4	6.000	6.000	6.000		4.460	
				1.260	1.260		30.000		4, 5, 6
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.663	16.826		3.860	
		Iteq IT180A Prepreg 106	Dielectric	3.100	1.750	-		3.790	
		Iteq IT180A 8 mil core H/H	FR4	8.000	8.000	-		4.410	
		Iteq IT180A Prepreg 106	Dielectric	3.100	1.750	-		3.790	
		Iteq IT180A Prepreg 1080	Dielectric	4.195	2.663	-		3.860	
4				1.260	1.260		30.000		7, 8, 9
5		Iteq IT180A 6 mil core 1/1	FR4	6.000	6.000	6.000		4.460	
				1.260	1.260		60.000		
		Iteq IT180A Prepreg 106	Dielectric	3.100	1.848	3.696		3.790	
		Iteq IT180A Prepreg 106	Dielectric	3.100	1.848	-		3.790	
6		Copper Foil 12 microns	Copper	0.472	1.850		100.000		10, 11, 12
		Taiyo PSR 4000	SolderMask		2.000			4.000	

Copper Thickness = 8.740 || Dielectric Thickness = 36.218 |Solder Mask Thickness = 4.000 | Stack Up Thickness = 44.959 |Stack Up Thickness with Soldermask = 48.959

Fig 10

3.4 Mechanical Characteristics

Module Dimensions: The PhyCORE-A5D2x SOM has dimensions of overall 36mm x 36mm with the specific following 2D-mechanical characteristics.

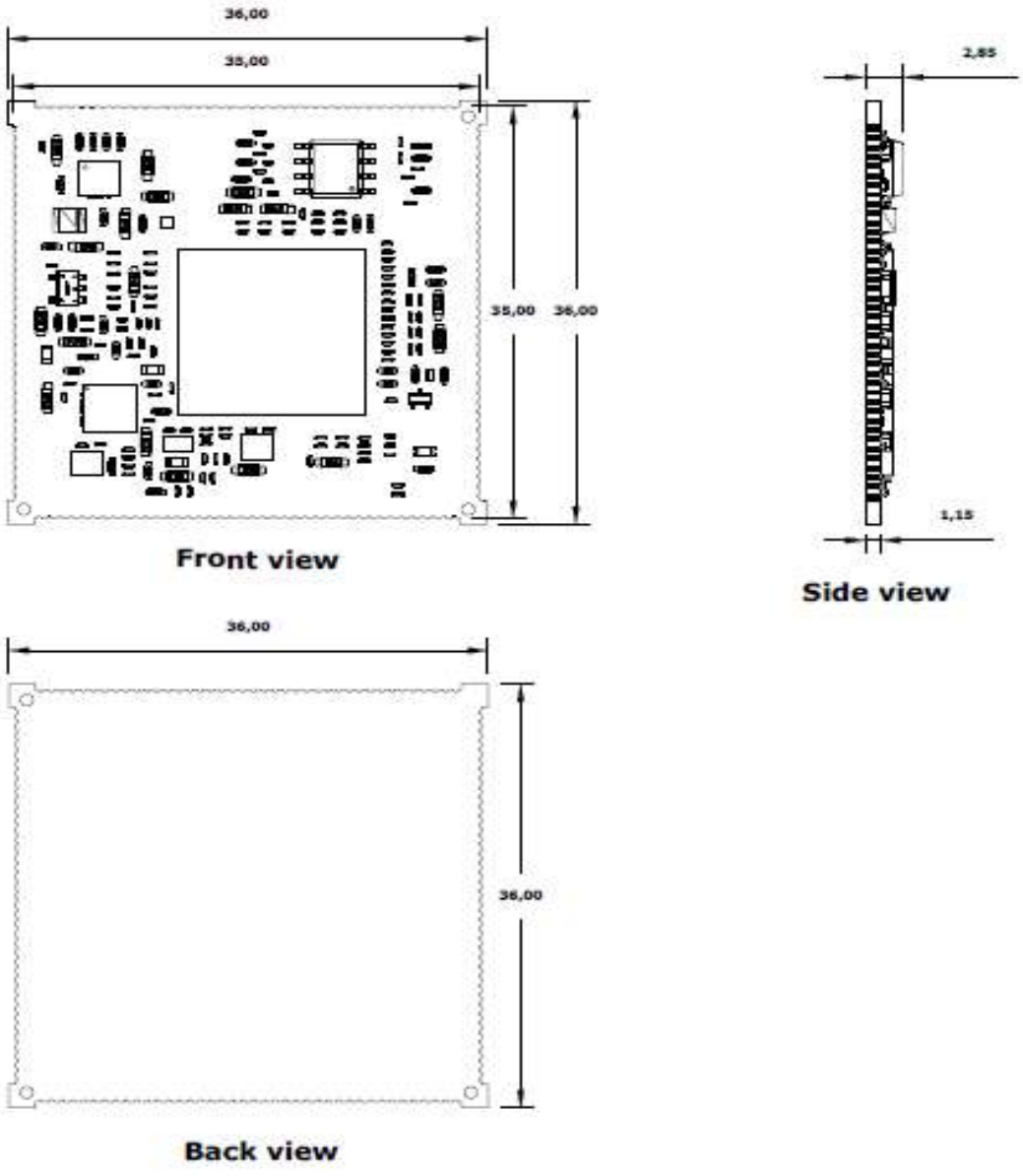


Fig 11

The physical dimensions of the square PhyCORE-A5D2x SOM are represented in above.The module's profile is max. 2.85 mm thick, with a maximum component height of 1.15 mm on the top side of the PCB. The board itself can be easily soldered direct onto your carrier board.

Product Temperature Grades

Caution!

The right temperature grade of the Module depends very much on the use case. It is mandatory to determine if the use case suites the temperature range of the chosen module (see below). If necessary, a heat spreader can be used for temperature compensation

The feasible operating temperature of the SOM highly depends on the use case of your software application. Modern high performance microcontrollers and other active parts as the ones described within this manual are usually rated by qualifications based on tolerable junction or case temperatures. Therefore, making a general statement about maximum or minimum ambient temperature ratings for the described SOM is not possible. However, the above mentioned parts are available still in different temperature qualification levels by the producers. We offer our SOM's in different configurations making use of those temperature qualifications. To indicate which level of temperature qualification is used for active and passive parts of a SOM configuration we have categorized our SOM's in three temperature grades. The table below describes these grades in detail. These grades describe a set of components which in combination add up to a useful set of product options with different temperature grades. This enables us to make use of cost optimizations depending on the required temperature range.

In order to determine the right temperature grade and whether the maximum or minimum qualification levels are met within an application the following conditions must be defined by considering the use case:

- Determined processing load for the given software use case
- Maximum temperature ranges of components (see table below)
- Power consumption resulting from a base load and the calculating power required (in consideration of peak loads as well as time periods for system cool down)
- Surrounding temperatures and existing airflow in case the system is mounted into a housing
- Heat resistance of the heat dissipation paths within the system along with the considered usage of a heat spreader or a heatsink to optimize heat dissipation.

3.4.1 Main Chipset Part Number

SL#	Description	MFG	MFG_PN	QTY	Temperature Range	Component Sourcing
1	SOC+RAM (SIP): Cortex-A5, 64MB RAM	Microchip	ATSAMA5D27C-D5M-CU	1	-40°C ~ 85°C	Microchip/Arrow
2	IC REG TRPL BUCK/LINEAR 16MLF	Microchip	MIC2800-G1JJYML	1	-40°C ~ 125°C	Microchip/Arrow
3	IC FLASH 32M SPI 104MHZ 8SOIJ	Microchip	SST26VF032B-104I/SM	1	-40°C ~ 85°C	Microchip/Arrow
4	IC TXRX ETHERNET 24QFN	Microchip	KSZ8081RNAIA	1	-40°C ~ 85°C	Microchip/Arrow
5	IC EEPROM 2K I2C 400KHZ SOT23-5	Microchip	24AA02E48T-I/OT	1	-40°C ~ 85°C	Microchip/Arrow

Table 11

Important Reference Documents

Type	Document Title	Available	Ref. No./Product
Datasheet	SAMA5D2	www.microchip.com/SAMA5D2	DS60001476
Datasheet	SAMA5D2 System-In-Package (SIP)	www.microchip.com/SAMA5D2 SIP	DS60001484
Datasheet	Serial EEPROMs with EUI-48 Node Identity	www.microchip.com/24AA02E48	24AA02E48T-I/OT
Datasheet	10BASE-T/100BASE-TX Ethernet PHY	www.microchip.com/ksz8081	KSZ8081RNAIA
Datasheet	Serial Quad I/O (SQI) Flash Memory	www.microchip.com/sst26vf064b	SST26VF064BT-104I/MF
Datasheet	Digital Power Management IC	www.microchip.com/mic2800	MIC2800-G1JJYML

Other Reference Documents

Boot Process: Flow Chart "C"

Refer Chipset Processor Doc:

http://ww1.microchip.com/downloads/en/devicedoc/ds60001476b.pdf

Boot Configuration

Refer Chipset Processor Doc:

http://ww1.microchip.com/downloads/en/devicedoc/ds60001476b.pdf

SAMA5D2 Low-Power Modes Implementation Process:

http://ww1.microchip.com/downloads/en/AppNotes/SAMA5D2-Low-Power-Modes-Implementation-Application-Note-DS00002896A.pdf

IC NOR FLASH 256Mbit

http://www.macronix.com/Lists/Datasheet/Attachments/7549/MX25L25645G,%203V,%20256Mb,%20v1.7.pdf

IC NOR FLASH 256Mbit

http://www.macronix.com/Lists/Datasheet/Attachments/7444/MX25L25673G,%203V,%20256Mb,%20v1.4.pdf

IC NOR FLASH 512Mbit

http://www.macronix.com/Lists/Datasheet/Attachments/7437/MX25L51245G,%203V,%20512Mb,%20v1.6.pdf

Note:

Please go to the Download Zone or the Knowledge Database in the Support Center on the Phytec.in website for product manuals, installation guides, device driver software and technical tips. Submit your technical support questions to our customer support engineers via the Support Center on the Connect Tech website.

To Be decided:☹SIP with 2Gbit and 1Gbit

We have released with LPDDR SiP with 2Gbit and 1Gbit do you see we need to use LPDDR SiP in place of DDR2 please confirm. Please let me know for any clarification.

https://www.microchip.com/wwwproducts/en/ATSAMA5D27C-LD2G

https://www.microchip.com/wwwproducts/en/ATSAMA5D27C-LD1G

Check ***SIP LPDDR is footprint and Core voltage and IO voltage's compactible with DDR SIP package TFBGA289…?

Table 6-1. Packages

Package Name	Ball Count	Ball Pitch	Package Size
TFBGA196	196	0.75 mm	11 x 11 (mm)
TFBGA289[1]	289	0.8 mm	14 x 14 (mm)
TFBGA361[2]	361	0.8 mm	16 x 16 (mm)

Note:

1. 512 Mbit and 1 Gbit DDR2 in TFBGA289 have the same ballout.
2. 1 Gbit and 2 Gbit LPDDR2 in TFBGA361 have the same ballout.

Rugged BOARD (An open source hardware initiative)

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