ENEL469: Analog Electronic Circuits

Department of Electrical and Computer Engineering
University of Calgary

Project: AM Receiver System Design

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Lab group number	4	Lab section (B01/B02)?	BO1

Instructions:

- All members in a lab group will **work together** on the same circuit even when there are flexibilities in circuit design.
- **Each group member** is required to submit their work, and a random one will be chosen to be marked. You all can have the same answers, but you should have your own simulation results. (all the submissions will be checked but one will be marked)
- The project must be completed using Multisim 14. You can use the following parameters for the 2N3904 transistor: β = 160, VA = 120V, VT = 25mV, VCE(sat) = 0.2 V, VBE(ON) = 0.7 V
- All parts of **the project must be saved** in the separate design and **named as directed**.
- The submission is only one zip file named "Prj_StudentName_StudentID#.zip" which contains two folders. One named "Simulation" which contains all the *.ms14 files and the other one is "Document" that contains a single pdf file with the answers to the questions. You **should** use this project manual word template to answer the question and then extract a pdf for the submission.
- Each group should upload **a short video** (5 min max), where they go through their results and design quickly and highlight their work and pitch their Receiver design. All members of the group should contribute equally, and each member should introduce themselves (No camera recording needed). The video should be **uploaded** to (youtube, google drive, one drive, dropbox .. etc, and a link should be added the the description of your submission)
- The project is **due at 11:59 pm on Dec. 4th**.

Objectives:

1. To analyze and understand different system design perspectives of an amplitude modulation (AM) receiver.
2. To design and implement an AM receiver system.
3. To test and evaluate the performances of the developed AM receiver system
    a. To probe different signals at different points of the circuit.
    b. To receive and listen a real-time AM broadcast channel.

Overview of an AM Receiver System:

Amplitude modulation (AM) refers to modify the amplitude of a carrier signal to convey the information in a wireless system. For example, the amplitude of a radio carrier is varied in Figure 1 according to the audio signal which gives the amplitude modulated signal. From a broadcast station, generally, AM signals are transmitted and to listen to that certain station, an AM receiver system is required.

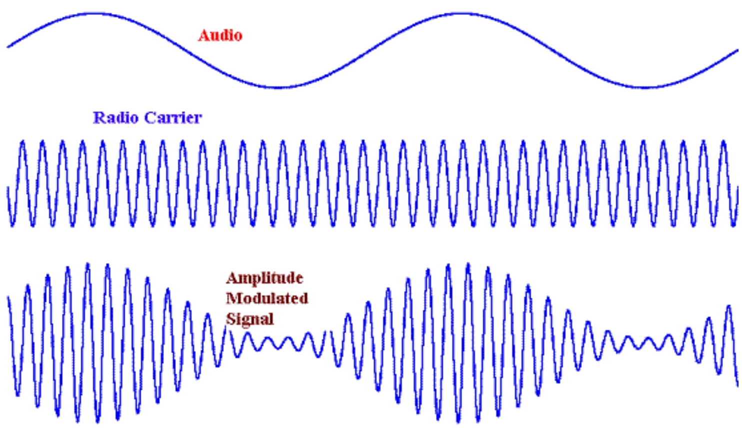


Figure 1: Amplitude modulation

A block diagram of an AM receiver system is shown in Figure 2.

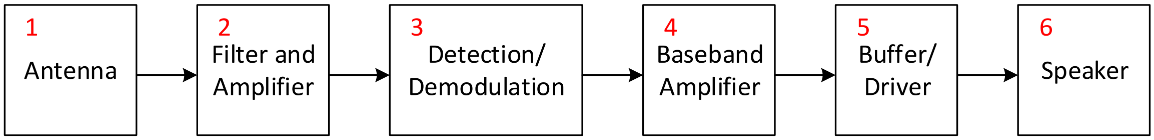


Figure 2: AM receiver system.

The antenna in Figure 2 mainly acts as a transducer to convert the radio signal to an electrical one. However, when receiving the signal by the antenna, it is important to filter out the unnecessary out-of-band signals. A band pass filter is required to select the specific band of interest. For example, if we want to receive the AM 660 kHz channel, the antenna and the filter should be tuned at this 660 kHz. To boost the received signal, an amplifier can be used. To perform both filtering and amplification, active filters are the first choice.

Now to hear back the audio signal which was amplitude modulated earlier, it is now time to demodulate. For this purpose, an envelop detector circuit can be used. The concept of envelop detection is shown in Figure 3 where a diode first rectifies the signal and the RC circuit acts as a low pass filter to sense the envelop of the AM signal which is actually the desired audio signal. As you can see, this simple circuit is the key of the whole receiver system. To get it working, make sure that the RC time constant of the envelop detector circuit is selected properly so that it can detect the envelop and follows it properly. Also, select the diode fast enough so that it can operate at the high carrier frequency.

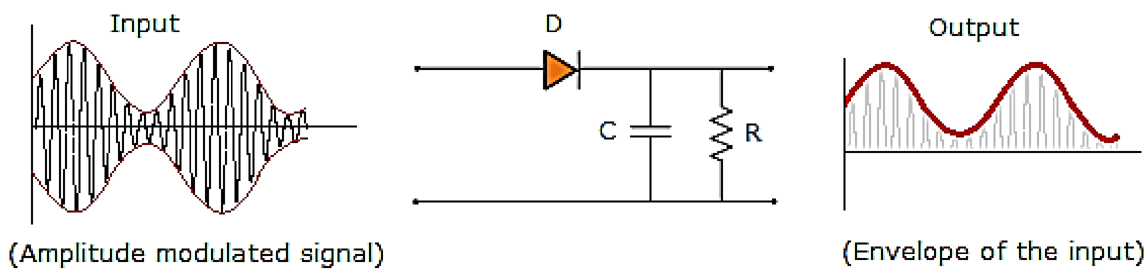


Figure 3: Envelop detection.

Once the audio signal is detected, note that, the signal frequency is now down converted from carrier (high frequency) to audio signal (low frequency in the order of 150-300 Hz). This low frequency is sometimes called as baseband signal. To hear the AM station, this detected audio signal/baseband signal is amplified and fed to the speaker with an output stage/buffer stage. As you already know, the buffer/output stage is necessary to avoid loading effect.

A common emitter stage can be used as a baseband amplifier where a common collector stage can be used for the buffer/output driver stage. To design these amplifier and output stages, it is important to select the coupling and bypass capacitors properly so that the desired signal gets amplified and passed to the speaker.

AM Receiver Circuit:

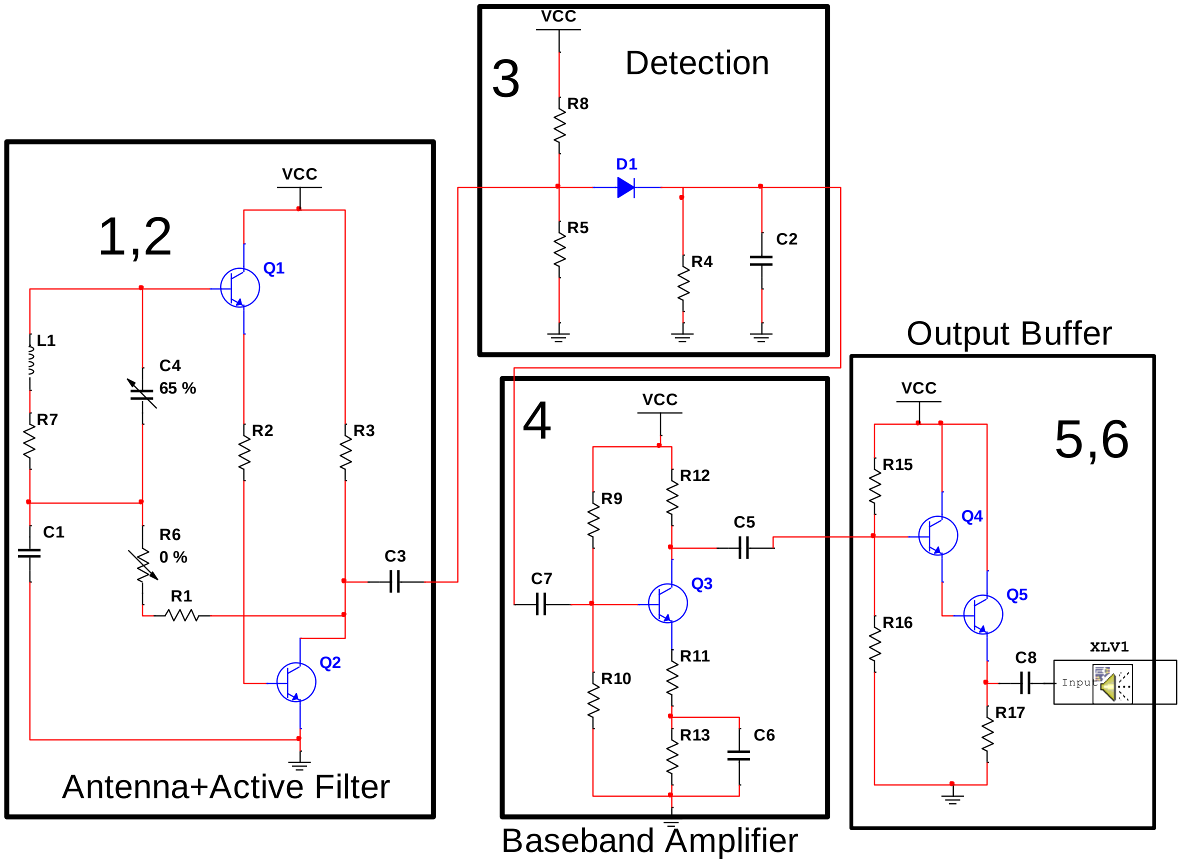


Figure 4: AM receiver circuit.

An example of AM receiver circuit is shown in Figure 4. Different blocks of the AM receiver system shown in Figure 2 are implemented in the AM receiver circuit shown in Figure 4 and the blocks are marked from 1-6.

Part A:

The response of an LC tank circuit is shown in Figure 5. As you can see, such circuit generally passes the certain frequency band centered at f_0 which is determined by:

$$f_0 = \frac{1}{2\pi\sqrt{(LC)}}$$

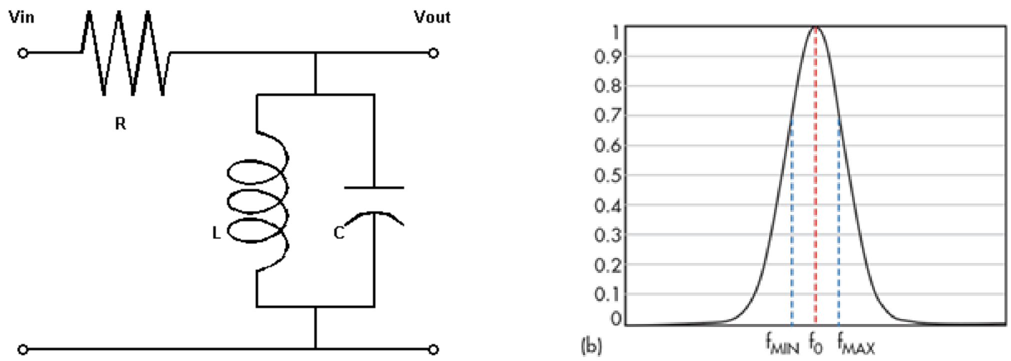


Figure 5: LC circuit response.

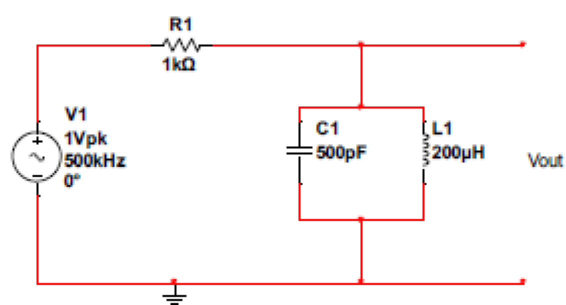


Figure 6: Detection circuit response analysis

1. Observe the band-pass filter response of the Antenna + LC circuit.

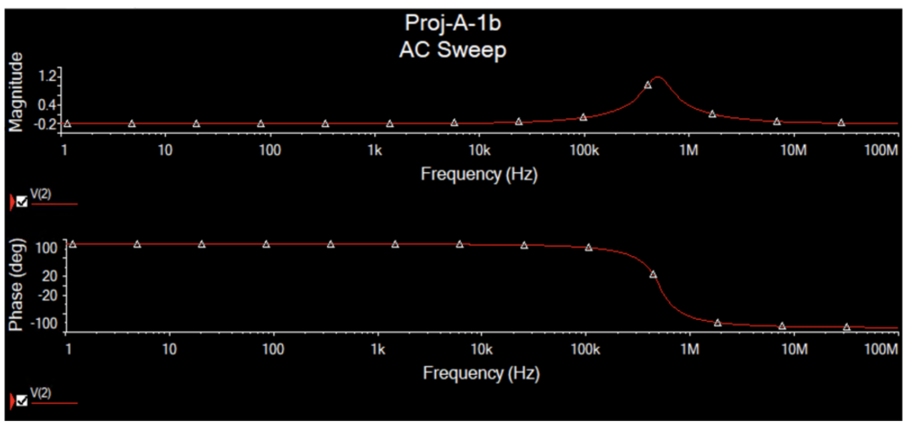
   a) Calculate the resonance frequency of the following circuit shown in Figure 6. What should be the output voltage at resonant frequency and why?

   The resonance frequency can be calculated by doing the following:

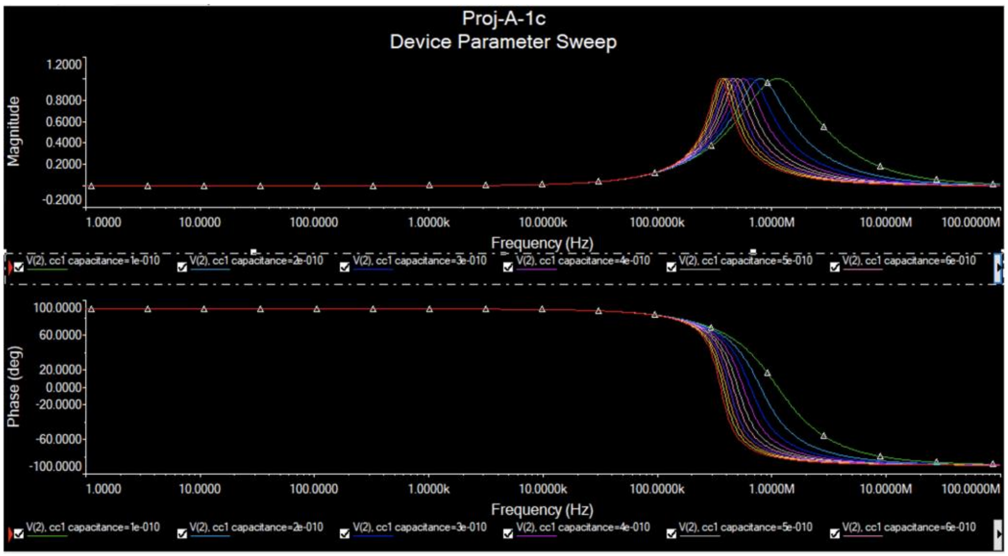
$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$
$$= \frac{1}{2\pi\sqrt{200\times10^{-6}\times 500\times10^{-12}}}$$
$$= 503.29121 \text{ kHz}$$
$$= 503.3 \text{ kHz}$$

At this frequency, that is 503.3 kHz, the output voltage should simply be the same as the input voltage. This is because at the resonant frequency, the combined impedance of the inductor and capacitor looks like an open circuit, meaning that no current is flowing. Thus, there is no drop across R1 and the voltage gain is 1.

b) Simulate the circuit in Figure 6 using AC analysis, to get the response over the frequency range from 1 Hz-100 MHz (choose linear scaled frequency axis and around 100 point per decade). Add your simulated results plot below and save your simulation filed as “Proj-A-1b. ms14”.



c) Redo the simulation in part 1a while doing a parametric sweep and change the capacitor value C1 from 100 pf to 1 nf with 10 point. Add your simulated results plot below and save your simulation filed as “Proj-A-1c. ms14”.

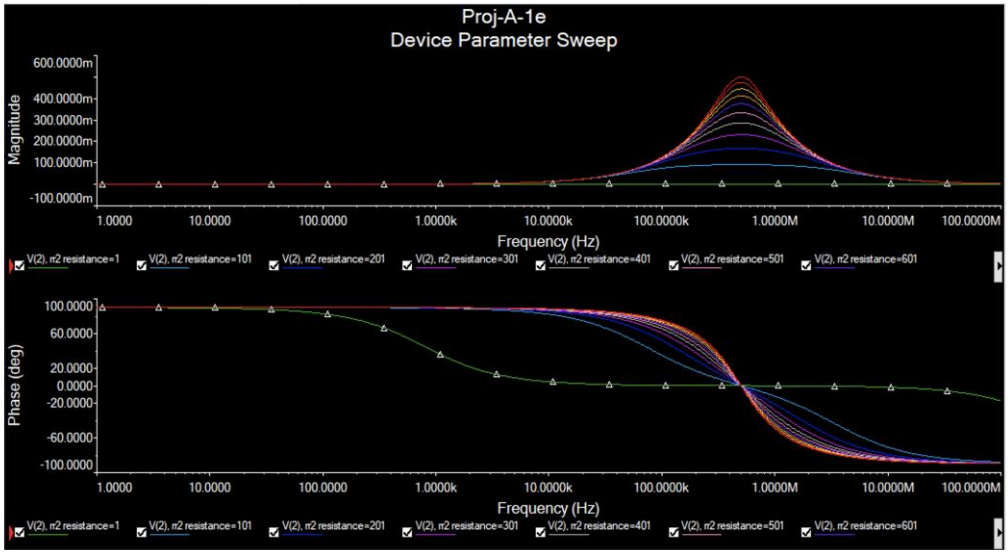


d) Explain the results obtained above, what is the effect of changing the capacitor on the circuit?

As C is increased, the rightmost plot is continuously further and further shifted left. This makes sense because as C is increased, the resonance frequency decreases. If thought about from an impedance perspective, as C increases, a lower frequency is required to effectively make the capacitor a short circuit.

e) Simulate the circuit in Figure 6 using AC analysis again with a parallel resistor to the LC, to get the response over the frequency range from 100 kHz-10 MHz (choose linear scaled frequency axis). Add your simulated results plot below and save your simulation filed as “Proj-A-1e. ms14”. ***Hints****: choose your resistor range or value accordingly to be able to answer the questions below.*

Note, R2 (the resistor added) was varied from 1 ohm to 1k, with a step of 100 ohms.



f) Explain the results obtained above, what is the effect of this resistor on the circuit?

The added resistor will effectively impact the voltage seen at the output. The larger it is, the larger the peak of the output voltage is. This makes sense because the added resistor impacts the overall impedance seen between Vo and GND, meaning that as the resistor value increases, the parallel resistance of the capacitor, inductor, and the added resistance also increases. This then means that, when compared to R1, the parallel resistance will have an increasingly higher voltage drop (refer to voltage divider model). This is then seen at Vo.

One can also notice that as R2 increases, the output curve becomes more curved, sharp, and defined.

g) If we moved the resistor to be in series with the inductor, what are we changing now? Do you observe the same behavior and why?

If this was done, then the high pass filter effect part of the bandpass filter would be cast away. That is, for lower frequencies at which the inductor previously caused the output voltage to be zero, the output would now be a non-zero value because it is now in series with a resistor. This effectively makes the circuit behave like a lowpass filter.

2. Develop the active filter circuit with the antenna shown in Figure 7.

a) Perform a DC and a small signal analysis of the circuit shown below in Figure 6 and find the value of the parameters listed in Table below at **resonance frequency.**

__Hints__: For DC, capacitors are open, and inductor is short. For small signal analysis, consider R1, L1, R7 and C2 altogether as a high impedance $\approx$R1. Use C1 and C3 as 100 nF and during analysis consider that they will remain short circuited.]

Parameter	Hand Calculation	Simulation
V_{CE1}	8.20 V	8.157 V
V_{CE2}	1.56 V	1.54 V
I_{C1}	98.313 uA	98.8 uA
I_{C2}	15.83 mA	15.9 mA
Small signal Gain	-50	-40.5

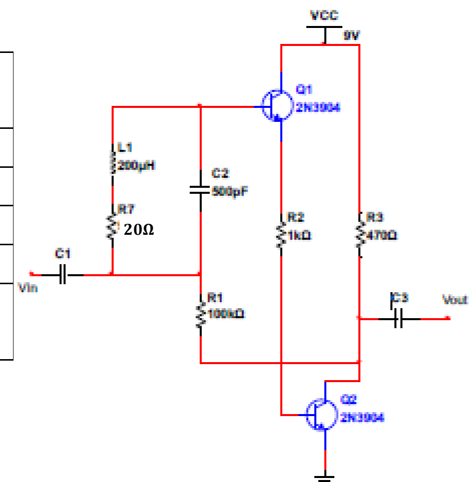
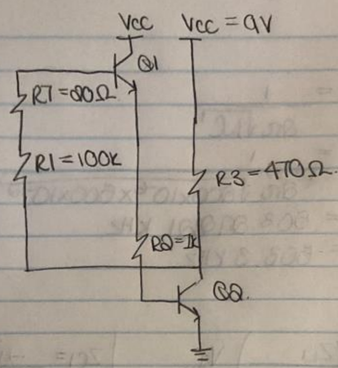


Figure 7: Receiving amplifier circuit.



$V_{CC} = I_3R_3 + I_{B1}(R_7+R_1) + I_{E1}R_2 + 2V_{BE(ON)}$

$I_3 = I_{C2} + I_{B1}$
$\quad = \beta I_{B2} + I_{B1}$, but $I_{B2} = I_{E1} = (\beta+1)I_{B1}$
$\quad = \beta(\beta+1)I_{B1} + I_{B1}$
$\quad = I_{B1}\left[\beta(\beta+1)+1\right]$

$= \left[\beta(\beta+1)+1\right]I_{B1}R_3 + I_{B1}(R_7+R_1) + (\beta+1)I_{B1}R_2 + 2V_{BE(ON)}$

Solving,
$9 = \left[160(161)+1\right]I_{B1}(0.47) + I_{B1}(0.02+100) + (161)(1)I_{B1} + 2(0.7)$

$7.6 = 12368.69\,I_{B1}$

$I_{B1} = 614.46472\ldots\ nA$

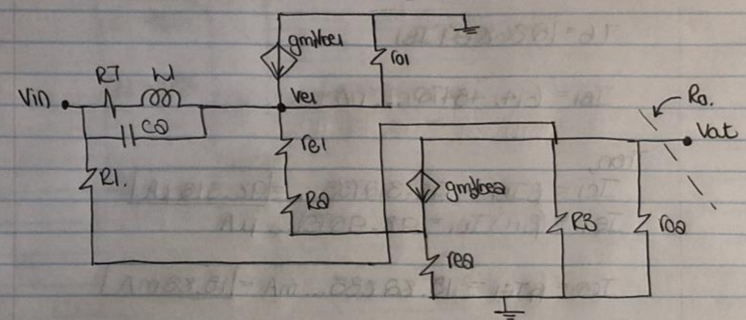
Then,
$I_{C1} = \beta I_{B1} = 98.312755\ldots = \boxed{98.313\ \mu A}$
$I_{E1} = (\beta+1)I_{B1} = 98.92751\ldots\ \mu A$

$I_{C2} = \beta I_{E1} = 15.82835\ldots\ mA = \boxed{15.83\ mA}$

$V_{CE2} = V_{CC} - (I_{B1} + I_{C2})R_3$
$\quad = 9 - (614.45\ldots\times10^{-6} + 15.82\ldots)(0.47)$
$\quad = 1.560383\ldots$
$\quad = \boxed{1.56\ V}$

$V_{CE1} = V_{CC} - I_{E1}R_2 - V_{BE(ON)}$
$\quad = 9 - (98.9\ldots\times10^{-3})(1) - 0.7$
$\quad = 8.20107\ldots$
$\quad = \boxed{8.20\ V}$

To calculate the small signal gain,



① Assume r_{o1} and r_{o2} are great enough to ignore.

calculating needed parameters,

$$g_{m2} = \frac{I_{CQ}}{V_T} = \frac{15.82\ldots\ mA}{25\ mV} = 0.633134\ \Omega^{-1}$$

$$r_{e1} = \frac{V_T}{I_{E1}} = \frac{25\ mV}{98.927\ldots\ \mu A} = 0.252711\ldots\ k\Omega$$

$$r_{e2} = \frac{V_T}{I_{E2}} = \frac{V_T}{(\beta+1)I_{E1}} = \frac{25\ mV}{(161)(98.927\ldots)\ \mu A} = 0.00156963\ k\Omega$$

① $R_o = \left(\frac{r_{e1}+R_2}{\beta+1} + R_1 + r_{e2}\right) // R_3$ assuming $r_{o1}/r_{o2} \to \infty$

but R_3 is significantly smaller than R_1, let alone the series equivalent resistance so,

$R_o \approx R_3$.

⑤ Also, $v_{be2} = \left(\frac{(\beta+1)r_{e2}}{(\beta+1)r_{e2} + r_{e1} + R_2}\right) V_{in}$.

⑥ Then, $V_{out} = -g_{m2} V_{be2} R_3$ / by Vin

$$A_V = -g_{m2} R_3 \left(\frac{(\beta+1)r_{e2}}{(\beta+1)r_{e2} + r_{e1} + R_2}\right)$$

$$= -0.633\ldots \cdot 10^3 \cdot 0.47 \cdot \left(\frac{161 \cdot 0.0015\ldots}{161 \cdot 0.0015\ldots + 0.252\ldots + 1}\right)$$

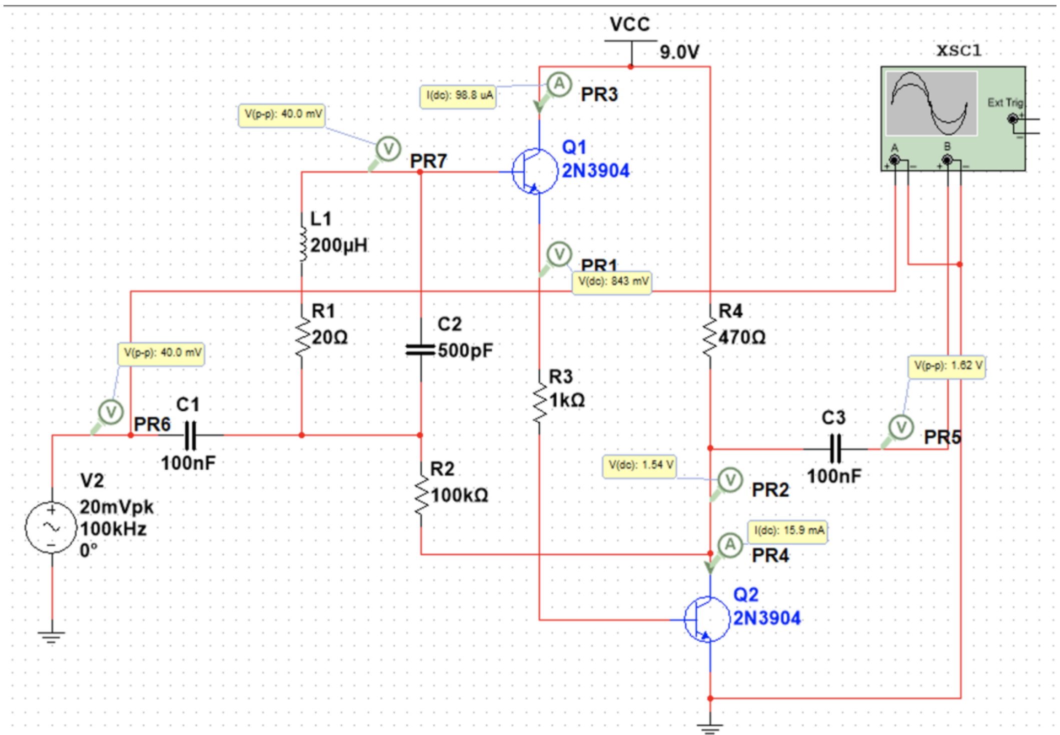
$$= -49.9526\ldots$$

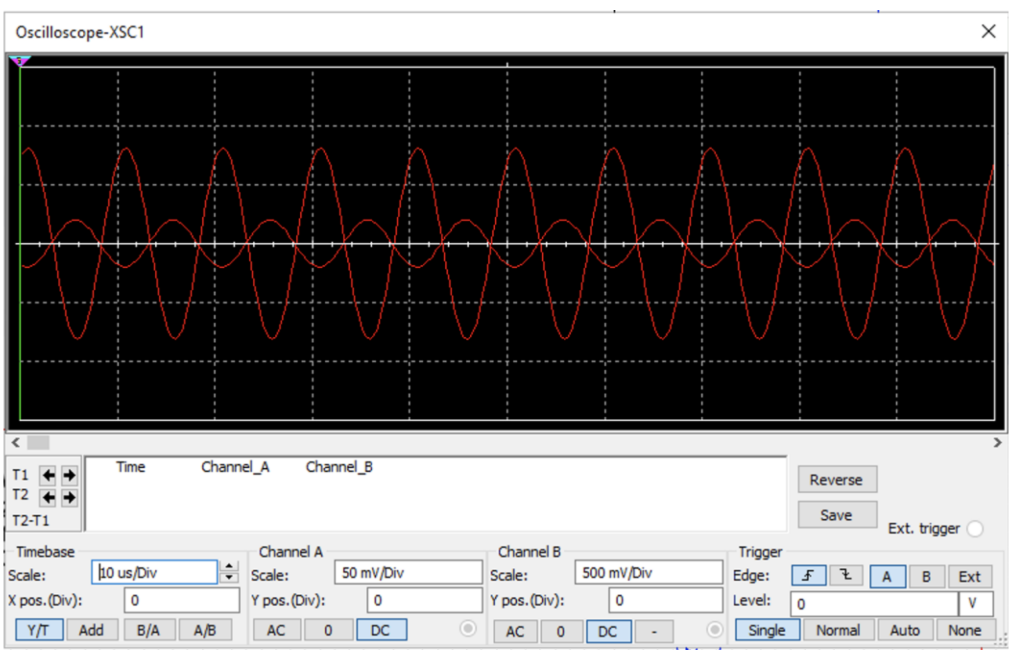
so,

$\boxed{A_V \approx -50}$

b) Simulate the circuit in Figure 7 to verify the results you got from your calculations and add them to the same table. Take a screenshot for the simulation with the results of the DC simulations and add it below. Add your simulated results plot below and save your simulation filed as "Proj-A-2b. ms14".

Note, an AC signal was applied to the input in order to determine the small signal gain.

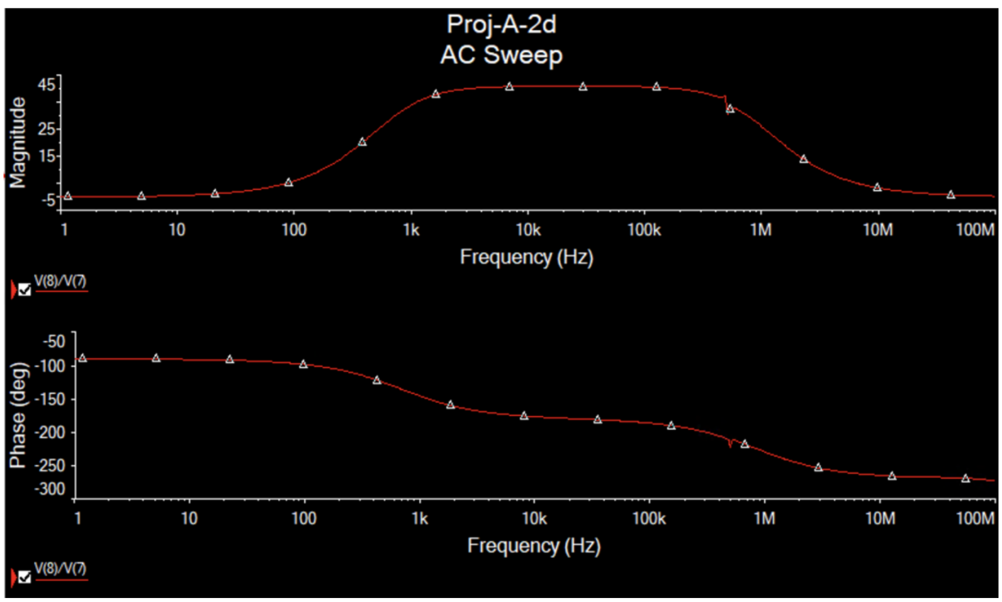




c) Is there a difference between the calculated and simulated values if so why?

Yes, there is a difference. There is a minor variation between the parameters calculated and those simulated due to assumptions made during calculation, such as VBE(on) = 0.7 V. This is not true for both transistors in the circuit, if the VBE voltages are measured. Also, the VA effect was ignored, which will impact the currents and voltages calculated. Another assumption made was that C1 and C3 are zero impedance, which is not technically true. They are negligible, but do still present a slight impedance.

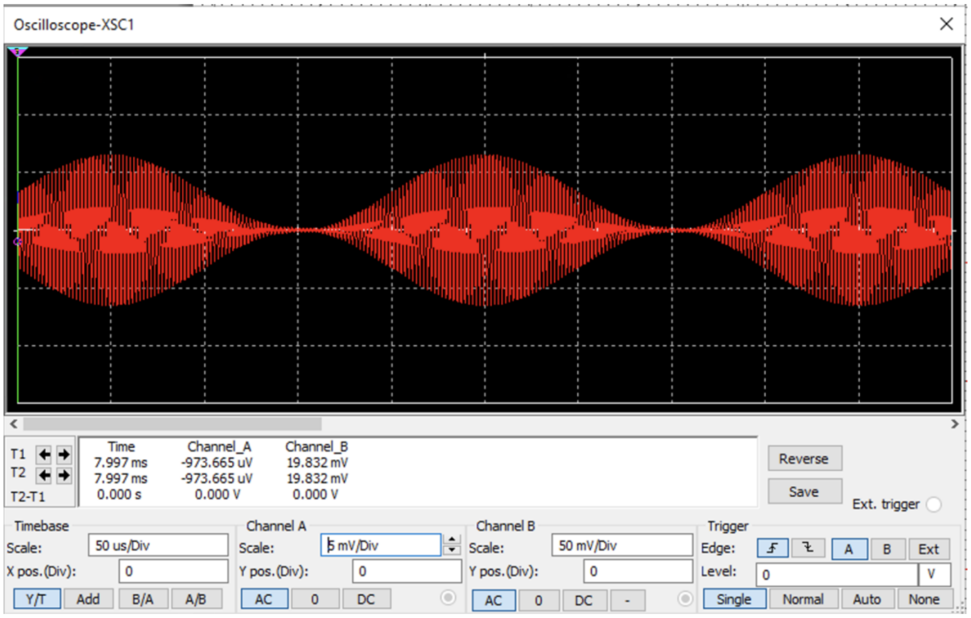
d) Apply an AC signal to the input of the active filter in Figure 7, and Set the amplitude about 10 mV peak. Using AC analysis, plot the small signal gain of the circuit. Add your simulated results plot below and save your simulation filed as "Proj-A-2d. ms14



e) Explain why there is a glitch at resonance frequency?

The glitch that occurs at the resonance frequency is likely due to the fact that at this point, the inductor and capacitor combined have extremely high impedance. As such, it is as if the base of Q1 is floating and the output wavers unpredictably. This is why we see a glitch.

f) Apply amplitude modulated signal to the input of the active filter in Figure 7 with carrier frequency of 500 kHz and modulating frequency of 5 kHz. Set the amplitude about 1mV peak. Plot the input and output waveform in an oscilloscope. Add your simulated results plot below and save your simulation filed as “Proj-A-2f. ms14”.



g) What is the gain of the circuit?

The small signal gain is -32.5 (by inspection using the oscilloscope).

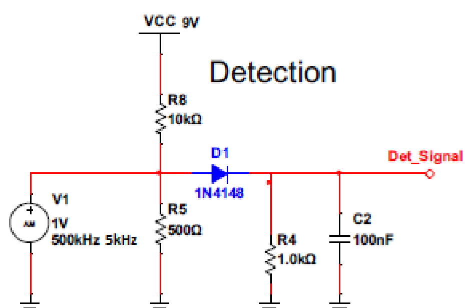
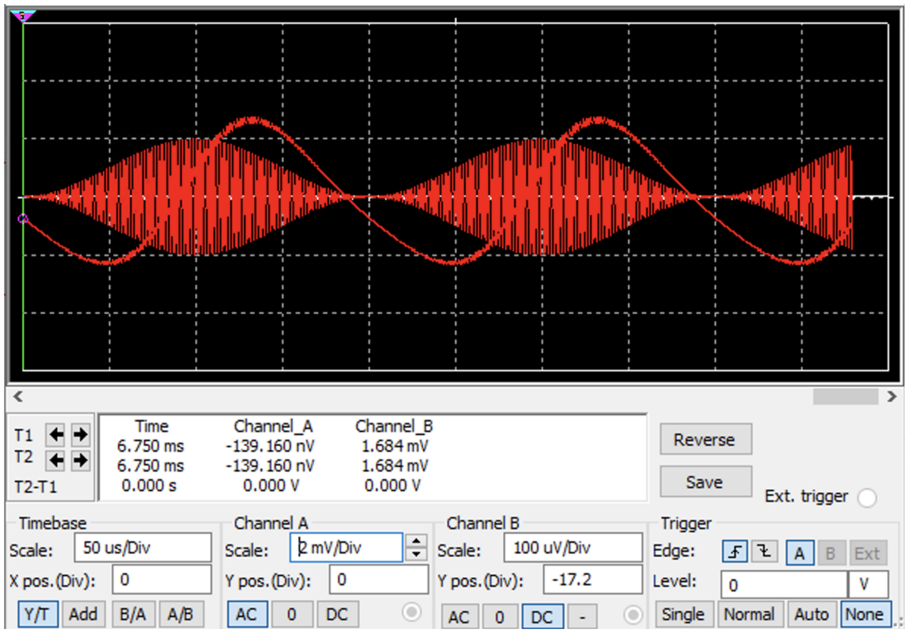


Figure 8: Detection Circuit

h) Observe and test the response of the detection circuit shown in Figure 8. Connect the circuit shown in Figure 8 at the output of the active filter circuit shown in Figure 7. Observe the detected signal in an oscilloscope. Plot the input and output waveform in an oscilloscope. Add your simulated results plot below and save your simulation filed as “Proj-A-2h. ms14”.



Part B:

Hints:

1. Be careful when you are designing sub-systems so that they don't face the loading effect.
2. In the detection circuit, the diode should be biased properly to get the modulated signal rectified!

1. Design and simulate the base-band amplifier shown in Figure 9 with a small signal gain of about 20 and of quiescent point about (6 V, 1.5 mA). Present both simulated input and output signal.
   [Hints: Consider an input sinusoidal signal of several kHz to perform the analysis and simulation.]

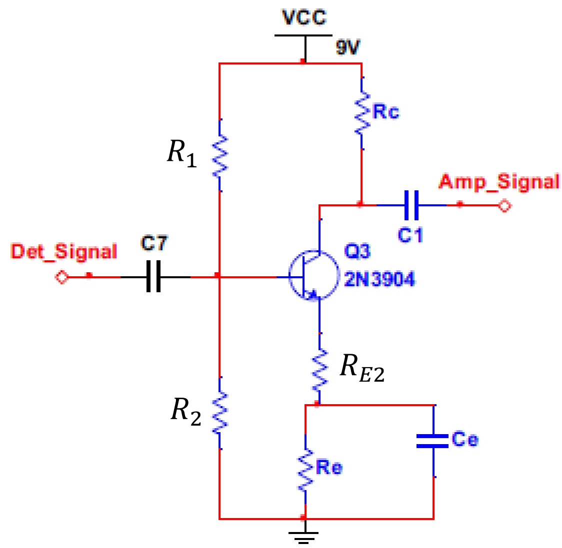


Figure 9: Baseband Amplifier

a) Show your design procedure and record your values below.

Parameter	Value
R_1	160k
R_2	25.4k
R_e	145
RE2	72.5
R_c	1.8k
C_e	20u
C_7	1u
C_1	1u

Parameter	Calculated/Designed for	Simulation
V_{CE}	6 V	5.93 V
I_C	1.5 mA	1.52 mA
Small signal Gain	-20	-19.7

Initial design process:

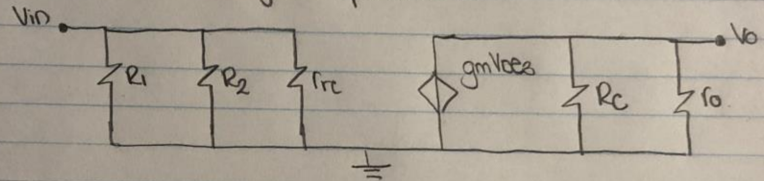
start by trying if $R_{E2}=0$ (change later on if it doesn't work).

① Then we can write

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \qquad \text{Assuming } I_C \approx I_E$$
$$= I_C(R_C + R_E) + V_{CE}$$

$$9 = 1.5(R_C + R_E) + 6 \Rightarrow R_C + R_E = 2k\Omega \leftarrow \text{combined!}$$

② Then, the small signal equivalent is:



we can write,

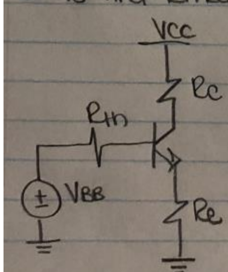
$$V_o = -g_m V_{be2}(R_C \,//\, r_o)$$
$$-A_V = g_m(R_C//r_o)$$
$$20 = 0.06\times10^3\left(\frac{1}{1/R_C + 1/80k}\right)$$
$$R_C = 0.334708\ldots k\Omega$$
$$= \boxed{330\,\Omega}$$

$$g_m = \frac{I_C}{V_T} = \frac{1.5mA}{25mV} = 0.06\Omega^{-1}$$

$$r_o = \frac{V_A}{I_C} = \frac{120V}{1.5mA} = 80k\Omega$$

③ This means that $R_E = 2 - R_C = 1.665271\ldots = \boxed{1.665k\Omega}$

④ To find R1/R2



• set $V_{BB} = 4.5V$ which will allow us to say $R1 = R2 = R$

$R_{th} = R1//R2 = R/2$

Then,

$$V_{BB} - I_B R/2 = V_{BE(ON)} + I_E R_E$$
$$V_{BB} - \frac{I_C}{\beta}\frac{R}{2} = V_{BE(ON)} + \frac{(\beta+1)}{\beta} I_C R_E$$
$$4.5 - \frac{1.5}{160}\frac{R}{2} = 0.7 + \frac{(161)}{160}(1.5)(1.66\ldots)$$
$$R = 274.4494\ldots = \boxed{274.449k\Omega}$$

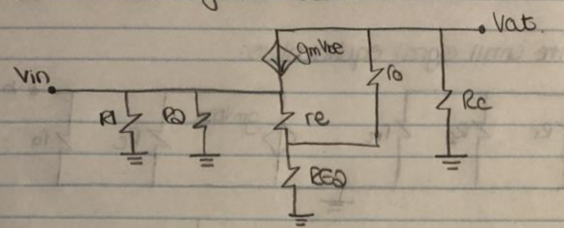
However, with the above design it was noticed that the output was clipping. Therefore the circuit was redesigned with a non-zero value for RE2, as shown below.

From previous work done, we know that.

① $R_C + R_E + R_{E2} = 2k$, $V_{CE} = 6\,V$ $I_C = 1.5\ mA$

If we make the decision $R_E = 2R_{E2}$ then this reduces to.
$2k = R_C + 3R_{E2}$

② The small signal model is:



Now, assume $r_o \to \infty$

g_m = remains the same $= 0.06\,\Omega^{-1}$

$r_e = \dfrac{V_T}{I_C} = \dfrac{25mV}{1.5mA} = 16.\bar{6}\,\Omega$

we can then write,

$V_{out} = -g_m V_{be} R_C$, $V_{be} = \left(\dfrac{r_e}{r_e + R_{E2}}\right) V_{in}$

$A_V = -g_m \left(\dfrac{r_e}{r_e + R_{E2}}\right)(2k - 3R_{E2})$.

$20 = (0.06)\left(\dfrac{16.\bar{6}}{16.\bar{6} + R_{E2}}\right)(2000 - 3R_{E2})$.

solving,

$\boxed{R_{E2} = 72.5\,\Omega}$ $\boxed{R_C = 2k - 3R_{E2} = 1.8k}$

$\boxed{R_E = 2R_{E2} = 145\,\Omega}$

③ To determine R1/R2.

we know that:

$V_B = (R_E + R_{E2}) I_E + 0.7$ assuming $I_C \approx I_E$

$V_B = 1.026\ V$

we also know that:

$I_B = I_C/\beta = 1.5mA/160 = 9.375\ \mu A$.

Then, $\dfrac{9 - V_B}{R_1} > I_B$ we need to supply at least this much current

Then, assume $I_1 = 50\ \mu A$.

$\dfrac{9 - V_B}{R_1} = 50\ \mu A \Rightarrow$ yields $\boxed{R_1 = 160\ k.}$

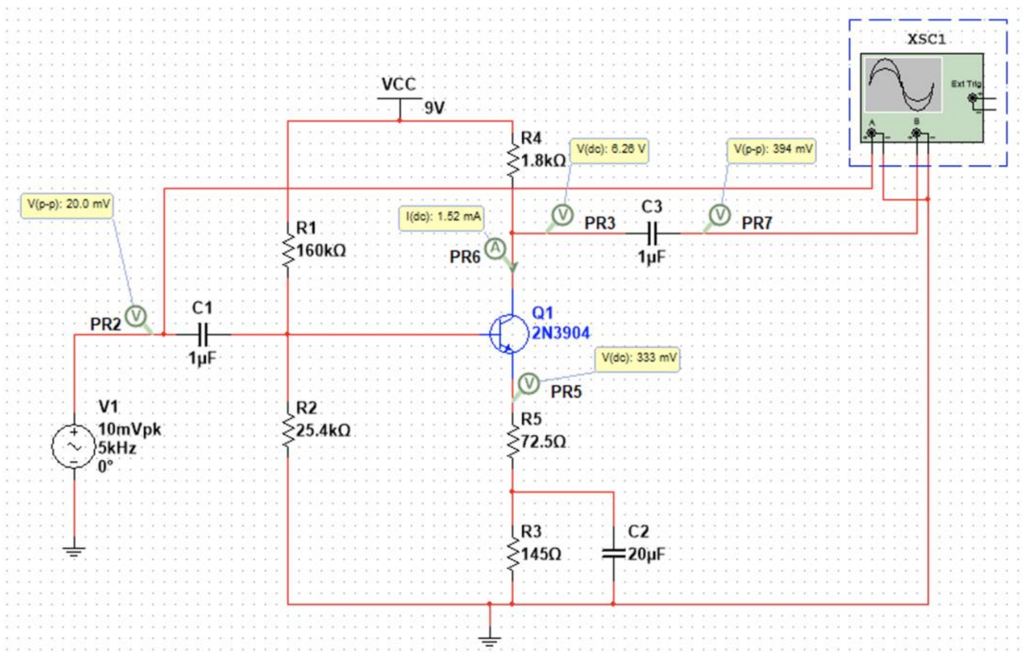
This then means that,

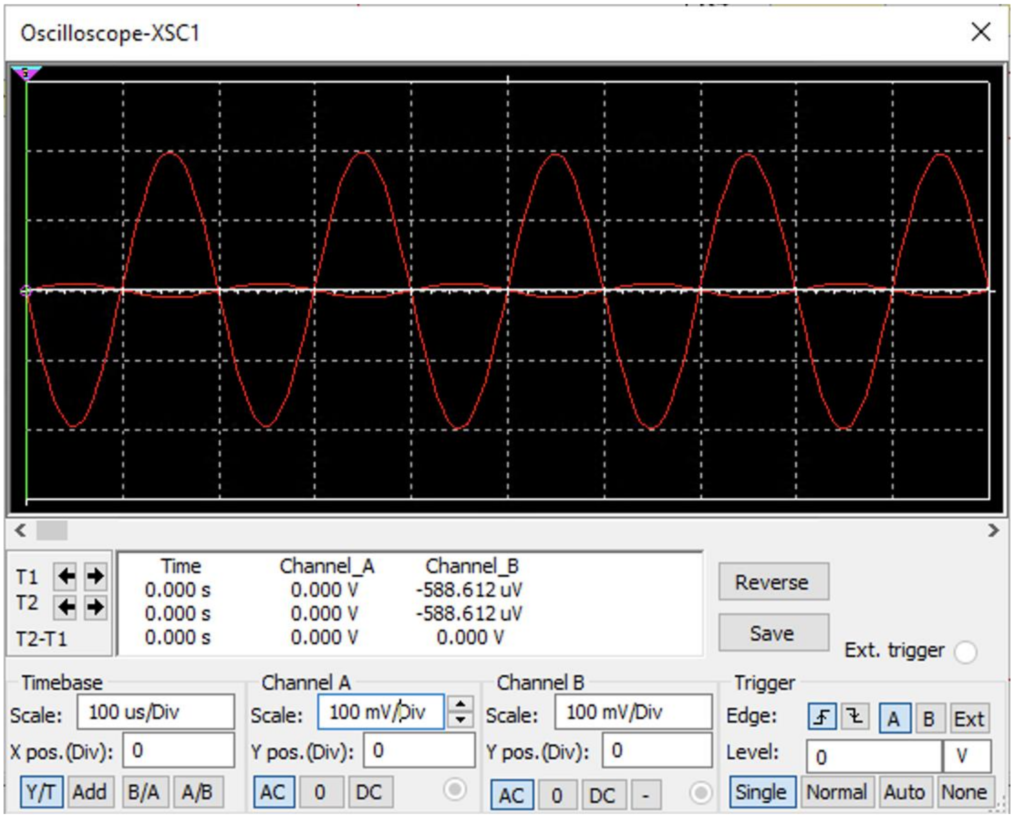
$R_2 = \dfrac{V_2}{I_{R2}} = \dfrac{V_B}{I_1 - I_B} \Rightarrow$ yields $\boxed{R_2 = 26.4k}$

Note that the capacitor values were obtained by using trial and error through simulation. They were initially all set to 1uF and seeing that the phase difference between the input and output signals was less than 180 degrees, each capacitor was experimented with. It was noticed that changing Ce to 20 uF set the phase difference to 180 degrees, so that was changed, while the other 2 were kept at 1 uF.

b) Simulate the circuit in Figure 9 to verify the results you got from your calculations and add them to the same table. Take a screenshot for the simulation with the results of the DC simulations and add it below. Add your simulated results plot below and save your simulation filed as “Proj-B-1b. ms14”.

Note, an AC input signal was applied to determine the small signal gain.

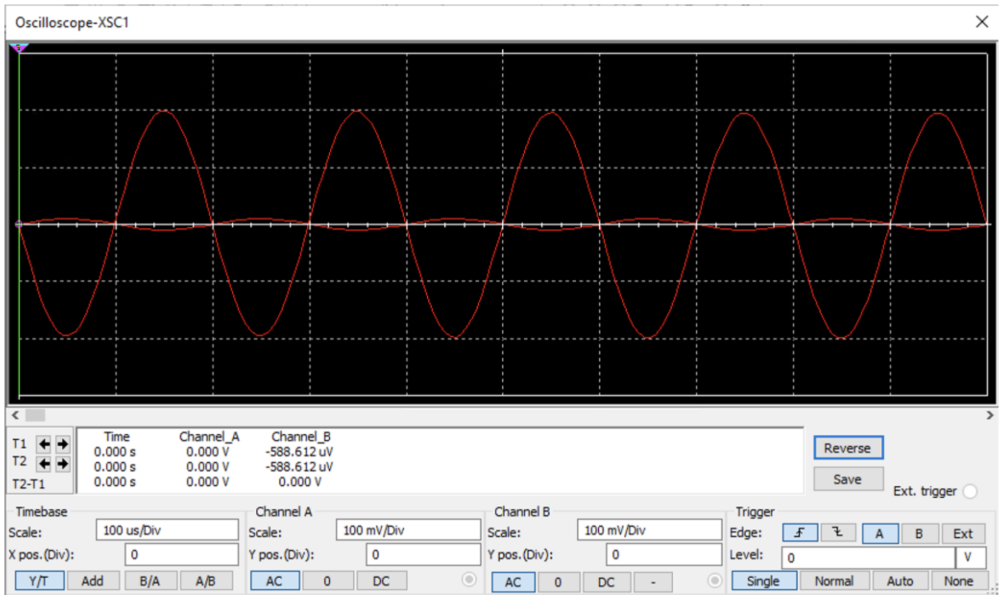




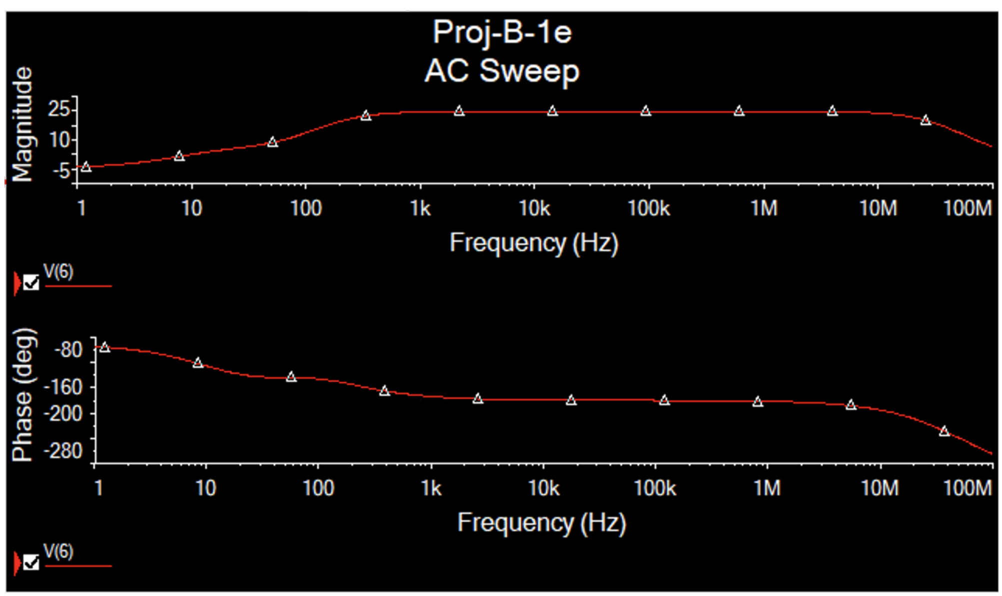
c) Is there a difference between the calculated and simulated values if so why?

Yes, once again, the calculated values yield a slightly different Q point and gain of -19.7, instead of 20. This difference is acceptable and makes sense due to the fact that once again VBE voltages were not precisely 0.7 V in the simulation. Also, for the design calculations, the assumption that IC ~= IE is made throughout. This is not true as there is a very slight difference, which can then be seen in the difference in the simulated Q point. Also, the output resistance of the BJT was assumed to be infinite, which is not entirely true. As usual, the VA effect was ignored during the design process and B was assumed to be constant (can change with IC). These all would affect the simulation results and create deviations from the calculations.

d) Apply an input signal to the input of the Baseband Amplifier in Figure 9. Set the signal Frequency to around 5 kHz and set the amplitude about 10 mV peak. Plot the input and output waveform in an oscilloscope. Add your simulated results plot below and save your simulation filed as “Proj-B-1d. ms14”.



e) Perform an AC analysis on your design and show the response over the frequency range from 1 Hz-100 MHz (choose log scaled frequency axis and around 100 point per decade). Add your simulated results plot below and save your simulation filed as "Proj-B-1e. ms14".



2. Design and simulate the output buffer amplifier shown in Figure 10 with a speaker resistance in the range of 8-16 Ω. Present both simulated input and output signal.

    [Hints: Consider an input sinusoidal signal of several kHz to perform the analysis and simulation. Also, consider quiescent point of Q4 as (8V, 40 uA) and Q5 as (8.5 V, 6.5 mA)]

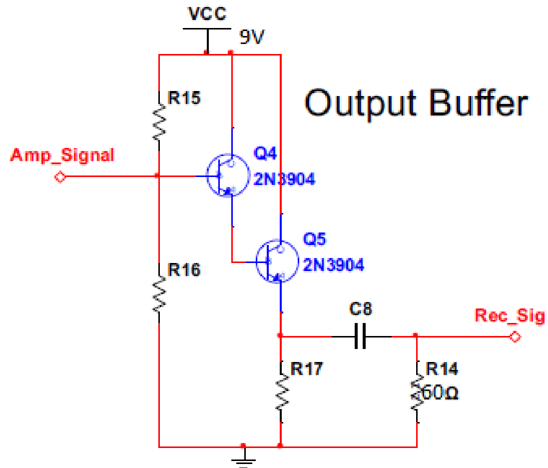


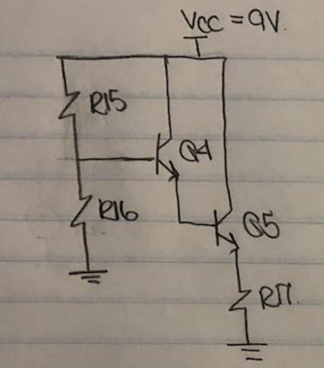
Figure 10: Output Buffer

a) Show your design procedure and your values below.

Parameter	Value
R_{15}	100k
R_{16}	27k
R_{17}	77
C_8	20u

Parameter	Calculated/Designed for	Simulation
V_{CE4}	7.8 V	7.68 V
V_{CE5}	8.5 V	8.40 V
I_{C4}	40.4 uA	43.9 uA
I_{C5}	6.5 mA	7.77 mA
Small signal Gain	1	0.83

Initial design:



$R_{th} = R15 // R16$.

Setting the Q point of Q8 to 8.5V and 6.8mA,

$R17 = \frac{9 - 8.5}{6.8} = \boxed{76.92\Omega}$ $(I_C \approx I_E)$.

We also know that $V_{B4} = 9 - 8.5 + 2(0.7) = 1.9\,V$

This means that $1.9 = \left(\frac{R16}{R16 + R15}\right)(9)$.

set $\boxed{R15 \text{ to } 5k\Omega}$ then R16 is:

$R16 = 1.3380\ldots = \boxed{1.34k\Omega}$

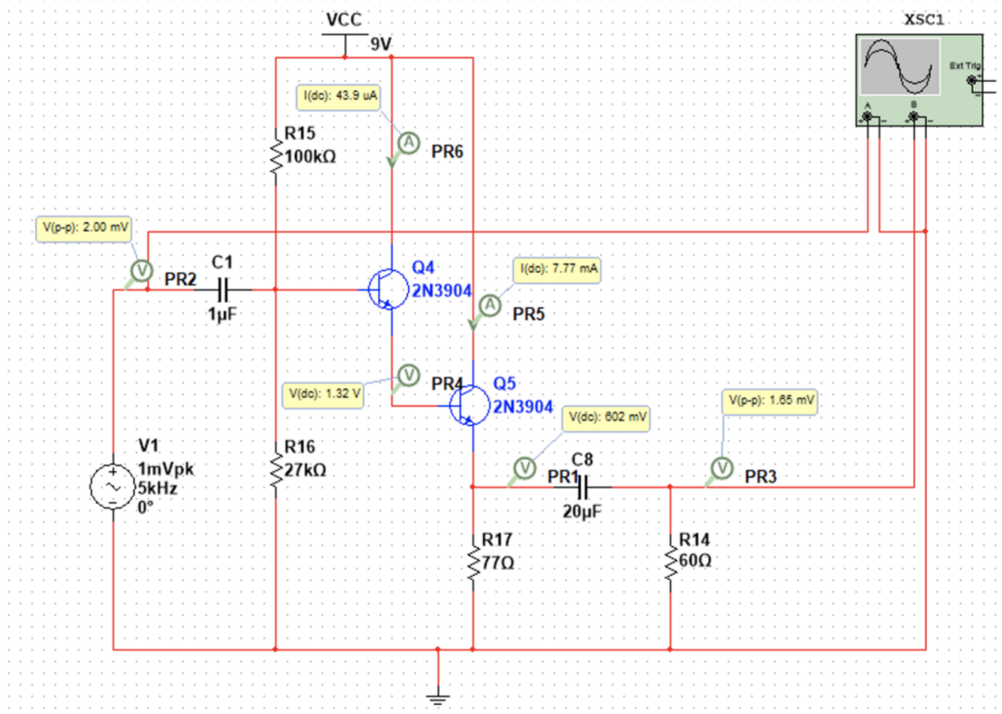
$I_{B4} = \frac{I_{C5}}{\beta(\beta+1)} = \frac{6.5}{160(161)} = 252.329\,nA$

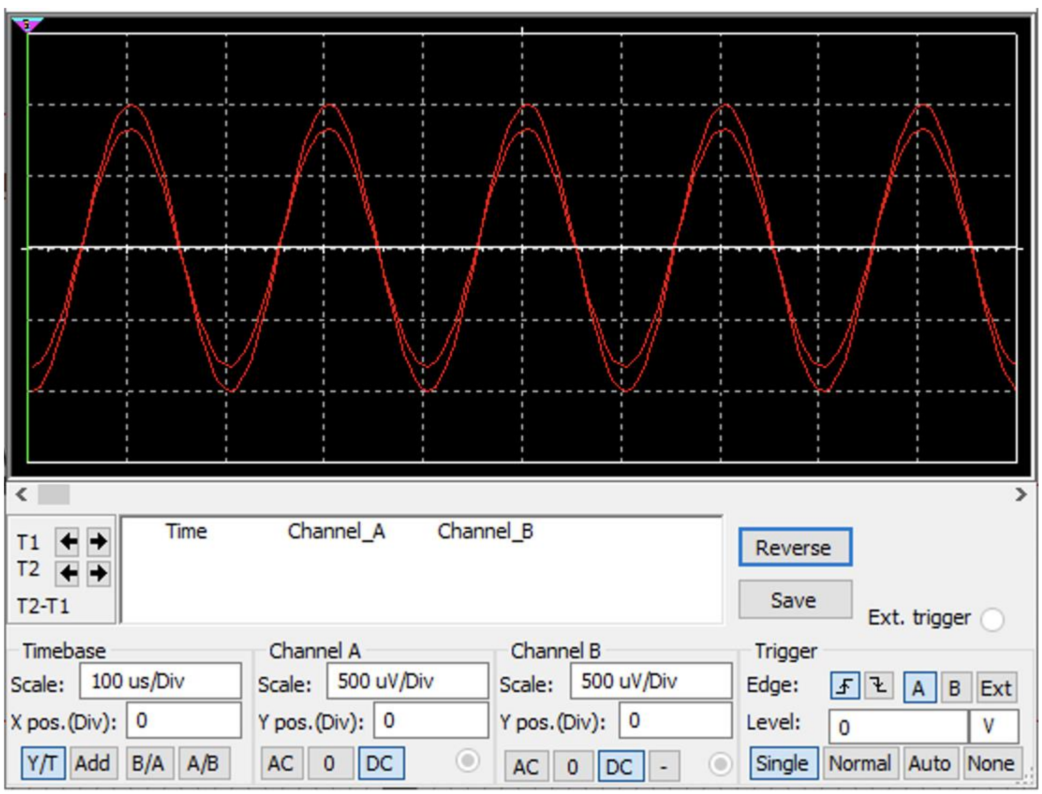
After simulating and loading the previous part of the circuit with the buffer, we noticed the loading effect occuring. To combat this, we tweaked R15 and R16 to better imepdance match the preceding baseband amplifier. This was done by simply choosing R15 as 100k, and then using the voltage divider relation between R15 and R16 to find R16 to be 27k.

Also note that C8 was chosen based on previous experience designing for the bandpass amplifier. We intially simulated with 20uF and since it worked within the circuit, we used that value.

b) Simulate the circuit in Figure 10 to verify the results you got from your calculations and add them to the same table. Take a screenshot for the simulation with the results of the DC simulations and add it below. Add your simulated results plot below and save your simulation filed as "Proj-B-2b. ms14".

Note C1 in the circuit was added for the sake of the simulation (to ensure proper biasing). R16 and R17 were rounded up from the calculated values as they yielded better Q points. An AC input signal was added to measure the small signal gain.

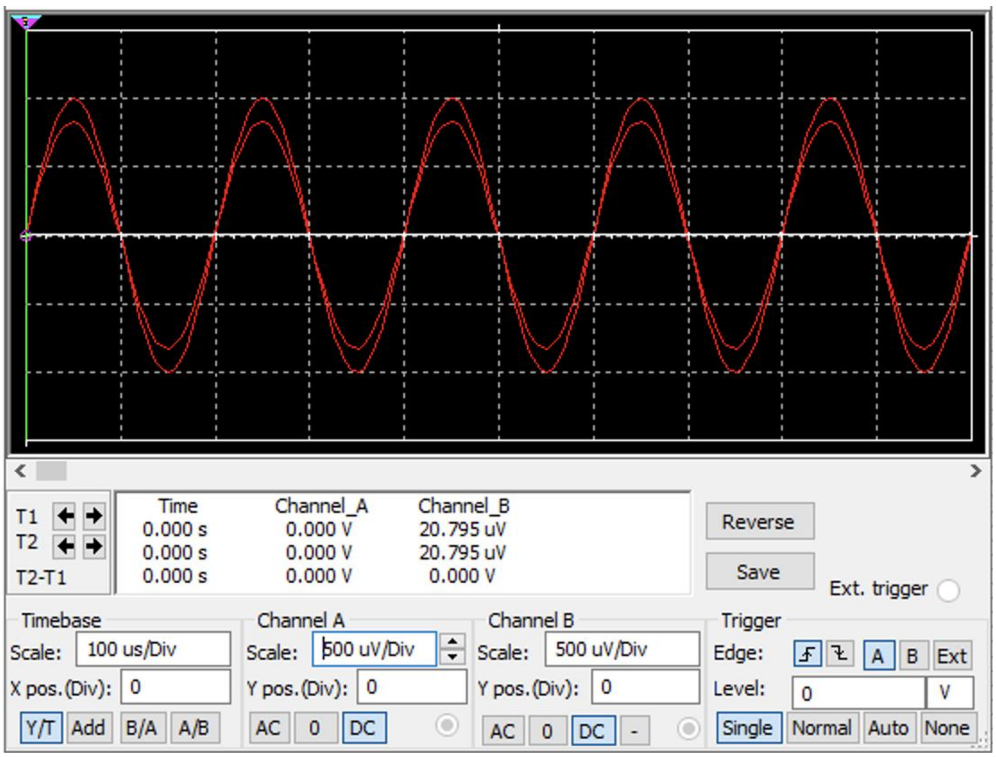




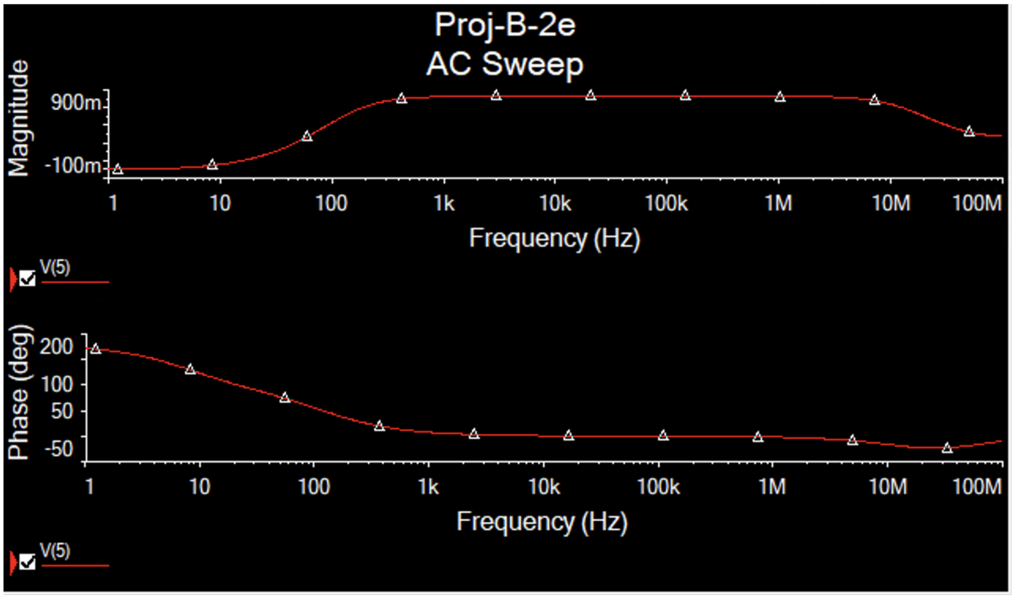
c) Is there a difference between the calculated and simulated values if so why?

Yes there is. This can be because of a variety of different reasons. One, the assumption that IC ~= IE is made at the beginning. We know that this is not exactly true. As usual, VBE was assumed to be 0.7 V, which is not necessarily true. Once again, the VA effect was ignored, and B was thought to be constant. All of these factors cause the simulation values to be slightly different than those calculated.

d) Apply an input signal to the input of the output buffer in Figure 10. Set the signal Frequency to around 5 kHz and set the amplitude to 1 mV peak. Plot the input and output waveform in an oscilloscope. Add your simulated results plot below and save your simulation filed as "Proj-B-2d. ms14".



e) Perform an AC analysis on your output buffer design and show the response over the frequency range from 1 Hz-100 MHz (choose log scaled frequency axis and around 100 point per decade). Add your simulated results plot below and save your simulation filed as "Proj-B-2e. ms14".



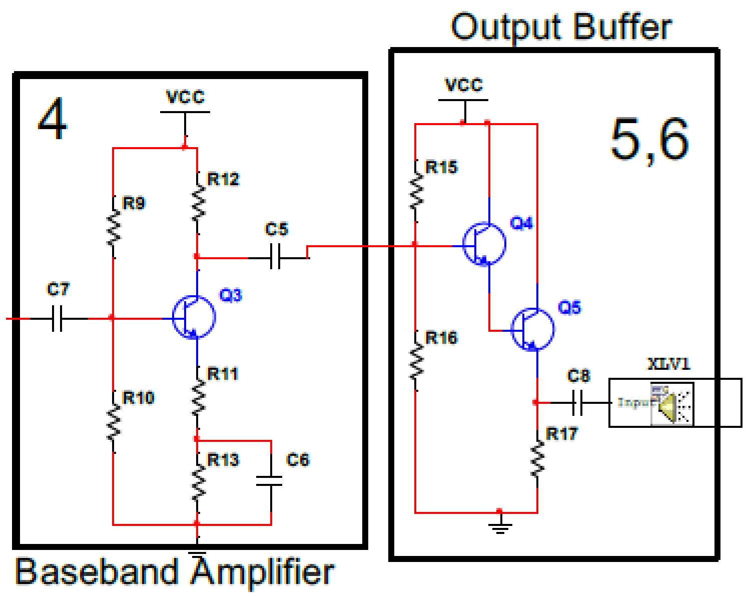
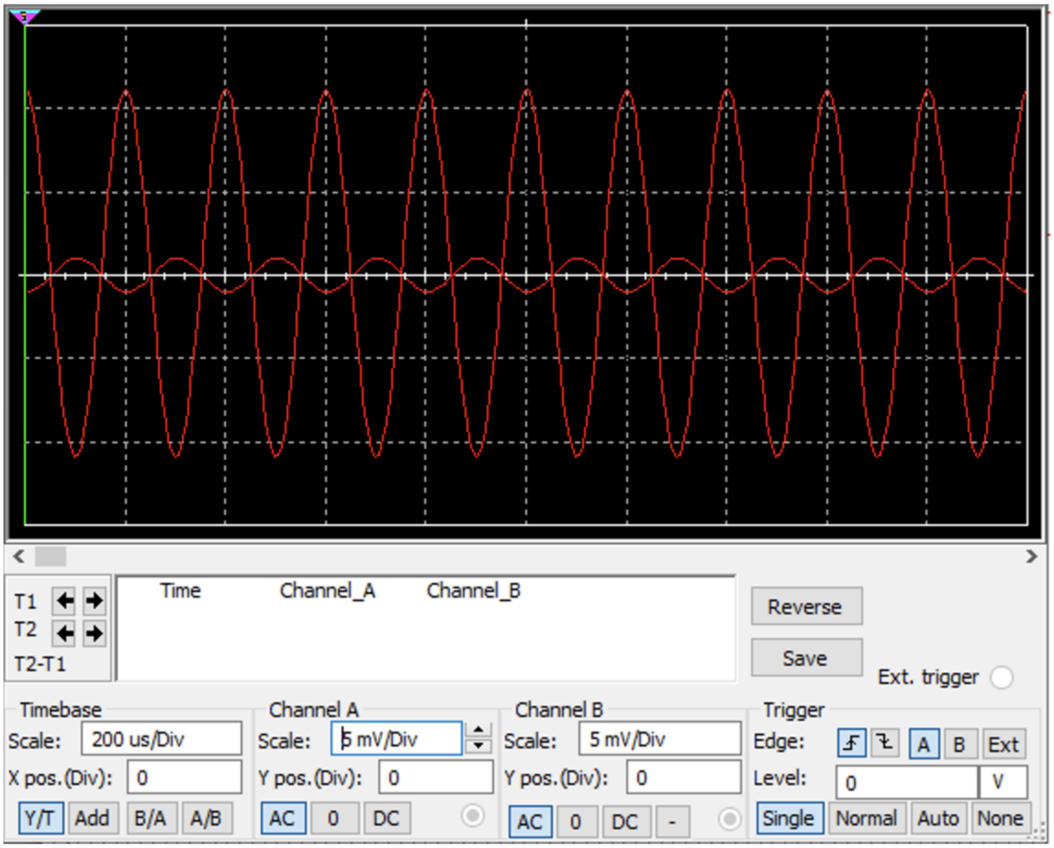


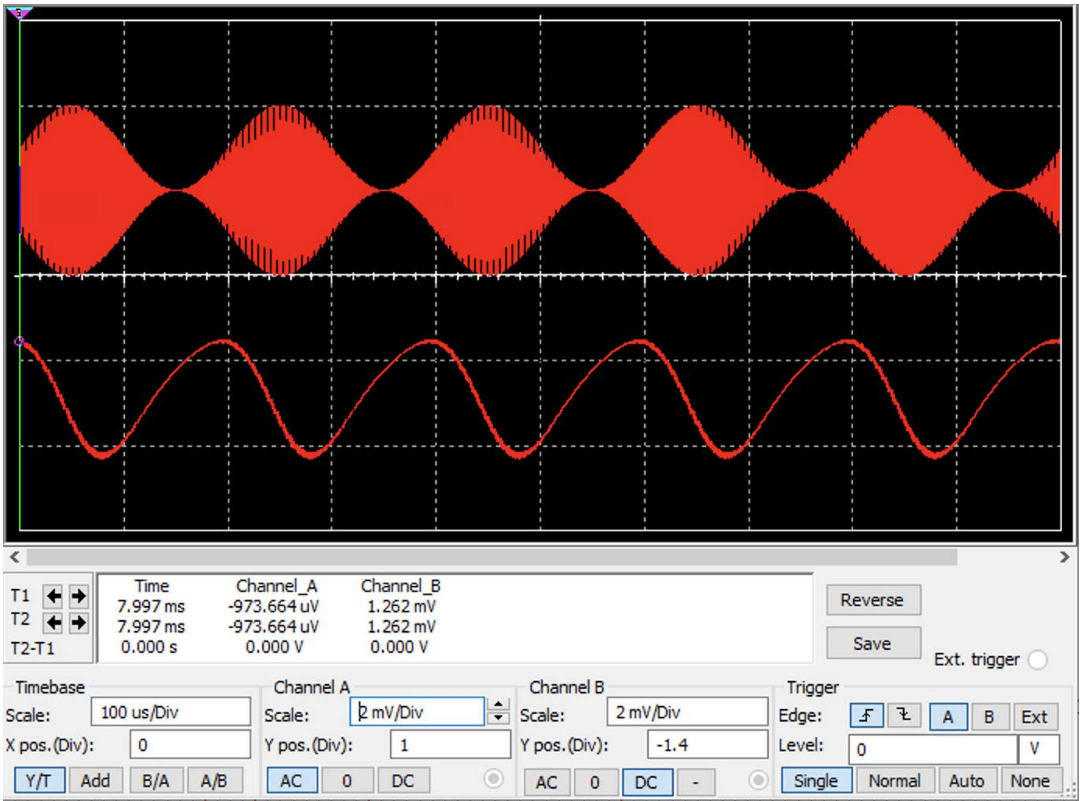
Figure 11: AM receiver sub-circuits.

3. Construct the circuit shown in Figure 11 by connecting individual circuit simulated in 1-2. Present both input and output voltage waveforms. Add your simulated results plot below and save your simulation filed as “Proj-B-3. ms14”.
   [You should see a sinusoidal voltage at the output.]



Part C:

1. **Implement an AM receiver circuit shown in Figure 4: AM receiver circuit.** Apply an AM modulated signal and observe the response of your receiver circuit. Add your simulated results plot below and save your simulation filed as "Proj-C-1.ms14".



Part D:

1. Video link:
   https://www.youtube.com/watch?v=G09PH6DSO7E&feature=youtu.be&fbclid=IwAR06rAxS9ts_UB4O_v3deaAF51K-g3p4_GDZ57311NILOuEmrYW7fXtWnqA