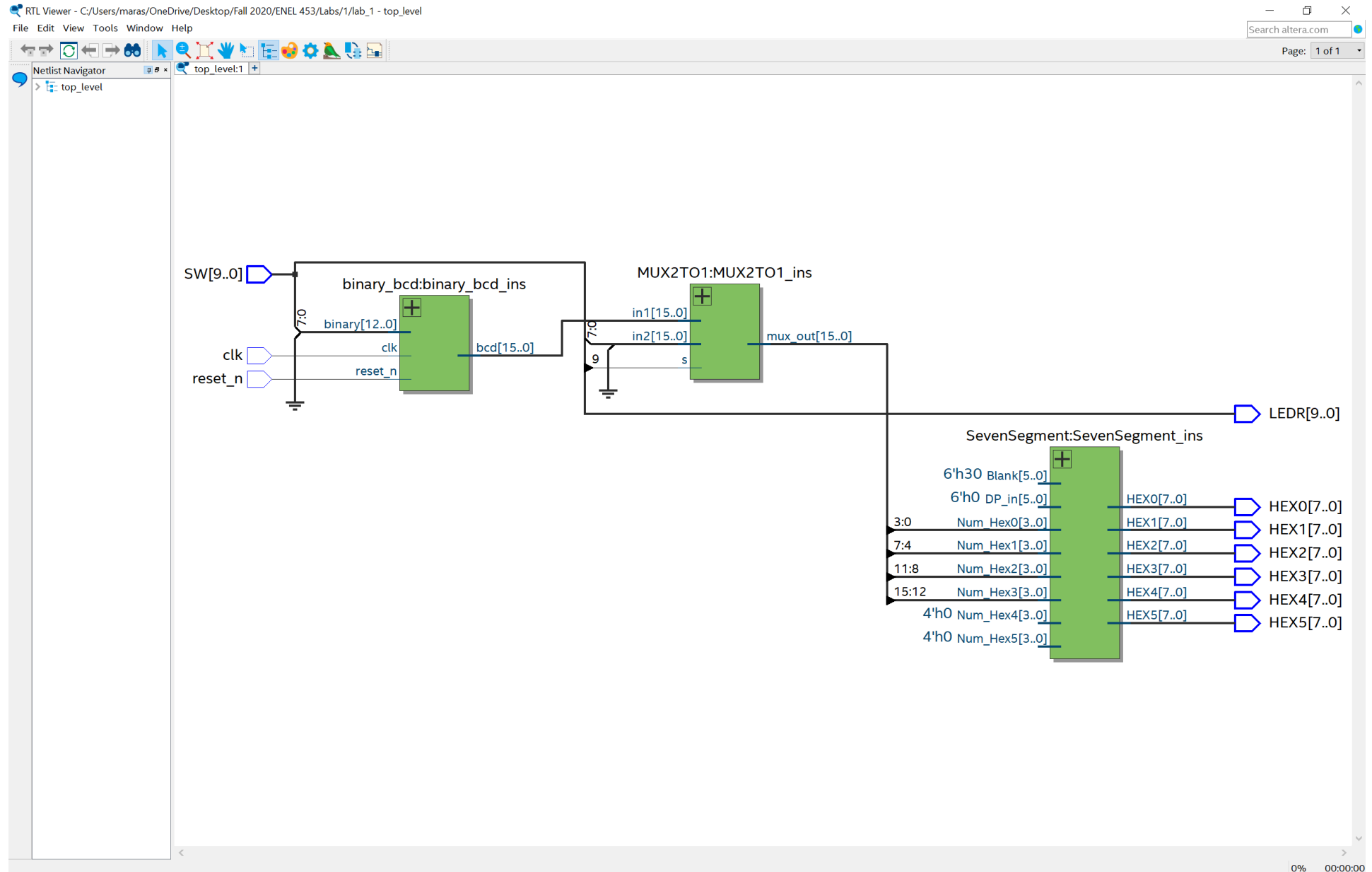


Lab 1 Design Record

Students: Maral Rasuli Arasi, Alaa Khalil, Ruha Javed

RTL Viewer:



Fmax Summary for 85C Model:

Quartus Prime Lite Edition - C:/Users/maras/OneDrive/Desktop/Fall 2020/ENEL 453/Labs/1/lab_1 - top_level

File Edit View Project Assignments Processing Tools Window Help

top_level

Project Navigator

- Files
 - top_level.SDC
 - top_level.vhd
 - top_level.sdc
 - top_level.qsf
 - SevenSegment_decoder.vhd
 - SevenSegment.vhd
 - binary_bcd.vhd
 - MUX2TO1.vhd

Tasks

Compilation

- Task
 - Design Assistant (Post-Mapping)
 - I/O Assignment Analysis
 - Fitter (Place & Route)
 - Assembler (Generate programming files)
 - Timing Analysis
 - Edit Settings
 - View Report
 - Timing Analyzer
 - EDA Netlist Writer
 - Edit Settings
 - Program Device (Open Programmer)

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global S
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
 - Flow Messages
 - Flow Suppressed Message
- Assembler
- Timing Analyzer
 - Summary
 - Parallel Compilation
 - SDC File List
 - Clocks
 - Slow 1200mV 85C Model
 - Fmax Summary
 - Setup Summary
 - Hold Summary
 - Recovery Summary
 - Removal Summary
 - Minimum Pulse Width
 - Metastability Summa
 - Slow 1200mV 0C Model
 - Fast 1200mV 0C Model
 - Multicorner Timing Ana
 - Advanced I/O Timing
 - Clock Transfers
 - Report TCCS
 - Report RSKM
 - Unconstrained Paths
 - Messages

Slow 1200mV 85C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	146.82 MHz	146.82 MHz	clk	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX such that the duty cycle (in terms of a percentage) is maintained.

Partition Name

Netlist Type

Color

Recommendation: 0 of 0 for

Details...

Find...

Find Next

Messages

System (1)

Processing (134)

Task View

100% 00:00:02

Messages Window:

Quartus Prime Lite Edition - C:/Users/maras/OneDrive/Desktop/Fall 2020/ENEL 453/Labs/1/lab_1 - top_level

File Edit View Project Assignments Processing Tools Window Help

top_level

Project Navigator

Files

- top_level.SDC
- top_level.vhd
- top_level.sdc
- top_level.qsf

Tasks

Compilation

Task

Design Assistant (Post-Mapping)

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- Flow Summary
- Flow Settings
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- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Filter
- Flow Messages

Slow 1200mV 85C Model Fmax Summary

<<Filter>>

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IP Catalog

Installed IP

- Project Directory
 - No Selection Available
- Library
 - Basic Functions
 - DSP
 - Interface Protocols
 - Memory Interfaces and Controllers

+ Add...

Design Partiti...

Partition Name

Netlist Type

Color

Recommendation: 0 of 0 for

Find...

Find Next

Messages

System

Processing (22)

100% 00:00:02

18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.

13024 Output pins are stuck at VCC or GND.

18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.

292013 Feature LogicLock is only available with a valid subscription license. You can purchase a software subscription to gain full access to this feature.

15714 Some pins have incomplete I/O assignments. Refer to the I/O Assignment warnings report for details.

332174 Ignored filter at top_level.sdc(9): ADC_CLK_10 could not be matched with a port

332049 Ignored create_clock at top_level.sdc(9): Argument <targets> is an empty collection

332174 Ignored filter at top_level.sdc(11): MAX10_CLK2_50 could not be matched with a port

332049 Ignored create_clock at top_level.sdc(11): Argument <targets> is an empty collection

15705 Ignored locations or region assignments to the following nodes

334000 Timing characteristics of device 10M50DAF484C6GES are preliminary

334000 Timing characteristics of device 10M50DAF484C6GES are preliminary

171167 Found invalid Fitter assignments. See the Ignored Assignments panel in the Fitter Compilation Report for more information.

169177 12 pins must meet Intel FPGA requirements for 3.3-, 3.0-, and 2.5-V interfaces. For more information, refer to AN 447: Interfacing MAX 10 Devices with 3.3/3.0/2.5-V LVTTTL/LVCMOS I/O Systems.

18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.

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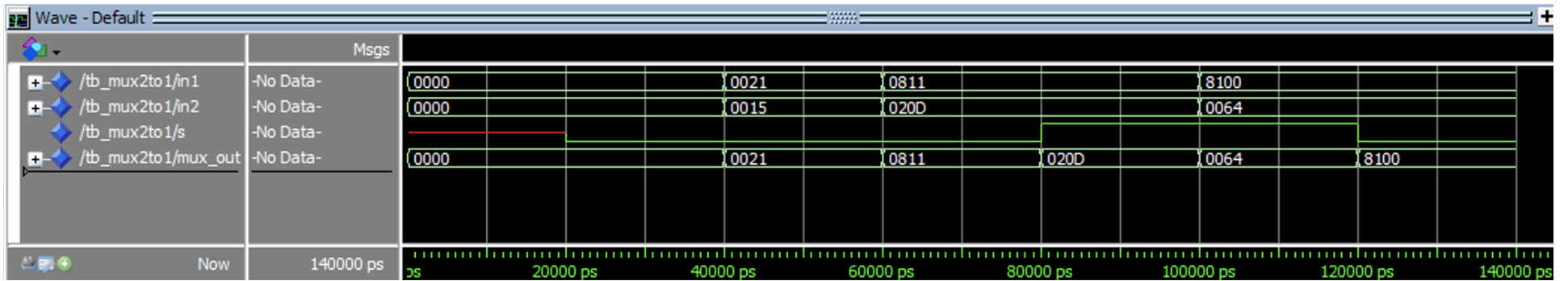
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MUX2TO1 Simulation:



top_level Simulation

