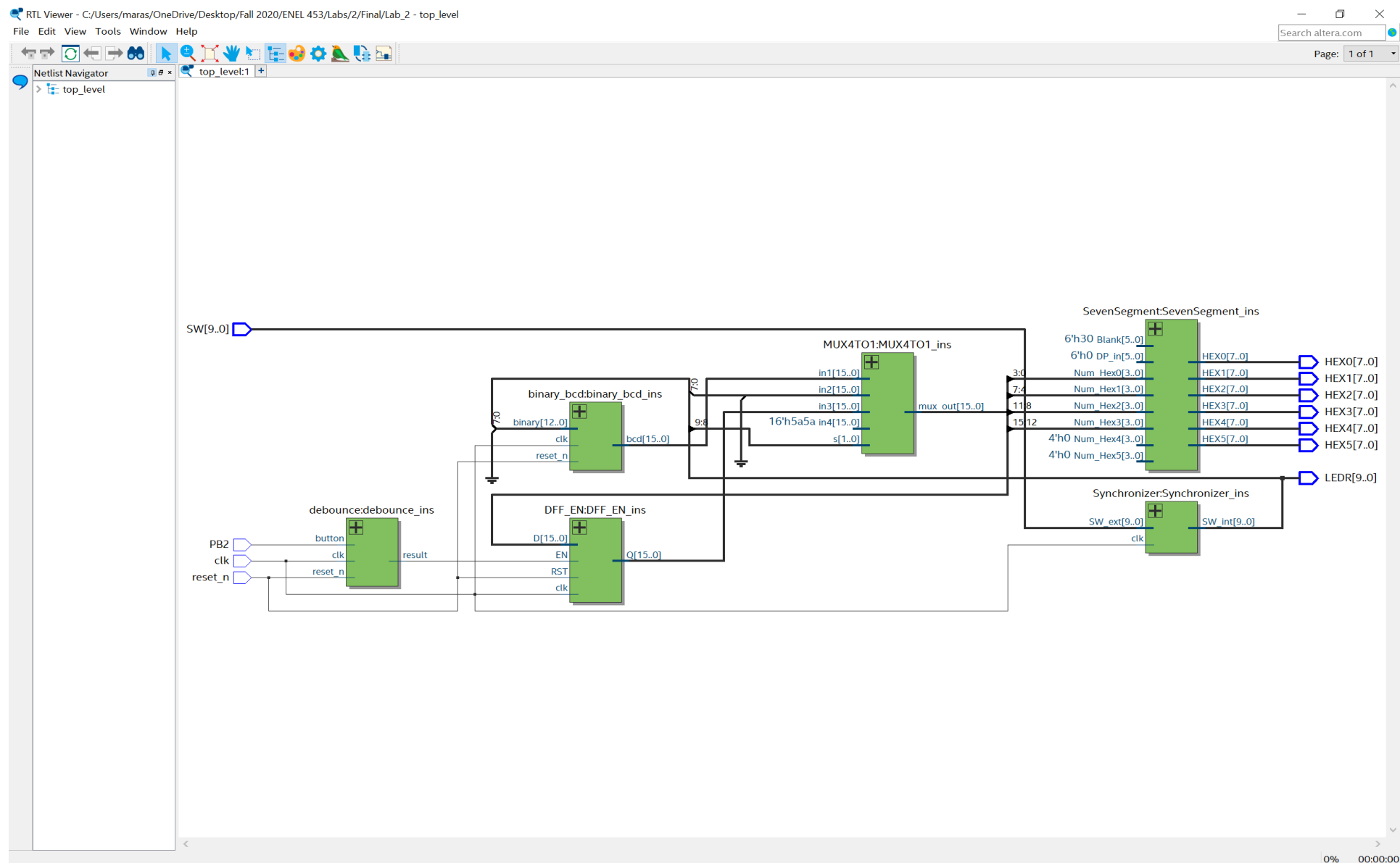


## Lab 2 Design Record

**Students:** Maral Rasuli Arasi, Alaa Khalil, Ruha Javed

### RTL Viewer:



## Fmax Summary for 85C Model:

Quartus Prime Lite Edition - C:/Users/maras/OneDrive/Desktop/Fall 2020/ENEL 453/Labs/2/Final/Lab\_2 - top\_level

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

top\_level

Project Navigator

Files

- top\_level.vhd
- top\_level.sdc
- top\_level.qsf
- SevenSegment\_decoder.vhd
- SevenSegment.vhd
- binary\_bcd.vhd
- MUX2TO1.vhd

Tasks

Compilation

- Task
- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programming)
- Timing Analysis
- Edit Settings
- View Report
- Timing Analyzer
- EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

Table of Contents

- Flow Summary
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- Parallel Compilation
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- Slow 1200mV 85C M
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- Fast 1200mV 0C Mo
- Multicorner Timin
- Advanced I/O Timin

Slow 1200mV 85C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	139.41 MHz	139.41 MHz	clk	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX such that the duty cycle (in terms of a percentage) is maintained. Altera recommends that you

Partition Name

Netlist Type

Color

Recommendation: 0 of 0 for

Details...

All

<<Filter>>

Find...

Find Next

Messages

System (1)

Processing (154)

100%

00:01:53

## Messages Window:

Quartus Prime Lite Edition - C:/Users/maras/OneDrive/Desktop/Fall 2020/ENEL 453/Labs/2/Final/Lab\_2 - top\_level

File Edit View Project Assignments Processing Tools Window Help

top\_level

Project Navigator Files

Files

- top\_level.vhd
- top\_level.sdc
- top\_level.qsf
- SevenSegment\_decoder.vhd

Tasks

Compilation

Task

Compile Design

top\_level.vhd

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use ieee.numeric_std.all;
4
5 entity top_level is
6   Port ( clk           : in  STD_LOGIC;
7         reset_n        : in  STD_LOGIC;
8         SW              : in  STD_LOGIC_VECTOR (9 downto 0);
9         PB2             : in  STD_LOGIC;
10        LEDR            : out STD_LOGIC_VECTOR (9 downto 0);
11        HEX0,HEX1,HEX2,HEX3,HEX4,HEX5 : out STD_LOGIC_VECTOR (7 downto 0)
12      );
```

Compilation Report - top\_level

IP Catalog

Installed IP

- Project Directory
 No Selection Available
- Library
 > Basic Functions
 > DSP
 > Interface Protocols
 > Memory Interfaces and Controllers

+ Add...

Design Partitions

Partition Name	Netlist Type	Color
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Recommendation: 0 of 0 for

Find... Find Next

Messages

System Processing (29)

100% 00:01:53

18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM\_PARALLEL\_PROCESSORS in your QSF to an appropriate value for best performance.

12019 Can't analyze file -- file MUX2T01.vhd is missing

12125 Using design file synchronizer.vhd, which is not specified as a design file for the current project, but contains definitions for 2 design units and 1 entities in project

12125 Using design file debounce.vhd, which is not specified as a design file for the current project, but contains definitions for 2 design units and 1 entities in project

12125 Using design file dff\_en.vhd, which is not specified as a design file for the current project, but contains definitions for 2 design units and 1 entities in project

12125 Using design file mux4to1.vhd, which is not specified as a design file for the current project, but contains definitions for 2 design units and 1 entities in project

13024 Output pins are stuck at VCC or GND

18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM\_PARALLEL\_PROCESSORS in your QSF to an appropriate value for best performance.

292013 Feature LogicLock is only available with a valid subscription license. You can purchase a software subscription to gain full access to this feature.

15714 Some pins have incomplete I/O assignments. Refer to the I/O Assignment Warnings report for details

332174 Ignored filter at top\_level.sdc(9): ADC\_CLK\_10 could not be matched with a port

332049 Ignored create\_clock at top\_level.sdc(9): Argument <targets> is an empty collection

332174 Ignored filter at top\_level.sdc(11): MAX10\_CLK2\_50 could not be matched with a port

332049 Ignored create\_clock at top\_level.sdc(11): Argument <targets> is an empty collection

15705 Ignored locations or region assignments to the following nodes

334000 Timing characteristics of device 10M50DAF484C6GES are preliminary

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171167 Found invalid Fitter assignments. See the Ignored Assignments panel in the Fitter Compilation Report for more information.

169177 13 pins must meet Intel FPGA requirements for 3.3-, 3.0-, and 2.5-V interfaces. For more information, refer to AN 447: Interfacing MAX 10 Devices with 3.3/3.0/2.5-V LVTTTL/LVCMOS I/O Systems.

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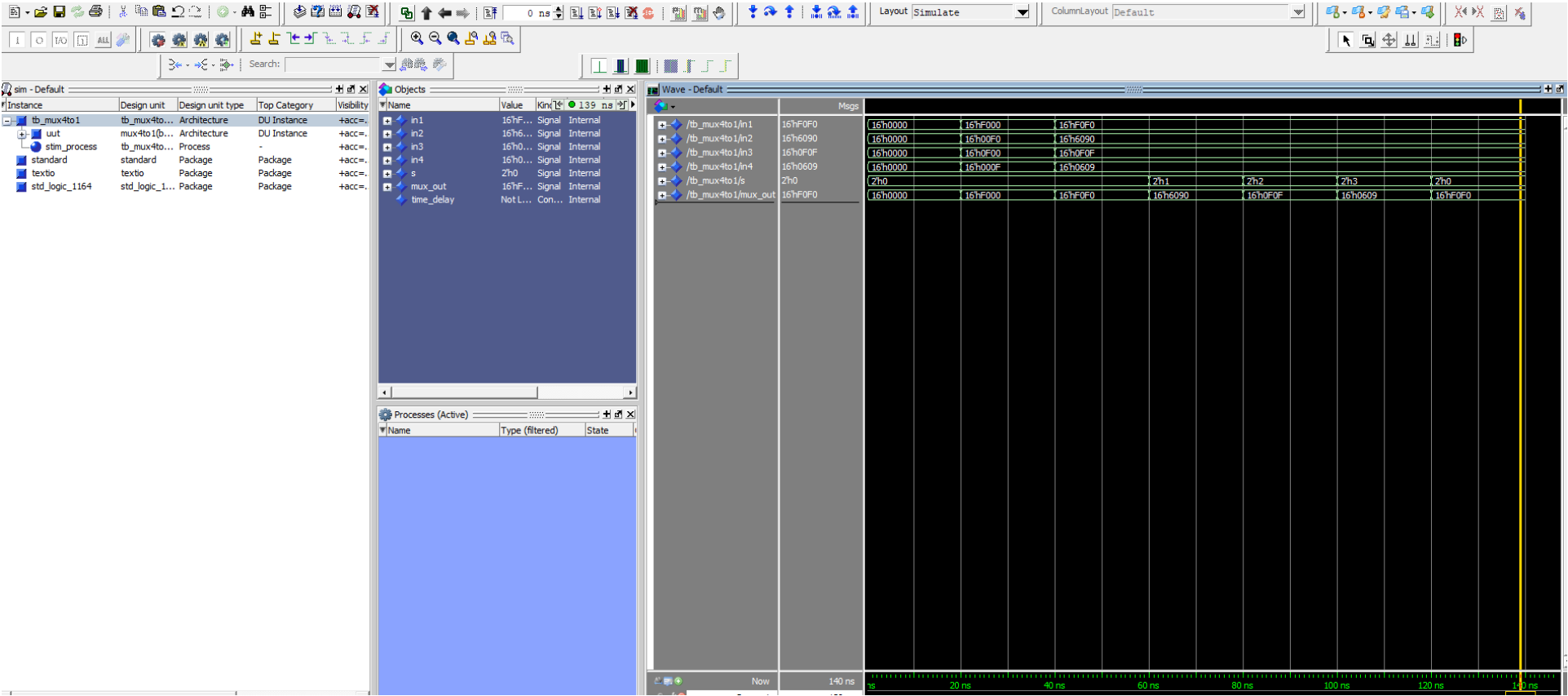
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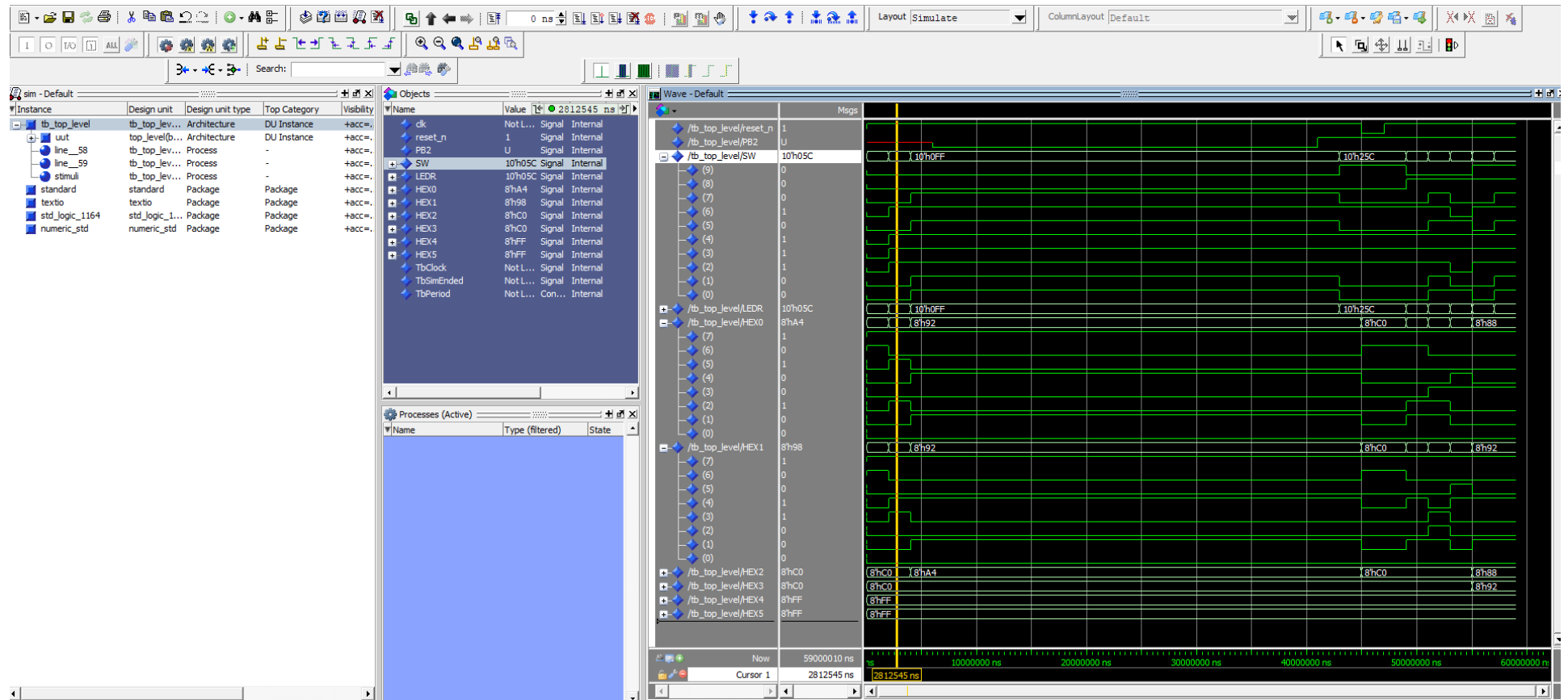
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM\_PARALLEL\_PROCESSORS in your QSF to an appropriate value for best performance.

TestBench:

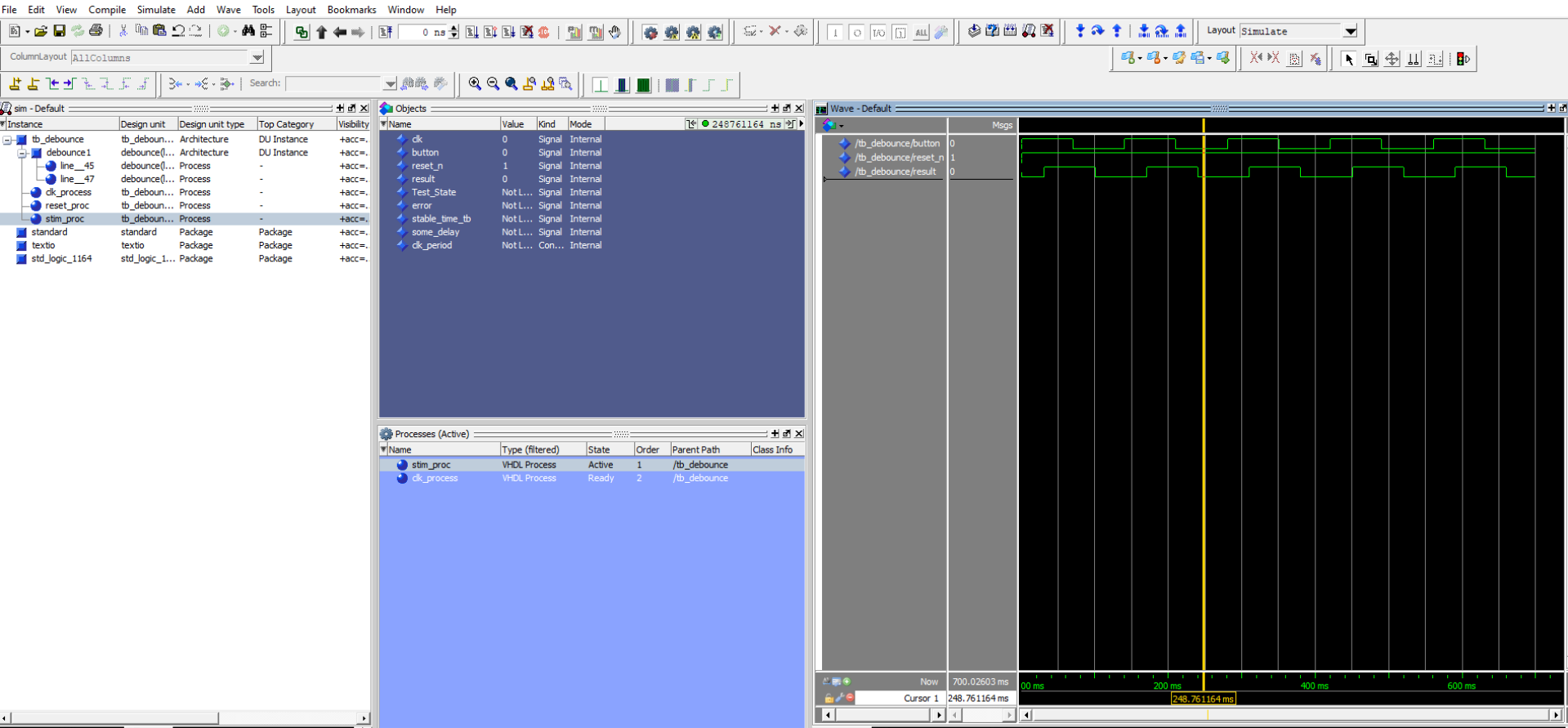
MUX4TO1 Simulation:



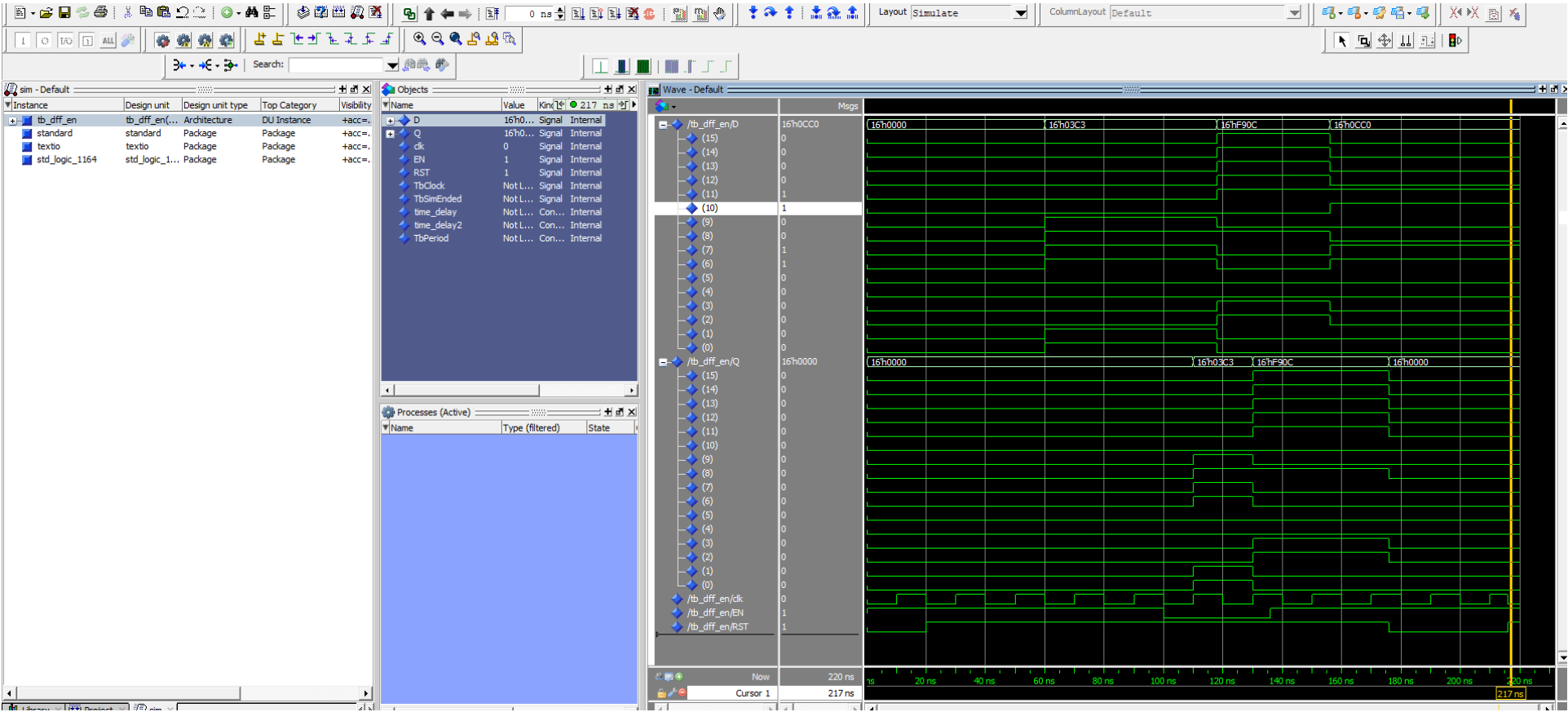
**top\_level Simulation:**



Debounce Simulation:



Register Simulation:



Synchronizer Simulation:

