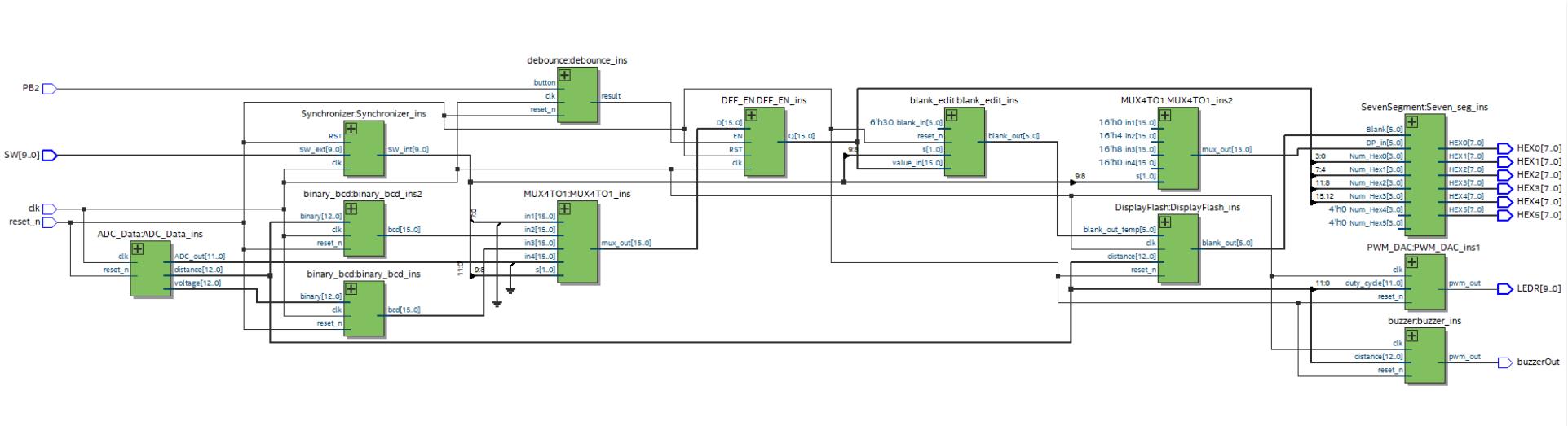


Lab 4 Design Record

Students: Maral Rasuli Arasi, Ruha Javed, Alaa Khalil

RTL Viewer:



Fmax Summary for 85C Model:

Slow 1200mV 85C Model Fmax Summary				
	Fmax	Restricted Fmax	Clock Name	Note
1	57.09 MHz	57.09 MHz	clk	
2	164.34 MHz	164.34 MHz	ADC_Data_ins ADC_ins ADC_Conversion_ins u0 altpll_sys sd1 pll7 clk[0]	

## Messages Window:

All

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Type	ID	Message
⚠	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
⚠	10036	Verilog HDL or VHDL warning at top_level.vhd(34): object "ADC_raw" assigned a value but never read
⚠	10036	Verilog HDL or VHDL warning at ADC_Conversion.v(97): object "cur_adc_ch" assigned a value but never read
⚠	10036	Verilog HDL or VHDL warning at ADC_Conversion.v(98): object "adc_sample_data" assigned a value but never read
⚠	10036	Verilog HDL or VHDL warning at altera_modular_adc_control_fsm.v(70): object "sync_ctrl_state_nxt" assigned a value but never read
⚠	10492	VHDL Process Statement warning at averager256.vhd(85): signal "temp2" is read inside the Process Statement but isn't in the Process Statement's sensitivity list
⚠	10492	VHDL Process Statement warning at averager256.vhd(99): signal "temp3" is read inside the Process Statement but isn't in the Process Statement's sensitivity list
⚠	10540	VHDL Signal Declaration warning at PWM_DAC2.vhd(25): used explicit default value for signal "temp" because signal was never assigned a value
⚠	10540	VHDL Signal Declaration warning at PWM_DAC2.vhd(26): used explicit default value for signal "duty_cycle" because signal was never assigned a value
⚠	10492	VHDL Process Statement warning at PWM_DAC2.vhd(41): signal "EN" is read inside the Process Statement but isn't in the Process Statement's sensitivity list
>	14284	synthesized away the following node(s):
⚠	12241	1 hierarchies have connectivity warnings - see the Connectivity Checks report folder
>	13024	Output pins are stuck at VCC or GND
>	18061	Ignored Power-Up Level option on the following registers
⚠	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
⚠	292013	Feature LogicClock is only available with a valid subscription license. You can purchase a software subscription to gain full access to this feature.
⚠	15714	Some pins have incomplete I/O assignments. Refer to the I/O Assignment Warnings report for details
⚠	332174	Ignored filter at top_level.sdc(9): ADC_CLK_10 could not be matched with a port
>	332049	Ignored create_clock at top_level.sdc(9): Argument <targets> is an empty collection
⚠	332174	Ignored filter at top_level.sdc(11): MAX10_CLK2_50 could not be matched with a port
>	332049	Ignored create_clock at top_level.sdc(11): Argument <targets> is an empty collection
>	15705	Ignored locations or region assignments to the following nodes

All

<<Filter>>

Find...

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Type	ID	Message
⚠	15714	Some pins have incomplete I/O assignments. Refer to the I/O Assignment warnings report for details
⚠	332174	Ignored filter at top_level.sdc(9): ADC_CLK_10 could not be matched with a port
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⚠	332174	Ignored filter at top_level.sdc(11): MAX10_CLK2_50 could not be matched with a port
>	332049	Ignored create_clock at top_level.sdc(11): Argument <targets> is an empty collection
>	15705	Ignored locations or region assignments to the following nodes
⚠	334000	Timing characteristics of device 10M50DAF484C6GES are preliminary
⚠	334000	Timing characteristics of device 10M50DAF484C6GES are preliminary
⚠	171167	Found invalid Fitter assignments. See the Ignored Assignments panel in the Fitter Compilation Report for more information.
>	169177	13 pins must meet Intel FPGA requirements for 3.3-, 3.0-, and 2.5-V interfaces. For more information, refer to AN 447: Interfacing MAX 10 Devices with 3.3/3.0/2.5-V LVTT/LVCMOS I/O Systems.
⚠	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
⚠	12914	The file, c:/Users/maras/OneDrive/Desktop/Fall 2020/ENEL 453/Labs/4/Lab_4_5/adc_qsys.sopcinfo, is not embedded into sof file as expected. Some tools, such as System Console, may not function fully.
⚠	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
⚠	332174	Ignored filter at top_level.sdc(9): ADC_CLK_10 could not be matched with a port
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Testbench:

