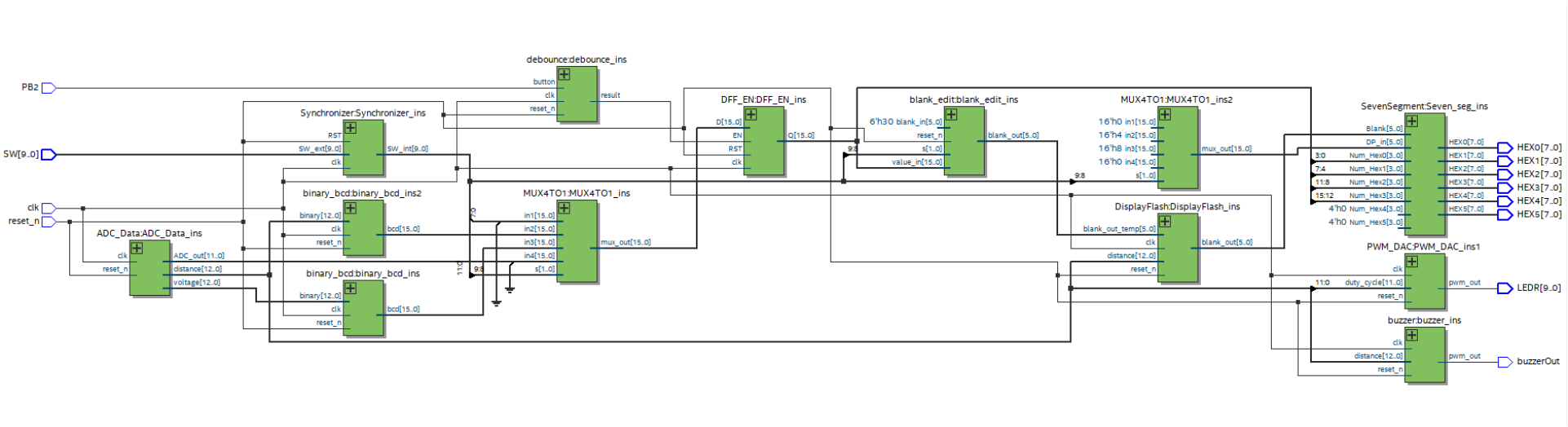
Lab 4 Design Record

Students: **Maral Rasuli Arasi, Ruha Javed, Alaa Khalil**

RTL Viewer:



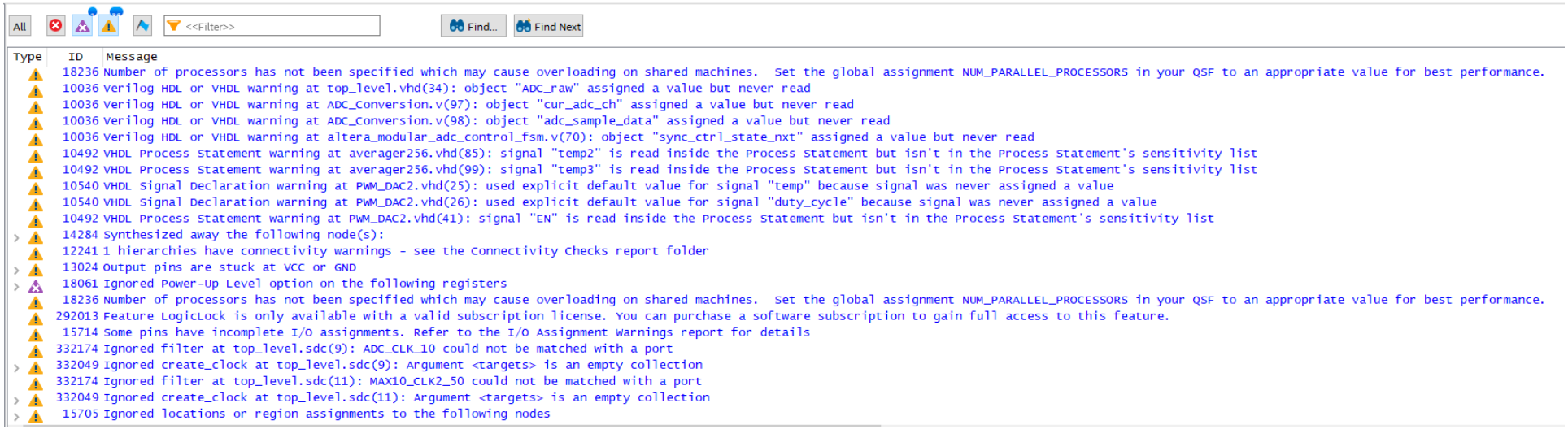
Fmax Summary for 85C Model:

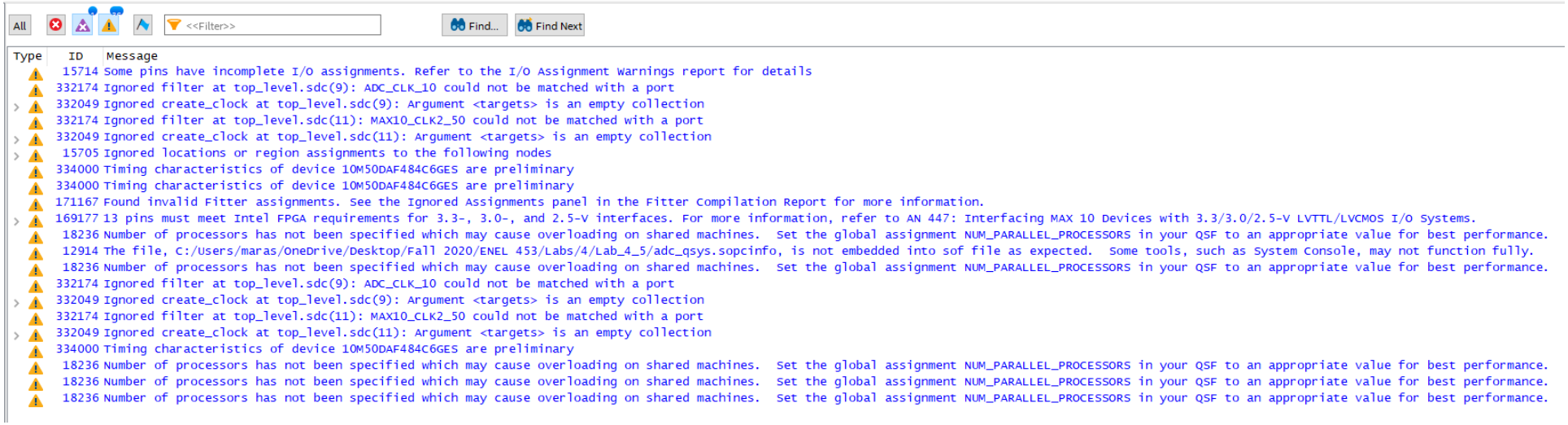
Slow 1200mV 85C Model Fmax Summary

<<Filter>>

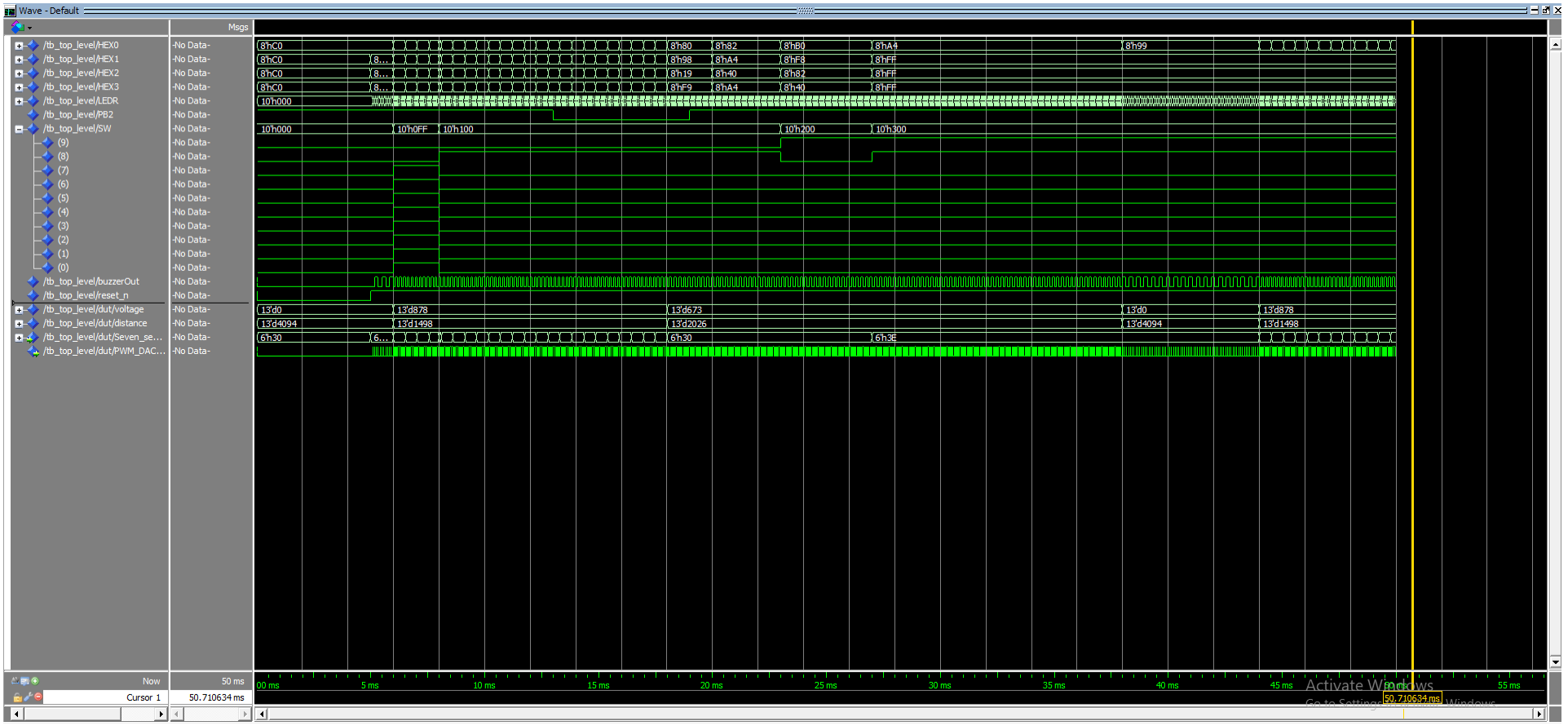
	Fmax	Restricted Fmax	Clock Name	Note
1	57.09 MHz	57.09 MHz	clk	
2	164.34 MHz	164.34 MHz	ADC_Data_ins|ADC_ins|ADC_Conversion_ins|u0|altpll_sys|sd1|pll7|clk[0]	

Messages Window:





Testbench:


Wave - Default
Msgs
/tb_top_level/HEX0
/tb_top_level/HEX1
/tb_top_level/HEX2
/tb_top_level/HEX3
/tb_top_level/LEDR
/tb_top_level/PB2
/tb_top_level/SW
(9)
(8)
(7)
(6)
(5)
(4)
(3)
(2)
(1)
(0)
/tb_top_level/buzzerOut
/tb_top_level/reset_n
/tb_top_level/dut/voltage
/tb_top_level/dut/distance
/tb_top_level/dut/Seven_se...
/tb_top_level/dut/PWM_DAC...
-No Data-
8'hC0
8'h80
8'h82
8'hB0
8'hA4
8'h99
8'h98
8'hF8
8'hFF
8'h19
8'h40
8'h92
8'hF9
10'h000
10'h0FF
10'h100
10'h200
10'h300
13'd0
13'd878
13'd673
13'd4094
13'd1498
13'd2026
6'h30
6'h3E
Now
50 ms
Cursor 1
50.710634 ms
00 ms
5 ms
10 ms
15 ms
20 ms
25 ms
30 ms
35 ms
40 ms
45 ms
50 ms
55 ms
Activate Windows