Course Code	ECE611
Course Name	Memory Design and Testing
Credits	4
Course Offered to	UG/PG
Course Description	The course gives a detailed view of Memory Design topics from SRAM cell design and constraints.

Pre-requisites

Pre-requisite (Mandatory)	**Pre-requisite (Desirable)**	**Pre-requisite(other)**
Digital circuits; Basic MOS Theory; Basic Electronics Desirable: Basic Computer Architecture; PSPICE/ Eldo know-how		

Post Conditions

CO1	**CO2**	**CO3**	**CO4**	**CO5**
Evaluate and Design SRAM Cell	Evaluate Memory Architecture	Design of Data Path and Control circuits for (Non Volatile) Memory operations	Concept of Yield and trade-off with performance	Overview of Memory Test Requirements and Test Flow

Weekly Lecture Plan

Week Number	**Lecture Topic**	**COs Met**	**Assignment/Labs/Tutorial**
Week 1	Memory Hierarchy and Types		
Week 2-3	Metrics		
Week 4-5	Memory Read/ Write Path - Address to Q path (Decoders to Sense Amplifiers and associated timing circuits)		
Week 6-7	Case Studies: 1) High Speed Memory 2) Low Voltage Memory		
Week 7	DRAM array design and related constraints (refresh rate)		
Week 8-9	DRAM interface – address decoding; pipelining; date interface; charge pumps		
Week 10	Non Volatile Memory Cell – Basic Principle and Operation		
Week 11	Read/ Program/ Erase Path (including)		
Week 12	Case Study 2		
Week 13	Reliability Considerations of NVM, Testability, Yield and Repair		

Assessment Plan

Type of Evaluation	**% Contribution in Grade**
Homework	20
Class tests / quizzes	20
Mid-Sem	30
End-Sem	30

Resource Material

Type	**Title**
Reference	Digital Integrated Circuits: A Design Perspective: J.M. Rabaey, Anantha Chandrakasan, Borivoje Nikolik; Prentice Hall
Reference	CMOS Digital Integrated Circuits: Yusuf Leblebici and Sung-Mo Kang; Tata McGraw Hill
Reference	Reference: Flash Memory: Paolo Cappelletti, Carla Golla, Piero Olivo, Enrico Zononi; Kluwer Academic Publishers