Course Code	ECE 516
Course Name	System on Chip Design and Test
Credits	4
Course Offered to	UG/PG
Course Description	This course introduces students to design trends in deep submicron (DSM) era, including scaling trend, clock cycle and power issues; Role of interconnects in contemporary SoC Design; System-on-chip and Platform-based design – IP-based design and reusability, Multiprocessor SoC platform design, 3D integration, on-chip optical and wireless communication,

Pre-requisites

Pre-requisite (Mandatory)	Pre-requisite (Desirable)	Pre-requisite(other)
Introduction to VLSI Design, basic computer organization and architecture		

Post Conditions

CO1	CO2	CO3
1. Have knowledge and understanding of the design and technology trends, role of interconnects in contemporary SoC design, platform based design, reusability, clock and power distribution networks.	1. Have knowledge of Design for testability (DFT), Test Access Mechanism (TAM), concept of core-based test & IEEE P1500 standard for SoC test	3. Analyze, simulate and design complex CMOS circuits/ sub-systems with emphasis on low power and high-speed.

Weekly Lecture Plan

Week Number	Lecture Topic	Assignment/Labs/Tutorial
1	Design and Technology trends	Reading Assignment 1
2	reusability	Reading Assignment 2
3,4	Delay in long wires and performance limitations, Interconnect coupling capacitance and its effect on wire delay, Crosstalk avoidance coding schemes (CAC)	Reading Assignment 3, Quiz I
5	Interconnect Inductance	Reading Assignment 4, Quiz II
6	Power and Clock distribution networks	Reading Assignment 5, Quiz III
7	Fault modeling,	HW 1, Reading Assignment 6
8	Design for Testability (DFT)	Reading Assignment 7, Quiz IV
9	Test Access Mechanism (TAM)	Reading Assignment 8, Quiz V
10	Concept of core-based test & IEEE P1500 standard for SoC test	HW 2, Reading Assignment 9
11	Design and Test of low-voltage CMOS circuits, Multiple Threshold CMOS (MTCMOS), Variable Threshold CMOS and other related methodologies for leakage power reduction	Reading Assignment 10, Quiz VI
12	Power minimization through architecture level optimization	Reading Assignment 11, Quiz VII
13	Future of SoCs: 3D integration, on-chip optical and wireless communication	Project Report & Poster

Assessment Plan

Type of Evaluation	% Contribution in Grade
Homework	5
Quizzes	5
Reading Assignment	15
Mid-Sem	20
End-Sem	25
Project	30

Resource Material

Type	Title
Reference	Analysis and Design of Digital Integrated Circuits - In Deep Submicron Technology, Hodges, Jackson and Saleh, McGraw-Hill, Third Edition, 2004.
Reference	Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits by M. L. Bushnell and V. D. Agrawal, Boston: Springer, 2005.
Reference	Research Papers