Course Code	ECE 511/ CSE 511
Course Name	Computer Architecture
Credits	4
Course Offered to	UG/PG
Course Description	This course forms a strong foundation in the understanding and design of modern computing systems. Building on a computer organization base, this course explores techniques that go into designing a modern microprocessor. Fundamental understanding of computer architecture is key not only for students interested in hardware and processor design, but is a foundation for students interested in compilers, operating systems, and high performance programming. This course will explore how the computer architect can utilize the increasing number of transistors available to improve the performance of a processor. Focus will be given to architectures that can exploit different forms of parallelism, whether they be implicit or explicit. This course covers architectural techniques such as multi-issue superscalar processors, out-of-order processors, Very Long Instruction Word (VLIW) processors, advanced caching, and multiprocessor systems.

Pre-requisites	
Pre-requisite (Mandatory)	**Pre-requisite (Desirable)**

*Please insert more rows if required

Post Conditions			
CO1	**CO2**	**CO3**	**CO4**
Able to explain basic concepts like micro-architecture, ISA, pipeline and related hazards, caches etc.	Able to explain common issues of superscalar architectures, different kinds of out-of-order processors along with common methods to improve their performance.	Able to use concepts like VLIW, branch prediction, mechanism to improve cache performance, memory management, vector processors etc.	Able to use simulators like Gem5 to evaluate and understand hardware and software optimization techniques.

Weekly Lecture Plan			
Week Number	**Lecture Topic**	**COs Met**	**Assignment/Labs/Tutorial**
Week 1	Introduction: Architecture and Micro-architecture, Machine Models, ISA Characteristics	CO1	Assignment
Week 2	Introduction: Architecture and Micro-architecture, Machine Models, ISA Chara	CO1	Assignment and Tutorial
Week 3	Pipelining: Basics, Structural Hazards, Data Hazards, Control Hazards	CO1	Assignment and Quiz
Week 4	Superscalar: In-Order, Out-of-Order, Bypassing, Interrupts, Exceptions, Speculation, Register Renaming	CO2	Assignment, Quiz and Project
Week 5	Superscalar: In-Order, Out-of-Order, Bypassing, Interrupts, Exceptions, Speculation, Register Renaming	CO2	Assignment, Quiz and Project
Week 6	VLIW: Compiler Optimizations, Challenges, Predication, Case Study	CO2 & CO3	Assignment, Quiz and Project
Week 7	Branch Prediction: Static and Dynamic Outcome Prediction, Target Address Prediction	CO2 & CO3	Assignment, Quiz and Project
Week 8	Caches: Motivation, Performance, Optimizations	CO1, CO2 & CO3	Assignment, Quiz and Project
Week 9	Memory Management: Base and Bound Registers, Page based Memory Systems, Translation and Protection, TLB, Cache and Memory Protection Interaction	CO3	Assignment, Quiz and Project
Week 10	Vector Processor and GPU: Vector Parallelism, Vector Hardware Optimizations, Vector Software and Compiler Optimizations, Reduction, Scatter/Gather, SIMD, GPU	CO2, CO3 & CO4	Assignment, Quiz and Project
Week 11	Parallelism: Coarse grain Multithreading, SMT, Synchronization, Sequential Consistency, Cache Coherence Protocols, Message Passing	CO2, CO3 & CO4	Assignment, Quiz and Project

Week 12	Multiprocessor Interconnections: Interconnect Design, Topology, Network Performance, Routing and Flow Control	CO2, CO3 & CO4	Project
Week 13	Architectures for AI/ ML	CO2, CO3 & CO4	Project

Assessment Plan

Type of Evaluation	% Contribution in Grade
Assignment	15
Quiz	15
Mid-sem	25
End-sem	25
Project	20

Resource Material

Type	Title
Textbook	Computer Architecture: A Quantitative Approach, 5th Edition: John L Hennessy and David A Patterson (Elsevier)
Reference	