Course Code	ECE 314/ECE514
Course Name	Digital VLSI Design
Credits	4
Course Offered to	UG/PG
Course Description	This course introduces students to CMOS circuits, develops first-order current-voltage and capacitance-voltage models for transistors, transfer characteristics of CMOS inverter, performance estimation for circuits through logical effort, interconnects, combinational circuit design, circuit families, sequential circuit design including clocking and latching techniques, design of datapath subsystems (adders, shifters, multipliers etc.), design of memory subsystems. A course project using state-of-the-art computer aided design (CAD) tools in VLSI gives students hands-on exposer to the most current technology/process.

Pre-requisites			
Pre-requisite (Mandatory)	Knowledge of digital logic, basic computer organization and some understanding of RC circuits		
*Please insert more rows if required			

Post Conditions				
CO1	**CO2**	**CO3**	**CO4**	**CO5**
Students are be able to evaluate characteristics of CMOS inverter and interconnects specifically in terms of current and capacitance that are essential for estimating delay and power	Students are able to quickly estimate the best number of stages for a path, the minimum possible delay for the given topology, and the gate sizes that achieve this delay using logical effort.	Students are able to describe various sources of power dissipation in a CMOS chip and apply techniques to minimize that.	Students are able to optimize combinational circuits for lower delay and/or energy; analyze sequential circuits including clocking and latching techniques.	Students are able to use computer aided design (CAD) tools in VLSI and experiment with the current technology/process, and able to design state-of-the-art CMOS circuits

Weekly Lecture Plan			
Week Number	**Lecture Topic**	**COs Met**	**Assignment/Labs/Tutorial**
Week 1	Introduction (MOS transistors, CMOS Logic)	CO1	Reading Assignment 1
Week 2	CMOS circuit theory	CO1	Quiz I
Week 3	MOS Capacitance model/ Parasitic capacitances	CO1	Reading Assignment 2, Quiz 2, Tutorial on Cadence
Week 4	DC Transfer Characteristics of Inverter	CO1	HW 1, Quiz 3
Week 5	Delay Estimation	CO1 & CO2	Lab 1, Term project (problem definition)
Week 6	Logical effort and transistor sizing	CO2	Reading Assignment 3, Quiz 4, Tutorial on Synopsys
Week 7	Combinational Circuit Design	CO4	HW 2

Week 8	Sequential Circuit Design	CO4	Lab 2, Quiz 5
Week 9 & 10	Power Dissipation, Interconnects, Scaling	CO3	Reading Assignment 4, HW 3, Quiz 6
Week 11	Datapath Subsystems	CO3, CO4, CO5	Lab 3, Quiz 7
Week 12	Memory Subsystems	CO3, CO4, CO5	Reading Assignment 5, HW 4, Quiz 8
Week 13	Review and Term project evaluation	CO3, CO4, CO5	Project Report

Weekly Lab Plan			
Week Number	**Laboratory Exercise**	**COs Met**	**Platform (Hardware/Software)**
*Please insert more rows if required			

Assessment Plan	
Type of Evaluation	**% Contribution in Grade**
Mid-sem	25
Homework	10
Quiz	5
End-sem	25
Laboratory	15
Project	20

Resource Material	
Type	**Title**
Textbook	N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective. Third Edition. Pearson, 2006.
Textbook	Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic; Digital Integrated Circuits: A Design Perspective, Phi Learning, 2009.
ECE 514: Additional Assignments and evaluation mechanism	
· **Midsem and Final Exam: One extra question for ECE 514 (no extra time)**	
· **Lab assignments: Each Lab assignment will have one extra task only for ECE 514**	
· **Term Project: ECE 514 students will be evaluated separately**	