Course Code	ECE 270			
Course Name	Embedded Logic Design			
Credits	4			
Course Offered to	UG			
Course Description	This course will introduce students to the various programmable logic devices (PLDs) available in the market and get them started with how to program such devices to develop simple applications. First half of this course will cover FPGA programming using Verilog and second half will focus on ARM processor programming using C followed by an integration of ARM with FPGA using Zynq board.			
Pre-requisites				
Pre-requisite (Mandatory)	**Pre-requisite (Desirable)**			
None	None			
*Please insert more rows if required				
Post Conditions				
CO1	CO2	CO3	CO4	C05
Students are able to design and implement combinational circuits on FPGA	Students are able to design and implement sequential circuits on FPGA	Students are able to write Verilog codes and testbenches to integrate on-board FPGA switches, leds, displays etc.	Students are able to explain the Zynq SoC architecture and its applications	
Weekly Lecture Plan				
Week Number	**Lecture Topic**	**COs Met**	**Assignment/Labs/Tutorial**	
Week 1 & Week2	FPGA architecture and Verilog Basics	C01, C03	Introduction to Vivado and FPGA design flow	
Week 3 & Week4	Combinational logic design, Verilog testbench	C01, C03	Decoders/Encoders, code converters, ALU	
Week 5 & Week 6	Synchronous and asynchronous logic design and arithmetic circuits, Advanced Verilog	C01, C02, C03	Verilog code, simulation and implementation: Counters, pulse-width modulation, Fibonacci sequence	
Week 7 & Week 8	Finite state machines and Advanced Verilog	C01, C02, C03	Verilog code, simulation and implementation: Door lock code, traffic lights, Sequence detectors	
Week 9 & Week 10	FPGA Memory, Zynq architecture (ARM + FPGA)	C01, C02, C03, C04	Programming ARM processor, timers, interrupts, UART communication with Zedboard	
Week 11 & Week 12	Zynq architecture (ARM + FPGA), C programming for ARM	C04	Lab for integration of ARM with FPGA on Zynq board	

Week 13	Zynq architecture (ARM + FPGA), C programming for ARM	C04	Lab for integration of ARM with FPGA on Zynq board
Weekly Lab Plan			
Week Number	**Laboratory Exercise**	**COs Met**	**Platform (Hardware/Software)**
*Please insert more rows if required			
Assessment Plan			
Type of Evaluation	**% Contribution in Grade**		
Mid-sem	30		
Assignment	15		
Quiz	20		
End-sem	35		
Resource Material			
Type	**Title**		
Textbook	Engineering Circuit analysis, William H. Hayt Jr., Jack E. Kemmerly and Steven M. Durbin, 8thEdition, Tata McGraw Hill		
Datasheets	Xilinx Zynq Family, Xilinx Vivado		
Reference manuals	Basys3 and Zedboard reference manual		
Schematics	Basys3 and Zedboard Schematics		
Softwares	Vivado		
Hardwares	Basys3 and Zedboard by Digilent		
Also recommended:			
Book	D. Harris and S. Harris, “Digital Design and Computer Architecture”, Morgan Kauffmann, 2012.		
Internet Resource	Verilog tutorials: http://www.asic-world.com/verilog/veritut.html		