Course Code	ECE513
Course Name	VLSI Design Flow
Credits	4
Course Offered to	UG/PG
Course Description	The objective of this course is to develop a basic understanding of the methods, tools and technologies that go into transforming an “idea” into an “integrated circuit”. This course is intended to give an overall perspective of the VLSI design flow, going through various stages of designing such as synthesis, floorplanning, placement, routing etc. and various steps of verification such as simulation, formal methods and timing/power analysis. In this course, ample opportunities will be provided to employ the-state-of-the-art CAD tools and gain a practical understanding of the VLSI design flow. A few representative algorithms that work inside the CAD tools will also be discussed.

Pre-requisites

Pre-requisite (Mandatory)	Pre-requisite (Desirable)	Pre-requisite (Other)
Digital Circuits	Comfortable with working on UNIX	
Basics of CMOS	Scripting language such as TCL	

Post Conditions

CO1	CO2	CO3	CO4	CO5
Students are able to explain the design and verification steps in the VLSI design flow and their purpose and significance	Students are able to evaluate various trade-offs that need to be made at various steps in the VLSI design flow.	Students are able to design and verify simple VLSI circuits using the state-of-the-art computer aided design (CAD) tools at different levels of abstractions.	Students are able to apply representative algorithms that are used in implementing CAD tools to design and verify integrated circuits.	

Weekly Lecture Plan

Week Number	Lecture Topic	COs Met	Assignment/Labs/Tutorial
1	Designing vs. Fabrication; Processes involved in taking an "Idea" to RTL: Software/Hardware Partitioning, Behavioral	CO1, CO2	Introduction to UNIX and TCL
2	Verification and Test Flow; Processes after GDS Tapeout to Final Chip;	CO1, CO2	Assignment 1: Based on UNIX and TCL
3	Constraints;	CO1, CO2, CO3	Assignment 2: RTL Designing
4	Timing Analysis; Power Analysis;	CO1, CO2, CO3, CO4	Assignment 2: RTL Simulation and Synthesis
5	Equivalence Checking, BDD, SAT;	CO1, CO2, CO3, CO4	Assignment 2: Equivalence Checking
6	Mapping;	CO1, CO2, CO3, CO4	Assignment 2: STA and Logic Optimization
7	Insertion, ATPG, BIST	CO1, CO2, CO3, CO4	Assignment 2: Scan Chain Insertion
8	Basics of Physical Design	CO1, CO2, CO3	Assignment 2: continued
9	Floorplanning, Power Planning;	CO1, CO2, CO3	Assignment 2: continued
10	Placement: Techniques and Optimization;	CO1, CO2, CO3, CO4	Assignment 3: Floorplanning and Placement
11	Optimization; Routing: Global and Detailed; ECO	CO1, CO2, CO3, CO4	Assignment 3: Routing
12	DRC; Sign-off	CO1, CO2, CO3	Assignment 3: Extraction and Sign-off
13	Summing-up and Paper Presentations	CO1, CO2, CO3, CO4	

Weekly Lab Plan

Week Number	Laboratory Exercise	COs Met	Platform (Hardware/Software)
8	Demonstration/Viva for Assignment1/Assignment2	CO1, CO2, CO3, CO4	CAD Tool
12	Demonstration/Viva for Assignment3	CO1, CO2, CO3, CO4	CAD Tool

Assessment Plan

Type of Evaluation	% Contribution in Grade
Assignment	25
Paper presentation	15
Mid-sem	20
End-sem	40

Resource Material

Type	Title
Reference	Electronic Design Automation for Integrated Circuits Handbook, Second Edition, Luciano Lavagno, Igor L. Markov, Grant E. Martin, Louis K. Scheffer, - 2016, - CRC Press
Reference	Application-Specific Integrated Circuits, Michael Smith, Addison-Wesley Professional; 1 edition (June 20, 1997)
Reference	Synthesis and Optimization of Digital Circuits, Giovanni De Micheli, McGraw-Hill, 1994
Reference	Static Timing Analysis For Nanometer Designs: A Practical Approach, by J. Bhasker, Rakesh Chadha, Springer; 2009 edition
Reference	Silicon VLSI Technology: Fundamentals, Practice, and Modeling. J. D. Plummer, M. Deal, and P. B. Griffin, Pearson, 2000
Reference	Verilog HDL synthesis : a practical primer, J. Bhaskar
Reference	Papers (Pointers will be given in the class)
Reference	User Guides of CAD Tools.
Internet Resource	Information from reliable internet sources