Course Code	ECE 510
Course Name	Digital Hardware Design (DHD)
Credits	4
Course Offered to	UG/PG
Course Description	distributed and parallel architecture. FPGAs also allows complete control over arithmetic world-lengths and dynamic partial reconfigurability thereby leading to optimal computational efficiency. Integration of FPGA with ARM processor has led to significant interests in Zynq SoC because of their usefulness in applications such as software defined radios, cellular base stations, data centers, video processing and computer vision etc. In this course, students will learn how to implement algorithms in an FPGA using Verilog. Though this course assumes

Pre-requisites

Pre-requisite (Mandatory)	**Pre-requisite (Desirable)**
ECE270 Embedded Logic Design	

*Please insert more rows if required

Post Conditions

CO1	**CO2**	**CO3**	**CO4**
Students are able to design and implement sequential and combinational logic design on FPGA	Students are able to write Verilog code to integrate on-board FPGA switches, VGA interface, memory, embedded hardware units etc.	Students are able to implement the algorithms on Zynq SoC via hardware software co-design	Students are able to design new IP with appropriate AXI interface

Weekly Lecture Plan

Week Number	**Lecture Topic**	**COs Met**	**Assignment/Labs/Tutorial**
Week 1-3	Theory: FPGA Architecture (CLB, BRAM, DSP48) Lab: Combinational logic design, Synchronous and asynchronous logic design and arithmetic circuits	CO1, CO3	Lab + Homework: Verilog code, simulation and implementation: Comparators, Decoders/Encoders, code converters, ALU, counters, pulse-width modulation, Fibonacci sequence
Week 4	Theory: FPGA Architecture (Clock) Lab: IP, Finite state machines	CO1, CO3	Lab + Homework: Door lock code, traffic lights, sequence detectors etc.
Week 5-6	Theory: AXI protocol Lab: VGA based game design	CO1, CO2, CO3	Lab + Homework: VGA stripes, screen saver, Video game
Week 7-9	Theory: Zynq Architecture Lab: Hardware software co-design	CO2, CO3	Lab + Homework: Hardware software co-design
Week 10-13	Theory: Zynq Architecture Lab: Hardware software co-design	CO2, CO3	Lab + Homework: Hardware software co-design

Week Number	**Laboratory Exercise**	**COs Met**	**Platform (Hardware/Software)**

*Please insert more rows if required

Assessment Plan

Type of Evaluation	**% Contribution in Grade**
Quiz	20
Assignment	20
Mid-sem	25
End-sem	35

Resource Material

Type	**Title**
Textbook	D. Harris and S. Harris, “Digital Design and Computer Architecture”, Morgan Kauffmann, 2012.

Textbook	R. Haskell and D. Hanna, “Learning by example using Verilog advanced digital design”, LBE Books, 2014
Textbook	Uwe Meyer-Baese, Digital Signal Processing with Field Programmable Gate Arrays, Springer, 2007
Internet Resource	Verilog tutorials: http://www.asic-world.com/verilog/veritut.html