Basic Physics (~70 MCQ) 1. CoulombÃ¢â‚¬â„¢s law defines the force between: a) Two moving charges b) Two point charges at rest Ã¢Å“â€¦ c) A charge and a magnetic field d) A current -carrying wire and a charge 2. The SI unit of electric flux is: a) Volt b) Coulomb c) NewtonÃ‚·meterÃ‚²/Coulomb Ã¢Å“â€¦ d) Tesla 3. GaussÃ¢â‚¬â„¢s law is applicable to: a) Only point charges b) Any closed surface Ã¢Å“â€¦ c) Open surfaces d) Conductors only 4. Electric potential at a point is: a) Energy per unit charge Ã¢Å“â€¦ b) Force per unit charge c) Charge per unit en ergy d) None of these 5. FaradayÃ¢â‚¬â„¢s law relates: a) Electric field and charge b) Induced EMF and rate of change of magnetic flux Ã¢Å“â€¦ c) Current and resistance d) Voltage and capacitance 6. MaxwellÃ¢â‚¬â„¢s equations describe: a) Motion of electrons b) Electromagnetic fiel ds Ã¢Å“â€¦ c) Quantum particles d) Wave propagation in air only 7. The speed of light in vacuum is: a) 3Ã*f*â€”10Ã‚³ m/s b) 3Ã*f*â€”10Ã¢â€‹Âµ m/s c) 3Ã*f*â€”10Ã¢â€‹Â¸ m/s Ã¢Å“â€¦ d) 3Ã*f*â€”10Ã‚¹Ã¢â€‹Â° m/s 8. Photoelectric effect demonstrates that light: a) Travels in waves b) Has particle nature Ã¢Å“â€¦ c) Is longitudinal d) Has no energy 9. Compton effect proves: a) Wave nature of light b) Particle nature of light Ã¢Å“â€¦ c) Magnetic field effect d) Electric field effect 10. De Broglie wavelength is associated with: a) Photons b) Electrons and matter particles Ã¢Å“â€¦ c) Only protons d) Only neutrons 11. Phase velocity is: a) Velocity of energy transfer b) Velocity of wave crests Ã¢Å“â€¦ c) Same as group velocity d) None of these 12. Group velocity is: a) Speed of individual wave b) Speed of envelope of wave packet Ã¢Å“â€¦ c) Always greater than phase velocity d) Zero 13. Quantum theory of light was proposed by: a) Newton b) Einstein Ã¢Å“â€¦ c) Maxwell d) Planck 14. X-ray diffraction is used to study: a) Atomic structure Ã¢Å“â€¦ b) Magnetic field c) Electric circuits d) Sound waves 15. Wave function in quantum mechanics represents: a) Probability amplitude Ã¢Å“â€¦ b) Energy only c) Force d) Velocity 16. The integral of electric field over a closed surface equals: a) Zero b) Charge enclosed/ÃŽÂµÃ¢â€šâ‚¬ Ã¢Å“â€¦ c) Current enclosed d) Voltage 17. Magnetic field is produced by: a) Static charges b) Moving charges Ã¢Å“â€¦ c) Stationary neutral objects d) Heat only 18. FaradayÃ¢â‚¬â„¢s law is a consequence of: a) Conservation of energy Ã¢Å“â€¦ b) OhmÃ¢â‚¬â„¢s law c) CoulombÃ¢â‚¬â„¢s law d) KirchoffÃ¢â‚¬â„¢s law 19. Unit of magnetic flux is: a) Tesla b) Weber Ã¢Å“â€¦ c) Ampere d) Henry 20. Lorentz force acts on: a) Stationary char ge b) Moving charge in magnetic field Ã¢Å“â€¦ c) Neutral particles d) Light only 21. Capacitance is defined as: a) Q/V Ã¢Å“â€¦ b) V/Q c) I/R d) P/V 22. Energy stored in a capacitor: a) Ã‚½ CVÃ‚² Ã¢Å“â€¦ b) CVÃ‚² c) 2CVÃ‚² d) C/VÃ‚² 23. Inductor opposes: a) Voltage b) Current change Ã¢Å“â€¦ c) Resistan ce d) Power 24. RLC circuit resonates when: a) XL = XC Ã¢Å“â€¦ b) XL > XC c) XL < XC d) R = 0 25. Electric field inside a conductor is: a) Maximum b) Zero Ã¢Å“â€¦ c) Depends on charge d) Constant 26. Magnetic flux density is measured in: a) Tesla Ã¢Å“â€¦ b) Weber c) Henry d) Ampere 27. AmpereÃ¢â‚¬â„¢s law relates: a) Current and magnetic field Ã¢Å“â€¦ b) Voltage and resistance c) Capacitance and charge d) Energy and power 28. Biot-Savart law gives: a) Force on a charge b) Magnetic field due to current element Ã¢Å“â€¦ c) Electric field d) Voltage 29. Self-inductance unit is: a) Henry Ã¢Å“â€¦ b) Farad c) Ohm d) Tesla 30. Mutual inductance occurs between: a) Two resistors b) Two coils Ã¢Å“â€¦ c) Capacitor and coil d) Wire and battery 31. Maxwell added which term to AmpereÃ¢â‚¬â„¢s law? a) Displacement current Ã¢Å“â€¦ b) Conduction current c) Electric flux d) Magnetic flux 32. Electromagnetic waves are: a) Longitudinal b) Transverse Ã¢Å“â€¦ c) Stationary d) Random 33. Energy of a photon: a) hf Ã¢Å“â€¦ b) h/f c) h + f d) hfÃ‚² 34. Threshold frequency in photoelectric effect depends on: a) Intensity b) Metal type Ã¢Å“â€¦ c) Distance from source d) Angle of incidence 35. Quantum number n indicates: a) Angular momentum b) Principal energy level Ã¢Å“â€¦ c) Magnetic orientation d) Spin 36. Planck constant h has units: a) JouleÃ‚·second Ã¢Å“â€¦ b) Volt c) Coulomb d) AmpereÃ‚·second 37. Compton wavelength for mula is: a) ÃŽÂ»c = h/mc Ã¢Å“â€¦ b) ÃŽÂ»c = mc/h c) ÃŽÂ»c = hÃ‚²/m d) ÃŽÂ»c = h/m 38. X-ray wavelength is in the range: a) 0.01 Ã¢â‚¬â€œ10 nm Ã¢Å“â€¦ b) 1Ã¢â‚¬â€œ100 ÃŽÂ¼m c) 100 Ã¢â‚¬â€œ1000 nm d) 10 Ã¢â‚¬â€œ100 cm 39. Electromagnetic spectrum order (low to high frequency): a) Radio, Microwave, IR, Visible, UV, X -ray, Gam ma Ã¢Å“â€¦ b) X-ray, UV, Visible, IR, Microwave, Radio c) Gamma, X -ray, UV, Visible, IR, Microwave, Radio d) Radio, IR, Microwave, Visible, UV, X -ray, Gamma 40. Photoelectric current depends on: a) Light frequency b) Light intensity Ã¢Å“â€¦ c) Metal temperature d) None 41. Heisenberg uncertainty principle relates: a) Energy and time Ã¢Å“â€¦ b) Position and momentum Ã¢Å“â€¦ c) Force and mass d) Both a & b Ã¢Å“â€¦ 42. Wave equation describes: a) Electric field only b) Magnetic field only c) Propagation of waves Ã¢Å“â€¦ d) Particle motion 43. EM wave in vacuum travels at: a) 3Ã*f*â€”10Ã¢â€‹Â¸ m/s Ã¢Å“â€¦ b) 3Ã*f*â€”10Ã¢â€‹Âµ m/s c) 3Ã*f*â€”10Ã‚³ m/s d) 3Ã*f*â€”10Ã‚¹Ã¢â€‹Â° m/s 44. Polarization of light involves: a) Frequency change b) Direction change of E vector Ã¢Å“â€¦ c) Amplitude only d) Wavelength only 45. BrewsterÃ¢â‚¬â„¢s angle gives: a) Total reflection b) Zero reflection for one polarization Ã¢Å“â€¦ c) Maximum reflection d) None 46. Critical angle is related to: a) Refraction Ã¢Å“â€¦ b) Diffraction c) Polarization d) Interference 47. Phase difference of 180Ã‚° gives: a) Constructive interference b) Destructive interference Ã¢Å“â€¦ c) No interference d) Random waves 48. Energy of X -ray photon is: a) E = hf Ã¢Å“â€¦ b) E = h/f c) E = hfÃ‚² d) E = f/h 49. Quantum tunneling explains: a) Classical reflection b) Particle crossing potential barrier Ã¢Å“â€¦ c) Wave interference d) Magnetic effect 50. Electron diffraction proves: a) Partic le nature b) Wave nature Ã¢Å“â€¦ c) EM wave d) Photoelectric effect 51. Wavefunction normalization ensures: a) Energy conservation b) Total probability = 1 Ã¢Å“â€¦ c) Momentum conservation d) Mass conservation 52. SchrÃ*f*Â¶dinger equation is: a) Time - independent Ã¢Å“â€¦ b) Time -dependent Ã¢Å“â€¦ c) Both d) None 53. Potential energy in quantum well is: a) Infinite b) Zero c) Finite Ã¢Å“â€¦ d) Negative 54. Electron in hydrogen atom has: a) Continuous energy b) Quantized energy Ã¢Å“â€¦ c) Zero energy d) Infinite energy 55. First Boh r orbit radius: a) 0.529 Ã*f*â€¦ b) 0.529 nm Ã¢Å“â€¦ c) 5.29 nm d) 5.29 cm 56. Photon momentum is: a) p = mv b) p = hf/c Ã¢Å“â€¦ c) p = h/f d) p = mc 57. Heisenberg principle formula: a) ÃŽâ€xÃŽâ€p Ã¢â€°Â¥ Ã‚§/2 Ã¢Å“â€¦ b) ÃŽâ€xÃŽâ€p Ã¢â€°Â¤ Ã‚§/2 c) ÃŽâ€EÃŽâ€t Ã¢â€°Â¤ Ã‚§ d) ÃŽâ€EÃŽâ€t Ã¢â€°Â¥ Ã‚§ 58. Group velocity < Phase velocity in: a) Norma l dispersion b) Anomalous dispersion Ã¢Å“â€¦ c) Vacuum d) Free space 59. Standing wave forms due to: a) Single wave b) Superposition Ã¢Å“â€¦ c) Refraction d) Diffraction 60. Node is point of: a) Maximum amplitude b) Zero amplitude Ã¢Å“â€¦ c) Half amplitude d) Random amplitude 61. Antin ode is point of: a) Maximum amplitude Ã¢Å“â€¦ b) Zero amplitude c) Half amplitude d) Random amplitude 62. EM wave energy density: a) u = ÃŽÂµÃ¢â€šâ‚¬EÃ‚²/2 Ã¢Å“â€¦ b) u = ÃŽÂ¼Ã¢â€šâ‚¬HÃ‚² c) u = EH d) u = 0 63. Maxwell predicts: a) EM waves travel at speed of light Ã¢Å“â€¦ b) EM waves are longitudinal c) EM waves have mass d) EM waves stationary 64. Quantum of light is: a) Electron b) Photon Ã¢Å“â€¦ c) Neutron d) Proton 65. Wavelength of electron decreases with: a) Increasing momentum Ã¢Å“â€¦ b) Decreasing momentum c) Constant d) None 66. Principle of superposition applies to: a) Linear systems Ã¢Å“â€¦ b) Nonlinear systems c) Magnetic fields only d) Electric fields only 67. Electric field inside a

hollow conductor: a) Zero Ã¢Å“â€¦ b) Non -zero c) Depends on shape d) Depends on charge 68. Magnetic permeability of free space: a) 4Ãâ‚¬Ã*f*â€”10Ã¢â€‹Â»Ã¢â€‹Â· H/m Ã¢Å“â€¦ b) 8.85Ã*f*â€”10 Ã¢â€‹Â»Ã‚¹Ã‚² F/m c) 1 H/m d) 0 69. Magnetic flux ÃŽÂ¦ = BÃ‚·A cosÃŽÂ¸ ÃŽÂ¦ is: a) Angle between B and area normal Ã¢Å“â€¦ b) Angle between B and surface c) Always 0 d) Always 90Ã‚° 70. RLC series circuit resonant frequency: a) f = 1/(2Ãâ‚¬Ã¢Ë†Å¡LC) Ã¢Å“â€¦ b) f = 2Ãâ‚¬Ã¢Ë†Å¡LC c) f = Ã¢Ë†Å¡LC d) f = 1/(LC) Introducti on to Computer Systems (~60 MCQ) 1. The binary number system uses how many digits? a) 2 Ã¢Å“â€¦ b) 8 c) 10 d) 16 2. The octal number system

uses how many digits? a) 2 b) 8 Ã¢Å“â€¦ c) 10 d) 16 3. The hexadecimal number system uses how many digits? a) 8 b) 10 c) 16 Ã¢Å“â€¦ d) 2 4. Which of the following is NOT an input device? a) Keyboard b) Mouse c) Printer Ã¢Å“â€¦ d) Scanner 5. CPU stands for: a) Central Processing Unit Ã¢Å“â€¦ b) Central Peripheral Unit c) Control Processing Unit d) Computer Processing Unit 6. The main function of the CPU is: a) Storage of data b) Processing of data Ã¢Å“â€¦ c) Communication d) Display 7. RAM is: a) Volatile memory Ã¢Å“â€¦ b) Non -volatile memory c) Secondary storage d) Input device 8. ROM is: a) Volatile memory b) Non -volatile memory Ã¢Å“â€¦ c) Cache memory d) Input device 9. Which of the following is secondary storage? a) RAM b) Hard Disk Ã¢Å“â€¦ c) Cache d) Register 10. Which of the following is an example of application software? a) Windows OS b) Microsoft Word Ã¢Å“â€¦ c) BIOS d) Device driver 11. Operating system manages: a) Hardware resources Ã¢Å“â€¦ b) Only so ftware c) Only memory d) Only CPU 12. Assembly language uses: a) Binary code b) Mnemonics Ã¢Å“â€¦ c) High -level commands d) Natural language 13. Early computers used which number system? a) Binary b) Decimal Ã¢Å“â€¦ c) Octal d) Hexadecimal 14. First generation computers used: a) Vacuum tubes Ã¢Å“â€¦ b) Transistors c) ICs d) Microprocessors 15. Second generation computers used: a) Vacuum tubes b) Transistors Ã¢Å“â€¦ c) ICs d) Microprocessors 16. Third generation computers used: a) Vacuum tubes b) Transistors c) ICs Ã¢Å“â€¦ d) Microprocessors 17. Fourth generati on computers used: a) Vacuum tubes b) Transistors c) ICs d) Microprocessors Ã¢Å“â€¦ 18. Which is NOT a main component of a computer? a) CPU b) Memory c) Printer Ã¢Å“â€¦ d) I/O devices 19. The ALU performs: a) Arithmetic and logical operations Ã¢Å“â€¦ b) Only arithmetic c) Only logi c d) Data storage 20. The CU (Control Unit) manages: a) Arithmetic operations b) Instruction execution Ã¢Å“â€¦ c) Data storage d) Input/output 21. BIOS is stored in: a) RAM b) ROM Ã¢Å“â€¦ c) Cache d) Register 22. Number of bits in a byte: a) 4 b) 8 Ã¢Å“â€¦ c) 16 d) 32 23. 1 KB = ? a) 1024 Bytes Ã¢Å“â€¦ b) 1000 Bytes c) 512 Bytes d) 2048 Bytes 24. Internet is an example of: a) LAN b) MAN c) WAN Ã¢Å“â€¦ d) PAN 25. Which is a type of software? a) Operating system Ã¢Å“â€¦ b) Compiler Ã¢Å“â€¦ c) Word processor Ã¢Å“â€¦ d) All of the above Ã¢Å“â€¦ 26. Binary addition: 101 + 110 = ? a) 1001 Ã¢Å“â€¦ b) 111 c) 1010 d) 1100 27. Decimal 15 in binary is: a) 1010 b) 1111 Ã¢Å“â€¦ c) 1101 d) 1001 28. Decimal 255 in hexadecimal is: a) 0xFF Ã¢Å“â€¦ b) 0xAA c) 0xF0 d) 0xFE 29. The fastest memory in computer is: a) RAM b) Cache Ã¢Å“â€¦ c) ROM d) Hard Disk 30. Number of general -purpose registers in 8086: a) 4 b) 8 Ã¢Å“â€¦ c) 16 d) 2 31. What is the base of the hexadecimal system? a) 2 b) 8 c) 10 d) 16 Ã¢Å“â€¦ 32. A nibble consists of: a) 2 bits b) 4 bits Ã¢Å“â€¦ c) 8 bits d) 16 bits 33. CPU clock speed is measured in: a) Hertz Ã¢Å“â€¦ b) Volt c) Ampere d) Joule 34. Program that translates high-level language to machine code: a) Compiler Ã¢Å“â€¦ b) Assembler c) Interpreter d) Loader 35. Which memory is used to store BIOS? a) ROM Ã¢Å“â€¦ b) RAM c) Cache d) Register 36. The main memory is: a) RAM Ã¢Å“â€¦ b) ROM c) Hard Disk d) Cache 37. Cache memory is located: a) Between CPU and main memory Ã¢Å“â€¦ b) On hard disk c) In I/O device d) In printer 38. The smallest unit of data in a computer: a) Byte b) Bit Ã¢Å“â€¦ c) Nibble d) Word 39. ASCII is used for: a) Images b) Text Ã¢Å“â€¦ c) Audio d) Video 40. Unicode supports: a) English only b) Multip le languages Ã¢Å“â€¦ c) Binary d) Hexadecimal 41. Operating system is: a) System software Ã¢Å“â€¦ b) Application software c) Firmware d) Hardware 42. Instruction cycle consists of: a) Fetch Ã¢Å“â€¦ b) Decode Ã¢Å“â€¦ c) Execute Ã¢Å“â€¦ d) All of the above Ã¢Å“â€¦ 43. Which of the following is NOT a high-level language? a) C b) Python c) Assembly Ã¢Å“â€¦ d) Java 44. HDD stores data in: a) RAM b) Magnetic disks Ã¢Å“â€¦ c) SSD d) Cache 45. SSD is faster than HDD because: a) Uses flash memory Ã¢Å“â€¦ b) Uses magnetic disks c) Less durable d) Has moving parts 46. Input devices convert : a) Digital Ã¢â€ â€™ Analog b) Human data Ã¢â€ â€™ Digital Ã¢Å“â€¦ c) Digital Ã¢â€ â€™ Human readable d) None 47. Output devices convert: a) Digital Ã¢â€ â€™ Analog b) Digital Ã¢â€ â€™ Human readable Ã¢Å“â€¦ c) Analog Ã¢â€ â€™ Digital d) None 48. Primary memory is: a) Volatile Ã¢Å“â€¦ b) Non -volatile c) Permanent d) Secon dary 49. Secondary memory is: a) Volatile b) Non -volatile Ã¢Å“â€¦ c) Faster than RAM d) Registers 50. Software that helps run other programs: a) Operating system Ã¢Å“â€¦ b) Application c) Utility d) Driver 51. Early computer Ã¢â‚¬Å“ENIACÃ¢â‚¬â€ used: a) Transistors b) Vacuum tubes Ã¢Å“â€¦ c) ICs d) Microprocessors 52. Which is NOT a characteristic of computer? a) Speed b) Accuracy c) Emotions Ã¢Å“â€¦ d) Storage 53. Binary subtraction: 1010 - 0110 = ? a) 0100 Ã¢Å“â€¦ b) 1001 c) 0011 d) 1110 54. ASCII stands for: a) American Standard Code for Information Interchange Ã¢Å“â€¦ b) Au tomatic System Code for Input c) Analog Standard Code for Information d) All of the above 55. Word length in 8086 microprocessor: a) 8-bit b) 16 -bit Ã¢Å“â€¦ c) 32 -bit d) 64 -bit 56. Early computers were used mainly for: a) Gaming b) Calculations Ã¢Å“â€¦ c) Internet browsing d) Social media 57. Input to CPU is through: a) Registers Ã¢Å“â€¦ b) ALU c) CU d) Memory 58. Output from CPU is via: a) Registers b) Memory c) I/O devices Ã¢Å“â€¦ d) ALU 59. Instruction set architecture defines: a) Hardware b) Software c) CPU instructions Ã¢Å“â€¦ d) Memory only 60. Which dev ice connects a computer to the internet? a) Router Ã¢Å“â€¦ b) Printer c) Keyboard d) Monitor Electrical Circuits (~60 MCQ) 1. OhmÃ¢â‚¬â„¢s law states: a) V = IR Ã¢Å“â€¦ b) P = IVÃ‚Â² c) I = V/P d) V = IÃ‚Â²R 2. In a series circuit, the current is: a) Same in all elements Ã¢Å“â€¦ b) Different in each element c) Zero d) Depends on voltage only 3. In a parallel circuit, the voltage across each branch is: a) Same Ã¢Å“â€¦ b) Different c) Zero d) Depends on resistance 4. KirchhoffÃ¢â‚¬â„¢s Current Law (KCL) is based on: a) Energy conservation b) Charge conservation Ã¢Å“â€¦ c) OhmÃ¢â‚¬â„¢s law d) FaradayÃ¢â‚¬â„¢s law 5. KirchhoffÃ¢â‚¬â„¢s Voltage Law (KVL) is based on: a) Energy conservation Ã¢Å“â€¦ b) Charge conservation c) Power conservation d) Resistance law 6. Power in a resistive circuit: a) P = VI Ã¢Å“â€¦ b) P = VÃ‚Â²/R Ã¢Å“â€¦ c) P = IÃ‚Â²R Ã¢Å“â€¦ d) All of the above Ã¢Å“â€¦ 7. Voltage divider formula: a) Vx = V(Rx/Rtotal) Ã¢Å“â€¦ b) Vx = IR c) Vx = V/R d) Vx = IRÃ‚Â² 8. Current divider formula applies to: a) Series circuit b) Parallel circuit Ã¢Å“â€¦ c) Both d) None 9. TheveninÃ¢â‚¬â„¢s theorem simplifies a circuit to: a) Voltage source and series resistor Ã¢Å“â€¦ b) Current

source and series resistor c) Voltage source and parallel resistor d) Current source and parallel resistor 10. NortonÃ¢â‚¬â„¢s theorem simplifies a circuit to: a) Current source and parallel resistor Ã¢Å“â€¦ b) Voltage sourc e and series resistor c) Current source and series resistor d) Voltage source and parallel resistor 11. Maximum power transfer occurs when: a) Load R = Source R Ã¢Å“â€¦ b) Load R > Source R c) Load R < Source R d) Load R = 0 12. Superposition theorem is applicable for: a) Linear circuits Ã¢Å“â€¦ b) Non -linear circuits c) Series circuits only d) Parallel circuits only 13. Resistance unit is: a) Ohm Ã¢Å“â€¦ b) Volt c) Ampere d) Watt 14. Voltage unit is: a) Ohm b) Volt Ã¢Å“â€¦ c) Ampere d) Watt 15. Current unit is: a) Ohm b) Volt c) Ampere Ã¢Å“â€¦ d) Watt 16. Capacitance unit is: a) Farad Ã¢Å“â€¦ b) Henry c) Ohm d) Tesla 17. Inductance unit is: a) Henry Ã¢Å“â€¦ b) Farad c) Ohm d) Tesla 18. Capacitors in series: a) 1/Ceq = ÃŽÂ£(1/Ci) Ã¢Å“â€¦ b) Ceq = ÃŽÂ£Ci c) Ceq = ÃŽÂ£CÃ‚Â² d) Ceq = 1/ÃŽÂ£C 19. Capacitors in parallel: a) Ceq = ÃŽÂ£Ci Ã¢Å“â€¦ b) 1/Ceq = ÃŽÂ£(1/Ci) c) Ce q = Ã¢Ë†Å¡ÃŽÂ£Ci d) Ceq = None 20. Inductors in series: a) Leq = ÃŽÂ£Li Ã¢Å“â€¦ b) 1/Leq = ÃŽÂ£(1/Li) c) Leq = Ã¢Ë†Å¡ÃŽÂ£Li d) None 21. Inductors in parallel: a) Leq = ÃŽÂ£Li b) 1/Leq = ÃŽÂ£(1/Li) Ã¢Å“â€¦ c) Leq = Ã¢Ë†Å¡ÃŽÂ£Li d) None 22. RLC series circuit resonance condition: a) XL = XC Ã¢Å“â€¦ b) XL > XC c) XL < XC d) R = 0 23. Reactance of inductor: a) XL = 2Ãâ‚¬fL Ã¢Å“â€¦ b) XL = 1/2Ãâ‚¬fL c) XL = L/f d) XL = 1/L 24. Reactance of capacitor: a) XC = 1/2Ãâ‚¬fC Ã¢Å“â€¦ b) XC = 2Ãâ‚¬fC c) XC = 1/C d) XC = 2C 25. Impedance of series RLC: a) Z = Ã¢Ë†Å¡(RÃ‚Â² + (XL -XC)Ã‚Â²) Ã¢Å“â€¦ b) Z = R + XL + XC c) Z = R/(XL -XC) d) Z = RÃ‚Â² + LÃ‚Â²

+ CÃ‚Â² 26. Power factor = cosÃŽÂ¸ ÃŽÂ¸ is: a) Phase difference between voltage and current Ã¢Â€Â“â€¦ b) Voltage c) Current d) Resistance 27. Energy stored in inductor: a) W = Ã‚Â½ LIÃ‚Â² Ã¢Â€Â“â€¦ b) W = Ã‚Â½ CVÃ‚Â² c) W = IÃ‚Â²R d) W = VI 28. Energy stored in capacitor: a) W = Ã‚Â½ CVÃ‚Â² Ã¢Â€Â“â€¦ b) W = Ã‚Â½ L IÃ‚Â² c) W = VI d) W = IÃ‚Â²R 29. Node voltage method is used for: a) Parallel analysis Ã¢Â€Â“â€¦ b) Series analysis c) Superposition d) None 30. Mesh current method is used for: a) Series analysis b) Loop analysis Ã¢Â€Â“â€¦ c) Node analysis d) Both 31. Source transformation converts: a) Voltage source + series R Ã¢â€ â€™ Current source + parallel R Ã¢Â€Â“â€¦ b) Current source + parallel R Ã¢â€ â€™ Voltage source + series R Ã¢Â€Â“â€¦ c) Both a & b Ã¢Â€Â“â€¦ d) None 32. Dependent source is: a) Independent voltage b) Controlled by another circuit variable Ã¢Â€Â“â€¦ c) Uncontrol led d) Always current source 33. Capacitor blocks: a) DC Ã¢Â€Â“â€¦ b) AC c) Both d) None 34. Inductor blocks: a) AC Ã¢Â€Â“â€¦ b) DC c) Both d) None 35. Time constant of RC circuit: a) Ã‚Â€Ž = RC Ã¢Â€Â“â€¦ b) Ã‚Â€Ž = L/R c) Ã‚Â€Ž = R/L d) Ã‚Â€Ž = 1/RC 36. Time constant of RL circuit: a) Ã‚Â€Ž = RC b) Ã‚Â€Ž = L/R Ã¢Â€Â“â€¦ c) Ã‚Â€Ž = R/L d) Ã‚Â€Ž = 1/L 37. For AC series RLC, resonance frequency: a) f = 1/2Ã‚Â¬Ã¢Ë†Å¡LC Ã¢Â€Â“â€¦ b) f = Ã¢Ë†Å¡LC c) f = 2Ã‚Â¬Ã¢Ë†Å¡LC d) f = LC 38. In resonance, current is: a) Minimum b) Maximum Ã¢Â€Â“â€¦ c) Zero d) Constant 39. Voltage across L or C at resonance: a) Less than supply b) Equal to supply c) Can be greater than supply Ã¢Â€Â“â€¦ d) Zero 40. RMS value of sinusoidal current: a) Imax b) Imax/Ã¢Ë†Å¡2 Ã¢Â€Â“â€¦ c) Imax/2 d) Ã¢Ë†Å¡2 Imax 41. RMS value of sinusoidal voltage: a) Vmax b) Vmax/Ã¢Ë†Å¡2 Ã¢Â€Â“â€¦ c) Vmax/2 d) Ã¢Ë†Å¡2 Vmax 42. Average power in AC circuit: a) Vrms Ãƒâ€” Irms Ãƒâ€” cosÃŽÂ¸ Ã¢Â€Â“â€¦ b) Vrms Ãƒ â€” Irms Ãƒâ€” sinÃŽÂ¸ c) Vrms Ãƒâ€” Irms d) IrmsÃ‚Â² Ãƒâ€” R 43. Impedance in series AC circuit: a) Z = R + j(XL - XC) Ã¢Â€Â“â€¦ b) Z = R + XL + XC c) Z = R + 1/(XL - XC) d) Z = RÃ‚Â² + (XL -XC)Ã‚Â² 44. Admittance Y = a) 1/Z Ã¢Â€Â“â€¦ b) Z c) R/Z d) Z/R 45. Phase angle Ã¢Â€ = a) tanÃ¢Â€Â‹Â»Ã‚Â¹((XL - XC)/R) Ã¢Â€Â“â€¦ b) tanÃ¢Â€Â‹Â»Ã‚Â¹(R/(XL -XC)) c) cosÃ¢Â€Â‹Â»Ã‚Â¹((XL -XC)/R) d) sinÃ¢Â€Â‹Â»Ã‚Â¹((XL -XC)/R) 46. Wye to Delta conversion is used for: a) Resistors Ã¢Â€Â“â€¦ b) Capacitors Ã¢Â€Â“â€¦ c) Inductors Ã¢Â€Â“â€¦ d) All Ã¢Â€Â“â€¦ 47. Delta to Wye conversion is used for: a) Resistors Ã¢Â€Â“â€¦ b) Capacitors Ã¢Â€Â“â€¦ c) Inductors Ã¢Â€Â“â€¦ d) All Ã¢Â€Â“â€¦ 48. RMS voltage of triangular waveform : a) Vm/Ã¢Ë†Å¡2 b) Vm/Ã¢Ë†Å¡3 Ã¢Â€Â“â€¦ c) Vm/2 d) Vm 49. In AC circuits, instantaneous power: a) p = vi Ã¢Â€Â“â€¦ b) p = iÃ‚Â²R c) p = vÃ‚Â²/R d) p = Vavg Ãƒâ€” Iavg 50. Current leads voltage in: a) Capacitive circuit Ã¢Â€Â“â€¦ b) Inductive circuit c) Resistive circuit d) None 51. Current lags voltage in: a) Capacitive b) Inductive Ã¢Â€Â“â€¦ c) Resistive d) None 52. Power dissipated in resistor: a) IÃ‚Â²R Ã¢Â€Â“â€¦ b) VÃ‚Â²/R Ã¢Â€Â“â€¦ c) VI Ã¢Â€Â“â€¦ d) All of the above Ã¢Â€Â“â€¦ 53. Series LC circuit at resonance: a) Impedance minimum Ã¢Â€Â“â€¦ b) Impedance maximum c) Current minimum d) Voltage minimum 54. Parallel LC circu it at resonance: a) Impedance minimum b) Impedance maximum Ã¢Â€Â“â€¦ c) Current maximum d) Voltage zero 55. Quality factor Q = a) XL/R Ã¢Â€Â“â€¦ b) XC/R c) R/XL d) R/XC 56. Transient response occurs in: a) DC circuits with L or C Ã¢Â€Â“â€¦ b) Pure resistive DC circuits c) AC steady -state d) None 57. Charging capacitor current: a) Maximum at t=0 Ã¢Â€Â“â€¦ b) Zero at t=0 c) Constant d) None 58. Discharging capacitor current: a) Maximum at t=0 Ã¢Â€Â“â€¦ b) Zero at t=0 c) Constant d) None 59. DC steady -state inductor acts as: a) Open circuit b) Short circuit Ã¢Â€Â“â€¦ c) Capacitor d) Resistor 60. DC steady -state capacitor acts as: a) Open circuit Ã¢Â€Â“â€¦ b) Short circuit c) Inductor d) Resistor Digital Logic Design (~70 MCQ) 1. Boolean algebra was introduced by: a) Newton b) Boole Ã¢Â€Â“â€¦ c) Einstein d) Maxwell 2. The AND gate output is 1 only when: a) Both inputs are 0 b) Both inputs are 1 Ã¢Â€Â“â€¦ c) One input is 1 d) Any input is 0 3. The OR gate output is 0 only when: a) Both inputs are 0 Ã¢Â€Â“â€¦ b) Both inputs are 1 c) One input is 1 d) Any input is 1 4. The NOT gate inverts: a) 1Ã¢â€ â€™0, 0Ã¢â€ â€™1 Ã¢Â€Â“â€¦ b) 1Ã¢â€ â€™1, 0Ã¢â€ â€™0 c) 1Ã¢â€ â€™1, 0Ã¢â€ â€™1 d) None 5. De MorganÃ¢â‚¬â„¢s theorem states: a) (AÃ‚Â·B)Ã¢â‚¬â„¢ = Ã¢â‚¬â„¢ + BÃ¢â‚¬â„¢ Ã¢Â€Â“â€¦ b) (A+B)Ã¢â‚¬â„¢ = A + B c) (A+B)Ã¢â‚¬â„¢ = Ã¢â‚¬â„¢BÃ¢â‚¬â„¢ Ã¢Â€Â“â€¦ d) Both a & c Ã¢Â€Â“â€¦ 6. NAND gate is called: a) Universal gate Ã¢Â€Â“â€¦ b) Basic gate c) Logic gate d) None 7. NOR gate is called: a) Universal gate Ã¢Â€Â“â€¦ b) Basic gate c) Logic gate d) None 8. XOR gate output is 1 when: a) Inputs same b) Inputs different Ã¢Â€Â“â€¦ c) Both inputs 0 d) Both inputs 1 9. XNOR gate output is 1 when: a) Inputs same Ã¢Â€Â“â€¦ b) Inputs different c) Both 0 d) Both 1 10. Sum-of- Products (SOP) is: a) OR of AND terms Ã¢Â€Â“â€¦ b) AND of OR terms c) XOR of AND terms d) NAND of OR terms 11. Product -of-Sums (POS) is: a) OR of AND terms b) AND of OR terms Ã¢Â€Â“â€¦ c) XOR of OR terms d) NOR of AND terms 12. K-map is used for: a) Minimization of Boolean expression Ã¢Â€Â“â€¦ b) Maximization c) M ultiplexing d) Latching 13. 2-to-1 multiplexer has: a) 2 inputs, 1 select Ã¢Â€Â“â€¦ b) 2 outputs, 1 input c) 1 input, 2 select d) 2 outputs, 2 select 14. 4- to-1 multiplexer has: a) 4 inputs, 2 select Ã¢Â€Â“â€¦ b) 4 outputs, 2 select c) 2 inputs, 4 select d) 1 input, 4 select 15. Demu ltiplexer converts: a) 1 input Ã¢â€ â€™ many outputs Ã¢Â€Â“â€¦ b) Many inputs Ã¢â€ â€™ 1 output c) OR operation d) AND operation 16. Decoder converts: a) n inputs Ã¢â€ â€™ 2Ã¢â€ Â¿ outputs Ã¢Â€Â“â€¦ b) 2Ã¢â€ Â¿ inputs Ã¢â€ â€™ n outputs c) n outputs Ã¢â€ â€™ n inputs d) None 17. Encoder converts: a) 2Ã¢â€ Â¿ inputs Ã¢â€ â€™ n outputs Ã¢Â€Â“â€¦ b) n inputs Ã¢â€ â€™ 2Ã¢â€ Â¿ outputs c) OR Ã¢â€ â€™ AND d) None 18. Half adder produces: a) Sum only b) Carry only c) Sum & Carry Ã¢Â€Â“â€¦ d) Difference & Borrow 19. Full adder has: a) 2 inputs b) 3 inputs Ã¢Â€Â“â€¦ c) 4 inputs d) 1 input

20. Flip-flops store: a) Voltage b) Bit of information Ã¢Â€Â“â€¦ c) Curre nt d) Logic gate 21. SR flip -flop is built using: a) NAND/NOR gates Ã¢Â€Â“â€¦ b) XOR c) XNOR d) AND 22. JK flip -flop overcomes: a) Race condition in SR Ã¢Â€Â“â€¦ b) Memory loss c) Input error d) Timing error 23. D flip - flop output = a) Input D Ã¢Â€Â“â€¦ b) Input Q c) Inverted D d) Sum 24. T flip-flop toggles on: a) T=1 Ã¢Â€Â“â€¦ b) T=0 c) Clock high d) Reset 25. Asynchronous counter uses: a) Same clock Ã¢Â€Â“â€¦ b) Ripple effect c) Parallel clocking d) Both a & b Ã¢Â€Â“â€¦ 26. Synchronous counter: a) All flip - flops clocked simultaneously Ã¢Â€Â“â€¦ b) Ripple clocked c) Not clocked d) None 27. Mealy machine output depends on: a) Present state only b) Present input only c) Present state & input Ã¢Â€Â“â€¦ d) Previous state 28. Moore machine output depends on: a) Present state only Ã¢Â€Â“â€¦ b) Present input c) Previous state d) Both state & input 29. PLA stands fo r: a) Programmable Logic Array Ã¢Â€Â“â€¦ b) Parallel Logic Array c) Primary Logic Adder d) None 30. PLA used for: a) Logic function implementation Ã¢Â€Â“â€¦ b) Storage c) Multiplexing d) None 31. Race around problem occurs in: a) SR flip -flop b) JK flip -flop Ã¢Â€Â“â€¦ c) D flip -flop d) T flip-flop 32. Pulse mode design avoids: a) Multiple triggering Ã¢Â€Â“â€¦ b) Single triggering c) Flip -flop operation d) Logic minimization 33. Fundamental mode design uses: a) Only one input change at a time Ã¢Â€Â“â€¦ b) Multiple inputs c) Asynchronous d) None 34. Combinational circ uit output depends on: a) Present inputs only Ã¢Â€Â“â€¦ b) Present & past inputs c) Clock d) State 35. Sequential circuit output depends on: a) Present inputs only b) Present & past inputs Ã¢Â€Â“â€¦ c) Clock only d) None 36. Boolean expression simplification reduces: a) Gate coun t Ã¢Â€Â“â€¦ b) Power consumption Ã¢Â€Â“â€¦ c) Complexity Ã¢Â€Â“â€¦ d) All Ã¢Â€Â“â€¦ 37. XOR gate is equivalent to: a) AÃ¢â‚¬â„¢B + ABÃ¢â‚¬â„¢ Ã¢Â€Â“â€¦ b) AB + AÃ¢â‚¬â„¢BÃ¢â‚¬â„¢ c) A + B d) AÃ‚Â·B 38. XNOR gate is equivalent to: a) AB + AÃ¢â‚¬â„¢BÃ¢â‚¬â„¢ Ã¢Â€Â“â€¦ b) AÃ¢â‚¬â„¢B + ABÃ¢â‚¬â„¢ c) A + B d) AÃ‚Â·B 39. NAND gate expression: a) (AB)Ã¢â‚¬â„¢ Ã¢Â€Â“â€¦ b) A + B c) AB d) (A + B)Ã¢â‚¬â„¢ 40. NOR gate expression: a) (A+B)Ã¢â‚¬â„¢ Ã¢Â€Â“â€¦ b) A + B c) AB d) (AB)Ã¢â‚¬â„¢ 41. Number of minterms for n variables: a) n b) 2Ã¢â€ Â¿ Ã¢Â€Â“â€¦ c) nÃ‚Â² d) 2n 42. Number of maxterms for n variables: a) n b) 2Ã¢â€ Â¿ Ã¢Â€Â“â€¦ c) nÃ‚Â² d) 2n 43. Canonical SOP uses: a) Minterms Ã¢Â€Â“â€¦ b)

Maxterms c) Sum d) Product 44. Canonical POS uses: a) Minterms b) Maxterms Ã¢Å“â€¦ c) Sum d) Product 45. Logic minimization reduces: a) Cost Ã¢Å“â€¦ b) Speed c) Complexity Ã¢Å“â€¦ d) Both a & c Ã¢Å“â€¦ 46. Flip-flop stores: a) 1 bit Ã¢Å“â€¦ b) 2 bits c) 4 bits d) Variable 47. Latches are: a) Level triggered Ã¢Å“â€¦ b) Edge triggered c) Pulse mode d) None 48. Flip-flops are: a) Level triggered b) Edge triggered Ã¢Å“â€¦ c) Pulse mode d) None 49. Pulse -triggered flip -flops help avoid: a) Race around Ã¢Å“â€¦ b) Memory loss c) Logic error d) Power consumption 50. Asynchronous counter also called: a) Ripple counter Ã¢Å“â€¦ b) Ri ng counter c) Synchronous counter d) Johnson counter 51. Synchronous counter is: a) Ripple type b) Clocked simultaneously Ã¢Å“â€¦ c) Level triggered d) None 52. 4-bit asynchronous counter counts: a) 0Ã¢â‚¬â€œ7 b) 0Ã¢â‚¬â€œ15 Ã¢Å“â€¦ c) 0Ã¢â‚¬â€œ31 d) 0Ã¢â‚¬â€œ63 53. 3-bit synchronous counter max count: a) 7 Ã¢Å“â€¦ b) 3 c) 8 d) 15 54. Edge triggering refers to: a) Clock rising/falling Ã¢Å“â€¦ b) Clock high c) Clock low d) Pulse width 55. JK flip -flop toggles when: a) J=K=1 Ã¢Å“â€¦ b) J=1, K=0 c) J=0, K=1 d) J=K=0 56. Clock frequency determines: a) Circuit speed Ã¢Å“â€¦ b) Gate numbe r c) Power d) Output only 57. Race around occurs when propagation delay < pulse width: a) True Ã¢Å“â€¦ b) False c) Sometimes d) None 58. Edge -triggered flip -flop avoids: a) Multiple toggles Ã¢Å“â€¦ b) Memory c) Delay d) Logic error 59. MUX selects: a) One input Ã¢Å“â€¦ b) All inputs c) Output d) Gate 60. DEMUX distributes: a) Input to one output Ã¢Å“â€¦ b) Input to all outputs c) Gate d) None 61. SOP minimization reduces: a) AND gates b) OR gates c) Both Ã¢Å“â€¦ d) XOR 62. POS minimization reduces: a) OR gates b) AND gates c) Both Ã¢Å“â€¦ d) NAND 63. Universal gate can implement: a) All logic Ã¢Å“â€¦ b) None c) Only OR d) Only AND 64. Flip-flop characteristic table lists: a) Inputs & outputs Ã¢Å“â€¦ b) Inputs only c) Outputs only d) Clock only 65. Level -triggered latch changes state: a) Clock high Ã¢Å“â€¦ b) Clock low c) Both d) Edge 66. Edge -trigger ed flip -flop changes state: a) Rising/falling Ã¢Å“â€¦ b) Level high c) Level low d) None 67. Pulse mode design avoids: a) Multiple toggles Ã¢Å“â€¦ b) Race c) Timing errors Ã¢Å“â€¦ d) All Ã¢Å“â€¦ 68. State diagram represents: a) Sequential behavior Ã¢Å“â€¦ b) Combinational logic c) Input only d) Output only 69. Mealy machine faster than Moore because: a) Output depends on input Ã¢Å“â€¦ b) Output depends on state c) Uses fewer flip -flops d) None 70. Fundamental mode design ensures: a) Only one input changes at a time Ã¢Å“â€¦ b) Multiple input changes c) Synchronous d) None Basic Electronics (~60 MCQ) 1. Diode allows current to flow in: a) Both directions b) One direction Ã¢Å“â€¦ c) No direction d) Depends on voltage 2. Forward biased diode has: a) High resistance b) Low resistance Ã¢Å“â€¦ c) Infinite resistance d) Zero resistance 3. Reve rse biased diode has: a) High resistance Ã¢Å“â€¦ b) Low resistance c) Zero resistance d) Low voltage 4. Zener diode is used for: a) Amplification b) Voltage regulation Ã¢Å“â€¦ c) Switching d) Oscillation 5. Half-wave rectifier uses: a) 1 diode Ã¢Å“â€¦ b) 2 diodes c) 4 diodes d) None 6. Full-wave rectifier uses: a) 1 diode b) 2 diodes Ã¢Å“â€¦ c) 4 diodes d) None 7. Bridge rectifier uses: a) 2 diodes b) 3 diodes c) 4 diodes Ã¢Å“â€¦ d) 1 diode 8. Clipper circuit: a) Clips voltage above/below reference Ã¢Å“â€¦ b) Amplifies signal c) Rectifies signal d) Filters signal 9. Clamper circuit: a) Shifts signal DC level Ã¢Å“â€¦ b) Clips voltage c) Rectifies d) Amplifies 10. Bipolar junction transistor (BJT) has: a) 2 terminals b) 3 terminals Ã¢Å“â€¦ c) 4 terminals d) 5 terminals 11. BJT modes: a) Active Ã¢Å“â€¦ b) Cut -off Ã¢Å“â€¦ c) Saturation Ã¢Å“â€¦ d) All Ã¢Å“â€¦ 12. Common emitter configuration provides: a) Voltage gain Ã¢Å“â€¦ b) Current gain Ã¢Å“â€¦ c) Power gain Ã¢Å“â€¦ d) All Ã¢Å“â€¦ 13. Common base configuration has: a) Current gain <1 Ã¢Å“â€¦ b) Voltage gain high Ã¢Å“â€¦ c) Input low d) Output low 14. Common collector configuratio n is also called: a) Emitter follower Ã¢Å“â€¦ b) Base follower c) Collector follower d) None 15. BJT used as switch operates in: a) Active region b) Cut -off & saturation Ã¢Å“â€¦ c) Reverse bias d) None 16. Load line represents: a) Relationship between V & I Ã¢Å“â€¦ b) Current only c) Voltage only d) None 17. Stability factor determines: a) BJT bias stability Ã¢Å“â€¦ b) Voltage c) Current d) Resistance 18. Small signal model of BJT uses: a) h- parameters Ã¢Å“â€¦ b) Z-parameters c) Y-parameters d) None 19. Voltage gain of CE amplifier: a) High Ã¢Å“â€¦ b) Low c) Zer o d) Negative 20. Current gain of CE amplifier: a) High Ã¢Å“â€¦ b) Low c) Zero d) Negative 21. Input impedance of CB amplifier: a) High b) Low Ã¢Å“â€¦ c) Medium d) Variable 22. Output impedance of CE amplifier: a) Low b) High Ã¢Å“â€¦ c) Medium d) Variable 23. Field effect transistor (FET) has: a) High input impedance Ã¢Å“â€¦ b) Low input impedance c) Medium d) Variable 24. JFET gate is: a) Forward biased b) Reverse biased Ã¢Å“â€¦ c) Floating d) None 25. MOSFET can be: a) Depletion type Ã¢Å“â€¦ b) Enhancement type Ã¢Å“â€¦ c) Both Ã¢Å“â€¦ d) None 26. FET operates on: a) Voltage contr ol Ã¢Å“â€¦ b) Current control c) Both d) None 27. Diodeâ‚¬â„¢s knee voltage ~ a) 0.7V for silicon Ã¢Å“â€¦ b) 0.3V for silicon c) 0.7V for germanium d) 0.3V for germanium 28.

Zener voltage is: a) Breakdown voltage Ã¢Å“â€¦ b) Forward voltage c) Knee voltage d) None 29. Half-wave rectifier out put frequency = a) Input frequency b) Same as input Ã¢Å“â€¦ c) Twice input d) Half input 30. Full-wave rectifier output frequency = a) Same as input b) Twice input Ã¢Å“â€¦ c) Half input d) None 31. Capacitor filter removes: a) AC ripples Ã¢Å“â€¦ b) DC c) Voltage d) Current 32. Diode re verse recovery time: a) Time to turn off Ã¢Å“â€¦ b) Time to turn on c) Forward voltage d) None 33. Transistor as amplifier operates in: a) Cut -off b) Active Ã¢Å“â€¦ c) Saturation d) Reverse 34. Transistor as switch operates in: a) Active b) Cut -off & saturation Ã¢Å“â€¦ c) Reverse d) None 35. BJT has: a) Base, emitter, collector Ã¢Å“â€¦ b) Gate, source, drain c) Emitter, collector d) None 36. FET has: a) Base, collector, emitter b) Gate, source, drain Ã¢Å“â€¦ c) Input, output d) None 37. MOSFET input impedance: a) Low b) Very high Ã¢Å“â€¦ c) Medium d) Variable 38. Clipper removes: a) Part of waveform Ã¢Å“â€¦ b) Entire waveform c) DC d) AC 39. Clamper shifts: a) DC level Ã¢Å“â€¦ b) AC level c) Both d) None 40. Forward biased diode resistance: a) High b) Low Ã¢Å“â€¦ c) Infinite d) Zero 41. Reverse biased diode leakage current: a) High b) Low Ã¢Å“â€¦ c) Zero d) Medium 42. Power dissipation in transistor: a) VCE Ãƒâ€” IC Ã¢Å“â€¦ b) VBE Ãƒâ€” IB c) IC Ãƒâ€” IB d) None 43. CE amplifier phase shift: a) 0Ã‚Â° b) 180Ã‚Â° Ã¢Å“â€¦ c) 90Ã‚Â° d) None 44. CB amplifier phase shift: a) 0Ã‚Â° Ã¢Å“â€¦ b) 180Ã‚Â° c) 90Ã‚Â° d) None 45. CC amplifier phase shift: a) 0Ã‚Â° Ã¢Å“â€¦ b) 180 Ã‚Â° c) 90Ã‚Â° d) None 46. Small signal model helps determine: a) Gain Ã¢Å“â€¦ b) Impedance Ã¢Å“â€¦ c) Both Ã¢Å“â€¦ d) None 47. Junction diode symbol: a) Triangle Ã¢â€ â€™ line Ã¢Å“â€¦ b) Line Ã¢â€ â€™ triangle c) Circle d) Square 48. Zener diode symbol: a) Line with bent bar Ã¢Å“â€¦ b) Triangle Ã¢â€ â€™ line c) Circle d) Square 49. Half-wave rectifier uses: a) Transformer Ã¢Å“â€¦ b) Diode Ã¢Å“â€¦ c) Capacitor Ã¢Å“â€¦ d) All Ã¢Å“â€¦ 50. Full-wave rectifier bridge has: a) 2 diodes b) 4 diodes Ã¢Å“â€¦ c) 3 diodes d) 1 diode 51. Peak inverse voltage (PIV) in diode: a) Max reverse voltage Ã¢Å“â€¦ b) Forward voltage c) Average voltage d) None 52. Transistor cutoff: a) IB=0 Ã¢Å“â€¦ b) IC=0 c) VCE small d) Active 53. Transistor saturation: a) VCEÃ¢â€°Ë†0 Ã¢Å“â€¦ b) ICÃ¢â€°Ë†0 c) IBÃ¢â€°Ë†0 d) Active 54. JFET operates: a) Forward biased Ã¢Å“â€¦ b) Reverse biased c) Zero bias d) None 55. MOSFET enhancement mode needs: a) Gate voltage Ã¢Å“â€¦ b) Gate current c) Source voltage d) Drain voltage 56. MOSFET depletion mode: a) Naturally conducting Ã¢Å“â€¦ b) Needs gate voltage c) Switch off d) None 57. Load line intersects: a) DC and AC curves Ã¢Å“â€¦ b) Input curve c) Output curve d) None 58. Diode cut -in voltage: a) Minimum voltage to conduct Ã¢Å“â€¦ b) Maximum c) Zero d) Infinite 59. Voltage multiplier uses: a) Diodes & capacitors Ã¢Å“â€¦ b) Transistors c) Resistors d) Inductors 60. Zener regulator provides: a) Constant voltage Ã¢Å“â€¦ b) Constant current c) Constant resistance d) None Microprocessor & Interfacing (~60 MCQ) 1. Microprocessor is: a) A software b) Central processing unit on a single chip Ã¢Å“â€¦ c) Memory chip d) Input device 2. Difference between microprocessor and microcontroller: a) Microprocessor lacks RAM/ROM Ã¢Å“â€¦ b) Microcontroller has built -in RAM/ROM Ã¢Å“â€¦ c) Both a & b Ã¢Å“â€¦ d)

None 3. 8086/8088 belongs to: a) 4-bit family b) 8-bit family c) 16 -bit family Ã¢Å“â€¦ d) 32 -bit family 4. 8086 has: a) 8-bit data bus b) 16 -bit data bus Ã¢Å“â€¦ c) 32 -bit data bu s d) 64 -bit data bus 5. Memory segmentation in 8086: a) Code, data, stack, extra Ã¢Å“â€¦ b) Input, output c) Registers only d) None 6. Instruction set of 8086 contains: a) Data transfer Ã¢Å“â€¦ b) Arithmetic Ã¢Å“â€¦ c) Logical Ã¢Å“â€¦ d) All Ã¢Å“â€¦ 7. Addressing mode specifies: a) How to acces s operands Ã¢Å“â€¦ b) Data size c) Clock d) Power 8. Immediate addressing uses: a) Constant value Ã¢Å“â€¦ b) Memory address c) Register d) Input 9. Register addressing uses: a) CPU register Ã¢Å“â€¦ b) Memory c) Input d) Constant 10. Direct addressing uses: a) Memory address Ã¢Å“â€¦ b) Regi ster c) Immediate d) Port 11. Indirect addressing uses: a) Register contains address Ã¢Å“â€¦ b) Memory contains address c) Immediate d) Port 12. Single -processor system has: a) One CPU Ã¢Å“â€¦ b) Multiple CPUs c) None d) All 13. Multi -processor system: a) One CPU b) Multiple CPUs Ã¢Å“â€¦ c) None d) All 14. Assembler converts: a) Assembly Ã¢â€ â€™ Machine code Ã¢Å“â€¦ b) High - level Ã¢â€ â€™ Assembly c) Machine Ã¢â€ â€™ Assembly d) None 15. Debugger is used for: a) Detecting errors Ã¢Å“â€¦ b) Writing code c) Compiling d) Executing only 16. 8255A is: a) Programmable Peripheral Interf ace Ã¢Å“â€¦ b) Timer c) DMA d) Memory 17. 8254 is: a) Programmable interval timer Ã¢Å“â€¦ b) PPI c) Interrupt controller d) UART 18. Keyboard interfacing can be done via: a) 8255 Ã¢Å“â€¦ b) 8254 c) 8259 d) DMA 19. LCD interfacing uses: a) 8255 Ã¢Å“â€¦ b) 8254 c) 8259 d) None 20. Printer interfac ing uses: a) Parallel Ã¢Å“â€¦ b) Serial c) Both Ã¢Å“â€¦ d) None 21. Stepper motor interfacing: a) 8255 Ã¢Å“â€¦ b) 8259 c) 8254 d) None 22. A/D converter converts: a) Analog Ã¢â€ â€™ Digital Ã¢Å“â€¦ b) Digital Ã¢â€ â€™ Analog c) Voltage d) Current 23. D/A converter converts: a) Analog Ã¢â€ â€™ Digital b) Digital Ã¢â€ â€™ Analog Ã¢Å“â€¦ c) Both d) None 24. 8259A is: a) Programmable interrupt controller Ã¢Å“â€¦ b) Timer c) PPI d) DMA 25. Interrupt vector table stores: a) Addresses of interrupt routines Ã¢Å“â€¦ b) Data c) Instructions d) None 26. DMA stands for: a) Direct Memory Access Ã¢Å“â€¦ b) Dynamic Memory Access c) Dual Memory Access d) Data Memory Access 27. Serial communication can be: a) Synchronous Ã¢Å“â€¦ b) Asynchronous Ã¢Å“â€¦ c) Both Ã¢Å“â€¦ d) None 28. EIA RS232 is: a) Physical communication standard Ã¢Å“â€¦ b) Protocol c) Memory d) Timer 29. Microprocessor clock controls: a) Instruction timing Ã¢Å“â€¦ b) Data c) Voltage d) Current 30. Bus demultiplexer separates: a) Address & data lines Ã¢Å“â€¦ b) Input lines c) Output lines d) Power 31. Bus controller manages: a) Data transfer Ã¢Å“â€¦ b) Instruction fetch c) Clock d) None 32. Programmed I/O means: a) CPU actively polls Ã¢Å“â€¦ b) CPU interrupts c) DMA d) None 33. Interrupt driven I/O: a) CPU waits b) CPU responds to interrupt Ã¢Å“â€¦ c) CPU ignores d) None 34. Parallel I/O port transfers: a) 1 bit b) Multiple bits simultaneously Ã¢Å“â€¦ c) Serially d) None 35. SRAM stands for: a) Static RAM Ã¢Å“â€¦ b) Serial RAM c) Synchronous RAM d) None 36. EEPROM stands for: a) Electrically Erasable Programmable ROM Ã¢Å“â€¦ b) RAM c) Flash d) None 37. Clock generator produces: a) Timing pulses Ã¢Å“â€¦ b) Data c) Instructions d) None 38. Stepper m otor moves in: a) Continuous rotation b) Steps Ã¢Å“â€¦ c) Random d) None 39. Timer applications include: a) Delay Ã¢Å“â€¦ b) Event counting Ã¢Å“â€¦ c) Pulse generation Ã¢Å“â€¦ d) All Ã¢Å“â€¦ 40. Asynchronous serial communication uses: a) Start & stop bits Ã¢Å“â€¦ b) Clock c) Both d) None 41. Microproces sor I/O address decoding ensures: a) Correct device access Ã¢Å“â€¦ b) Timing c) Speed d) None 42. Interrupt vector points to: a) Interrupt routine Ã¢Å“â€¦ b) Main program c) Data d) Timer 43. Single -step execution helps in: a) Debugging Ã¢Å“â€¦ b) Speeding c) Storage d) Communicati on 44. Flag registers store: a) Status Ã¢Å“â€¦ b) Data c) Address d) Control 45. Carry flag is set when: a) Addition exceeds limit Ã¢Å“â€¦ b) Subtraction negative c) Overflow d) Zero 46. Zero flag is set when: a) Result = 0 Ã¢Å“â€¦ b) Result > 0 c) Carry occurs d) None 47. Sign flag indica tes: a) Positive/negative Ã¢Å“â€¦ b) Zero c) Carry d) Overflow 48. Parity flag checks: a) Even/odd bits Ã¢Å“â€¦ b) Zero c) Carry d) Sign

49. Program counter stores: a) Next instruction address Ã¢Å“â€¦ b) Current instruction c) Data d) Stack pointer 50. Stack pointer points to: a) Top o f stack Ã¢Å“â€¦ b) Bottom c) Memory d) None 51. PUSH instruction: a) Store in stack Ã¢Å“â€¦ b) Retrieve from stack c) Clear stack d) None 52. POP instruction: a) Store b) Retrieve Ã¢Å“â€¦ c) Clear d) None 53. Software interrupt generated by: a) Instruction Ã¢Å“â€¦ b) External device c) Timer d) DMA 54. Hardware interrupt generated by: a) Device Ã¢Å“â€¦ b) Instruction c) Program d) Memory 55. Instruction cycle includes: a) Fetch Ã¢Å“â€¦ b) Decode Ã¢Å“â€¦ c) Execute Ã¢Å“â€¦ d) All Ã¢Å“â€¦ 56. Data bus width determines: a) Data size per transfer Ã¢Å“â€¦ b) Address c) Instruction d) Clock 57. Address bus width determines: a) Maximum memory accessible Ã¢Å“â€¦ b) Data size c) Instruction size d) Clock 58. Control signals include: a) RD, WR Ã¢Å“â€¦ b) ALE Ã¢Å“â€¦ c) INTA Ã¢Å“â€¦ d) All Ã¢Å“â€¦ 59. Microprocessor interfacing requires: a) Address decoding Ã¢Å“â€¦ b) Timing c) Data bus d) All Ã¢Å“â€¦ 60. Multi -processor system advantage: a) High speed Ã¢Å“â€¦ b) Parallel processing Ã¢Å“â€¦ c) Reliability Ã¢Å“â€¦ d) All Ã¢Å“â€¦ Communication Theory (~50 MCQ) 1. Fourier series represents: a) Continuous signals Ã¢Å“â€¦ b) Discrete signals c) Both d) None 2. Fourier transform converts: a) Time Ã¢â€ â€™ Frequency Ã¢Å“â€¦ b) Frequency Ã¢â€ â€™ Time c) Voltage Ã¢â€ â€™ Current d) None 3. Convolution in time domain equals: a) Multiplication in frequency domain Ã¢Å“â€¦ b) Addition c) Subtraction d) Division 4. ParsevalÃ¢â‚¬â„¢s theorem relates: a) Energy in time & frequency Ã¢Å“â€¦ b) Power c) Voltage d) Current 5. Entropy in information theory measures: a) Uncertainty Ã¢Å“â€¦ b) Speed c) Bandwidth d) Amplitude 6. ShannonÃ¢â‚¬â„¢s theorem gives: a) Maximum channel capacity Ã¢Å“â€¦ b) Minimum noise c) Maximum power d) None 7. Channel capacity depends on: a) Bandwidth Ã¢Å“â€¦ b) Signal -to-noise ratio Ã¢Å“â€¦ c) Both Ã¢Å“â€¦ d) None 8. Analog modulation includes: a) AM Ã¢Å“â€¦ b) FM Ã¢Å“â€¦ c) PM Ã¢Å“â€¦ d) All Ã¢Å“â€¦ 9. AM stands for: a) Amplitude Modulation Ã¢Å“â€¦ b) Angular Modulation c) Analog Modulation d) None 10. FM stands for: a) Frequency Modulation Ã¢Å“â€¦ b) Phase Modulation c) Amplitude Modulation d) None 11. PM stands for: a) Phase Modulation Ã¢Å“â€¦ b) Frequency Modulation c) Amplitude Modulation d) None 12. Modulation purpose: a) Efficient transmission Ã¢Å“â€¦ b) Amplification c) Rectification d) None 13. Demodulation recovers: a) Original signal Ã¢Å“â€¦ b) Noise c) Carrier d) None 14. Pulse Amplitude Modulation (PAM) uses: a) Amplitude of pulses Ã¢Å“â€¦ b) Frequency c) Phase d) None 15. Pulse Code Modulation (PCM) is: a) Digital modulation Ã¢Å“â€¦ b) Analog modulation c) Hybrid d) None 16. Delta modulation (DM) encodes: a) Di fference between samples Ã¢Å“â€¦ b) Absolute value c) Average d) None 17. Adaptive delta modulation (ADM) adjusts: a) Step size Ã¢Å“â€¦ b) Frequency c) Phase d) None 18. Time -Division Multiplexing (TDM) divides: a) Time slots Ã¢Å“â€¦ b) Frequency c) Phase d) None 19. Frequency -Division Multiplexing (FDM) divides: a) Frequency Ã¢Å“â€¦ b) Time c) Phase d) None 20. TDMA is: a) Time -division multiple access Ã¢Å“â€¦ b) Frequency -division c) Code -division d) None 21. FDMA is: a) Time -division b) Frequency -division multiple access Ã¢Å“â€¦ c) Code -division d) None 22. CDMA uses: a) Codes to separate users Ã¢Å“â€¦ b) Time slots c) Frequency bands d) None 23. Nyquist sampling theorem states: a) Fs Ã¢â€°Â¥ 2 Ãƒâ€” fmax Ã¢Å“â€¦ b) Fs < fmax c) Fs = fmax d) None 24. Aliasing occurs if: a) Fs < 2 Ãƒâ€” fmax Ã¢Å“â€¦ b) Fs Ã¢â€°Â¥ 2 Ãƒâ€” fmax c) Fs = 2 Ãƒâ€” fmax d) None 25. SNR stands for: a) Signal -to-Noise Ratio Ã¢Å“â€¦ b) Signal -to-Number c) Sound -to-Noise d) None 26. Power spectrum represents: a) Distribution of power over frequency Ã¢Å“â€¦ b) Time c) Amplitude d) None 27. Baseband signal is: a) Original signal Ã¢Å“â€¦ b) Modulated signal c) Carrier d) None 28. Bandpass signal is: a) Centered around carrier Ã¢Å“â€¦ b) Original signal c) Noise d) None 29. AM modulated signal has: a) Carrier + sidebands Ã¢Å“â€¦ b) Carrier only c) Sidebands only d) None 30.

FM bandwidth depends on: a) Frequency deviation Ã¢Å“â€¦ b) Amplitude c) Phase d) None 31. PM bandwidth depends on: a) Phase deviation Ã¢Å“â€¦ b) Frequency c) Amplitude d) None 32. Coherent detection used for: a) AM demodulation Ã¢Å“â€¦ b) FM c) PM d) None 33. Envelope detection used for: a) AM Ã¢Å“â€¦ b) FM c) PM d) None 34. Multiplexing purpose: a) Efficient utiliz ation Ã¢Å“â€¦ b) Amplification c) Modulation d) None 35. Information rate formula: a) R = H Ãƒâ€” symbols/sec Ã¢Å“â€¦ b) R = H Ãƒâ€” f c) R = P Ãƒâ€” t d) None 36. Signal bandwidth affects: a) Data rate Ã¢Å“â€¦ b) Power c) Voltage d) None 37. Noise degrades: a) SNR Ã¢Å“â€¦ b) Bandwidth c) Time d) None 38. Shannon capacity formula: a) C = B log2(1 + S/N) Ã¢Å“â€¦ b) C = B Ãƒâ€” S/N c) C = B / S/N d) None 39. Analog vs digital communication: a) Analog continuous Ã¢Å“â€¦ b) Digital discrete Ã¢Å“â€¦ c) Both correct Ã¢Å“â€¦ d) None 40. Multiplexing reduces: a) Number of channels Ã¢Å“â€¦ b) Bandwidth c) Noise d) None 41. Demultiplexer separates: a) Combined signals Ã¢Å“â€¦ b) Carrier c) Modulation d) None 42. Fourier series uses: a) Sin & cos Ã¢Å“â€¦ b) Exponential only c) Step function d) None 43. Power spectrum integral = a) Signal energy Ã¢Å“â€¦ b) Noise c) Bandwidth d) None 44. Pulse duration affects: a) Bandwidth Ã¢Å“â€¦ b) Power c) Noise d) None 45. PCM uses: a) Sampling Ã¢Å“â€¦ b) Quantization Ã¢Å“â€¦ c) Encoding Ã¢Å“â€¦ d) All Ã¢Å“â€¦ 46. Delta modulation advantage: a) Simple Ã¢Å“â€¦ b) Requires low bandwidth Ã¢Å“â€¦ c) Adaptive possible Ã¢Å“â€¦ d) All Ã¢Å“â€¦ 47. CDMA allows: a) Multiple use rs Ã¢Å“â€¦ b) Single user c) Only one channel d) None 48. Nyquist rate = a) 2 Ãƒâ€” fmax Ã¢Å“â€¦ b) fmax c) fmax / 2 d) None 49. Pulse shaping reduces: a) Inter -symbol interference Ã¢Å“â€¦ b) Noise c) Bandwidth d) None 50. Communication system goal: a) Reliable data transfer Ã¢Å“â€¦ b) Maximum n oise c) Minimum bandwidth d) None Computer Networking & Security (~60 MCQ) 1. Protocol hierarchy defines: a) Layered communication Ã¢Å“â€¦ b) Hardware only c) Software only d) None 2. Data link layer provides: a) Reliable link Ã¢Å“â€¦ b) Routing c) Application d) Transport 3. HLDC stands for: a) High -Level Data Link Control Ã¢Å“â€¦ b) High -Level Device Control c) Hardware Link Device Control d) None 4. LAN protocols include: a) IEEE 802.3 Ã¢Å“â€¦ b) IEEE 802.11 Ã¢Å“â€¦ c) Both Ã¢Å“â€¦ d) None 5. Hub operates at: a) Physical layer Ã¢Å“â€¦ b) Data link c) Network d) Transport 6. Switch operates at: a) Physical b) Data link Ã¢Å“â€¦ c) Network d) Transport 7. Bridge connects: a) Two LANs Ã¢Å“â€¦ b) Two computers c) Router d) None 8. FDDI uses: a) Fiber optic Ã¢Å“â€¦ b) Copper c) Wireless d) None 9. Fast Ethernet speed: a) 10 Mbps b) 100 Mbps Ã¢Å“â€¦ c) 1 Gbps d) 10 Gbps 10. Routing algorithm decides: a) Path selection Ã¢Å“â€¦ b) Bandwidth c) Speed d) None 11. Congestion control prevents: a) Network overload Ã¢Å“â€¦ b) Data loss c) Security d) None 12. Internetworking involves: a) Connecting LANs/WANs Ã¢Å“â€¦ b) Hardware onl y c) Software only d) None 13. Fragmentation occurs when: a) Packet > MTU Ã¢Å“â€¦ b) Packet < MTU c) Router fails d) None 14. Firewall purpose: a) Network security Ã¢Å“â€¦ b) Routing c) Switching d) None 15. IPV4 address length: a) 32 bits Ã¢Å“â€¦ b) 64 bits c) 128 bits d) 16 bits 16. IPV6 address length: a) 32 bits b) 64 bits c) 128 bits Ã¢Å“â€¦ d) 16 bits 17. ARP resolves: a) IP Ã¢â€ â€™ MAC Ã¢Å“â€¦ b) MAC

Ã¢â€ â€™ IP c) Port Ã¢â€ â€™ IP d) None 18. RARP resolves: a) MAC Ã¢â€ â€™ IP Ã¢Å“â€¦ b) IP Ã¢â€ â€™ MAC c) Port Ã¢â€ â€™ IP d) None 19. Mobile IP enables: a) Device mobility Ã¢Å“â€¦ b) Routing c) Switching d) None 20. Transport protocol for reliable communication: a) TCP Ã¢Å“â€¦ b) UDP c) ICMP d) None 21. TCP provides: a) Connection -oriented Ã¢Å“â€¦ b) Error checking Ã¢Å“â€¦ c) Flow control Ã¢Å“â€¦ d) All Ã¢Å“â€¦ 22. UDP provides: a) Connectionless Ã¢Å“â€¦ b) No guarantee Ã¢Å“â€¦ c) Both Ã¢Å“â€¦ d) None 23. AAL of ATM: a) Adaptation layer Ã¢Å“â€¦ b) Application layer c) Transport layer d) None 24. Network security includes: a) Cryptography Ã¢Å“â€¦ b) Authentication Ã¢Å“â€¦ c) Digital signatures Ã¢Å“â€¦ d) All Ã¢Å“â€¦ 25. DES stands for: a) Data Encryption Standard Ã¢Å“â€¦ b) Digital Encryption Standard c) Data Encoding System d) None 26. IDEA stands for: a) International Data Encryption Algorithm Ã¢Å“â€¦ b) Data Encryption Algorithm c) Information Encoding d) None 27. Public key algorithm uses: a) Two keys Ã¢Å“â€¦ b) One key c) Both d) None 28. Authentication ensures: a) Identity verification Ã¢Å“â€¦ b) Data transfer c) Speed d) None 29. Digital signature ensures: a) Authentication Ã¢Å“â€¦ b) Integrity Ã¢Å“â€¦ c) Both Ã¢Å“â€¦ d) None 30. Gigabit Ethernet speed: a) 100 Mbps b) 1 Gbps Ã¢Å“â€¦ c) 10 Gbps d) None 31. DNS resolves: a) Domain Ã¢â€ â€™ IP Ã¢Å“â€¦ b) IP Ã¢â€ â€™ Domain c) MAC Ã¢â€ â€™ IP d) None 32. Name servers store: a) Domain name info Ã¢Å“â€¦ b) IP only c) MAC only d) None 33. Email privacy is ensured by: a) Encryption Ã¢Å“â€¦ b) Routing c) Firewall d) None 34. SNMP stands for: a) Simple Network Management Protocol Ã¢Å“â€¦ b) Secure Network c) Standard Ne twork d) None 35. HTTP operates at: a) Application layer Ã¢Å“â€¦ b) Transport c) Network d) Data link 36. HTTPS ensures: a) Secure HTTP Ã¢Å“â€¦ b) Fast HTTP c) Normal HTTP d) None 37. LAN uses: a) Ethernet Ã¢Å“â€¦ b) FDDI Ã¢Å“â€¦ c) Both Ã¢Å“â€¦ d) None 38. WAN connects: a) Large area networks Ã¢Å“â€¦ b) Si ngle computer c) Router only d) None 39. Fragmentation handled by: a) Network layer Ã¢Å“â€¦ b) Transport c) Data link d) None 40. IPV4 provides: a) 4 billion addresses Ã¢Å“â€¦ b) 1 billion c) 128 bit d) None 41. IPV6 provides: a) 128 -bit address Ã¢Å“â€¦ b) 32 -bit c) 64 -bit d) None 42. TCP uses: a) Three -way handshake Ã¢Å“â€¦ b) UDP c) ICMP d) None 43. UDP uses: a) No handshake Ã¢Å“â€¦ b) Handshake c) Connection -oriented d) None 44. Firewalls can be: a) Packet filtering Ã¢Å“â€¦ b) Proxy Ã¢Å“â€¦ c) Both Ã¢Å“â€¦ d) None 45. Cryptography converts: a) Plaintext Ã¢â€ â€™ Ciphertext Ã¢Å“â€¦ b) Ciphert ext Ã¢â€ â€™ Plaintext c) Data only d) None 46. VPN ensures: a) Secure private network Ã¢Å“â€¦ b) Open network c) LAN only d) None 47. Transport layer manages: a) End -to-end communication Ã¢Å“â€¦ b) Node -to-node c) Data link d) Physical 48. ARP used in: a) Local network Ã¢Å“â€¦ b) Internet c) WAN d) None 49. RARP used to: a) Assign IP from MAC Ã¢Å“â€¦ b) Assign MAC c) DNS d) None 50. ICMP used for: a) Error reporting Ã¢Å“â€¦ b) Data transfer c) Encryption d) None 51. SMTP used for: a) Sending emails Ã¢Å“â€¦ b) Receiving emails c) Browsing d) None 52. POP3 used for: a) Receiving emails Ã¢Å“â€¦ b) Sending emails c) Browsing d) None 53. IMAP used for: a) Receiving emails Ã¢Å“â€¦ b) Sending c) Browsing d) None 54. VPN tunnel provides: a) Encrypted path Ã¢Å“â€¦ b) Open path c) Wireless path d) None 55. Network congestion occurs due to: a) Excessive tr affic Ã¢Å“â€¦ b) Low traffic c) Short cable d) None 56. Routing algorithms include: a) Distance vector Ã¢Å“â€¦ b) Link state Ã¢Å“â€¦ c) Both Ã¢Å“â€¦ d) None 57. MAC address is: a) Hardware address Ã¢Å“â€¦ b) IP address c) Domain name d) None 58. IPv4 address written in: a) Dot -decimal Ã¢Å“â€¦ b) Hex c) Binary only d) None 59. IPv6 address written in: a) Hexadecimal Ã¢Å“â€¦ b) Decimal c) Binary d) None 60. Network layer provides: a) Logical addressing Ã¢Å“â€¦ b) Physical addressing c) Transport d) Application