{'0': 'Basic Physics (~70 MCQ)\n1. Coulomb’s law defines the force between:\na) Two moving charges\nb) Two point charges at rest ✅\nc) A charge and a magnetic field\nd) A current -carrying wire and a charge\n2. The SI unit of electric flux is:\na) Volt\nb) Coulomb\nc) Newton·meter²/Coulomb ✅\nd) Tesla\n3. Gauss’s law is applicable to:\na) Only point charges\nb) Any closed surface ✅\nc) Open surfaces\nd) Conductors only\n4. Electric potential at a point is:\na) Energy per unit charge ✅\nb) Force per unit charge\nc) Charge per unit en ergy\nd) None of these\n5. Faraday’s law relates:\na) Electric field and charge\nb) Induced EMF and rate of change of magnetic flux ✅\nc) Current and resistance\nd) Voltage and capacitance\n6. Maxwell’s equations describe:\na) Motion of electrons\nb) Electromagnetic fiel ds ✅\nc) Quantum particles\nd) Wave propagation in air only\n7. The speed of light in vacuum is:\na) 3×10³ m/s\nb) 3×10⁵ m/s\nc) 3×10⁸ m/s ✅\nd) 3×10¹⁰ m/s\n8. Photoelectric effect demonstrates that light:\na) Travels in waves\nb) Has particle nature ✅\nc) Is longitudinal\nd) Has no energy\n9. Compton effect proves:'}

{'0': 'a) Wave nature of light\nb) Particle nature of light ✅\nc) Magnetic field effect\nd) Electric field effect\n10. De Broglie wavelength is associated with:\na) Photons\nb) Electrons and matter particles ✅\nc) Only protons\nd) Only neutrons\n11. Phase velocity is:\na) Velocity of energy transfer\nb) Velocity of wave crests ✅\nc) Same as group velocity\nd) None of these\n12. Group velocity is:\na) Speed of individual wave\nb) Speed of envelope of wave packet ✅\nc) Always greater than phase velocity\nd) Zero\n13. Quantum theory of light was proposed by:\na) Newton\nb) Einstein ✅\nc) Maxwell\nd) Planck\n14. X-ray diffraction is used to study:\na) Atomic structure ✅\nb) Magnetic field\nc) Electric circuits\nd) Sound waves\n15. Wave function in quantum mechanics represents:\na) Probability amplitude ✅\nb) Energy only\nc) Force\nd) Velocity\n16. The integral of electric field over a closed surface equals:\na) Zero\nb) Charge enclosed/ε₀ ✅\nc) Current enclosed\nd) Voltage\n17. Magnetic field is produced by:\na) Static charges\nb) Moving charges ✅'}

{'0': 'c) Stationary neutral objects\nd) Heat only\n18. Faraday’s law is a consequence of:\na) Conservation of energy ✅\nb) Ohm’s law\nc) Coulomb’s law\nd) Kirchoff’s law\n19. Unit of magnetic flux is:\na) Tesla\nb) Weber ✅\nc) Ampere\nd) Henry\n20. Lorentz force acts on:\na) Stationary char ge\nb) Moving charge in magnetic field ✅\nc) Neutral particles\nd) Light only\n21. Capacitance is defined as:\na) Q/V ✅\nb) V/Q\nc) I/R\nd) P/V\n22. Energy stored in a capacitor:\na) ½ CV² ✅\nb) CV²\nc) 2CV²\nd) C/V²\n23. Inductor opposes:\na) Voltage\nb) Current change ✅\nc) Resistan ce\nd) Power\n24. RLC circuit resonates when:\na) XL = XC ✅\nb) XL > XC\nc) XL < XC\nd) R = 0\n25. Electric field inside a conductor is:\na) Maximum\nb) Zero ✅\nc) Depends on charge\nd) Constant'}

{'0': '26. Magnetic flux density is measured in:\na) Tesla ✅\nb) Weber\nc) Henry\nd) Ampere\n27. Ampere’s law relates:\na) Current and magnetic field ✅\nb) Voltage and resistance\nc) Capacitance and charge\nd) Energy and power\n28. Biot-Savart law gives:\na) Force on a charge\nb) Magnetic field due to current element ✅\nc) Electric field\nd) Voltage\n29. Self-inductance unit is:\na) Henry ✅\nb) Farad\nc) Ohm\nd) Tesla\n30. Mutual inductance occurs between:\na) Two resistors\nb) Two coils ✅\nc) Capacitor and coil\nd) Wire and battery\n31. Maxwell added which term to Ampere’s law?\na) Displacement current ✅\nb) Conduction current\nc) Electric flux\nd) Magnetic flux\n32. Electromagnetic waves are:\na) Longitudinal\nb) Transverse ✅\nc) Stationary\nd) Random\n33. Energy of a photon:\na) hf ✅\nb) h/f\nc) h + f\nd) hf²\n34. Threshold frequency in photoelectric effect depends on:\na) Intensity'}

{'0': 'b) Metal type ✅\nc) Distance from source\nd) Angle of incidence\n35. Quantum number n indicates:\na) Angular momentum\nb) Principal energy level ✅\nc) Magnetic orientation\nd) Spin\n36. Planck constant h has units:\na) Joule·second ✅\nb) Volt\nc) Coulomb\nd) Ampere·second\n37. Compton wavelength for mula is:\na) λc = h/mc ✅\nb) λc = mc/h\nc) λc = h²/m\nd) λc = h/m\n38. X-ray wavelength is in the range:\na) 0.01 –10 nm ✅\nb) 1–100 μm\nc) 100 –1000 nm\nd) 10 –100 cm\n39. Electromagnetic spectrum order (low to high frequency):\na) Radio, Microwave, IR, Visible, UV, X -ray, Gam ma ✅\nb) X-ray, UV, Visible, IR, Microwave, Radio\nc) Gamma, X -ray, UV, Visible, IR, Microwave, Radio\nd) Radio, IR, Microwave, Visible, UV, X -ray, Gamma\n40. Photoelectric current depends on:\na) Light frequency\nb) Light intensity ✅\nc) Metal temperature\nd) None\n41. Heisenberg uncertainty principle relates:\na) Energy and time ✅\nb) Position and momentum ✅\nc) Force and mass\nd) Both a & b ✅\n42. Wave equation describes:\na) Electric field only\nb) Magnetic field only\nc) Propagation of waves ✅'}

{'0': 'd) Particle motion\n43. EM wave in vacuum travels at:\na) 3×10⁸ m/s ✅\nb) 3×10⁵ m/s\nc) 3×10³ m/s\nd) 3×10¹⁰ m/s\n44. Polarization of light involves:\na) Frequency change\nb) Direction change of E vector ✅\nc) Amplitude only\nd) Wavelength only\n45. Brewster’s angle gives:\na) Total reflection\nb) Zero reflection for one polarization ✅\nc) Maximum reflection\nd) None\n46. Critical angle is related to:\na) Refraction ✅\nb) Diffraction\nc) Polarization\nd) Interference\n47. Phase difference of 180° gives:\na) Constructive interference\nb) Destructive interference ✅\nc) No interference\nd) Random waves\n48. Energy of X -ray photon is:\na) E = hf ✅\nb) E = h/f\nc) E = hf²\nd) E = f/h\n49. Quantum tunneling explains:\na) Classical reflection\nb) Particle crossing potential barrier ✅\nc) Wave interference\nd) Magnetic effect\n50. Electron diffraction proves:\na) Partic le nature\nb) Wave nature ✅\nc) EM wave\nd) Photoelectric effect\n51. Wavefunction normalization ensures:'}

{'0': 'a) Energy conservation\nb) Total probability = 1 ✅\nc) Momentum conservation\nd) Mass conservation\n52. Schrödinger equation is:\na) Time -independent ✅\nb) Time -dependent ✅\nc) Both\nd) None\n53. Potential energy in quantum well is:\na) Infinite\nb) Zero\nc) Finite ✅\nd) Negative\n54. Electron in hydrogen atom has:\na) Continuous energy\nb) Quantized energy ✅\nc) Zero energy\nd) Infinite energy\n55. First Boh r orbit radius:\na) 0.529 Å\nb) 0.529 nm ✅\nc) 5.29 nm\nd) 5.29 cm\n56. Photon momentum is:\na) p = mv\nb) p = hf/c ✅\nc) p = h/f\nd) p = mc\n57. Heisenberg principle formula:\na) ΔxΔp ≥ ħ/2 ✅\nb) ΔxΔp ≤ ħ/2\nc) ΔEΔt ≤ ħ\nd) ΔEΔt ≥ ħ\n58. Group velocity < Phase velocity in:\na) Norma l dispersion\nb) Anomalous dispersion ✅\nc) Vacuum\nd) Free space\n59. Standing wave forms due to:\na) Single wave\nb) Superposition ✅'}

{'0': 'c) Refraction\nd) Diffraction\n60. Node is point of:\na) Maximum amplitude\nb) Zero amplitude ✅\nc) Half amplitude\nd) Random amplitude\n61. Antin ode is point of:\na) Maximum amplitude ✅\nb) Zero amplitude\nc) Half amplitude\nd) Random amplitude\n62. EM wave energy density:\na) u = ε₀E²/2 ✅\nb) u = μ₀H²\nc) u = EH\nd) u = 0\n63. Maxwell predicts:\na) EM waves travel at speed of light ✅\nb) EM waves are longitudinal\nc) EM waves have mass\nd) EM waves stationary\n64. Quantum of light is:\na) Electron\nb) Photon ✅\nc) Neutron\nd) Proton\n65. Wavelength of electron decreases with:\na) Increasing momentum ✅\nb) Decreasing momentum\nc) Constant\nd) None\n66. Principle of superposition applies to:\na) Linear systems ✅\nb) Nonlinear systems\nc) Magnetic fields only\nd) Electric fields only\n67. Electric field inside a hollow conductor:\na) Zero ✅\nb) Non -zero\nc) Depends on shape\nd) Depends on charge'}

{'0': '68. Magnetic permeability of free space:\na) 4π×10⁻⁷ H/m ✅\nb) 8.85×10 ⁻¹² F/m\nc) 1 H/m\nd) 0\n69. Magnetic flux Φ = B·A cosθ, θ is:\na) Angle between B and area normal ✅\nb) Angle between B and surface\nc) Always 0\nd) Always 90°\n70. RLC series circuit resonant frequency:\na) f = 1/(2π√LC) ✅\nb) f = 2π√LC\nc) f = √LC\nd) f = 1/(LC)\nIntroducti on to Computer Systems (~60 MCQ)\n1. The binary number system uses how many digits?\na) 2 ✅\nb) 8\nc) 10\nd) 16\n2. The octal number system uses how many digits?\na) 2\nb) 8 ✅\nc) 10\nd) 16\n3. The hexadecimal number system uses how many digits?\na) 8\nb) 10\nc) 16 ✅\nd) 2\n4. Which of the following is NOT an input device?\na) Keyboard\nb) Mouse\nc) Printer ✅\nd) Scanner\n5. CPU stands for:\na) Central Processing Unit ✅\nb) Central Peripheral Unit\nc) Control Processing Unit\nd) Computer Processing Unit\n6. The main function of the CPU is:'}

{'0': 'a) Storage of data\nb) Processing of data ✅\nc) Communication\nd) Display\n7. RAM is:\na) Volatile memory ✅\nb) Non -volatile memory\nc) Secondary storage\nd) Input device\n8. ROM is:\na) Volatile memory\nb) Non -volatile memory ✅\nc) Cache memory\nd) Input device\n9. Which of the following is secondary storage?\na) RAM\nb) Hard Disk ✅\nc) Cache\nd) Register\n10. Which of the following is an example of application software?\na) Windows OS\nb) Microsoft Word ✅\nc) BIOS\nd) Device driver\n11. Operating system manages:\na) Hardware resources ✅\nb) Only so ftware\nc) Only memory\nd) Only CPU\n12. Assembly language uses:\na) Binary code\nb) Mnemonics ✅\nc) High -level commands\nd) Natural language\n13. Early computers used which number system?\na) Binary\nb) Decimal ✅\nc) Octal\nd) Hexadecimal\n14. First generation computers used:\na) Vacuum tubes ✅\nb) Transistors'}

{'0': 'c) ICs\nd) Microprocessors\n15. Second generation computers used:\na) Vacuum tubes\nb) Transistors ✅\nc) ICs\nd) Microprocessors\n16. Third generation computers used:\na) Vacuum tubes\nb) Transistors\nc) ICs ✅\nd) Microprocessors\n17. Fourth generati on computers used:\na) Vacuum tubes\nb) Transistors\nc) ICs\nd) Microprocessors ✅\n18. Which is NOT a main component of a computer?\na) CPU\nb) Memory\nc) Printer ✅\nd) I/O devices\n19. The ALU performs:\na) Arithmetic and logical operations ✅\nb) Only arithmetic\nc) Only logi c\nd) Data storage\n20. The CU (Control Unit) manages:\na) Arithmetic operations\nb) Instruction execution ✅\nc) Data storage\nd) Input/output\n21. BIOS is stored in:\na) RAM\nb) ROM ✅\nc) Cache\nd) Register\n22. Number of bits in a byte:\na) 4\nb) 8 ✅\nc) 16\nd) 32'}

{'0': '23. 1 KB = ?\na) 1024 Bytes ✅\nb) 1000 Bytes\nc) 512 Bytes\nd) 2048 Bytes\n24. Internet is an example of:\na) LAN\nb) MAN\nc) WAN ✅\nd) PAN\n25. Which is a type of software?\na) Operating system ✅\nb) Compiler ✅\nc) Word processor ✅\nd) All of the above ✅\n26. Binary addition: 101 + 110 = ?\na) 1001 ✅\nb) 111\nc) 1010\nd) 1100\n27. Decimal 15 in binary is:\na) 1010\nb) 1111 ✅\nc) 1101\nd) 1001\n28. Decimal 255 in hexadecimal is:\na) 0xFF ✅\nb) 0xAA\nc) 0xF0\nd) 0xFE\n29. The fastest memory in computer is:\na) RAM\nb) Cache ✅\nc) ROM\nd) Hard Disk\n30. Number of general -purpose registers in 8086:\na) 4\nb) 8 ✅\nc) 16\nd) 2\n31. What is the base of the hexadecimal system?\na) 2'}

{'0': 'b) 8\nc) 10\nd) 16 ✅\n32. A nibble consists of:\na) 2 bits\nb) 4 bits ✅\nc) 8 bits\nd) 16 bits\n33. CPU clock speed is measured in:\na) Hertz ✅\nb) Volt\nc) Ampere\nd) Joule\n34. Program that translates high-level language to machine code:\na) Compiler ✅\nb) Assembler\nc) Interpreter\nd) Loader\n35. Which memory is used to store BIOS?\na) ROM ✅\nb) RAM\nc) Cache\nd) Register\n36. The main memory is:\na) RAM ✅\nb) ROM\nc) Hard Disk\nd) Cache\n37. Cache memory is located:\na) Between CPU and main memory ✅\nb) On hard disk\nc) In I/O device\nd) In printer\n38. The smallest unit of data in a computer:\na) Byte\nb) Bit ✅\nc) Nibble\nd) Word\n39. ASCII is used for:\na) Images\nb) Text ✅\nc) Audio'}

{'0': 'd) Video\n40. Unicode supports:\na) English only\nb) Multip le languages ✅\nc) Binary\nd) Hexadecimal\n41. Operating system is:\na) System software ✅\nb) Application software\nc) Firmware\nd) Hardware\n42. Instruction cycle consists of:\na) Fetch ✅\nb) Decode ✅\nc) Execute ✅\nd) All of the above ✅\n43. Which of the following is NOT a high-level language?\na) C\nb) Python\nc) Assembly ✅\nd) Java\n44. HDD stores data in:\na) RAM\nb) Magnetic disks ✅\nc) SSD\nd) Cache\n45. SSD is faster than HDD because:\na) Uses flash memory ✅\nb) Uses magnetic disks\nc) Less durable\nd) Has moving parts\n46. Input devices convert :\na) Digital → Analog\nb) Human data → Digital ✅\nc) Digital → Human readable\nd) None\n47. Output devices convert:\na) Digital → Analog\nb) Digital → Human readable ✅\nc) Analog → Digital\nd) None\n48. Primary memory is:'}

{'0': 'a) Volatile ✅\nb) Non -volatile\nc) Permanent\nd) Secon dary\n49. Secondary memory is:\na) Volatile\nb) Non -volatile ✅\nc) Faster than RAM\nd) Registers\n50. Software that helps run other programs:\na) Operating system ✅\nb) Application\nc) Utility\nd) Driver\n51. Early computer “ENIAC” used:\na) Transistors\nb) Vacuum tubes ✅\nc) ICs\nd) Microprocessors\n52. Which is NOT a characteristic of computer?\na) Speed\nb) Accuracy\nc) Emotions ✅\nd) Storage\n53. Binary subtraction: 1010 - 0110 = ?\na) 0100 ✅\nb) 1001\nc) 0011\nd) 1110\n54. ASCII stands for:\na) American Standard Code for Information Interchange ✅\nb) Au tomatic System Code for Input\nc) Analog Standard Code for Information\nd) All of the above\n55. Word length in 8086 microprocessor:\na) 8-bit\nb) 16 -bit ✅\nc) 32 -bit\nd) 64 -bit\n56. Early computers were used mainly for:\na) Gaming\nb) Calculations ✅'}

{'0': 'c) Internet browsing\nd) Social media\n57. Input to CPU is through:\na) Registers ✅\nb) ALU\nc) CU\nd) Memory\n58. Output from CPU is via:\na) Registers\nb) Memory\nc) I/O devices ✅\nd) ALU\n59. Instruction set architecture defines:\na) Hardware\nb) Software\nc) CPU instructions ✅\nd) Memory only\n60. Which dev ice connects a computer to the internet?\na) Router ✅\nb) Printer\nc) Keyboard\nd) Monitor\nElectrical Circuits (~60 MCQ)\n1. Ohm’s law states:\na) V = IR ✅\nb) P = IV²\nc) I = V/P\nd) V = I²R\n2. In a series circuit, the current is:\na) Same in all elements ✅\nb) Different in each element\nc) Zero\nd) Depends on voltage only\n3. In a parallel circuit, the voltage across each branch is:\na) Same ✅\nb) Different\nc) Zero\nd) Depends on resistance\n4. Kirchhoff’s Current Law (KCL) is based on:\na) Energy conservation\nb) Charge conservation ✅\nc) Ohm’s law'}

{'0': 'd) Faraday’s law\n5. Kirchhoff’s Voltage Law (KVL) is based on:\na) Energy conservation ✅\nb) Charge conservation\nc) Power conservation\nd) Resistance law\n6. Power in a resistive circuit:\na) P = VI ✅\nb) P = V²/R ✅\nc) P = I²R ✅\nd) All of the above ✅\n7. Voltage divider formula:\na) Vx = V(Rx/Rtotal) ✅\nb) Vx = IR\nc) Vx = V/R\nd) Vx = IR²\n8. Current divider formula applies to:\na) Series circuit\nb) Parallel circuit ✅\nc) Both\nd) None\n9. Thevenin’s theorem simplifies a circuit to:\na) Voltage source and series resistor ✅\nb) Current source and series resistor\nc) Voltage source and parallel resistor\nd) Current source and parallel resistor\n10. Norton’s theorem simplifies a circuit to:\na) Current source and parallel resistor ✅\nb) Voltage sourc e and series resistor\nc) Current source and series resistor\nd) Voltage source and parallel resistor\n11. Maximum power transfer occurs when:\na) Load R = Source R ✅\nb) Load R > Source R\nc) Load R < Source R\nd) Load R = 0\n12. Superposition theorem is applicable for:\na) Linear circuits ✅\nb) Non -linear circuits\nc) Series circuits only\nd) Parallel circuits only\n13. Resistance unit is:'}

{'0': 'a) Ohm ✅\nb) Volt\nc) Ampere\nd) Watt\n14. Voltage unit is:\na) Ohm\nb) Volt ✅\nc) Ampere\nd) Watt\n15. Current unit is:\na) Ohm\nb) Volt\nc) Ampere ✅\nd) Watt\n16. Capacitance unit is:\na) Farad ✅\nb) Henry\nc) Ohm\nd) Tesla\n17. Inductance unit is:\na) Henry ✅\nb) Farad\nc) Ohm\nd) Tesla\n18. Capacitors in series:\na) 1/Ceq = Σ(1/Ci) ✅\nb) Ceq = ΣCi\nc) Ceq = ΣC²\nd) Ceq = 1/ΣC\n19. Capacitors in parallel:\na) Ceq = ΣCi ✅\nb) 1/Ceq = Σ(1/Ci)\nc) Ce q = √ΣCi\nd) Ceq = None\n20. Inductors in series:\na) Leq = ΣLi ✅\nb) 1/Leq = Σ(1/Li)\nc) Leq = √ΣLi\nd) None\n21. Inductors in parallel:\na) Leq = ΣLi\nb) 1/Leq = Σ(1/Li) ✅'}

{'0': 'c) Leq = √ΣLi\nd) None\n22. RLC series circuit resonance condition:\na) XL = XC ✅\nb) XL > XC\nc) XL < XC\nd) R = 0\n23. Reactance of inductor:\na) XL = 2πfL ✅\nb) XL = 1/2πfL\nc) XL = L/f\nd) XL = 1/L\n24. Reactance of capacitor:\na) XC = 1/2πfC ✅\nb) XC = 2πfC\nc) XC = 1/C\nd) XC = 2C\n25. Impedance of series RLC:\na) Z = √(R² + (XL -XC)²) ✅\nb) Z = R + XL + XC\nc) Z = R/(XL -XC)\nd) Z = R² + L² + C²\n26. Power factor = cosθ, θ is:\na) Phase difference between voltage and current ✅\nb) Voltage\nc) Current\nd) Resistance\n27. Energy stored in inductor:\na) W = ½ LI² ✅\nb) W = ½ CV²\nc) W = I²R\nd) W = VI\n28. Energy stored in capacitor:\na) W = ½ CV² ✅\nb) W = ½ L I²\nc) W = VI\nd) W = I²R\n29. Node voltage method is used for:\na) Parallel analysis ✅\nb) Series analysis\nc) Superposition\nd) None'}

{'0': '30. Mesh current method is used for:\na) Series analysis\nb) Loop analysis ✅\nc) Node analysis\nd) Both\n31. Source transformation converts:\na) Voltage source + series R → Current source + parallel R ✅\nb) Current source + parallel R → Voltage source + series R ✅\nc) Both a & b ✅\nd) None\n32. Dependent source is:\na) Independent voltage\nb) Controlled by another circuit variable ✅\nc) Uncontrol led\nd) Always current source\n33. Capacitor blocks:\na) DC ✅\nb) AC\nc) Both\nd) None\n34. Inductor blocks:\na) AC ✅\nb) DC\nc) Both\nd) None\n35. Time constant of RC circuit:\na) τ = RC ✅\nb) τ = L/R\nc) τ = R/L\nd) τ = 1/RC\n36. Time constant of RL circuit:\na) τ = RC\nb) τ = L/R ✅\nc) τ = R/L\nd) τ = 1/L\n37. For AC series RLC, resonance frequency:\na) f = 1/2π√LC ✅\nb) f = √LC\nc) f = 2π√LC\nd) f = LC\n38. In resonance, current is:\na) Minimum'}

{'0': 'b) Maximum ✅\nc) Zero\nd) Constant\n39. Voltage across L or C at resonance:\na) Less than supply\nb) Equal to supply\nc) Can be greater than supply ✅\nd) Zero\n40. RMS value of sinusoidal current:\na) Imax\nb) Imax/√2 ✅\nc) Imax/2\nd) √2 Imax\n41. RMS value of sinusoidal voltage:\na) Vmax\nb) Vmax/√2 ✅\nc) Vmax/2\nd) √2 Vmax\n42. Average power in AC circuit:\na) Vrms × Irms × cosθ ✅\nb) Vrms × Irms × sinθ\nc) Vrms × Irms\nd) Irms² × R\n43. Impedance in series AC circuit:\na) Z = R + j(XL - XC) ✅\nb) Z = R + XL + XC\nc) Z = R + 1/(XL - XC)\nd) Z = R² + (XL -XC)²\n44. Admittance Y =\na) 1/Z ✅\nb) Z\nc) R/Z\nd) Z/R\n45. Phase angle φ =\na) tan⁻¹((XL -XC)/R) ✅\nb) tan⁻¹(R/(XL -XC))\nc) cos⁻¹((XL -XC)/R)\nd) sin⁻¹((XL -XC)/R)\n46. Wye to Delta conversion is used for:\na) Resistors ✅\nb) Capacitors ✅\nc) Inductors ✅'}

{'0': 'd) All ✅\n47. Delta to Wye conversion is used for:\na) Resistors ✅\nb) Capacitors ✅\nc) Inductors ✅\nd) All ✅\n48. RMS voltage of triangular waveform :\na) Vm/√2\nb) Vm/√3 ✅\nc) Vm/2\nd) Vm\n49. In AC circuits, instantaneous power:\na) p = vi ✅\nb) p = i²R\nc) p = v²/R\nd) p = Vavg × Iavg\n50. Current leads voltage in:\na) Capacitive circuit ✅\nb) Inductive circuit\nc) Resistive circuit\nd) None\n51. Current lags voltage in:\na) Capacitive\nb) Inductive ✅\nc) Resistive\nd) None\n52. Power dissipated in resistor:\na) I²R ✅\nb) V²/R ✅\nc) VI ✅\nd) All of the above ✅\n53. Series LC circuit at resonance:\na) Impedance minimum ✅\nb) Impedance maximum\nc) Current minimum\nd) Voltage minimum\n54. Parallel LC circu it at resonance:\na) Impedance minimum\nb) Impedance maximum ✅\nc) Current maximum\nd) Voltage zero'}

{'0': '55. Quality factor Q =\na) XL/R ✅\nb) XC/R\nc) R/XL\nd) R/XC\n56. Transient response occurs in:\na) DC circuits with L or C ✅\nb) Pure resistive DC circuits\nc) AC steady -state\nd) None\n57. Charging capacitor current:\na) Maximum at t=0 ✅\nb) Zero at t=0\nc) Constant\nd) None\n58. Discharging capacitor current:\na) Maximum at t=0 ✅\nb) Zero at t=0\nc) Constant\nd) None\n59. DC steady -state inductor acts as:\na) Open circuit\nb) Short circuit ✅\nc) Capacitor\nd) Resistor\n60. DC steady -state capacitor acts as:\na) Open circuit ✅\nb) Short circuit\nc) Inductor\nd) Resistor\nDigital Logic Design (~70 MCQ)\n1. Boolean algebra was introduced by:\na) Newton\nb) Boole ✅\nc) Einstein\nd) Maxwell\n2. The AND gate output is 1 only when:\na) Both inputs are 0\nb) Both inputs are 1 ✅\nc) One input is 1\nd) Any input is 0\n3. The OR gate output is 0 only when:'}

{'0': 'a) Both inputs are 0 ✅\nb) Both inputs are 1\nc) One input is 1\nd) Any input is 1\n4. The NOT gate inverts:\na) 1→0, 0→1 ✅\nb) 1→1, 0→0\nc) 1→1, 0→1\nd) None\n5. De Morgan’s theorem states:\na) (A·B)’ = A’ + B’ ✅\nb) (A+B)’ = A + B\nc) (A+B)’ = A’B’ ✅\nd) Both a & c ✅\n6. NAND gate is called:\na) Universal gate ✅\nb) Basic gate\nc) Logic gate\nd) None\n7. NOR gate is called:\na) Universal gate ✅\nb) Basic gate\nc) Logic gate\nd) None\n8. XOR gate output is 1 when:\na) Inputs same\nb) Inputs different ✅\nc) Both inputs 0\nd) Both inputs 1\n9. XNOR gate output is 1 when:\na) Inputs same ✅\nb) Inputs different\nc) Both 0\nd) Both 1\n10. Sum-of-Products (SOP) is:\na) OR of AND terms ✅\nb) AND of OR terms\nc) XOR of AND terms\nd) NAND of OR terms\n11. Product -of-Sums (POS) is:\na) OR of AND terms\nb) AND of OR terms ✅'}

{'0': 'c) XOR of OR terms\nd) NOR of AND terms\n12. K-map is used for:\na) Minimization of Boolean expression ✅\nb) Maximization\nc) M ultiplexing\nd) Latching\n13. 2-to-1 multiplexer has:\na) 2 inputs, 1 select ✅\nb) 2 outputs, 1 input\nc) 1 input, 2 select\nd) 2 outputs, 2 select\n14. 4-to-1 multiplexer has:\na) 4 inputs, 2 select ✅\nb) 4 outputs, 2 select\nc) 2 inputs, 4 select\nd) 1 input, 4 select\n15. Demu ltiplexer converts:\na) 1 input → many outputs ✅\nb) Many inputs → 1 output\nc) OR operation\nd) AND operation\n16. Decoder converts:\na) n inputs → 2ⁿ outputs ✅\nb) 2ⁿ inputs → n outputs\nc) n outputs → n inputs\nd) None\n17. Encoder converts:\na) 2ⁿ inputs → n outputs ✅\nb) n inputs → 2ⁿ outputs\nc) OR → AND\nd) None\n18. Half adder produces:\na) Sum only\nb) Carry only\nc) Sum & Carry ✅\nd) Difference & Borrow\n19. Full adder has:\na) 2 inputs\nb) 3 inputs ✅\nc) 4 inputs\nd) 1 input'}

{'0': '20. Flip-flops store:\na) Voltage\nb) Bit of information ✅\nc) Curre nt\nd) Logic gate\n21. SR flip -flop is built using:\na) NAND/NOR gates ✅\nb) XOR\nc) XNOR\nd) AND\n22. JK flip -flop overcomes:\na) Race condition in SR ✅\nb) Memory loss\nc) Input error\nd) Timing error\n23. D flip -flop output =\na) Input D ✅\nb) Input Q\nc) Inverted D\nd) Sum\n24. T flip-flop toggles on:\na) T=1 ✅\nb) T=0\nc) Clock high\nd) Reset\n25. Asynchronous counter uses:\na) Same clock ✅\nb) Ripple effect\nc) Parallel clocking\nd) Both a & b ✅\n26. Synchronous counter:\na) All flip -flops clocked simultaneously ✅\nb) Ripple clocked\nc) Not clocked\nd) None\n27. Mealy machine output depends on:\na) Present state only\nb) Present input only\nc) Present state & input ✅\nd) Previous state\n28. Moore machine output depends on:\na) Present state only ✅'}

{'0': 'b) Present input\nc) Previous state\nd) Both state & input\n29. PLA stands fo r:\na) Programmable Logic Array ✅\nb) Parallel Logic Array\nc) Primary Logic Adder\nd) None\n30. PLA used for:\na) Logic function implementation ✅\nb) Storage\nc) Multiplexing\nd) None\n31. Race around problem occurs in:\na) SR flip -flop\nb) JK flip -flop ✅\nc) D flip -flop\nd) T flip-flop\n32. Pulse mode design avoids:\na) Multiple triggering ✅\nb) Single triggering\nc) Flip -flop operation\nd) Logic minimization\n33. Fundamental mode design uses:\na) Only one input change at a time ✅\nb) Multiple inputs\nc) Asynchronous\nd) None\n34. Combinational circ uit output depends on:\na) Present inputs only ✅\nb) Present & past inputs\nc) Clock\nd) State\n35. Sequential circuit output depends on:\na) Present inputs only\nb) Present & past inputs ✅\nc) Clock only\nd) None\n36. Boolean expression simplification reduces:\na) Gate coun t ✅\nb) Power consumption ✅\nc) Complexity ✅'}

{'0': 'd) All ✅\n37. XOR gate is equivalent to:\na) A’B + AB’ ✅\nb) AB + A’B’\nc) A + B\nd) A·B\n38. XNOR gate is equivalent to:\na) AB + A’B’ ✅\nb) A’B + AB’\nc) A + B\nd) A·B\n39. NAND gate expression:\na) (AB)’ ✅\nb) A + B\nc) AB\nd) (A + B)’\n40. NOR gate expression:\na) (A+B)’ ✅\nb) A + B\nc) AB\nd) (AB)’\n41. Number of minterms for n variables:\na) n\nb) 2ⁿ ✅\nc) n²\nd) 2n\n42. Number of maxterms for n variables:\na) n\nb) 2ⁿ ✅\nc) n²\nd) 2n\n43. Canonical SOP uses:\na) Minterms ✅\nb) Maxterms\nc) Sum\nd) Product\n44. Canonical POS uses:\na) Minterms\nb) Maxterms ✅\nc) Sum\nd) Product\n45. Logic minimization reduces:'}

{'0': 'a) Cost ✅\nb) Speed\nc) Complexity ✅\nd) Both a & c ✅\n46. Flip-flop stores:\na) 1 bit ✅\nb) 2 bits\nc) 4 bits\nd) Variable\n47. Latches are:\na) Level triggered ✅\nb) Edge triggered\nc) Pulse mode\nd) None\n48. Flip-flops are:\na) Level triggered\nb) Edge triggered ✅\nc) Pulse mode\nd) None\n49. Pulse -triggered flip -flops help avoid:\na) Race around ✅\nb) Memory loss\nc) Logic error\nd) Power consumption\n50. Asynchronous counter also called:\na) Ripple counter ✅\nb) Ri ng counter\nc) Synchronous counter\nd) Johnson counter\n51. Synchronous counter is:\na) Ripple type\nb) Clocked simultaneously ✅\nc) Level triggered\nd) None\n52. 4-bit asynchronous counter counts:\na) 0–7\nb) 0–15 ✅\nc) 0–31\nd) 0–63\n53. 3-bit synchronous counter max count:\na) 7 ✅\nb) 3'}

{'0': 'c) 8\nd) 15\n54. Edge triggering refers to:\na) Clock rising/falling ✅\nb) Clock high\nc) Clock low\nd) Pulse width\n55. JK flip -flop toggles when:\na) J=K=1 ✅\nb) J=1, K=0\nc) J=0, K=1\nd) J=K=0\n56. Clock frequency determines:\na) Circuit speed ✅\nb) Gate numbe r\nc) Power\nd) Output only\n57. Race around occurs when propagation delay < pulse width:\na) True ✅\nb) False\nc) Sometimes\nd) None\n58. Edge -triggered flip -flop avoids:\na) Multiple toggles ✅\nb) Memory\nc) Delay\nd) Logic error\n59. MUX selects:\na) One input ✅\nb) All inputs\nc) Output\nd) Gate\n60. DEMUX distributes:\na) Input to one output ✅\nb) Input to all outputs\nc) Gate\nd) None\n61. SOP minimization reduces:\na) AND gates\nb) OR gates\nc) Both ✅\nd) XOR'}

{'0': '62. POS minimization reduces:\na) OR gates\nb) AND gates\nc) Both ✅\nd) NAND\n63. Universal gate can implement:\na) All logic ✅\nb) None\nc) Only OR\nd) Only AND\n64. Flip-flop characteristic table lists:\na) Inputs & outputs ✅\nb) Inputs only\nc) Outputs only\nd) Clock only\n65. Level -triggered latch changes state:\na) Clock high ✅\nb) Clock low\nc) Both\nd) Edge\n66. Edge -trigger ed flip -flop changes state:\na) Rising/falling ✅\nb) Level high\nc) Level low\nd) None\n67. Pulse mode design avoids:\na) Multiple toggles ✅\nb) Race\nc) Timing errors ✅\nd) All ✅\n68. State diagram represents:\na) Sequential behavior ✅\nb) Combinational logic\nc) Input only\nd) Output only\n69. Mealy machine faster than Moore because:\na) Output depends on input ✅\nb) Output depends on state\nc) Uses fewer flip -flops\nd) None\n70. Fundamental mode design ensures:\na) Only one input changes at a time ✅'}

{'0': 'b) Multiple input changes\nc) Synchronous\nd) None\nBasic Electronics (~60 MCQ)\n1. Diode allows current to flow in:\na) Both directions\nb) One direction ✅\nc) No direction\nd) Depends on voltage\n2. Forward biased diode has:\na) High resistance\nb) Low resistance ✅\nc) Infinite resistance\nd) Zero resistance\n3. Reve rse biased diode has:\na) High resistance ✅\nb) Low resistance\nc) Zero resistance\nd) Low voltage\n4. Zener diode is used for:\na) Amplification\nb) Voltage regulation ✅\nc) Switching\nd) Oscillation\n5. Half-wave rectifier uses:\na) 1 diode ✅\nb) 2 diodes\nc) 4 diodes\nd) None\n6. Full-wave rectifier uses:\na) 1 diode\nb) 2 diodes ✅\nc) 4 diodes\nd) None\n7. Bridge rectifier uses:\na) 2 diodes\nb) 3 diodes\nc) 4 diodes ✅\nd) 1 diode\n8. Clipper circuit:\na) Clips voltage above/below reference ✅\nb) Amplifies signal'}

{'0': 'c) Rectifies signal\nd) Filters signal\n9. Clamper circuit:\na) Shifts signal DC level ✅\nb) Clips voltage\nc) Rectifies\nd) Amplifies\n10. Bipolar junction transistor (BJT) has:\na) 2 terminals\nb) 3 terminals ✅\nc) 4 terminals\nd) 5 terminals\n11. BJT modes:\na) Active ✅\nb) Cut -off ✅\nc) Saturation ✅\nd) All ✅\n12. Common emitter configuration provides:\na) Voltage gain ✅\nb) Current gain ✅\nc) Power gain ✅\nd) All ✅\n13. Common base configuration has:\na) Current gain <1 ✅\nb) Voltage gain high ✅\nc) Input low\nd) Output low\n14. Common collector configuratio n is also called:\na) Emitter follower ✅\nb) Base follower\nc) Collector follower\nd) None\n15. BJT used as switch operates in:\na) Active region\nb) Cut -off & saturation ✅\nc) Reverse bias\nd) None\n16. Load line represents:\na) Relationship between V & I ✅\nb) Current only\nc) Voltage only'}

{'0': 'd) None\n17. Stability factor determines:\na) BJT bias stability ✅\nb) Voltage\nc) Current\nd) Resistance\n18. Small signal model of BJT uses:\na) h-parameters ✅\nb) Z-parameters\nc) Y-parameters\nd) None\n19. Voltage gain of CE amplifier:\na) High ✅\nb) Low\nc) Zer o\nd) Negative\n20. Current gain of CE amplifier:\na) High ✅\nb) Low\nc) Zero\nd) Negative\n21. Input impedance of CB amplifier:\na) High\nb) Low ✅\nc) Medium\nd) Variable\n22. Output impedance of CE amplifier:\na) Low\nb) High ✅\nc) Medium\nd) Variable\n23. Field effect transistor (FET) has:\na) High input impedance ✅\nb) Low input impedance\nc) Medium\nd) Variable\n24. JFET gate is:\na) Forward biased\nb) Reverse biased ✅\nc) Floating\nd) None\n25. MOSFET can be:'}

{'0': 'a) Depletion type ✅\nb) Enhancement type ✅\nc) Both ✅\nd) None\n26. FET operates on:\na) Voltage contr ol ✅\nb) Current control\nc) Both\nd) None\n27. Diode’s knee voltage ~\na) 0.7V for silicon ✅\nb) 0.3V for silicon\nc) 0.7V for germanium\nd) 0.3V for germanium\n28. Zener voltage is:\na) Breakdown voltage ✅\nb) Forward voltage\nc) Knee voltage\nd) None\n29. Half-wave rectifier out put frequency =\na) Input frequency\nb) Same as input ✅\nc) Twice input\nd) Half input\n30. Full-wave rectifier output frequency =\na) Same as input\nb) Twice input ✅\nc) Half input\nd) None\n31. Capacitor filter removes:\na) AC ripples ✅\nb) DC\nc) Voltage\nd) Current\n32. Diode re verse recovery time:\na) Time to turn off ✅\nb) Time to turn on\nc) Forward voltage\nd) None\n33. Transistor as amplifier operates in:\na) Cut -off\nb) Active ✅'}

{'0': 'c) Saturation\nd) Reverse\n34. Transistor as switch operates in:\na) Active\nb) Cut -off & saturation ✅\nc) Reverse\nd) None\n35. BJT has:\na) Base, emitter, collector ✅\nb) Gate, source, drain\nc) Emitter, collector\nd) None\n36. FET has:\na) Base, collector, emitter\nb) Gate, source, drain ✅\nc) Input, output\nd) None\n37. MOSFET input impedance:\na) Low\nb) Very high ✅\nc) Medium\nd) Variable\n38. Clipper removes:\na) Part of waveform ✅\nb) Entire waveform\nc) DC\nd) AC\n39. Clamper shifts:\na) DC level ✅\nb) AC level\nc) Both\nd) None\n40. Forward biased diode resistance:\na) High\nb) Low ✅\nc) Infinite\nd) Zero\n41. Reverse biased diode leakage current:\na) High\nb) Low ✅\nc) Zero\nd) Medium'}

{'0': '42. Power dissipation in transistor:\na) VCE × IC ✅\nb) VBE × IB\nc) IC × IB\nd) None\n43. CE amplifier phase shift:\na) 0°\nb) 180° ✅\nc) 90°\nd) None\n44. CB amplifier phase shift:\na) 0° ✅\nb) 180°\nc) 90°\nd) None\n45. CC amplifier phase shift:\na) 0° ✅\nb) 180 °\nc) 90°\nd) None\n46. Small signal model helps determine:\na) Gain ✅\nb) Impedance ✅\nc) Both ✅\nd) None\n47. Junction diode symbol:\na) Triangle → line ✅\nb) Line → triangle\nc) Circle\nd) Square\n48. Zener diode symbol:\na) Line with bent bar ✅\nb) Triangle → line\nc) Circle\nd) Square\n49. Half-wave rectifier uses:\na) Transformer ✅\nb) Diode ✅\nc) Capacitor ✅\nd) All ✅\n50. Full-wave rectifier bridge has:\na) 2 diodes'}

{'0': 'b) 4 diodes ✅\nc) 3 diodes\nd) 1 diode\n51. Peak inverse voltage (PIV) in diode:\na) Max reverse voltage ✅\nb) Forward voltage\nc) Average voltage\nd) None\n52. Transistor cutoff:\na) IB=0 ✅\nb) IC=0\nc) VCE small\nd) Active\n53. Transistor saturation:\na) VCE≈0 ✅\nb) IC≈0\nc) IB≈0\nd) Active\n54. JFET operates:\na) Forward biased ✅\nb) Reverse biased\nc) Zero bias\nd) None\n55. MOSFET enhancement mode needs:\na) Gate voltage ✅\nb) Gate current\nc) Source voltage\nd) Drain voltage\n56. MOSFET depletion mode:\na) Naturally conducting ✅\nb) Needs gate voltage\nc) Switch off\nd) None\n57. Load line intersects:\na) DC and AC curves ✅\nb) Input curve\nc) Output curve\nd) None\n58. Diode cut -in voltage:\na) Minimum voltage to conduct ✅\nb) Maximum\nc) Zero'}

{'0': 'd) Infinite\n59. Voltage multiplier uses:\na) Diodes & capacitors ✅\nb) Transistors\nc) Resistors\nd) Inductors\n60. Zener regulator provides:\na) Constant voltage ✅\nb) Constant current\nc) Constant resistance\nd) None\nMicroprocessor & Interfacing (~60 MCQ)\n1. Microprocessor is:\na) A software\nb) Central processing unit on a single chip ✅\nc) Memory chip\nd) Input device\n2. Difference between microprocessor and microcontroller:\na) Microprocessor lacks RAM/ROM ✅\nb) Microcontroller has built -in RAM/ROM ✅\nc) Both a & b ✅\nd) None\n3. 8086/8088 belongs to:\na) 4-bit family\nb) 8-bit family\nc) 16 -bit family ✅\nd) 32 -bit family\n4. 8086 has:\na) 8-bit data bus\nb) 16 -bit data bus ✅\nc) 32 -bit data bu s\nd) 64 -bit data bus\n5. Memory segmentation in 8086:\na) Code, data, stack, extra ✅\nb) Input, output\nc) Registers only\nd) None\n6. Instruction set of 8086 contains:\na) Data transfer ✅\nb) Arithmetic ✅\nc) Logical ✅\nd) All ✅'}

{'0': '7. Addressing mode specifies:\na) How to acces s operands ✅\nb) Data size\nc) Clock\nd) Power\n8. Immediate addressing uses:\na) Constant value ✅\nb) Memory address\nc) Register\nd) Input\n9. Register addressing uses:\na) CPU register ✅\nb) Memory\nc) Input\nd) Constant\n10. Direct addressing uses:\na) Memory address ✅\nb) Regi ster\nc) Immediate\nd) Port\n11. Indirect addressing uses:\na) Register contains address ✅\nb) Memory contains address\nc) Immediate\nd) Port\n12. Single -processor system has:\na) One CPU ✅\nb) Multiple CPUs\nc) None\nd) All\n13. Multi -processor system:\na) One CPU\nb) Multiple CPUs ✅\nc) None\nd) All\n14. Assembler converts:\na) Assembly → Machine code ✅\nb) High -level → Assembly\nc) Machine → Assembly\nd) None\n15. Debugger is used for:\na) Detecting errors ✅'}

{'0': 'b) Writing code\nc) Compiling\nd) Executing only\n16. 8255A is:\na) Programmable Peripheral Interf ace ✅\nb) Timer\nc) DMA\nd) Memory\n17. 8254 is:\na) Programmable interval timer ✅\nb) PPI\nc) Interrupt controller\nd) UART\n18. Keyboard interfacing can be done via:\na) 8255 ✅\nb) 8254\nc) 8259\nd) DMA\n19. LCD interfacing uses:\na) 8255 ✅\nb) 8254\nc) 8259\nd) None\n20. Printer interfac ing uses:\na) Parallel ✅\nb) Serial\nc) Both ✅\nd) None\n21. Stepper motor interfacing:\na) 8255 ✅\nb) 8259\nc) 8254\nd) None\n22. A/D converter converts:\na) Analog → Digital ✅\nb) Digital → Analog\nc) Voltage\nd) Current\n23. D/A converter converts:\na) Analog → Digital\nb) Digital → Analog ✅\nc) Both'}

{'0': 'd) None\n24. 8259A is:\na) Programmable interrupt controller ✅\nb) Timer\nc) PPI\nd) DMA\n25. Interrupt vector table stores:\na) Addresses of interrupt routines ✅\nb) Data\nc) Instructions\nd) None\n26. DMA stands for:\na) Direct Memory Access ✅\nb) Dynamic Memory Access\nc) Dual Memory Access\nd) Data Memory Access\n27. Serial communication can be:\na) Synchronous ✅\nb) Asynchronous ✅\nc) Both ✅\nd) None\n28. EIA RS232 is:\na) Physical communication standard ✅\nb) Protocol\nc) Memory\nd) Timer\n29. Microprocessor clock controls:\na) Instruction timing ✅\nb) Data\nc) Voltage\nd) Current\n30. Bus demultiplexer separates:\na) Address & data lines ✅\nb) Input lines\nc) Output lines\nd) Power\n31. Bus controller manages:\na) Data transfer ✅\nb) Instruction fetch\nc) Clock\nd) None\n32. Programmed I/O means:'}

{'0': 'a) CPU actively polls ✅\nb) CPU interrupts\nc) DMA\nd) None\n33. Interrupt driven I/O:\na) CPU waits\nb) CPU responds to interrupt ✅\nc) CPU ignores\nd) None\n34. Parallel I/O port transfers:\na) 1 bit\nb) Multiple bits simultaneously ✅\nc) Serially\nd) None\n35. SRAM stands for:\na) Static RAM ✅\nb) Serial RAM\nc) Synchronous RAM\nd) None\n36. EEPROM stands for:\na) Electrically Erasable Programmable ROM ✅\nb) RAM\nc) Flash\nd) None\n37. Clock generator produces:\na) Timing pulses ✅\nb) Data\nc) Instructions\nd) None\n38. Stepper m otor moves in:\na) Continuous rotation\nb) Steps ✅\nc) Random\nd) None\n39. Timer applications include:\na) Delay ✅\nb) Event counting ✅\nc) Pulse generation ✅\nd) All ✅\n40. Asynchronous serial communication uses:\na) Start & stop bits ✅\nb) Clock'}

{'0': 'c) Both\nd) None\n41. Microproces sor I/O address decoding ensures:\na) Correct device access ✅\nb) Timing\nc) Speed\nd) None\n42. Interrupt vector points to:\na) Interrupt routine ✅\nb) Main program\nc) Data\nd) Timer\n43. Single -step execution helps in:\na) Debugging ✅\nb) Speeding\nc) Storage\nd) Communicati on\n44. Flag registers store:\na) Status ✅\nb) Data\nc) Address\nd) Control\n45. Carry flag is set when:\na) Addition exceeds limit ✅\nb) Subtraction negative\nc) Overflow\nd) Zero\n46. Zero flag is set when:\na) Result = 0 ✅\nb) Result > 0\nc) Carry occurs\nd) None\n47. Sign flag indica tes:\na) Positive/negative ✅\nb) Zero\nc) Carry\nd) Overflow\n48. Parity flag checks:\na) Even/odd bits ✅\nb) Zero\nc) Carry\nd) Sign'}

{'0': '49. Program counter stores:\na) Next instruction address ✅\nb) Current instruction\nc) Data\nd) Stack pointer\n50. Stack pointer points to:\na) Top o f stack ✅\nb) Bottom\nc) Memory\nd) None\n51. PUSH instruction:\na) Store in stack ✅\nb) Retrieve from stack\nc) Clear stack\nd) None\n52. POP instruction:\na) Store\nb) Retrieve ✅\nc) Clear\nd) None\n53. Software interrupt generated by:\na) Instruction ✅\nb) External device\nc) Timer\nd) DMA\n54. Hardware interrupt generated by:\na) Device ✅\nb) Instruction\nc) Program\nd) Memory\n55. Instruction cycle includes:\na) Fetch ✅\nb) Decode ✅\nc) Execute ✅\nd) All ✅\n56. Data bus width determines:\na) Data size per transfer ✅\nb) Address\nc) Instruction\nd) Clock\n57. Address bus width determines:\na) Maximum memory accessible ✅'}

{'0': 'b) Data size\nc) Instruction size\nd) Clock\n58. Control signals include:\na) RD, WR ✅\nb) ALE ✅\nc) INTA ✅\nd) All ✅\n59. Microprocessor interfacing requires:\na) Address decoding ✅\nb) Timing\nc) Data bus\nd) All ✅\n60. Multi -processor system advantage:\na) High speed ✅\nb) Parallel processing ✅\nc) Reliability ✅\nd) All ✅\nCommunication Theory (~50 MCQ)\n1. Fourier series represents:\na) Continuous signals ✅\nb) Discrete signals\nc) Both\nd) None\n2. Fourier transform converts:\na) Time → Frequency ✅\nb) Frequency → Time\nc) Voltage → Current\nd) None\n3. Convolution in time domain equals:\na) Multiplication in frequency domain ✅\nb) Addition\nc) Subtraction\nd) Division\n4. Parseval’s theorem relates:\na) Energy in time & frequency ✅\nb) Power\nc) Voltage\nd) Current\n5. Entropy in information theory measures:\na) Uncertainty ✅'}

{'0': 'b) Speed\nc) Bandwidth\nd) Amplitude\n6. Shannon’s theorem gives:\na) Maximum channel capacity ✅\nb) Minimum noise\nc) Maximum power\nd) None\n7. Channel capacity depends on:\na) Bandwidth ✅\nb) Signal -to-noise ratio ✅\nc) Both ✅\nd) None\n8. Analog modulation includes:\na) AM ✅\nb) FM ✅\nc) PM ✅\nd) All ✅\n9. AM stands for:\na) Amplitude Modulation ✅\nb) Angular Modulation\nc) Analog Modulation\nd) None\n10. FM stands for:\na) Frequency Modulation ✅\nb) Phase Modulation\nc) Amplitude Modulation\nd) None\n11. PM stands for:\na) Phase Modulation ✅\nb) Frequency Modulation\nc) Amplitude Modulation\nd) None\n12. Modulation purpose:\na) Efficient transmission ✅\nb) Amplification\nc) Rectification\nd) None\n13. Demodulation recovers:\na) Original signal ✅\nb) Noise\nc) Carrier'}

{'0': 'd) None\n14. Pulse Amplitude Modulation (PAM) uses:\na) Amplitude of pulses ✅\nb) Frequency\nc) Phase\nd) None\n15. Pulse Code Modulation (PCM) is:\na) Digital modulation ✅\nb) Analog modulation\nc) Hybrid\nd) None\n16. Delta modulation (DM) encodes:\na) Di fference between samples ✅\nb) Absolute value\nc) Average\nd) None\n17. Adaptive delta modulation (ADM) adjusts:\na) Step size ✅\nb) Frequency\nc) Phase\nd) None\n18. Time -Division Multiplexing (TDM) divides:\na) Time slots ✅\nb) Frequency\nc) Phase\nd) None\n19. Frequency -Division Multiplexing (FDM) divides:\na) Frequency ✅\nb) Time\nc) Phase\nd) None\n20. TDMA is:\na) Time -division multiple access ✅\nb) Frequency -division\nc) Code -division\nd) None\n21. FDMA is:\na) Time -division\nb) Frequency -division multiple access ✅\nc) Code -division\nd) None\n22. CDMA uses:'}

{'0': 'a) Codes to separate users ✅\nb) Time slots\nc) Frequency bands\nd) None\n23. Nyquist sampling theorem states:\na) Fs ≥ 2 × fmax ✅\nb) Fs < fmax\nc) Fs = fmax\nd) None\n24. Aliasing occurs if:\na) Fs < 2 × fmax ✅\nb) Fs ≥ 2 × fmax\nc) Fs = 2 × fmax\nd) None\n25. SNR stands for:\na) Signal -to-Noise Ratio ✅\nb) Signal -to-Number\nc) Sound -to-Noise\nd) None\n26. Power spectrum represents:\na) Distribution of power over frequency ✅\nb) Time\nc) Amplitude\nd) None\n27. Baseband signal is:\na) Original signal ✅\nb) Modulated signal\nc) Carrier\nd) None\n28. Bandpass signal is:\na) Centered around carrier ✅\nb) Original signal\nc) Noise\nd) None\n29. AM modulated signal has:\na) Carrier + sidebands ✅\nb) Carrier only\nc) Sidebands only\nd) None\n30. FM bandwidth depends on:\na) Frequency deviation ✅\nb) Amplitude'}

{'0': 'c) Phase\nd) None\n31. PM bandwidth depends on:\na) Phase deviation ✅\nb) Frequency\nc) Amplitude\nd) None\n32. Coherent detection used for:\na) AM demodulation ✅\nb) FM\nc) PM\nd) None\n33. Envelope detection used for:\na) AM ✅\nb) FM\nc) PM\nd) None\n34. Multiplexing purpose:\na) Efficient utiliz ation ✅\nb) Amplification\nc) Modulation\nd) None\n35. Information rate formula:\na) R = H × symbols/sec ✅\nb) R = H × f\nc) R = P × t\nd) None\n36. Signal bandwidth affects:\na) Data rate ✅\nb) Power\nc) Voltage\nd) None\n37. Noise degrades:\na) SNR ✅\nb) Bandwidth\nc) Time\nd) None\n38. Shannon capacity formula:\na) C = B log2(1 + S/N) ✅\nb) C = B × S/N\nc) C = B / S/N\nd) None'}

{'0': '39. Analog vs digital communication:\na) Analog continuous ✅\nb) Digital discrete ✅\nc) Both correct ✅\nd) None\n40. Multiplexing reduces:\na) Number of channels ✅\nb) Bandwidth\nc) Noise\nd) None\n41. Demultiplexer separates:\na) Combined signals ✅\nb) Carrier\nc) Modulation\nd) None\n42. Fourier series uses:\na) Sin & cos ✅\nb) Exponential only\nc) Step function\nd) None\n43. Power spectrum integral =\na) Signal energy ✅\nb) Noise\nc) Bandwidth\nd) None\n44. Pulse duration affects:\na) Bandwidth ✅\nb) Power\nc) Noise\nd) None\n45. PCM uses:\na) Sampling ✅\nb) Quantization ✅\nc) Encoding ✅\nd) All ✅\n46. Delta modulation advantage:\na) Simple ✅\nb) Requires low bandwidth ✅\nc) Adaptive possible ✅\nd) All ✅\n47. CDMA allows:'}

{'0': 'a) Multiple use rs ✅\nb) Single user\nc) Only one channel\nd) None\n48. Nyquist rate =\na) 2 × fmax ✅\nb) fmax\nc) fmax / 2\nd) None\n49. Pulse shaping reduces:\na) Inter -symbol interference ✅\nb) Noise\nc) Bandwidth\nd) None\n50. Communication system goal:\na) Reliable data transfer ✅\nb) Maximum n oise\nc) Minimum bandwidth\nd) None\nComputer Networking & Security (~60 MCQ)\n1. Protocol hierarchy defines:\na) Layered communication ✅\nb) Hardware only\nc) Software only\nd) None\n2. Data link layer provides:\na) Reliable link ✅\nb) Routing\nc) Application\nd) Transport\n3. HLDC stands for:\na) High -Level Data Link Control ✅\nb) High -Level Device Control\nc) Hardware Link Device Control\nd) None\n4. LAN protocols include:\na) IEEE 802.3 ✅\nb) IEEE 802.11 ✅\nc) Both ✅\nd) None\n5. Hub operates at:\na) Physical layer ✅'}

{'0': 'b) Data link\nc) Network\nd) Transport\n6. Switch operates at:\na) Physical\nb) Data link ✅\nc) Network\nd) Transport\n7. Bridge connects:\na) Two LANs ✅\nb) Two computers\nc) Router\nd) None\n8. FDDI uses:\na) Fiber optic ✅\nb) Copper\nc) Wireless\nd) None\n9. Fast Ethernet speed:\na) 10 Mbps\nb) 100 Mbps ✅\nc) 1 Gbps\nd) 10 Gbps\n10. Routing algorithm decides:\na) Path selection ✅\nb) Bandwidth\nc) Speed\nd) None\n11. Congestion control prevents:\na) Network overload ✅\nb) Data loss\nc) Security\nd) None\n12. Internetworking involves:\na) Connecting LANs/WANs ✅\nb) Hardware onl y\nc) Software only\nd) None\n13. Fragmentation occurs when:\na) Packet > MTU ✅\nb) Packet < MTU\nc) Router fails'}

{'0': 'd) None\n14. Firewall purpose:\na) Network security ✅\nb) Routing\nc) Switching\nd) None\n15. IPV4 address length:\na) 32 bits ✅\nb) 64 bits\nc) 128 bits\nd) 16 bits\n16. IPV6 address length:\na) 32 bits\nb) 64 bits\nc) 128 bits ✅\nd) 16 bits\n17. ARP resolves:\na) IP → MAC ✅\nb) MAC → IP\nc) Port → IP\nd) None\n18. RARP resolves:\na) MAC → IP ✅\nb) IP → MAC\nc) Port → IP\nd) None\n19. Mobile IP enables:\na) Device mobility ✅\nb) Routing\nc) Switching\nd) None\n20. Transport protocol for reliable communication:\na) TCP ✅\nb) UDP\nc) ICMP\nd) None\n21. TCP provides:\na) Connection -oriented ✅\nb) Error checking ✅\nc) Flow control ✅\nd) All ✅\n22. UDP provides:'}

{'0': 'a) Connectionless ✅\nb) No guarantee ✅\nc) Both ✅\nd) None\n23. AAL of ATM:\na) Adaptation layer ✅\nb) Application layer\nc) Transport layer\nd) None\n24. Network security includes:\na) Cryptography ✅\nb) Authentication ✅\nc) Digital signatures ✅\nd) All ✅\n25. DES stands for:\na) Data Encryption Standard ✅\nb) Digital Encryption Standard\nc) Data Encoding System\nd) None\n26. IDEA stands for:\na) International Data Encryption Algorithm ✅\nb) Data Encryption Algorithm\nc) Information Encoding\nd) None\n27. Public key algorithm uses:\na) Two keys ✅\nb) One key\nc) Both\nd) None\n28. Authentication ensures:\na) Identity verification ✅\nb) Data transfer\nc) Speed\nd) None\n29. Digital signature ensures:\na) Authentication ✅\nb) Integrity ✅\nc) Both ✅\nd) None\n30. Gigabit Ethernet speed:\na) 100 Mbps'}

{'0': 'b) 1 Gbps ✅\nc) 10 Gbps\nd) None\n31. DNS resolves:\na) Domain → IP ✅\nb) IP → Domain\nc) MAC → IP\nd) None\n32. Name servers store:\na) Domain name info ✅\nb) IP only\nc) MAC only\nd) None\n33. Email privacy is ensured by:\na) Encryption ✅\nb) Routing\nc) Firewall\nd) None\n34. SNMP stands for:\na) Simple Network Management Protocol ✅\nb) Secure Network\nc) Standard Ne twork\nd) None\n35. HTTP operates at:\na) Application layer ✅\nb) Transport\nc) Network\nd) Data link\n36. HTTPS ensures:\na) Secure HTTP ✅\nb) Fast HTTP\nc) Normal HTTP\nd) None\n37. LAN uses:\na) Ethernet ✅\nb) FDDI ✅\nc) Both ✅\nd) None\n38. WAN connects:\na) Large area networks ✅\nb) Si ngle computer\nc) Router only'}

{'0': 'd) None\n39. Fragmentation handled by:\na) Network layer ✅\nb) Transport\nc) Data link\nd) None\n40. IPV4 provides:\na) 4 billion addresses ✅\nb) 1 billion\nc) 128 bit\nd) None\n41. IPV6 provides:\na) 128 -bit address ✅\nb) 32 -bit\nc) 64 -bit\nd) None\n42. TCP uses:\na) Three -way handshake ✅\nb) UDP\nc) ICMP\nd) None\n43. UDP uses:\na) No handshake ✅\nb) Handshake\nc) Connection -oriented\nd) None\n44. Firewalls can be:\na) Packet filtering ✅\nb) Proxy ✅\nc) Both ✅\nd) None\n45. Cryptography converts:\na) Plaintext → Ciphertext ✅\nb) Ciphert ext → Plaintext\nc) Data only\nd) None\n46. VPN ensures:\na) Secure private network ✅\nb) Open network\nc) LAN only\nd) None\n47. Transport layer manages:'}

{'0': 'a) End -to-end communication ✅\nb) Node -to-node\nc) Data link\nd) Physical\n48. ARP used in:\na) Local network ✅\nb) Internet\nc) WAN\nd) None\n49. RARP used to:\na) Assign IP from MAC ✅\nb) Assign MAC\nc) DNS\nd) None\n50. ICMP used for:\na) Error reporting ✅\nb) Data transfer\nc) Encryption\nd) None\n51. SMTP used for:\na) Sending emails ✅\nb) Receiving emails\nc) Browsing\nd) None\n52. POP3 used for:\na) Receiving emails ✅\nb) Sending emails\nc) Browsing\nd) None\n53. IMAP used for:\na) Receiving emails ✅\nb) Sending\nc) Browsing\nd) None\n54. VPN tunnel provides:\na) Encrypted path ✅\nb) Open path\nc) Wireless path\nd) None\n55. Network congestion occurs due to:\na) Excessive tr affic ✅\nb) Low traffic'}

{'0': 'c) Short cable\nd) None\n56. Routing algorithms include:\na) Distance vector ✅\nb) Link state ✅\nc) Both ✅\nd) None\n57. MAC address is:\na) Hardware address ✅\nb) IP address\nc) Domain name\nd) None\n58. IPv4 address written in:\na) Dot -decimal ✅\nb) Hex\nc) Binary only\nd) None\n59. IPv6 address written in:\na) Hexadecimal ✅\nb) Decimal\nc) Binary\nd) None\n60. Network layer provides:\na) Logical addressing ✅\nb) Physical addressing\nc) Transport\nd) Application'}