Circuit Theory and Electronics Fundamentals 2020/2021

Integrated Masters in Aerospace Engineering, Técnico, University of Lisbon

Third Laboratory Report

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Rui Rodrigues, 95844
Tiago Silva, 95850
Tomás Ribeiro, 95854

Contents

1 Introduction

The objective of this laboratory assignment is to The circuit can be seen in Figure 1.

In Section 2, a theoretical introduction is made in order to contextualize all the main principles that sustain our analysis of the circuit. This circuit is carefully analysed in Section, where the results are obtained in GNU Octave. Also, in Section, the circuit is analysed by simulation through the use of NGSpice to simulate the electric circuit behaviour. The results of the simulation of Section 4 are then compared to the theoretical results obtained in Section 3 and the comparative results are expressed in Se. The conclusions of this study are outlined in the final part of the report, in Section 6.

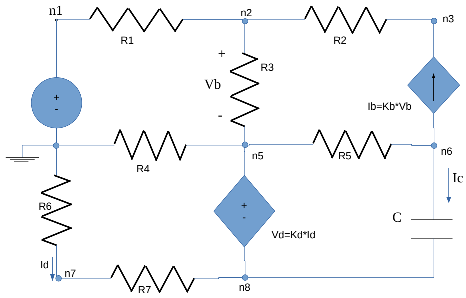

Figure 1: Third laboratory circuit.

2 Theoretical Introduction

3 Theoretical Analysis

THIS IS NOT ACTUAL In this section, we can find the results of each topic required in the theoretical analysis. The numeric results or graphics are presented alongside a short explanation of the interpretation of the problem.

$$\begin{cases} v_t = v_n + v_f \\ f = 1kHz = 1000Hz \\ NEEDTOBEIMPROVEDA = 14; T = 1/50; t = linspace(0, T/2, 1000); w = 2 * pi * (1/T); R = 1000C = \end{cases}$$

3.1 Envelope Detector Circuit

The voltage source v_S produces a sinusoidal wave and is defined by the following expression: $v_S = Acos(\omega t)$.

The envelope detector circuit includes a full-wave bridge rectifier, whose voltage output $v0_{rect}$ corresponds to the absolute value of the voltage source v_S.

$$v0_rect = \begin{cases} v_S, v_S \geq 0 \\ -v_S, v_S \leq 0 \end{cases}$$

Finally, the envelope detector circuit voltage v_0 is the highest between $v0_rect$, the full-wave bridge rectifier voltage, and the voltage $v0_{exp}$ induced when the capacitor C discharges through the resistor R, described by the following equation: $vO_{exp} = Acos(\omega t_{OFF})e^(\frac{-(tON-tOFF)}{RC})$.

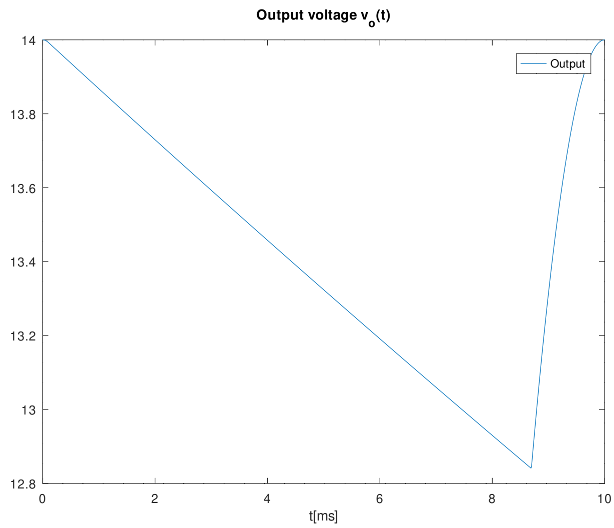

Figure 2: The final envelope detector circuit voltage v_0 during a half-period interval.

where t is expressed in miliseconds (ms) along the x-axis and v_0), the envelope output voltage, is expressed in Volts (V) along the y-axis.

3.2 Voltage Regulator Circuit

The voltage regulator attenuates oscillations in the input signal without frequency dependence and takes advantage of the non-linear characteristic of the N diodes included in the positive voltage limiter.

The voltage analysis of the regulator applies the incremental analysis method, separating the DC and incremental components.

The diode incremental resistance is calculated using the following expression: $r_d = \frac{\eta v_t}{I_s e^{(\frac{v_d}{\eta v_t}}}$.

Applying the voltage divider rule, the AC increment v_{out} is defined using the following relation: $vout = \frac{Nr_d}{Nrd+R2} vO$.

On the other hand, the DC voltage V_{OUT} is obatined multypling the diode voltage v_d by the number of diodes N used in the voltage regulator circuit: $V_{OUT} = Nv_d$.

$\{NEEDTOBEIMPROVEDn = 17; R2 = 10e3; eta = 1; vt = 25e-3; vd = 0.706; I_s = 1e-14;$

The final voltage of the regulator circuit v_{OUT} is obtained adding the results of the incremental analysis and the DC analysis: $v_{OUT} = v_{out} + V_{OUT}$.

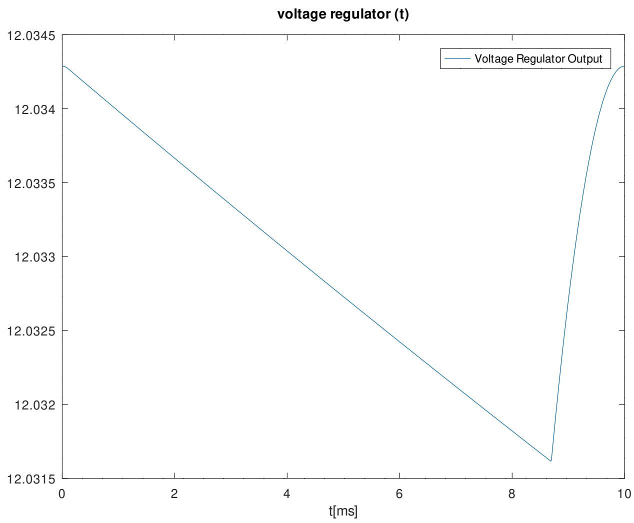

Figure 3: The final voltage v_{OUT} of the voltage regulator circuit during a half-period interval.

where t is expressed in miliseconds (ms) along the x-axis and v_{OUT}, the voltage of the regulator, is expressed in Volts (V) along the y-axis.

3.3 Voltage Ripple

The voltage ripple can be improved using a full-wave rectifier circuit in the envelope detector circuit.

The value of the voltage ripple v_{ripple} can be calculated relating the maximum and the minimum values of the final voltage of the regulator circuit v_{OUT}, using the following expression: $v_{ripple} = max(v_{OUT}) - min(v_{OUT})$.

THIS SHOULD PRINT THE RIPPLE BELOW	
THE OUTPUT VOLTAGE RIPPLE IS	0.00267197 V

3.4 The Output DC Level

The t_{ON} is calculated using the Newton-Raphson iterative method, starting with a function obtained through the following equation: $Acos(\omega t_{ON}) = Acos(\omega t_{OFF})e^{(\frac{-(t_{ON}-t_{OFF})}{RC}})$.

The DC level output average is obtained integrating the sinusoidal and exponential functions during a half-period interval. The calculations are shown below.

$t \in [0, t_{OFF})$
$\int_0^{t_{OFF}} = \frac{Nr_d}{Nr_d+R_2}\frac{A}{\omega}sin(\omega t_{OFF}) + Nv_d t_{OFF}$

$t \in [t_{OFF}, t_{ON})$
$\int_{t_{OFF}}^{t_{ON}} = \frac{Nr_d}{Nr_d+R_2}(-ARCcos(\omega t_{OFF})(e^{\frac{-(tON-tOFF)}{RC}} - 1)) + Nv_d(t_{ON} - t_{OFF})$

THIS SHOULD PRINT THE AVERAGE BELOW	
THE OUTPUT VOLTAGE AVERAGE LEVEL IS	12.0248 V

The Output DC Level accuracy can be evaluated through comparing the final voltage of the circuit v_{OUT} and the $12V$ constant function.

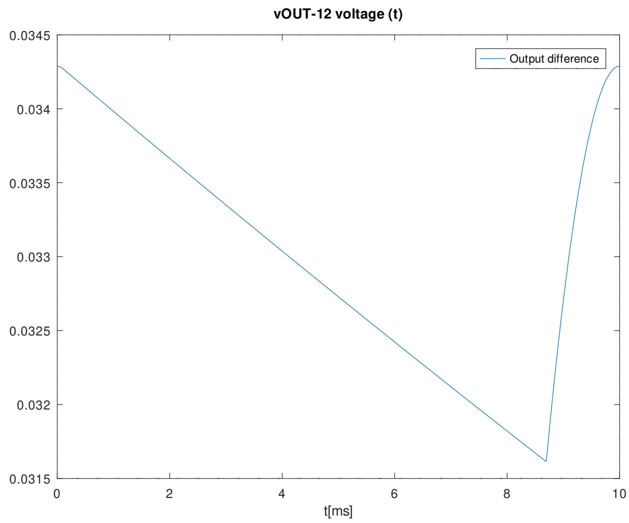

Figure 4: The voltage $v_{OUT} - 12$ during a half-period interval.

Where t is expressed in seconds (s) along the x-axis and $v_{OUT} - 12)$, the output voltage difference, is expressed in Volts (V) along the y-axis.

4 Simulation Analysis

In this section, we can find the results of each topic required in the simulation analysis. The numeric results or graphics are presented alongside a short explanation of the interpretation of the problem. All of the results were obatined usig NGSpice and the section is dividid in five different subsections

Ngspice is a circuit-simulation program that makes it possible to have an accurate representation of how the circuit would behave if it was actually assembled. The different tables shown below ilustrate the simulated operating point results for the circuit under analysis. As it can be seen, the tables show the values of the voltage in all nodes, the currents in all of the branches and also the currents in independent voltage sources.

5 Relative Error and Graphic Analysis

5.1 Topic I

6 Conclusion

In this second laboratory assignment, all the major goals of the project were achieved. We concluded with success a further interaction with a new software (Ubuntu), with a simulation platform (Ngspice), with a computational language program (GNU Octave) and with a text report editor (LaTeX). The analysis of the circuit was also finished with success through simulation and theoretical interpretation, which allowed a good comparative analysis between these two methods.