

1. Description

1.1. Project

Project Name	SmartCar
Board Name	custom
Generated with:	STM32CubeMX 6.1.1
Date	03/19/2021

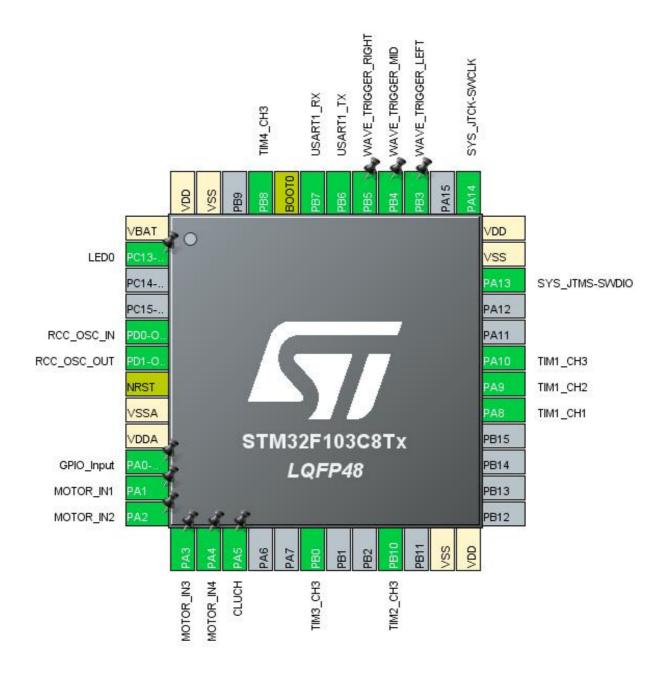
1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M3

2. Pinout Configuration

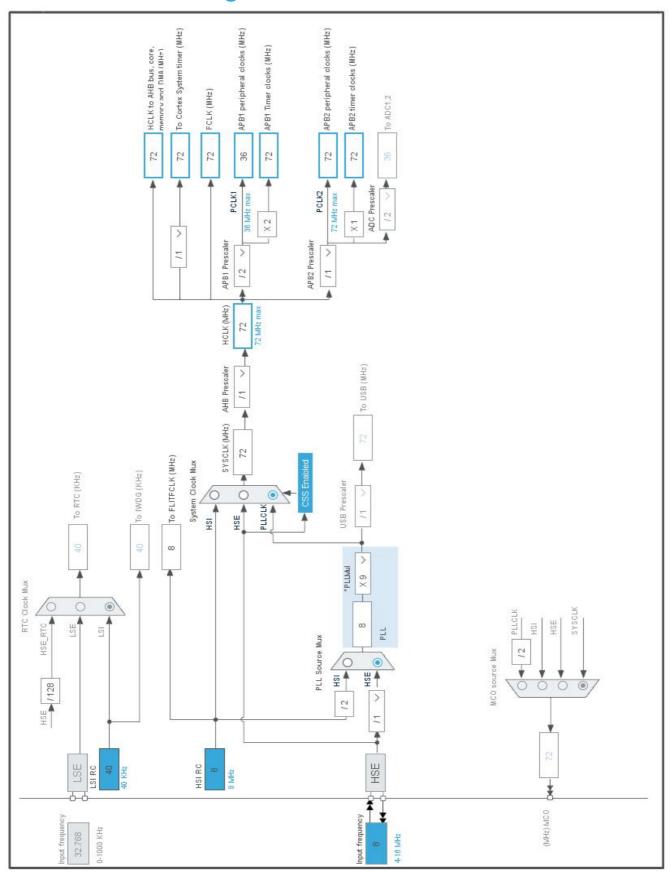


3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP48	(function after	, , ,	Function(s)	20.001
LQII 40			i dilodori(s)	
	reset)			
1	VBAT	Power		
2	PC13-TAMPER-RTC *	I/O	GPIO_Output	LED0
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP *	I/O	GPIO_Input	
11	PA1 *	I/O	GPIO_Output	MOTOR_IN1
12	PA2 *	I/O	GPIO_Output	MOTOR_IN2
13	PA3 *	I/O	GPIO_Output	MOTOR_IN3
14	PA4 *	I/O	GPIO_Output	MOTOR_IN4
15	PA5 *	I/O	GPIO_Output	CLUCH
18	PB0	I/O	TIM3_CH3	
21	PB10	I/O	TIM2_CH3	
23	VSS	Power		
24	VDD	Power		
29	PA8	I/O	TIM1_CH1	
30	PA9	I/O	TIM1_CH2	
31	PA10	I/O	TIM1_CH3	
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power	_	
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
39	PB3 *	I/O	GPIO_Output	WAVE_TRIGGER_LEFT
40	PB4 *	I/O	GPIO_Output	WAVE_TRIGGER_MID
41	PB5 *	I/O	GPIO_Output	WAVE_TRIGGER_RIGHT
42	PB6	I/O	USART1_TX	
43	PB7	I/O	USART1_RX	
44	воото	Boot		
45	PB8	I/O	TIM4_CH3	
47	VSS	Power	11_0110	
48	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value	
Project Name	SmartCar	
Project Folder	D:\Desktop\smart-car	
Toolchain / IDE	MDK-ARM V5	
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.3	
Application Structure	Advanced	
Generate Under Root	No	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_TIM1_Init	TIM1
4	MX_TIM3_Init	TIM3
5	MX_USART1_UART_Init	USART1
6	MX_TIM2_Init	TIM2
7	MX TIM4 Init	TIM4

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
мси	STM32F103C8Tx
Datasheet	DS5319_Rev17

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

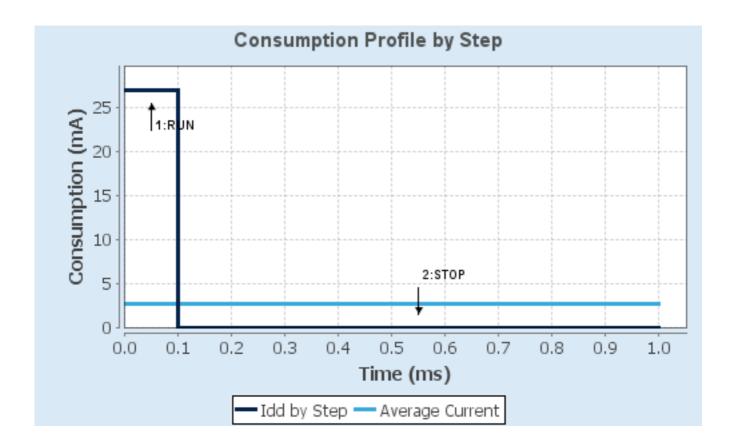
6.4. Sequence

	T	
Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	27 mA	14 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	100.1	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.71 mA
Battery Life	1 month, 21 days,	Average DMIPS	61.0 DMIPS
	17 hours		

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Prefetch Buffer Enabled

Flash Latency(WS) 2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

7.2. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.3. TIM1

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2 Channel3: PWM Generation CH3

7.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 71 *
Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 20000 *

Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0

auto-reload preload Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable

BRK Polarity High

Break And Dead Time management - Output Configuration:

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CH Idle State Reset

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CH Idle State Reset

PWM Generation Channel 3:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CH Idle State Reset

7.4. TIM2

Channel3: Input Capture direct mode

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

auto-reload preload

7199 *

Object

No Division

Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Input Capture Channel 3:

Polarity Selection Rising Edge
IC Selection Direct
Prescaler Division Ratio No division

Input Filter (4 bits value)

7.5. TIM3

Channel3: Input Capture direct mode

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

auto-reload preload

7199 *

Up

65535

No Division

Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Input Capture Channel 3:

Polarity Selection Rising Edge
IC Selection Direct
Prescaler Division Ratio No division

Input Filter (4 bits value) 0

7.6. TIM4

Channel3: Input Capture direct mode

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 65535

Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Input Capture Channel 3:

Polarity Selection Rising Edge
IC Selection Direct
Prescaler Division Ratio No division

Input Filter (4 bits value) 0

7.7. **USART1**

Mode: Asynchronous

7.7.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive Only *

Over Sampling 16 Samples

7.8. FREERTOS

Interface: CMSIS_V2

7.8.1. Config parameters:

API:

FreeRTOS API CMSIS v2

Versions:

FreeRTOS version 10.0.1 CMSIS-RTOS version 2.00

Kernel settings:

USE_PREEMPTION Enabled

CPU_CLOCK_HZ SystemCoreClock

TICK_RATE_HZ 1000
MAX_PRIORITIES 56
MINIMAL_STACK_SIZE 128

16 MAX_TASK_NAME_LEN USE_16_BIT_TICKS Disabled Enabled IDLE_SHOULD_YIELD Enabled USE_MUTEXES Enabled USE_RECURSIVE_MUTEXES Enabled USE_COUNTING_SEMAPHORES QUEUE_REGISTRY_SIZE 8 Disabled USE_APPLICATION_TASK_TAG Enabled ENABLE_BACKWARD_COMPATIBILITY Disabled USE_PORT_OPTIMISED_TASK_SELECTION Disabled USE_TICKLESS_IDLE Enabled USE_TASK_NOTIFICATIONS Disabled RECORD_STACK_HIGH_ADDRESS

Memory management settings:

Memory Allocation Dynamic / Static

TOTAL_HEAP_SIZE 3072

Memory Management scheme heap_4

Hook function related definitions:

USE_IDLE_HOOK Disabled
USE_TICK_HOOK Disabled
USE_MALLOC_FAILED_HOOK Disabled
USE_DAEMON_TASK_STARTUP_HOOK Disabled
CHECK_FOR_STACK_OVERFLOW Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS Disabled
USE_TRACE_FACILITY Enabled
USE_STATS_FORMATTING_FUNCTIONS Disabled

Co-routine related definitions:

USE_CO_ROUTINES Disabled MAX_CO_ROUTINE_PRIORITIES 2

Software timer definitions:

USE_TIMERS Enabled
TIMER_TASK_PRIORITY 2
TIMER_QUEUE_LENGTH 10
TIMER_TASK_STACK_DEPTH 256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY 15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY 5

7.8.2. Include parameters:

Include definitions:

vTaskPrioritySet Enabled uxTaskPriorityGet Enabled Enabled vTaskDelete vTaskCleanUpResources Disabled vTaskSuspend Enabled Enabled vTaskDelayUntil vTaskDelay Enabled xTaskGetSchedulerState Enabled Enabled xTaskResumeFromISRxQueueGetMutexHolder Enabled xSemaphoreGetMutexHolder Disabled Disabled pcTaskGetTaskName uxTaskGetStackHighWaterMark Enabled xTaskGetCurrentTaskHandle Disabled Enabled eTaskGetState xEventGroupSetBitFromISR Disabled xTimerPendFunctionCall Enabled xTaskAbortDelay Disabled xTaskGetHandle Disabled

7.8.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT Disabled

Project settings (see parameter description first):

Use FW pack heap file Enabled

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PD0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	n/a	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	n/a	Low	
	PA10	TIM1_CH3	Alternate Function Push Pull	n/a	Low	
TIM2	PB10	TIM2_CH3	Input mode	No pull-up and no pull-down	n/a	
TIM3	PB0	TIM3_CH3	Input mode	No pull-up and no pull-down	n/a	
TIM4	PB8	TIM4_CH3	Input mode	No pull-up and no pull-down	n/a	
USART1	PB6	USART1_TX	Alternate Function Push Pull	n/a	High *	
	PB7	USART1_RX	Input mode	No pull-up and no pull-down	n/a	
GPIO	PC13- TAMPER- RTC	GPIO_Output	Output Push Pull	Pull-up *	Low	LED0
	PA0-WKUP	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_IN1
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_IN2
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_IN3
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_IN4
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CLUCH
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WAVE_TRIGGER_LEFT
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WAVE_TRIGGER_MID
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WAVE_TRIGGER_RIGHT

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Prefetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	15	0	
System tick timer	true	15	0	
TIM2 global interrupt	true	5	0	
TIM3 global interrupt	true	5	0	
TIM4 global interrupt	true	5	0	
USART1 global interrupt	true	6	0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
TIM1 break interrupt	unused			
TIM1 update interrupt	unused			
TIM1 trigger and commutation interrupts	unused			
TIM1 capture compare interrupt	unused			

8.3.2. NVIC Code generation

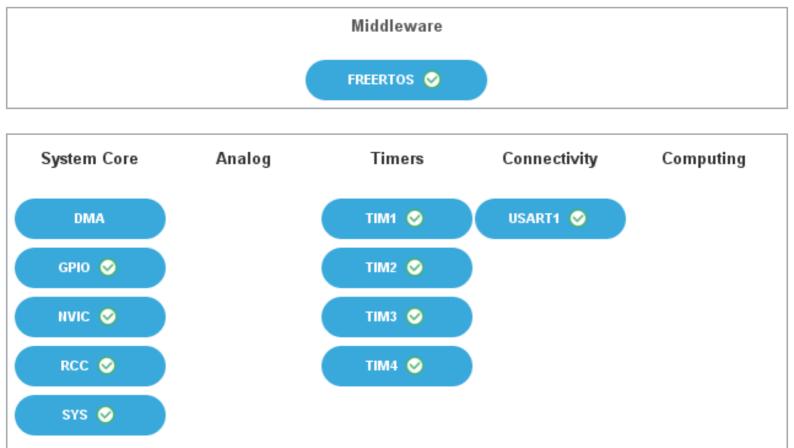
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	true
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	true	true
TIM2 global interrupt	false	true	true
TIM3 global interrupt	false	true	true
TIM4 global interrupt	false	true	true
USART1 global interrupt	false	true	true

SmartCar Project
Configuration Report

* User modified value

9. System Views

- 9.1. Category view
- 9.1.1. Current



10. Docs & Resources

Type Link

Datasheet http://www.st.com/resource/en/datasheet/CD00161566.pdf

Reference http://www.st.com/resource/en/reference_manual/CD00171190.pdf

manual

Programming http://www.st.com/resource/en/programming_manual/CD00228163.pdf

manual

Programming http://www.st.com/resource/en/programming_manual/CD00283419.pdf

manual

Errata sheet http://www.st.com/resource/en/errata_sheet/CD00190234.pdf

Application note http://www.st.com/resource/en/application_note/CD00160362.pdf

Application note http://www.st.com/resource/en/application_note/CD00164185.pdf

Application note http://www.st.com/resource/en/application_note/CD00167326.pdf

Application note http://www.st.com/resource/en/application_note/CD00167594.pdf

Application note http://www.st.com/resource/en/application_note/CD00211314.pdf

Application note http://www.st.com/resource/en/application_note/CD00249778.pdf

Application note http://www.st.com/resource/en/application_note/CD00259245.pdf

Application note http://www.st.com/resource/en/application_note/CD00264321.pdf

Application note http://www.st.com/resource/en/application_note/CD00264342.pdf

Application note http://www.st.com/resource/en/application_note/CD00264379.pdf

Application note http://www.st.com/resource/en/application_note/DM00024853.pdf

Application note http://www.st.com/resource/en/application_note/DM00032987.pdf

Application note http://www.st.com/resource/en/application_note/DM00033267.pdf

Application note http://www.st.com/resource/en/application_note/DM00033344.pdf

Application note http://www.st.com/resource/en/application_note/DM00042534.pdf

Application note http://www.st.com/resource/en/application_note/DM00052530.pdf

Application note http://www.st.com/resource/en/application_note/DM00073742.pdf

Application note http://www.st.com/resource/en/application_note/DM00080497.pdf

Application note http://www.st.com/resource/en/application_note/DM00129215.pdf

Application note http://www.st.com/resource/en/application_note/DM00160482.pdf http://www.st.com/resource/en/application_note/DM00156964.pdf Application note Application note http://www.st.com/resource/en/application_note/DM00209695.pdf Application note http://www.st.com/resource/en/application_note/DM00220769.pdf http://www.st.com/resource/en/application_note/DM00257177.pdf Application note Application note http://www.st.com/resource/en/application_note/DM00272912.pdf http://www.st.com/resource/en/application note/DM00236305.pdf Application note Application note http://www.st.com/resource/en/application_note/DM00296349.pdf Application note http://www.st.com/resource/en/application note/DM00325582.pdf Application note http://www.st.com/resource/en/application note/DM00327191.pdf Application note http://www.st.com/resource/en/application_note/DM00354244.pdf Application note http://www.st.com/resource/en/application_note/DM00315319.pdf Application note http://www.st.com/resource/en/application_note/DM00380469.pdf Application note http://www.st.com/resource/en/application_note/DM00395696.pdf http://www.st.com/resource/en/application_note/DM00493651.pdf Application note Application note http://www.st.com/resource/en/application_note/DM00536349.pdf Application note http://www.st.com/resource/en/application_note/DM00725181.pdf