**O2Micro Campus Recruiting**

**POSITION**

**DIGITAL IC DESIGN ENGINEER**

**（90 Minutes）**

**Applicant Name:**

**Phone number:**

**Degree and Major:**

**Date and Time:**

**Question-1: basic conception（70）**

**1-1:** Please describe the **setup-time, hold-time, recovery time**, **remove time** of a D-flip flop. You should draw diagram of the timing relation. **（8）**

**1-2**: What is metastability and what are it’s effects? **（5）**

**1-3**: Please draw a block diagram of a typical asynchronous FIFO, and describe the interface (e.g. clock A domain write data to clock B domain through asynchronous FIFO) **（10）**

**1-4:** Please point out the errors in the following circuit**（6）**



**1-5:** Please point out the issue of bellow code and fix it.**（5）**

always @(A or B ) begin

Y = A & B & C;

end

**1-6:** what is the difference between asynchronous reset and synchronous reset? **（5）**

**1-7:**  Please describe the difference of the synthesis result for below two sentences. Draw the circuit diagram by standard cell symbols. **（5）**



**1-8:**  Please describe the synthesis result of bellow code, What’s the issue of this design and how to optimize this design. **（5）**

always @( G or D ) begin

if ( G ) Q <= D ;

end

**1-9:** please list the CPU you know in SOC design, and explain what is the interruption**（5）**

**1-10:**  please write down your understanding of bellow items**（6）**

1. what is formality verification
2. what is STA
3. what is DFT

**1-11:** please describe the ASIC design flow of your understanding and list the EDA tools according to the flow. **（10）**

**Question-2: Logic design and coding by Verilog Language. You should write verilog code（30）**

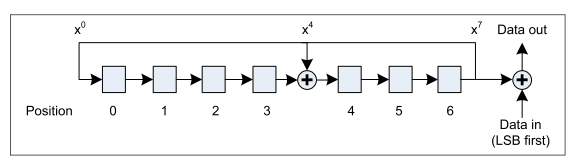
**2-1**: Please design rising edge detection for an input asynchronous signal.**（5）**

**2-2**: Please write a behavior model of 32M(period is 62.5ns) clock generator**（5）**

Note, default times unit is 1ns, e.g. #1 is 1ns.

**2-3**: Please synchronize “clk\_a” domain pulse “a” to “clk\_b” domain, clk\_a is faster then clk\_b**（10）**

**2-4**: please design bellow linear feedback shift register (LFSR) with enable, the initial value of LFSR is 7’h25 **（10）**



module data\_whitening(

input clk, //clock

input rst\_n, //reset, active low

//

input data\_i, //Date in on the figure

input data\_i\_en, //1: Date in is valid; 0: Date in is invalid

//

output data\_o, //Data out on the figure

output data\_o\_en //1: Date out is valid; 0: Date out is invalid

);

// Pls supplement verilog code