# CS 2110 Timed Lab 2

**Due Date and Time**

Day: Wednesday, February 15th

Time: Before the end of your assigned lab section

# Policy

## Submission

**TURN IN THIS ASSIGNMENT ELECTRONICALLY USING T-SQUARE SUBMISSIONS WHICH ARE LATE WILL NOT BE ACCEPTED. EMAIL SUBMISSIONS WILL NOT BE ACCEPTED UNDER ANY CIRCUMSTANCES! IN ADDITION IF YOU FORGET TO HIT THE SUBMIT BUTTON YOU WILL GET A ZERO.**

## Questions

If you are unsure of what questions mean, the TA's will clarify them to the best of their ability. We will not be able to answer any questions about how to reach a solution to the timed lab questions. You should know how by now!

## What's Allowed

- The assignment files
- Your previous homework and lab submissions
- Your mind
- Blank paper for scratch work

## What's Not Allowed

- The Internet (except the T-Square Assignment page to submit)
  - Any resource on T-Square that is not given in the assignment.
  - Textbook or notes on paper or saved on your computer.
  - Dropbox (If your harddrive crashes we will let you retake it).
  - Email/IM
  - Contact in any form with any other person besides TAs
  - If you have any questions on what you may not use then assume you can't use it and ask a TA.

## Other Restrictions

- You may not leave the classroom until we have verified that you have submitted the lab. If you leave the classroom without submitting you will receive a zero.

1. **YOU MUST SUBMIT BY THE END OF YOUR LAB PERIOD**. Bear in mind that the clock on your computer may be a few minutes slow. You are supposed to have a full class period to work, and we are letting you use the 15 minutes between classes to make sure you have submitted your work. **WE WILL NOT ACCEPT LATE SUBMISSIONS**, be they 1 second or 1 hour late.

2. The timed lab has been configured to accept one submission. If you accidentally submit or submit the wrong version flag one of the TAs and we will reopen submission for you.

## Violations

Failure to follow these rules will be in violation of the Georgia Tech Honor Code. **AND YOU WILL RECEIVE A ZERO** and you will be reported to Bill and the Office of Student Integrity.

We take cheating and using of unauthorized resources **VERY SERIOUSLY** and you will be in serious trouble if you are caught.

## Remember

1. There is partial credit given, and some of it is just following the directions.

2. We allow you to use your homework assignment.

3. Please don't get stressed out during a timed lab. You have plenty of time; however, use your time effectively

4. Again, remember: Don't get stressed. Partial credit will be given for things you have done correctly. Do the best you can!

5. If you don't know something at least **TRY.** Do not just walk out of the lab or submit an empty file. Partial credit!

6. Remember what you can and can't use. If you don't know, then don't use it and ask a TA if you can use it. If we catch you with unauthorized resources we will give you a zero, so better to be safe than sorry.

## The Assignment

You will build a finite state machine from a state transition diagram we provide you in this file to control a particular display device. You may build this using either one-hot or encoded state.

## Specifications

Your state machine will take in three inputs:

1. A “RST” input which you *must* use to clear out your register asynchronously. The provided tester will not work if you use the reset signal as part of your next state logic:

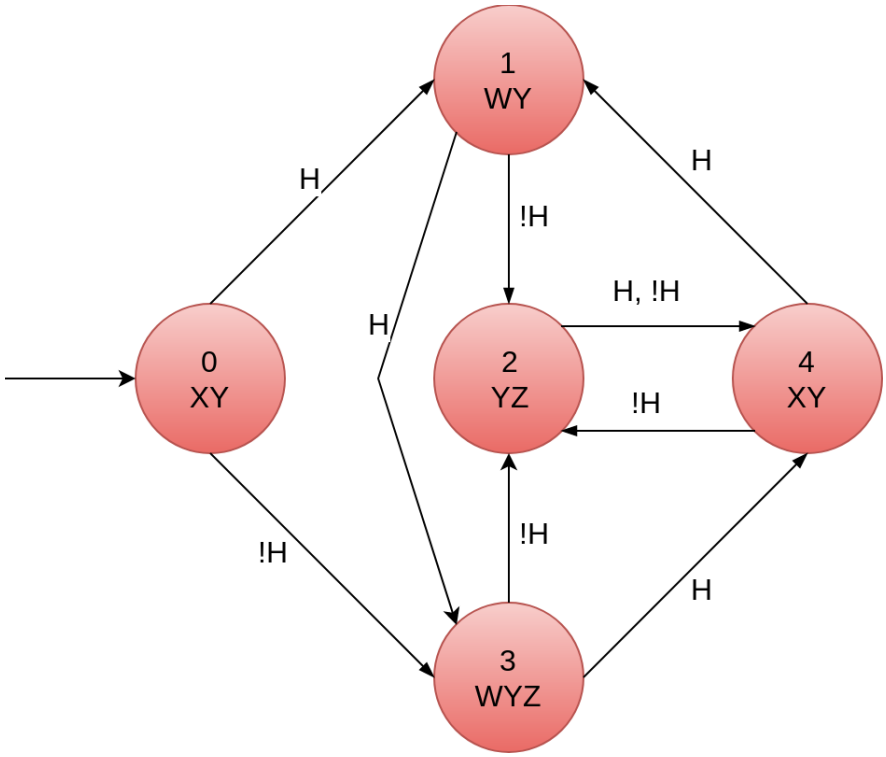

1. An “A” input which will help determine the current state
2. A “CLK” input which represents the clock (Note that this will hook up to the clock in the main circuit).

Your state machine will have 4 outputs: W, X, Y, and Z

Your state machine will have 5 states! You must have all 5 states to receive full credit!

## State Transition Diagram

Here is the state transition diagram:



## Tester Subcircuit

A comprehensive tester has been provided for you. To run it, press Ctrl+k to enable ticks, then click the "TEST" button. If you need to rerun the tester, you may reset it with the reset button or by pressing Ctrl+r.

If the tester fails, then at least one transition or output in your state machine is wrong. Neither the tester nor a TA will tell you which one is wrong. If it passes, then your state machine is 100% correct.

**RESTRICTIONS**

- You may only use BASIC GATES (multi input gates are fine), A single register, splitters, wires, tunnels, clock, input pins, and output pins. Anything else is just silly.
- Your state machine must implement all 5 states.
- Your state machine must be implemented in the provided subcircuit.
- Your state machine must be connected in the main circuit that is given to you (it already should be, but if you move any of the pins in the subcircuit then it may mess up the tester)

## Evaluation

You will be graded based on how close you are to the state diagram! And following directions, so make sure you follow them all.

## Deliverables

1) timed_lab_2a.circ

Note if your file is not named this you will lose points! You like free points right? Then name the file correctly.

**You may submit only the files listed above. We will not accept any internet links we want the files above and only these files!**

**Check over your submission after you submit it. If you submit the wrong file and leave the lab I will not be happy and we will grade what you submit so please check over what you submitted after you submit it!**

# Have fun and good luck!