ALC5672

Multi-Channel Audio Hub/CODEC with Gen.3 Voice DSP and SounzReal™ Post-Processing for Mobile Devices

Datasheet

Rev. 0.71

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek ALC5672 Audio Codec IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.4	2012/12/28	First full version release
0.5	2013/1/28	Modify register typos Modify order information
0.6	2013/3/4	Modify clock rate supporting for TDM interface Modify application circuit
0.7	2013/3/21	Modify typos Modify application circuit
0.71	2013/4/15	Modify IN2P pin share function

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1. General Description

The ALC5672 is a high performance, low power, dual I^2S interface audio CODEC with embedded low power/high performance Voice DSP. Dual I^2S interface can connect to different devices and let the ALC5672 to be an Audio Hub. Each device can pass through the Audio Hub and then perform as input or output application. Asynchronous Sample Rate Converter (ASRC) provides independent and asynchronous connections to different processors, such as an application processor, baseband processor or wireless transceiver(BT).

Stereo Class-D speaker amplifiers provide 1.5W per channel into 8Ω or 2.8W per channel into 4Ω with a 5V supply, with high THD+N performance, excellent PSRR and low EMI. A mono differential earpiece amplifier is also provided, providing output from any DAC or Analog-in.

The ALC5672 features an ultra low power cap-free headphone amplifier. It consumes only less than 5mW power during playback, providing mobile system longer battery life under headphone listening mode.

The integrated multi-section DRC(Dynamic Range Controller) and 14-band parametric Equalizer provide further digital sound processing capability of audio playback paths. The multi-section DRC in ALC5672 continuously monitors the DAC output level. When the power level is low, it increases the input signal gain to make it sound louder. At the same time, if a peaking signal is detected, it autonomously reduces the applied gain to avoid hard clipping. It ensures the maximum/consistent signal amplitude without producing audio clipping and speaker damage. The 14-band parametric Equalizer contains each channel has 7 independent filters with programmable gain, center frequency and bandwidth to tailor the frequency characteristics of embedded speaker system according to user preferences.

For microphone recording, the DRC in ALC5672 can be used as AGC(Auto Gain Controller) to maintain a constant recording volume. Besides, a dynamic wind reduction filter is built in on recording path. The filter can detect the level of wind noise and on/off dynamically to keep the recording quality. The ALC5672 also integrates independent 6-band parametric Equalizer for recording path. They can use to compensate microphone device frequency response.

ALC5672 embedded a low power, high performance voice processor. The 120MIPS voice processor provides advanced voice processing features, including exceptional noise suppression, echo cancellation and advanced Beam-Forming under low power consumption. The voice processor is optimized for advanced voice processing to improve voice quality for voice communication and recording in noisy environments.

SounzReal™ post-processing technology is configurable to provide better listening experience. BassBack EXP™ bring LFE(low frequency effect) to listeners without subwoofer needed. TruTreble EXP™ adds processed harmonic tones at high frequency, bringing more melody and details for music listening.

2. Features

- Digital Super Wideband Voice DSP
  - Voice communication enhancement (AEC, NS…etc.)
  - Advanced Beam-Forming (Voice Tracking)
  - Stereo Far field pick-up recording (48KHz Sample Rate)
- SounzReal™ post-processing
  - TruTreble
  - BassBack
- Parametric 14 bands equalizer (EQ) – each 7 bands for L/R playback path independent control
- Parametric 6 bands equalizer (EQ) for recording path
- Advanced DRC with multi-section compressor function for playback/recording path
- Sound detection wake up technology
- Wind noise reduction filter
- One 24bit/8kHz ~ 192kHz I2S/PCM/TDM digital interface
- One 24bit/8kHz ~ 192kHz I2S/PCM digital interface
- Digital asynchronous sampling rate converter (ASRC) function
- I2C control interface
- 3 stereo digital microphone interfaces
- 4 Digital-to-Analog Converter with 100dBA SNR
- 2 Analog-to-Digital Converter with 94dBA SNR
- 2 single-ended analog microphone inputs with pre-amplifiers (+20/24/30/35/40/44/50/52dB) and low noise microphone bias
  - MIC input to ADC with 50dB Boost, SNR>66dBA, THD+N<-65dB
  - Headset microphone and ground auto switch
- Stereo line input
  - -85dB THD+N (with 0dB gain path)
  - 94dBA SNR (with 0dB gain path)
- Stereo single-ended/mono differential line output
  - -85dB THD+N (with 0dB gain path, 10k ohm loading)
  - 100dBA SNR (with 0dB gain path, 10k ohm loading)
- Stereo BTL (Bridge-Tied Load) Class-D amplifier
  - 700mW/CH (AVDD=1.8V, SPKVDD=3.6V, THD+N <= 1%, 8Ohm)
  - 600mW/CH (AVDD=1.8V, SPKVDD=3.6V, THD+N <= 0.1%, 8Ohm)

- 2.8W/CH (AVDD=1.8V, SPKVDD=5.0V, THD+N <= 10%, 4Ohm)
- 2.3W/CH (AVDD=1.8V, SPKVDD=5.0V, THD+N <= 1%, 4Ohm)

- Speaker auto ratio gain and SPKVDD detection
  - Auto ratio gain for AVDD=1.8V with SPKVDD=3.3V ~ 5.0V
  - 4-bit PVDD Detection for SPKVDD=3.3V ~ 5.0V with AVDD=1.8V
- Stereo headphone output and without DC blocking capacitors
  - 20mW/CH (AVDD=CPVDD=1.8V, THD+N <= -80dB, 16Ohm)
- Ultra-Low-Power for headphone playback
  - Standby power consumption <=5mW (AVDD=DBVDD=CPVDD=1.8V, DCVDD=1.2V, 32Ohm, With I2S clock input)
  - Playback power consumption <=10mW (AVDD=DBVDD=CPVDD=1.8V, DCVDD=1.2V, 32Ohm, With I2S clock input, Po=1mW)
- Multiple audio jack insert detection function
- Headset in-line multi-function control support
- Power management and enhanced power saving
- Internal PLL can receive wide range clock input
- Two adjustable MICBIAS (0.9*MICVDD or 0.75*MICVDD)
- QFN-48 (6mmx6mm) package

3. Power/Ground Operation Conditions

POWER TYPE	DECSRIPTION	MIN	TYP	MAX	UNIT
DBVDD	Digital I/O Power	1.71	1.8	3.6	V
DCVDD	Digital Core Power	1.1	1.2	1.4	V
AVDD	Analog Power	1.71	1.8	1.9	V
MICVDD	Microphone Bias Power	3.0	3.3	3.6	V
CPVDD	Charge Pump Power	1.71	1.8	1.9	V
SPKVDDL/R	Speaker Power	3.0	5.0	5.5	V
DGND, AGND, CPGND, SPKGND,	Ground		0		V

4. System Application

- Smart Phones
- Tablet

5. Function Block and Mixer Path

5.1. Function Block

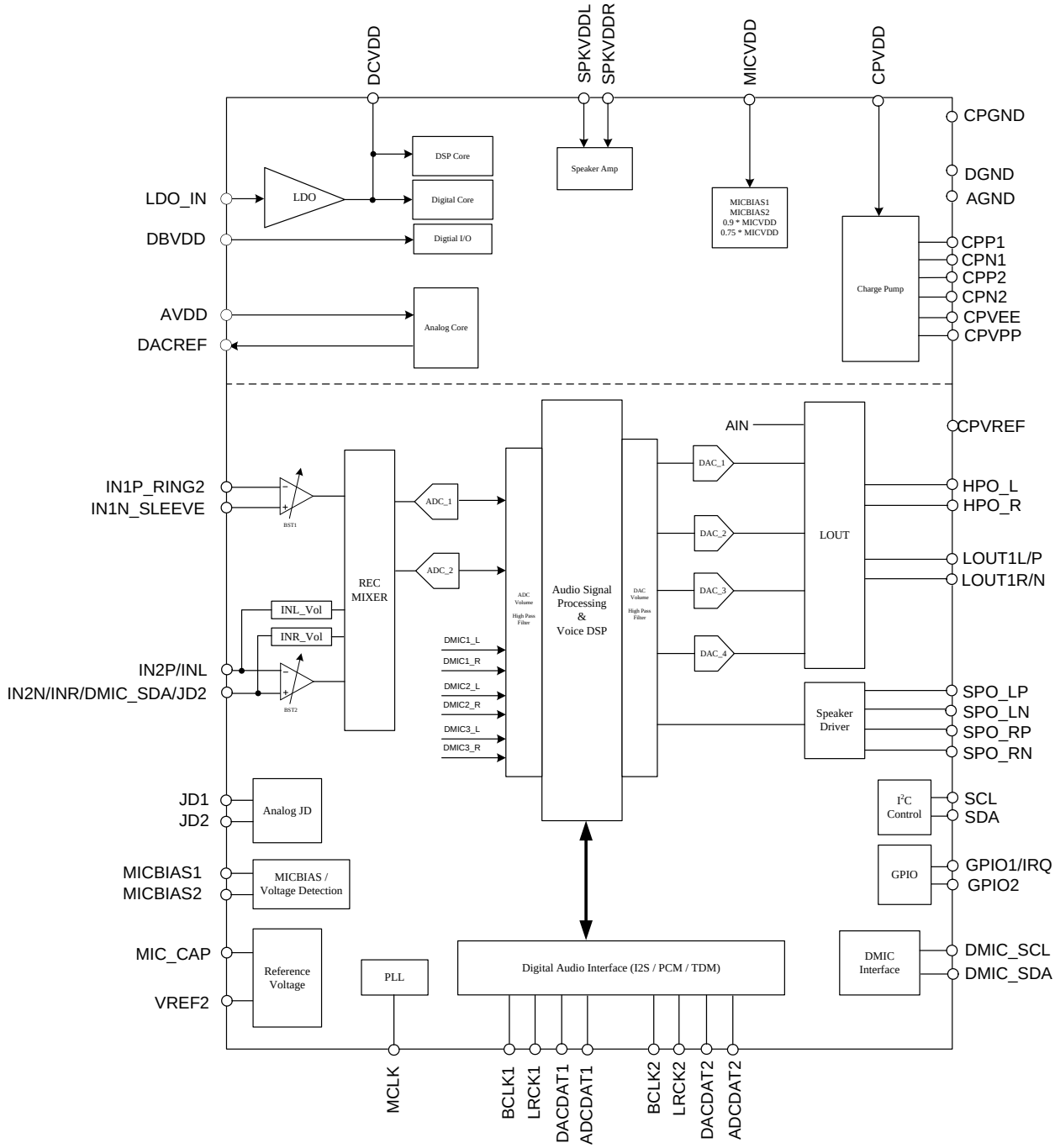


Figure 1. Block Diagram

5.2. Audio Mixer Path

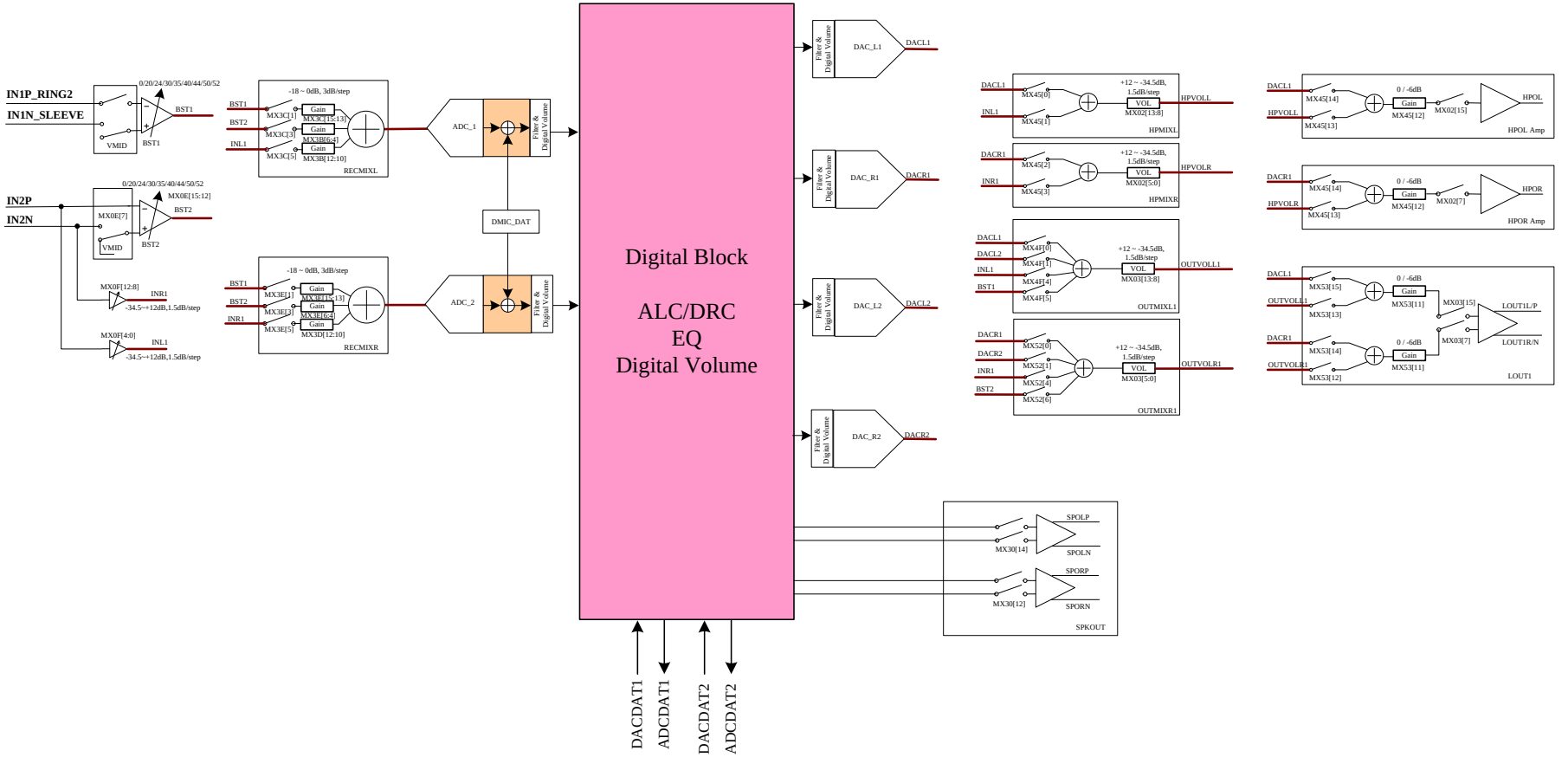


Figure 2. Audio Mixer Path

5.3. Digital Mixer Path

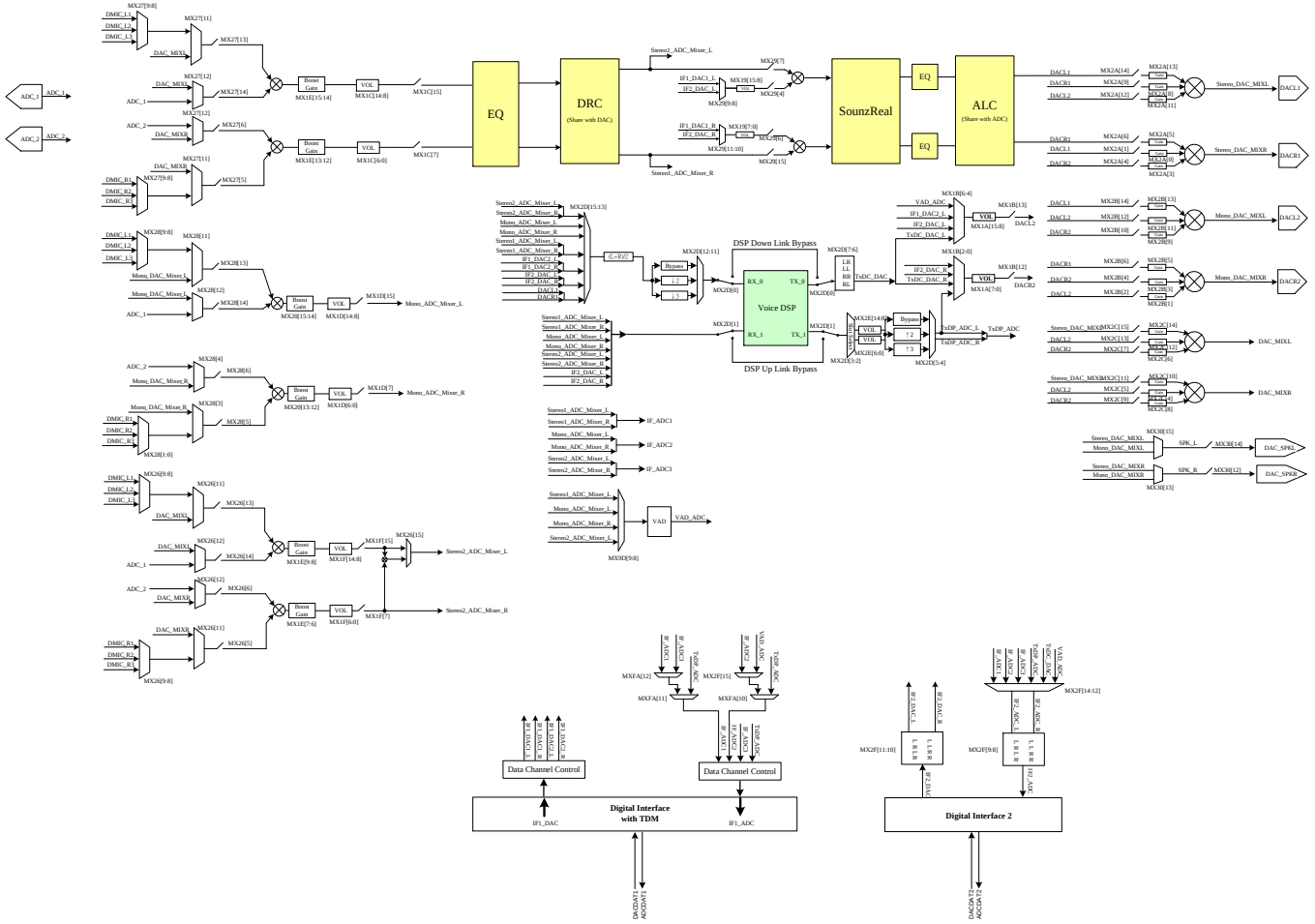


Figure 3. Digital Mixer Path

6. Pin Assignments

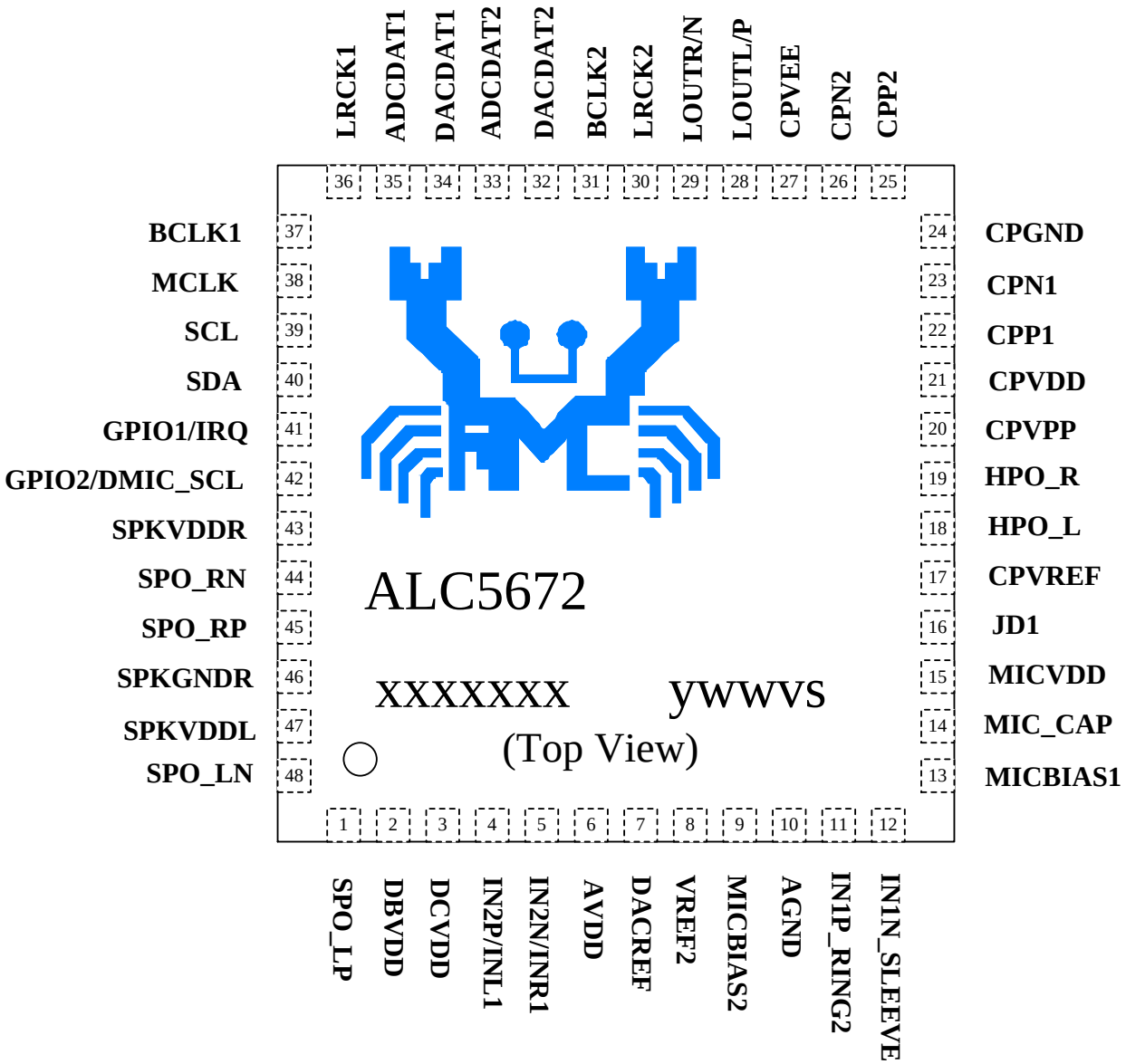


Figure 4. Pin Assignments

7. Pin Descriptions

7.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
DACDAT1	I	34	First I2S interface serial data input	Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
ADCDAT1	O	35	First I2S interface serial data output	V_{OL}=0.1*DBVDD, V_{OH}=0.9*DBVDD
BCLK1	I/O	37	First I2S interface serial bit clock	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
LRCK1	I/O	36	First I2S interface synchronous signal	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
DACDAT2	I	32	Multi-function pin: Second I2S interface serial data input GPIO function Digital microphone 3 data input	Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
ADCDAT2	O	33	Multi-function pin: Second I2S interface serial data output GPIO function Digital microphone 1 data input	V_{OL}=0.1*DBVDD, V_{OH}=0.9*DBVDD
BCLK2	I/O	31	Multi-function pin: Second I2S interface serial bit clock GPIO function	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
LRCK2	I/O	30	Multi-function pin: Second I2S interface synchronous signal GPIO function	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
SDA	I/O	40	I2C interface serial data	Open drain structure
SCL	I	39	I2C interface clock input	Schmitt trigger
MCLK	I	38	I2S interface master clock input	Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
GPIO1/IRQ	I/O	41	Multi-function pin: General purpose input and output Interrupt output	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger
GPIO2/ DMIC_SCL	I/O	42	Multi-function pin: General purpose input and output Digital microphone clock output	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger
				Total: 13 Pins

7.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
LOUTR/N	O	29	Line output type Single-ended output, right channel Differential output, negative channel	Analog output
LOUTL/P	O	28	Line output type Single-ended output, left channel Differential output, positive channel	Analog output
IN2P/INL1	I	4	Multi-function pin: Positive differential input for analog microphone 2 Left channel line input Digital microphone 1 data input	Analog input Digital input
IN2N/INR1	I	5	Multi-function pin: Negative differential input for analog microphone 2 Right channel line input Second jack detection pin Digital microphone 2 data input	Analog input JD threshold: V_{IL} = 0.2V, V_{IH} = 1.2V Digital input
IN1P_RING2	I	11	Positive differential input for analog microphone 1	Analog input
IN1N_SLEEVE	I	12	Negative differential input for analog microphone 1	Analog input
JD1	I	16	Analog jack detection function	Multi-level jack detection pin JD threshold: V_{t1} = 1.485V V_{t2} = 1.925V V_{t3} = 2.7V
HPO_R	O	19	Headphone amplifier output Right channel	Analog output
HPO_L	O	18	Headphone amplifier output Left channel	Analog output
SPO_LP	O	1	Speaker amplifier output Left differential positive output channel	Analog output
SPO_LN	O	48	Speaker amplifier output Left differential negative output channel	Analog output
SPO_RP	O	45	Speaker amplifier output Right differential positive output channel	Analog output

Name	Type	Pin	Description	Characteristic Definition
SPO_RN	O	44	Speaker amplifier output Right differential negative output channel	Analog output
				Total: 13 Pins

7.3. Filter/Reference

Table 3. Filter/Reference

Name	Type	Pin	Description	Characteristic Definition
MICBIAS1	O	13	Bias voltage output for microphone	Programmable analog DC output
MIC_CAP	-	14	Microphone input reference voltage	4.7uF capacitor to analog ground
MICBIAS2	O	9	Bias voltage output for microphone	Programmable analog DC output
VREF2	O	8	Second internal reference voltage	4.7uF capacitor to analog ground
DACREF	O	7	DAC/ADC reference voltage	4.7uF capacitor to analog ground
CPVREF	-	17	Headphone reference ground	Headphone ground
CPN1	-	23	First charge pump bucket capacitor	2.2uf capacitor to CPP1
CPP1	-	22	First charge pump bucket capacitor	2.2uf capacitor to CPN1
CPN2	-	26	Second charge pump bucket capacitor	2.2uf capacitor to CPP2
CPP2	-	25	Second charge pump bucket capacitor	2.2uf capacitor to CPN2
				Total: 10 Pins

7.4. Power/Ground

Table 4. Power/Ground

Name	Type	Pin	Description	Characteristic Definition
MICVDD	P	15	Analog power for MICBIAS	3.0V ~ 3.3V (Default 3.3V is recommended)
AVDD	P	6	Analog power	1.71V ~ 1.9V (Default 1.8V is recommended)
AGND	P	10	Analog ground	
CPVDD	P	21	Analog power for headphone charge pump	1.71V ~ 1.9V (Default 1.8V is recommended)
CPGND	P	24	Analog ground for headphone charge pump	
CPVEE	P	27	Charge pump negative voltage output	2.2uf capacitor to analog ground
CPVPP	P	20	Charge pump positive voltage output	2.2uf capacitor to analog ground
DCVDD	P	3	Digital power for digital core. (Internal LDO generated)	1.1V~1.3V
DBVDD	P	2	Digital power for digital I/O buffer	1.71V~3.3V (Default 1.8V is recommended)
SPKVDDL	P	47	Speaker AMP power for left channel	3.0V~5.0V (Default 5V or 3.3V)
SPKVDDR	P	43	Speaker AMP power for right channel	3.0V~5.0V (Default 5V or 3.3V)
SPKGND/ DGND	P	46, 49*	Speaker AMP ground Digital ground	Exposed-Pad
				Total: 12 Pins

8. Function Description

8.1. System Connection

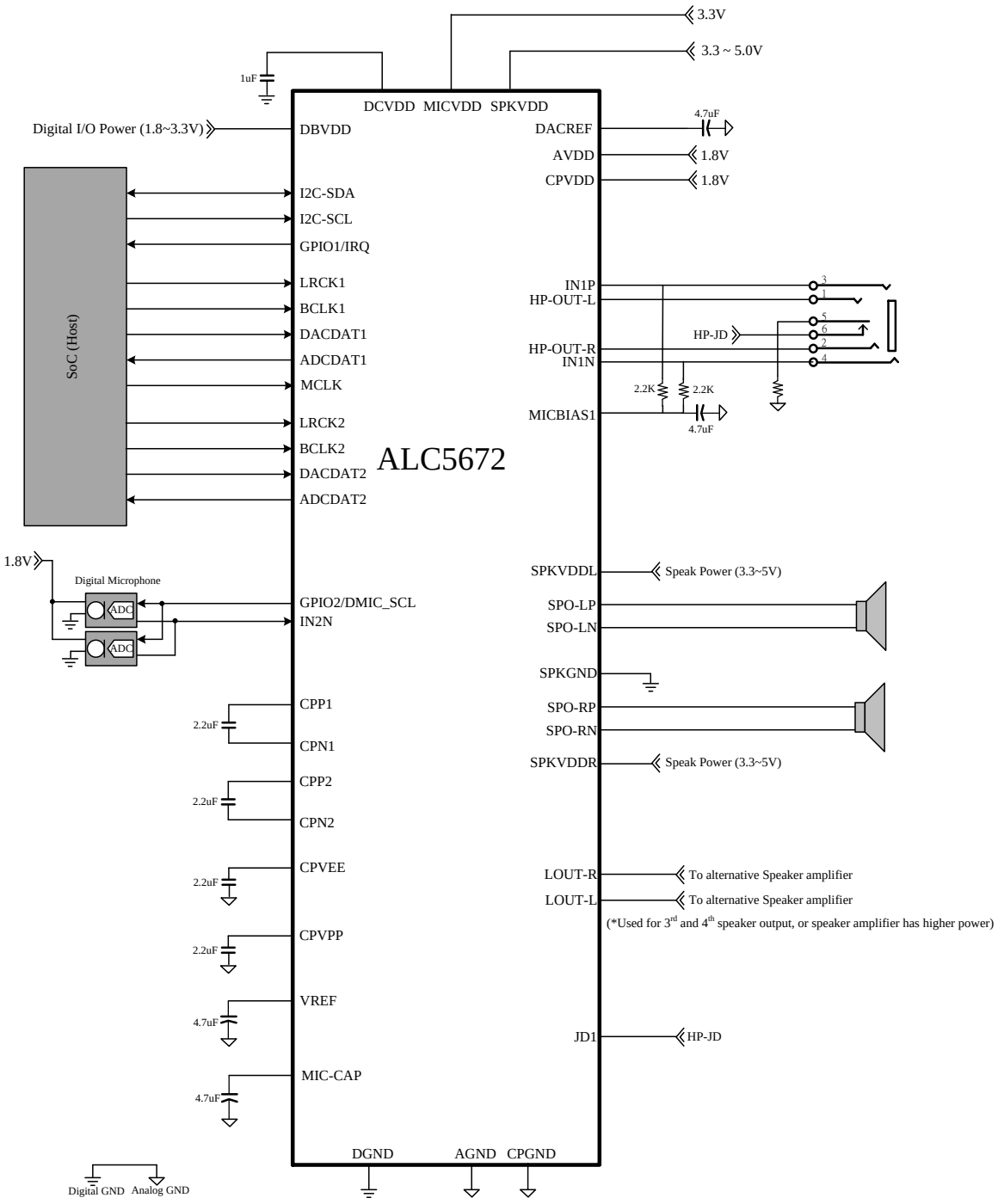


Figure 5. General System Connection

8.2. Power

There are different power types in ALC5672. DBVDD is for digital I/O power, DCVDD is for digital core power, AVDD is for analog power, CPVDD is for charge pump power, MICVDD is for MICBIAS power and SPKVDD is for speaker amplifier power.

The power supplier limit condition are DBVDD >= DCVDD and SPKVDD >= MICVDD > AVDD = CPVDD, AVDD > DCVDD, and for the best performance, our design setting is shown as below.

Table 5. Power Supply for Best Performance

Power	DBVDD	DCVDD	AVDD	CPVDD	MICVDD	SPKVDD
Setting	1.8V	1.2V	1.8V	1.8V	3.3V	5.0V

*1.2V DCVDD was generated by internal LDO.

To prevent all power down leakage, there are three settings for power supply. At these conditions, the leakage will be smaller. First setting is to power on all power pin. Second setting is to only power on SPKVDD and others are removed. The detail setting is shown as following table.

Table 6. Power Supply Condition for Power Down Leakage

Power	DBVDD	DCVDD	AVDD	CPVDD	MICVDD	SPKVDD
Setting-1	Supplied	Supplied	Supplied	Supplied	Supplied	Supplied
Setting-2	N/A	N/A	N/A	N/A	N/A	Supplied
Setting-3	Supplied	Supplied	Supplied	Supplied	Supplied	N/A

8.3. Power Supply On/Off Sequence

To prevent pop noise and make sure function work normally, following power on and off sequence are recommended.

Case1: For SPKVDD is from battery:

Power On Sequence:

1. SPKVDD power supply on
2. DBVDD/AVDD/CPVDD=1.8V power supply on
3. DBVDD power supply on (This step is required if DBVDD is supplied higher than 1.8V)
4. MICVDD power supply on
5. Initialize voice DSP of ALC5672.
6. Power down voice DSP of ALC5672.
7. S/W driver start to initial codec settings.

Power Off Sequence:

1. Power down voice DSP of ALC5672.
2. Power down all Codec function (Write 0x0000'h to register MX-00'h)
3. MICVDD power supply off
4. DBVDD power supply off (This step is required if DBVDD is supplied higher than 1.8V)
5. DBVDD/AVDD/CPVDD=1.8V power supply off
6. SPKVDD power supply off

Case2: For SPKVDD is from PMIC:

Power On Sequence:

1. SPKVDD power supply on
2. DBVDD/AVDD/CPVDD=1.8V power supply on
3. DBVDD power supply on (This step is required if DBVDD is supplied higher than 1.8V)
4. MICVDD power supply on
5. Initialize voice DSP of ALC5672.
6. Power down voice DSP of ALC5672.
7. S/W driver start to initial codec settings.

Power Off Sequence:

1. Power down voice DSP of ALC5672.
2. Power down all Codec function (Write 0x0000'h to register MX-00'h)
3. MICVDD power supply off
4. DBVDD power supply off (This step is required if DBVDD is supplied higher than 1.8V)
5. DBVDD/AVDD/CPVDD=1.8V power supply off
6. SPKVDD power supply off

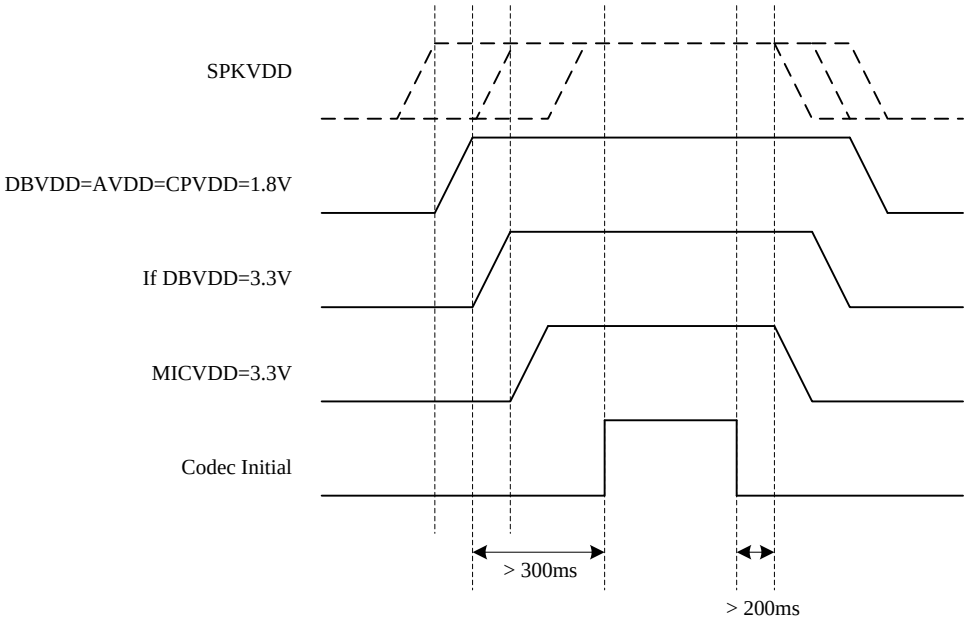


Figure 6. Power On/Off Timing

8.4. Reset

There are 2 types of reset operation: power on reset (POR) and register reset.

Table 7. Reset Operation

Reset Type	Trigger Condition	CODEC Response
POR	Monitor digital power supply voltage reach V_{POR}	Reset all hardware logic and all registers to default values.
Register Reset	Write MX-00h	Reset all registers to default values except some specify control registers and logic.

8.4.1. Power-On Reset (POR)

When powered on, DCVDD passes through the V_{POR} band of the ALC5672 (V_{POR_ON} ~V_{POR_OFF}). A power on reset (POR) will generate an internal reset signal (POR reset 'LOW') to reset the whole chip.

Table 8. Power-On Reset Voltage

Symbol	Min	Typical	Max	Unit
V_{POR_ON}	-	0.9	-	V
V_{POR_OFF}	-	0.5	-	V

Note:
1.V_{POR_OFF} must be below V_{POR_ON}
2. $T^oC = 25^oC$
3. When DCVDD is supplied 1.2V

8.4.2. Software Reset

When MX-00h is wrote, all registers become to default value.

8.5. Clocking

The system clock of ALC5672 can be selected from MCLK or PLL. MCLK is always provided externally while the reference clock of PLL can be selected from MCLK, BCLK1/2. The driver should arrange the clock of each block and setup each divider.

The Clk_sys_i2s1=256*Fs provides clocks into stereo DAC/ADC filter that can be selected from MCLK or PLL. Refer to Figure 5. Audio SYSCLK
The Clk_sys_i2s2=256*Fs provides clocks into mono DAC/ADC filter that can be selected from MCLK, PLL, refer to Figure 5. Audio SYSCLK

When enable ASRC (Asynchronous Sample Rate Converter) function, the clock sources from MCLK and BCLK1 (or BCLK2) are allowed to be asynchronous. The Realtek ASRC technology can ensure data accuracy and keep audio performance under clock source asynchronous.

When ALC5672 at master mode, the clock source from MCLK will be divided and be sent to external device. The ratio of BCLK and LRCK can set by register – MX-73.

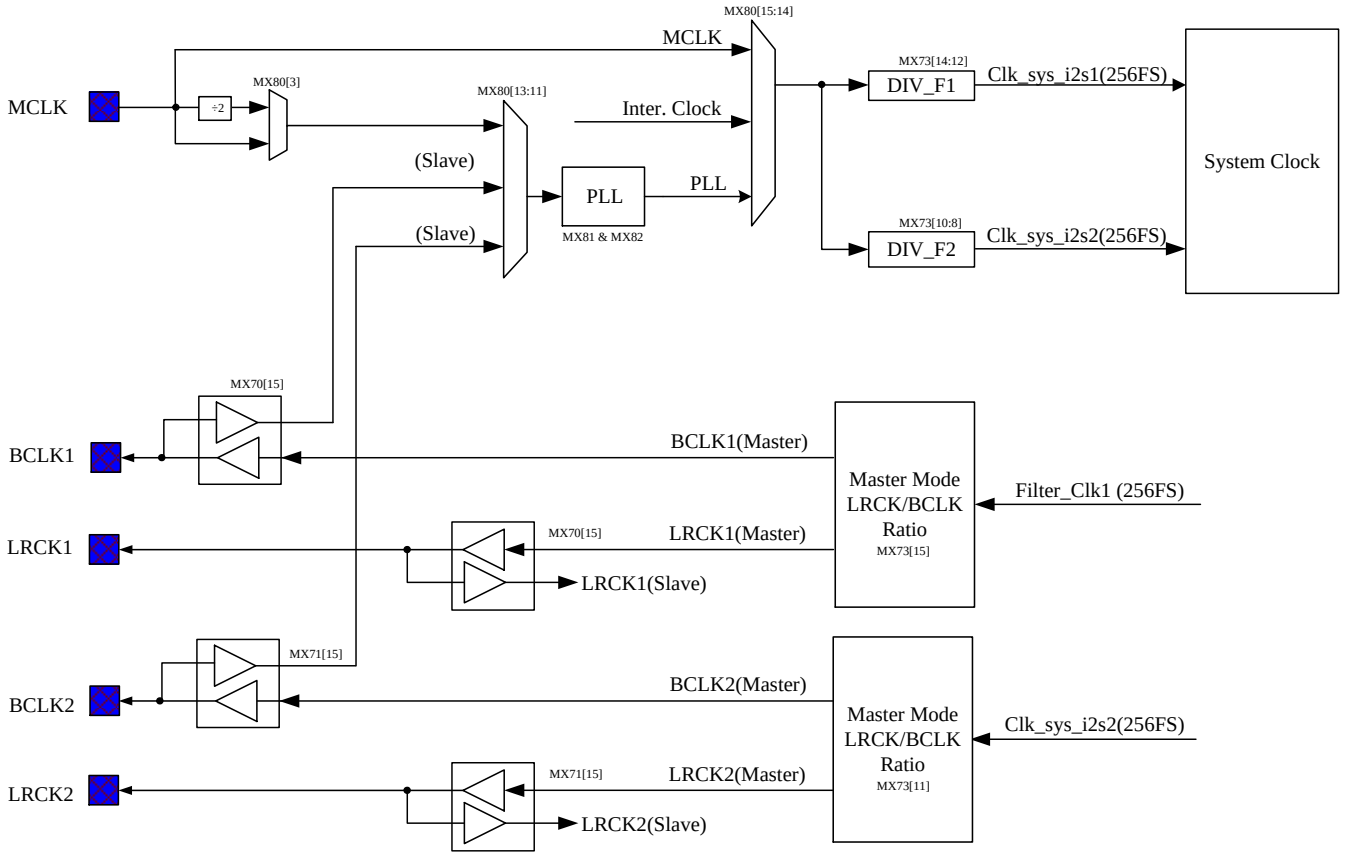


Figure 6. Audio Clock Tree

8.5.1. Phase-Locked Loop

A Phase-Locked Loop (PLL) is used to provide a flexible input clock from 2.048MHz to 40MHz. The source of the PLL can be set to MCLK, BCLK1 or BCLK2 by setting register.

The S/W driver can set up the PLL to output a frequency to match the requirement of system clock.

The PLL transmit formula as below:

F_{OUT} = (MCLK * (N+2)) / ((M+2) * (K+2)) {Typical K=2}

Table 9. Clock Setting Table for 48K (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	66	7	98.222	2	24.555
3.6864	78	1	98.304	2	24.576
2.048	94	0	98.304	2	24.576
4.096	70	1	98.304	2	24.576
12	80	8	98.4	2	24.6
15.36	81	11	98.068	2	24.517
16	78	11	98.462	2	24.615
19.2	80	14	98.4	2	24.6
19.68	78	14	98.4	2	24.6
24	39	8	98.4	2	24.6

Table 10. Clock Setting Table for 44.1K (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	68	8	91	2	22.75
3.6864	72	1	90.931	2	22.733
2.048	86	0	90.112	2	22.528
4.096	64	1	90.112	2	22.528
12	66	7	90.667	2	22.667
15.36	63	9	90.764	2	22.691
16	66	10	90.667	2	22.667
19.2	64	12	90.514	2	22.629
19.68	67	13	90.528	2	22.632
24	62	15	90.352	2	22.588

8.5.2. I²C and Two I²S/PCM Interface

The ALC5672 supports I²C for the digital control interface, and has two I²S/PCM for digital data interface. These two I²S/PCM audio digital interfaces are used to send data to 4 DACs or to receive data from a stereo ADC. These two I²S/PCM audio digital interfaces can be configured to Master mode or Slave mode.

Master Mode

Under master mode, BCLK and LRCK are configured as output. If I2S SYSCLK is selected from MCLK source, sel_sysclk1 (MX-80[15:14]) should set as 00'b. If selected from PLL output, sel_sysclk1 should set as 01'b. PLL's source is suggested to provide frequency from 2.048MHz to 40MHz. The driver should set each divider (MX-77 & MX-73) to arrange the clock distribution. Refer to Figure5. Audio Clock Tree, for details.

Table 11. The relative of SYSCLK/BCLK/LRCK

Register Settings	MCLK	BCLK	LRCK
MX-77[11:10]=00'b, I2S1 MX-73[11]=0'b, I2S2	256*FS=12.288MHz	32*FS=1.536MHz	FS=48KHz
MX-77[11:10]=11'b, I2S1 MX-73[11]=1'b, I2S2	256*FS=12.288MHz	64*FS=3.072MHz	FS=48KHz
MX-77[11:10]=00'b, I2S1 MX-73[11]=0'b, I2S2	256*FS=11.2896MHz	32*FS=1.4112MHz	FS=44.1KHz
MX-77[11:10]=11'b, I2S1 MX-73[11]=1'b, I2S2	256*FS=11.2896MHz	64*FS=2.8224MHz	FS=44.1KHz

Example for master mode:
Target format:
Sample Rate: 48 KHz
Channel Length: 32 bits
LRCK=48KHz
BCLK=3.072MHz (64 * 48KHz)

MCLK clock request:
MCLK=12.288MHz (256 * 48 KHz)

Register settings:
Set MX-FA[0] to "1" // For MCLK input clock getting control
Set MX-61[15] to "1" // Enable I2S-1
Set MX-70[15] to "0" // Enable Master mode
Set MX-77[11:10] to "11" // Select 64*FS for BCLK in master mode
Set MX-73[14:12] to "000" // Select I2S-1 pre-divider

Slave Mode

Under slave mode BCLK and LRCK are configured as input. The SYSCLK can be input from MCLK, and BCLK can be synchronous or asynchronous to MCLK. If the SYSCLK is selected from BCLK, the internal PLL should generate 256*FS as internal system clock. And the driver should set each divider to arrange the clock distribution. Refer to Figure5. Audio Clock Tree, for details.

If an asynchronous MCLK input for BCLK and LRCK, you can turn on ASRC function for this case. As Figure 6 shown, the MCLK is from external oscillator that clock is no relation (or asynchronous) with SOC and BT or 3G BaseBand. For the connection for SOC and BT can connect directly to Codec and let Codec as slave mode and SOC/BT as master mode.

For the clock requirement of MCLK must large than 512*FS as SYSCLK that FS is sample rate. If the MCLK is smaller than 512*FS, that can use internal PLL to generate higher than 512*FS clock.

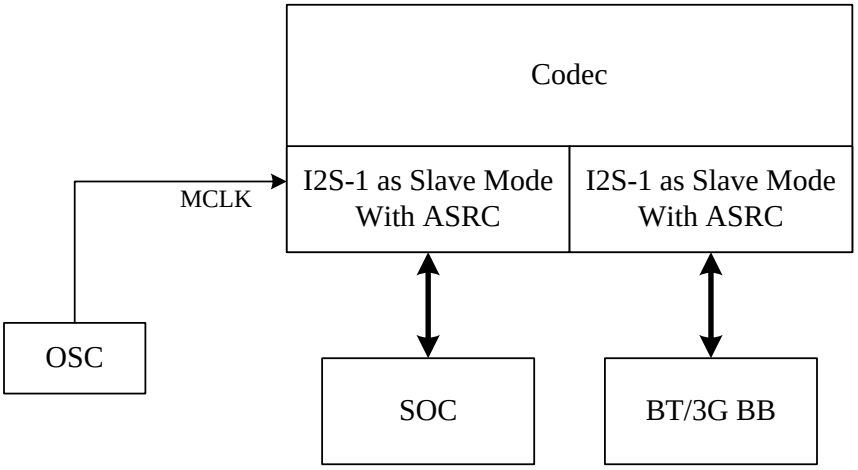


Figure 7. System Connection for ASRC Function

Table 12. Register Settings for ASRC Function on Slave Mode

Condition: **Codec as Slave Mode** **MCLK = 12MHz** **Frame Rate = 64*FS** **Target Sample Rate (FS) = 48KHz**		
Item	**Register Settings**	**Note**
PLL Settings	MX-81 = 0x1481'h MX-82 = 0x5000'h	PLL settings to generate 512*FS (24.576MHz) for SYSCLK
I2S-1 to DAC1	MX-83 = 0x8000'h MX-84 = 0x0020'h	For DAC1 playback ASRC settings
I2S-2 to DAC2	MX-83 = 0x1800'h MX-84 = 0xC000'h	For DAC2 playback ASRC settings
AMIC to Stereo ADC Filter to I2S-1	MX-83 = 0x8000'h MX-84 = 0x0800'h	For AMIC to Stereo ADC Filter record ASRC settings
AMIC to Mono ADC Filter to I2S-2	MX-83 = 0x1800'h MX-84 = 0x3800'h	For AMIC to Mono ADC Filter record ASRC settings
DMIC1 to Stereo ADC Filter to I2S-1	MX-83 = 0x8200'h	For DMIC1 to Stereo ADC Filter record ASRC settings
DMIC2 to Mono ADC Filter to I2S-2	MX-83 = 0x1900'h MX-84 = 0x3800'h	For DMIC2 to Mono ADC Filter record ASRC settings

8.6. Digital Data Interface

8.6.1. Two I²S/PCM Interface

The two I2S/PCM interface can be configured as master mode or slave mode. Four audio data formats are supported:

- PCM mode
- Left justified mode
- I²S mode
- TDM mode (Max. BCLK Rate is 12.288MHz)

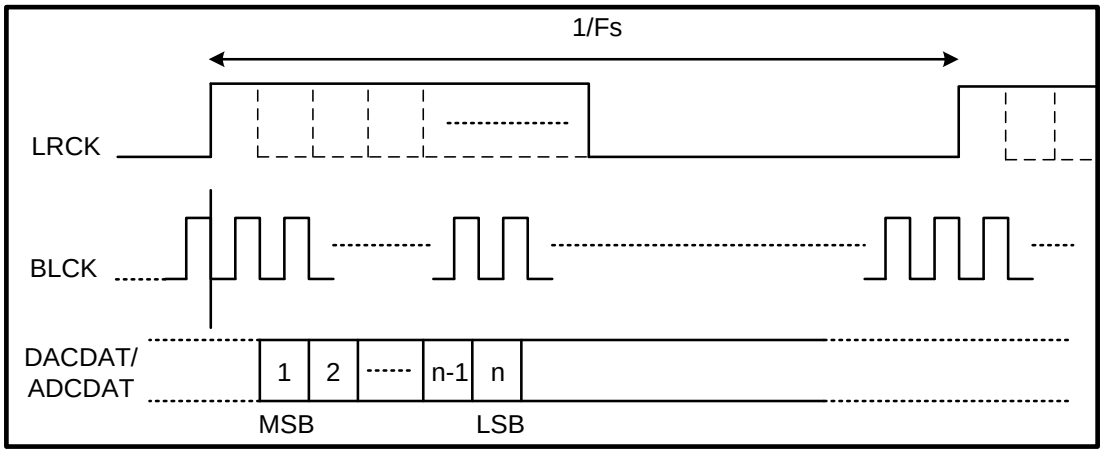


Figure 8. PCM MONO Data Mode A Format (BCLK POLARITY=0)

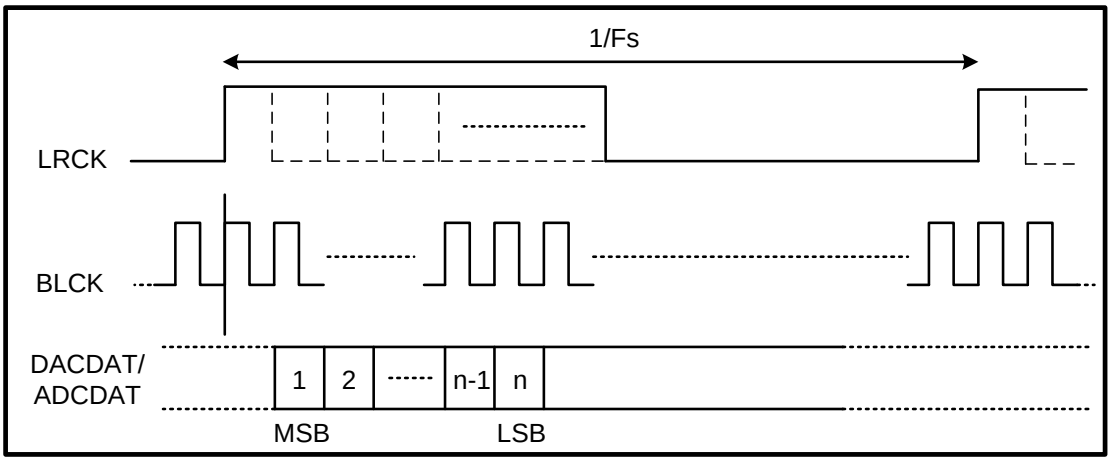


Figure 9. PCM MONO Data Mode A Format (BCLK POLARITY=1)

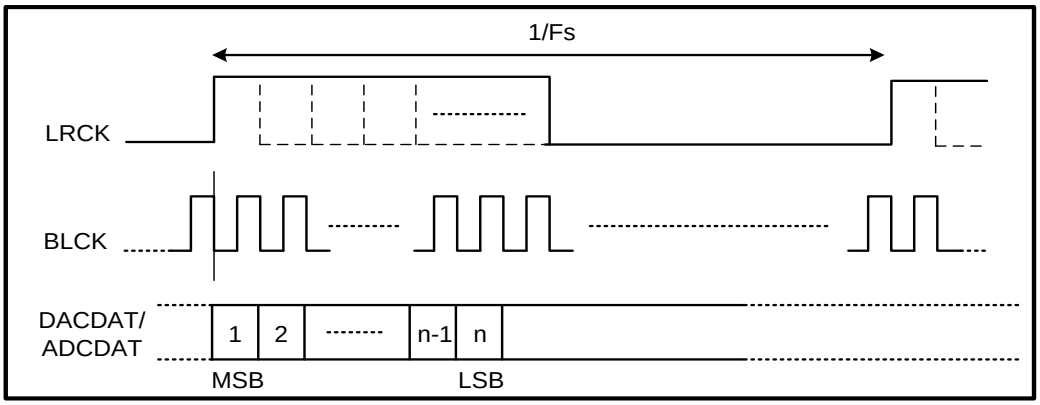


Figure 10. PCM MONO Data Mode B Format (BCLK POLARITY=0)

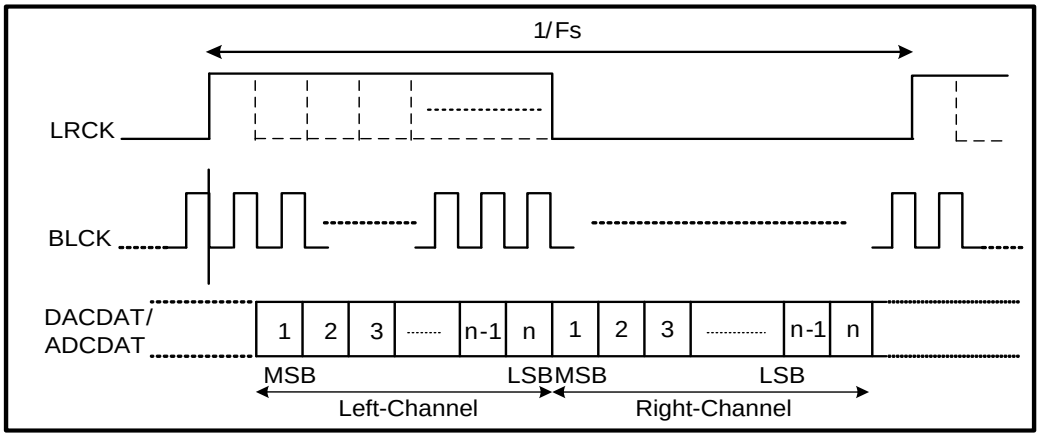


Figure 11. PCM Stereo Data Mode A Format (BCLK POLARITY=0)

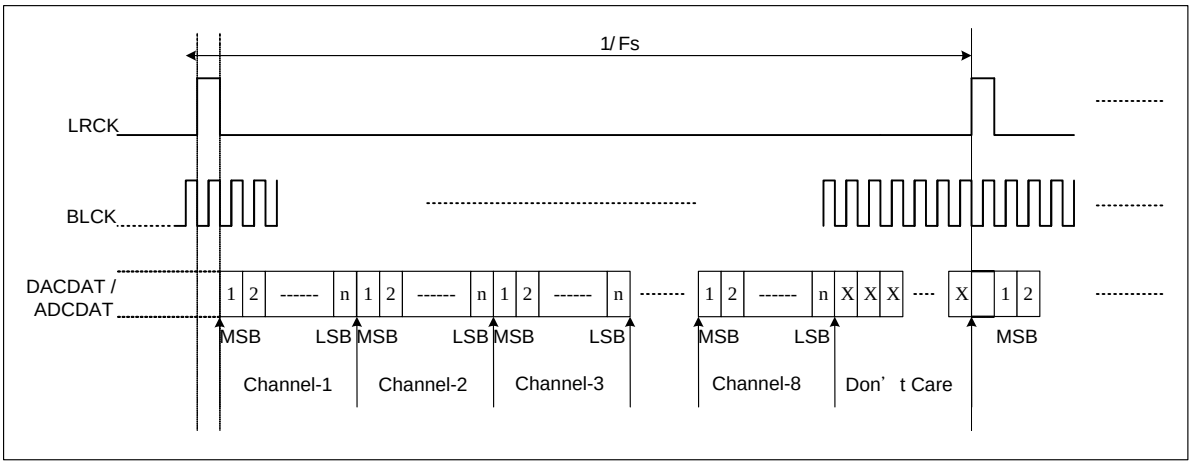


Figure 12. PCM TDM Data Mode A Format (BCLK POLARITY=0)

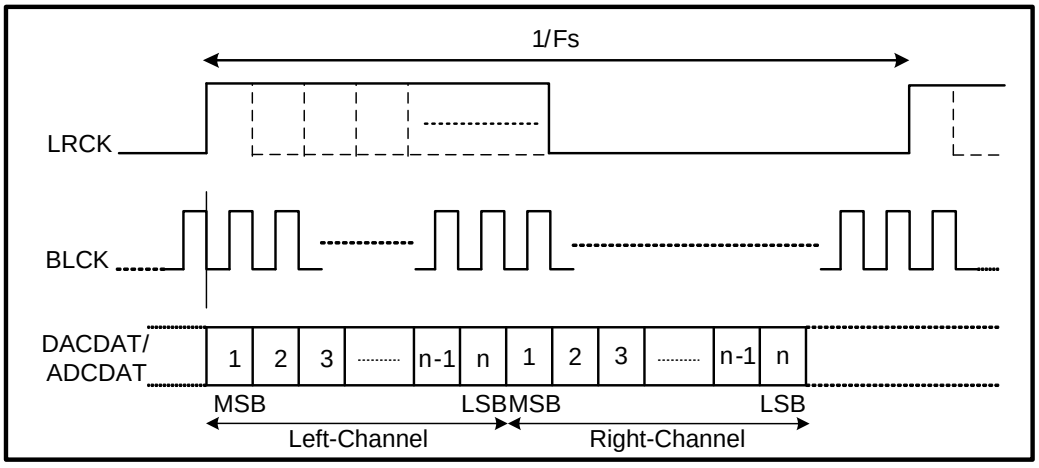


Figure 13. PCM Stereo Data Mode B Format (BCLK POLARITY=0)

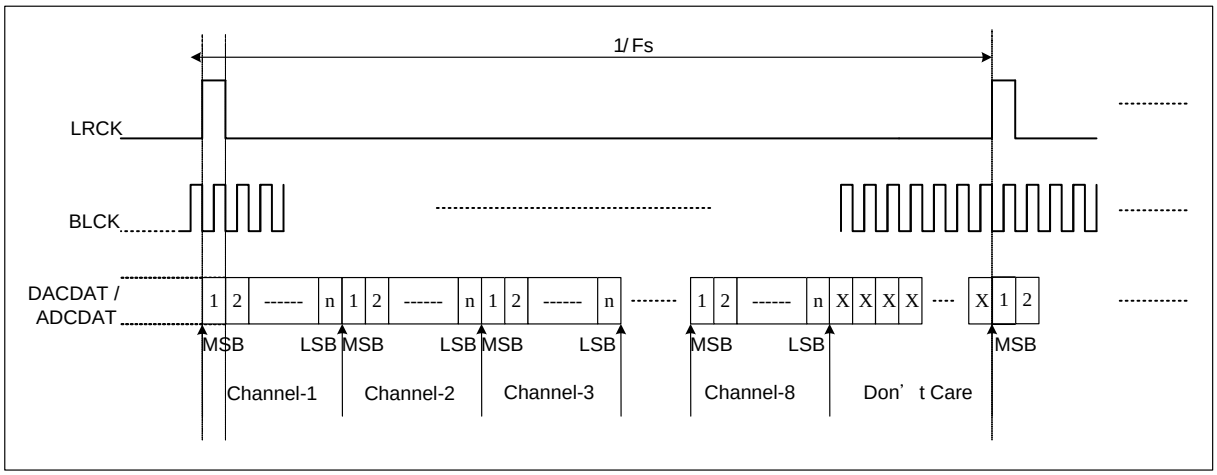


Figure 14. PCM TDM Data Mode B Format (BCLK POLARITY=0)

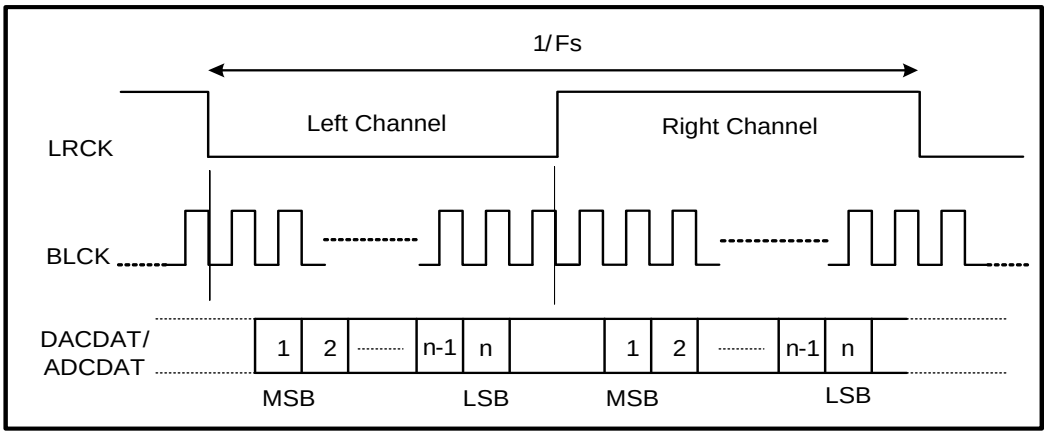


Figure 15. I²S Data Format (BCLK POLARITY=0)

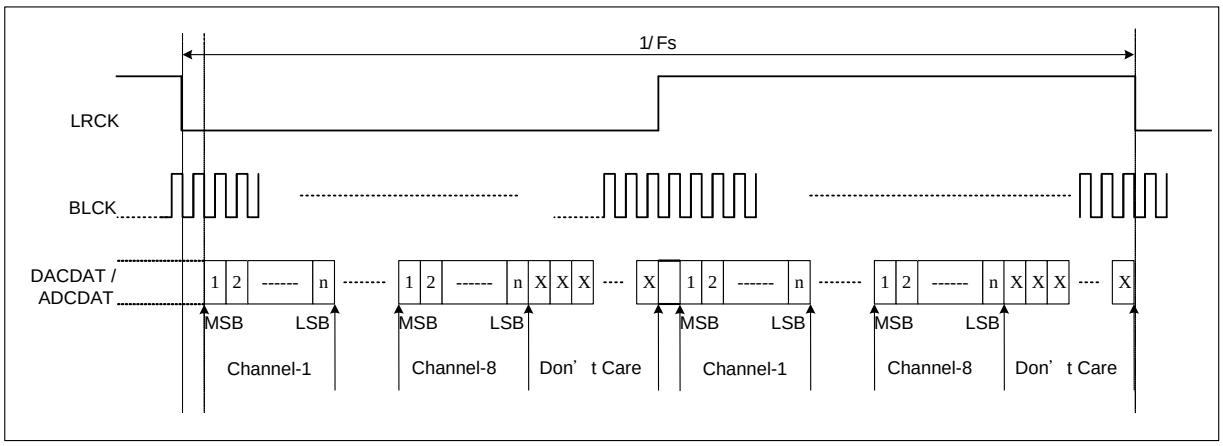


Figure 16. I²S TDM Data Format (BCLK POLARITY=0)

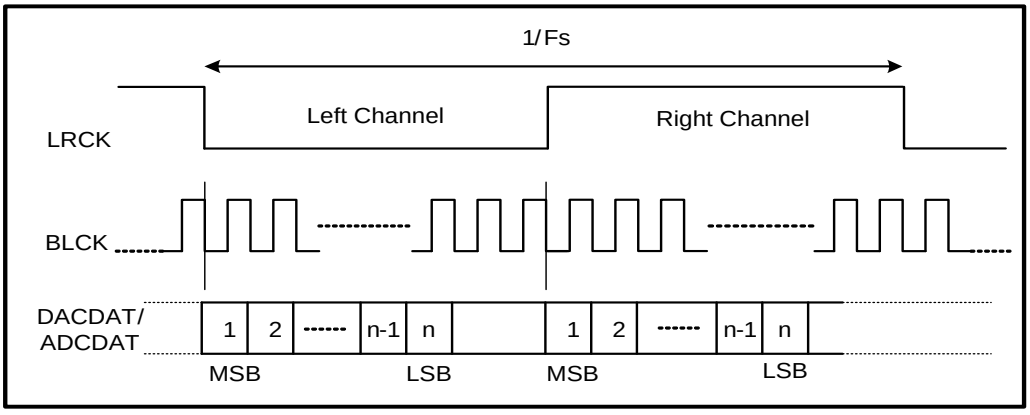


Figure 17. Left-Justified Data Format (BCLK POLARITY=0)

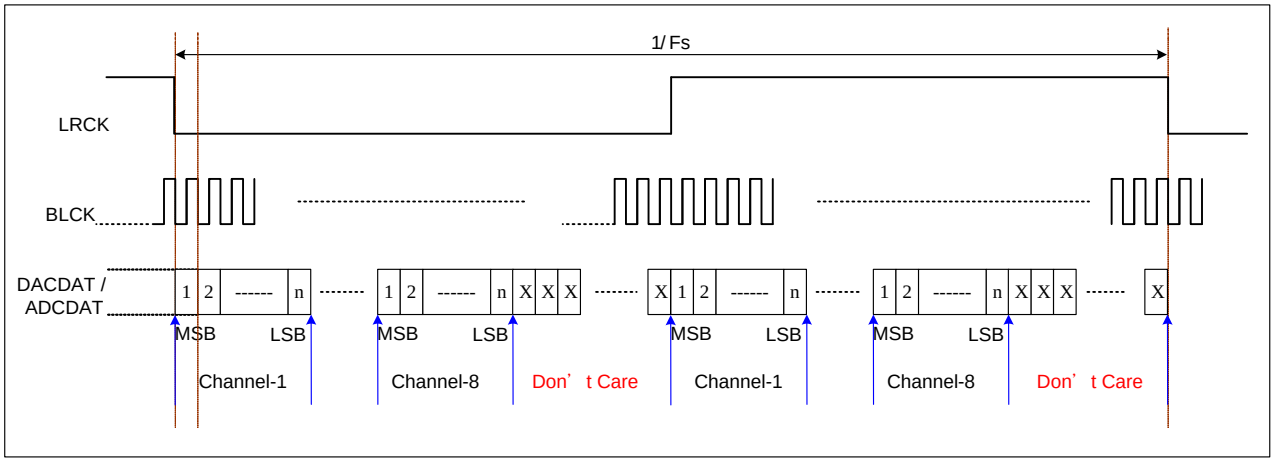


Figure 18. Left-Justified TDM Data Format (BCLK POLARITY=0)

8.7. Audio Data Path

The ALC5672 provides 4-channel analog DACs for playback and 2-channel analog ADCs for recording.

8.7.1. 2 Analog ADCs with 6-Channel Record Path

There are two analog ADCs and with up to 6-channel recording path. You can use two analog microphones pass to analog ADCs and four digital microphones to reach 6-channel recording. Or use three digital microphone interfaces to reach 6-channel recording. These 6-channel data can through I2S1 interface for recording. The I2S1 interface supports TDM interface and up to 8-CH, 24-bit/CH recording.

The full scale input of analog ADC is around 0.55Vrms. In order to save power, the left and right analog ADC can be powered down separately by setting pow_adc_l (MX-61[2]) and pow_adc_r (MX-61[1]). And the volume control of the stereo ADC is also separately controlled by ad_gain_l (MX-1C[14:8]) and ad_gain_r (MX-1C[6:0]).

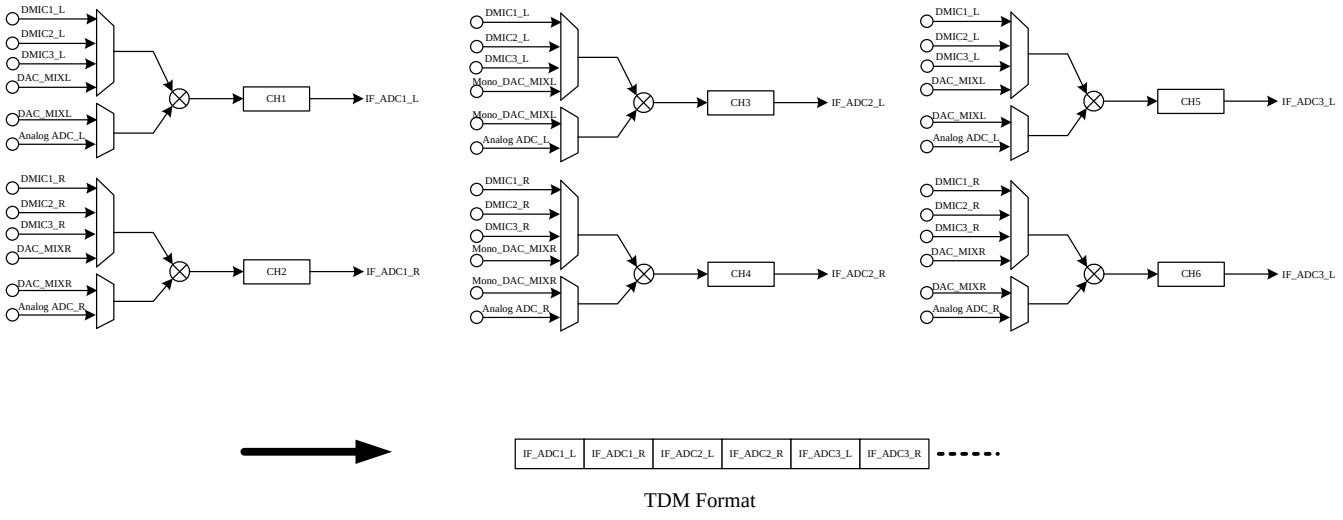


Figure 19. 4-Channel Recording Path

8.7.2. 4 DACs with 4-Channel Playback Path

There are four analog DACs and with up to 4-channel playback path. Two I2S interfaces provide four channels data to analog DACs. And analog DAC can output audio signal to speaker output, headphone output or line output. That also can use I2S1 TDM interface to support 4-channel playback.

The full scale output of analog DAC is around 1Vrms at line output port. In order to save power, the four analog DACs can be powered down separately by setting pow_dac_l_1 (MX-61[12]), pow_dac_r_1 (MX-61[11]), pow_dac_l_2 (MX-61[7]) and pow_dac_r_2 (MX-61[6]). And the digital volume control of the four DACs are also separately controlled by vol_dac1_l (MX-19[15:8]), vol_dac1_r (MX-19[7:0]), vol_mono_dacl (MX-1A[15:8] and vol_mono_dacr (MX-1A[7:0]).

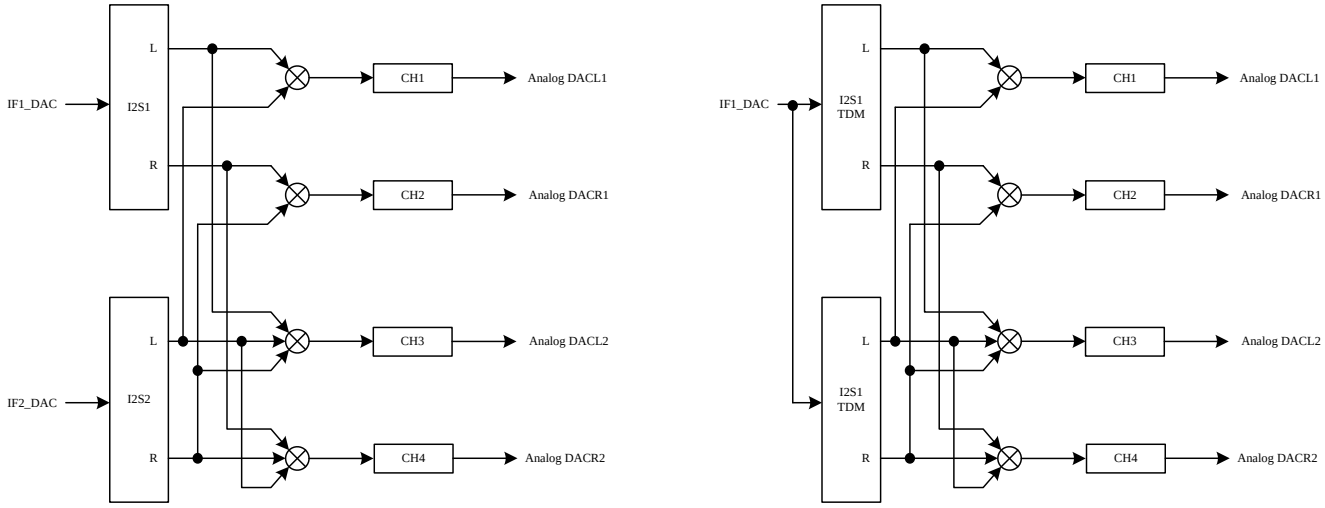


Figure 20. 4-Channel Playback Path

8.7.3. Mixers

The ALC5672 has digital and analog mixers build-in.

- **Output mixer - OUTMIXL/R**

  The stereo analog mixer can do mixing for DAC output and analog input. The mixer output is mainly for headphone output and line output. Each input path has it's mute control to the mixer block in MX-45. pow_outmixl and pow_outmixr can be used to power on/off OUTMIXL/R

- **Record mixer – RECMIXL/R**

  The stereo analog mixer can do mixing for analog input and OUTMIX output. The mixer output is for ADC input. Each input path has it's mute control to the mixer block in MX-3B ~ MX-3E. pow_recmixl and pow_recmixr can be used to power on/off RECMIXL/R.

- **HP mixer – HPMIXL/R**

  The stereo analog mixer can do mixing for headphone volume and DAC output. The mixer output directly output to external headphone device. Each input path has it's mute control to the mixer block in MX-45.

- **Digital mixer**

  There are twelve digital mixers in ALC5672. Six digital mixers are assigned for ADC recording. These six mixers can mix analog line input, analog microphone input and digital microphone input then output to I2S interface to other device. Another four digital mixers are assigned for DAC playback. These mixers can mix digital data from I2S interface or ADC data from external analog signal. The mixed data is output to analog DAC and output port to drive external device. The other two mixers are used for DA-AD processing. The incoming data from two I2S interfaces (DACDAT) uses these two mixers to do mixing and output to I2S interface (ADCDAT).

8.8. Analog Audio Input Port

The ALC5672 has two type analog input ports: microphone input and line input.

- **IN1P_RING2/IN1N_SLEEVE**

  The port is a microphone type input port. The input port only can be configured as single-ended mode. The microphone input port has its microphone bias and microphone boost. The low noise microphone bias can improve recording performance and enhance recording quality. Build-in short current detection scheme can be used for switch detection. Multi-steps microphone boost gain set by sel_bst1 (MX-0D[15:12]) is easy to use for microphone application. Pow_bst1 can be used to power down the MIC1 boost and pow_micbias1 can be used to power down the microphone bias 1.

- **IN2P/N**

  The IN2P/N is a dual type input port: microphone input and line input. Microphone input can be configured to differential input or single-ended input by MX-0E[7]. Multi-steps microphone boost gain set by sel_bst2 (MX-0E[15:12]) is easy to use for microphone application. Pow_bst2 can be used to power down the MIC2 boost.
  If as line input, it has volume control for tuning by MX-0F[12:8] and MX-0F[4:0].

8.9. Analog Audio Output Port

The ALC5672 supports three type output ports:

- **SPO_L/R_P/N**

  The speaker output of ALC5672 is a stereo BTL output with Class-D type amplifier.
  The power of speaker amplifier is an individual power pin and higher than AVDD. So the input and output of speaker amplifier has a gain ratio to enlarge or reduce the income analog signal. The ratio gain is auto tuning.
  The input source of the speaker output port can be selected from Stereo_DAC_MIXL/R or Mono_DAC_MIXL/R.

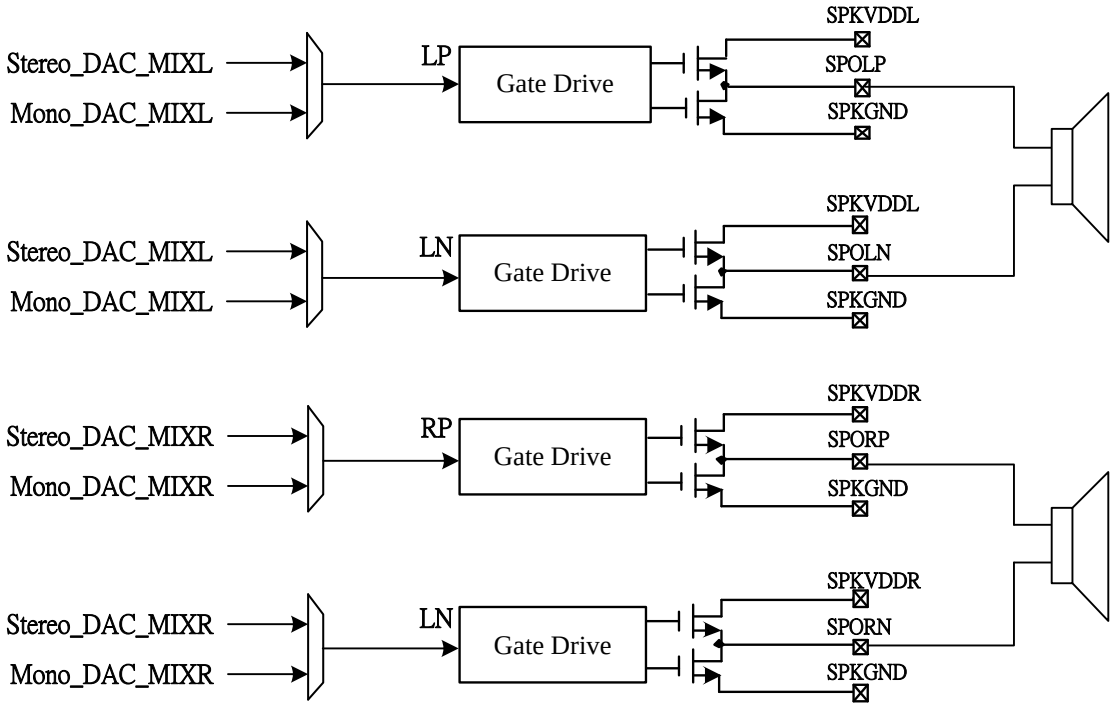


Figure 21. Stereo BTL Speaker Output

- **HPO_L/R**

  The headphone output of ALC5672 is a stereo output with cap-free type headphone amplifier. It does not need to connect external capacitor and can connect to earphone device directly. The headphone output source can mix from output mixer (HPMIX) and DAC by setting MX-45. The front stage of headphone output has volume control and gain control. The volume range is from +12dB to -46.5dB with 1.5dB/step by MX-02.
  En_l_hp and en_r_hp (MX-63[7/6]) can be used to power on/off Headphone Amplifier, and pow_hpo_voll and pow_hpo_volr (MX-66[11/10]) can be used to power on/off headphone volume control. In addition, pow_pump_hp (MX-8E[3]) can be used to power on/off charge pump circuit for Headphone Amplifier.

- **Line_OUT_L/R**

  The output type is line type output. The output is a stereo single ended output or mono differential. The input can be selected from OUTMIX or DAC output by setting MX-53[15:12]. The front stage of LOUT output has gain control for attenuation. The gain control is 0dB or -6dB by MX-53[11].

8.10. Multi-Function Pins

There are eight multi-function pins in ALC5672. For different functions of each pin are controlled by register. You need to set the right register settings for each multi-function pins by your application.

- **GPIO1/IRQ – Pin 41**

The pin default is GPIO function. It can change to IRQ output, write MX-C0[15] to 1'b will switch to IRQ function.

- **GPIO2/DMIC_SCL – Pin 42**

The pin default is GPIO function. It can change to DMIC clock output, write MX-C0[14] to 1'b will switch to DMIC clock output function.

- **IN2P/INL/DMIC1_DAT – Pin 4**

The pin can as analog microphone positive input or as line input. If as analog microphone input function needs to power on the power – MX-64[13] & MX64[4]. If as analog input function needs to power on the power – MX-66[9] & MX66[8].

Digital microphone input function:
1. Power down analog microphone input and line input.
2. Mute IN2 to each analog mixer - (RECMIXLR/OUTMIXLR/HPMIXLR).
3. Change IN2P pin share function, set MX-75[1:0] to 01'b.
4. Turn on digital microphone function – MX-75[14] = 1'b

- **IN2N/INR/DMIC2_DAT/JD2 – Pin 5**

There are four functions share this pin. For each function switching shows below:

Analog microphone input function, power on MX-64[13] & MX-64[4] and power off other functions.

Analog line input function, power on MX-66[9] & MX-66[8] and power off other functions.

Digital microphone input function:
1. Power down analog microphone input, line input and JD2 function
2. Mute IN2 to each analog mixer - (RECMIXLR/OUTMIXLR/HPMIXLR).
3. Change IN2N pin share function, set MX-75[10] to 1'b.
4. Turn on digital microphone function – MX-75[14] = 1'b

Jack detection function:
1. Power down analog microphone input, line input and digital microphone function.
2. Mute IN2 to each analog mixer - (RECMIXLR/OUTMIXLR/HPMIXLR).
3. Turn on JD2 power – MX-64[1] = 1'b

- **BCLK2/GPIO3 – Pin 31**

MX-C0[8] use to control pin31 is BCLK2 function or GPIO function.

- **LRCK2/GPIO4 – Pin 30**

MX-C0[8] use to control pin31 is LRCK2 function or GPIO function.

- **DACDAT2/GPIO5/DMIC3_SDA – Pin 32**

MX-C0[8] use to control pin31 is LRCK2 function or GPIO function.
MX-C0[7] use to control pin31 is GPIO function or DMIC_SDA3 function.

- **ADCDAT2/GPIO6/DMIC1_SDA – Pin 33**

MX-C0[8] use to control pin31 is LRCK2 function or GPIO function.
MX-C0[6] use to control pin31 is GPIO function or DMIC_SDA1 function.

8.11. DRC and AGC Function

The Dynamic Range Controller (DRC) dynamically adjusts the input signal and let the output signal achieve the target level. The ALC5672 supports playback DRC for DAC path, and the DRC can also be used as AGC(Auto Gain Controller) for ADC path. The control register is at MX-B4[15:14]. The function block is shown as below. The signal input pass through the Pre-Gain first, then DRC volume and Post-Gain then output. The Pre-Gain is use to enlarge the input signal. The DRC volume is use to attenuate the signal after detected by DRC. The Post-Gain is use to fine tune the signal after pass DRC tuning.

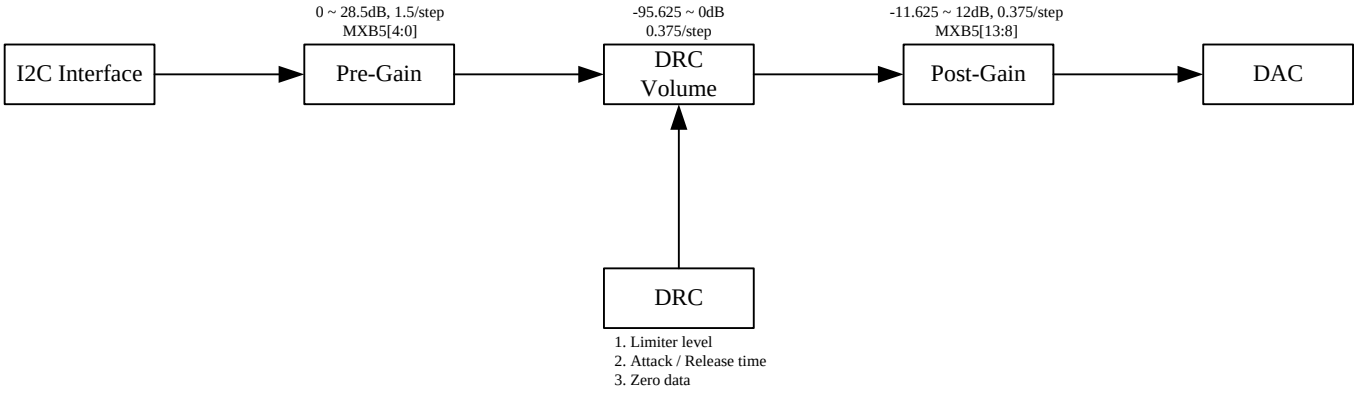


Figure 22. DAC DRC Function Block

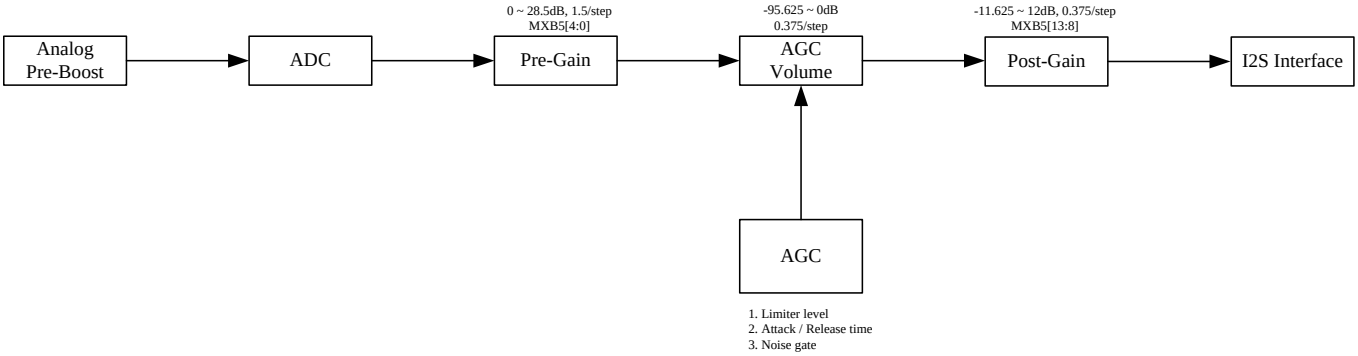


Figure 23. ADC AGC Function Block

Playback/Recording Mode:

For DAC playback or ADC recording mode, when the input signal exceeds target threshold, the signal will decrease “DRC/AGC Digital Volume” (0.375dB/step at every zero-crossing) until drop to target level then keep the digital volume. When input signal is below the target threshold, the signal will step-up “DRC/AGC Digital Volume” (0.375dB/step every zero-crossing) until return to original level. If want to return to the target level, need to set the pre-gain to achieve.

Fine tune parameters:

- Limiter Threshold: 0 ~ -46.5dB, 1.5dB/step, MX-B7[5:0]
- Attack Rate: T=(4*2^n)/sample rate, n = MX-B4[12:8]
- Recovery Rate: T=(4*2^n)/sample rate, n = MX-B4[4:0]

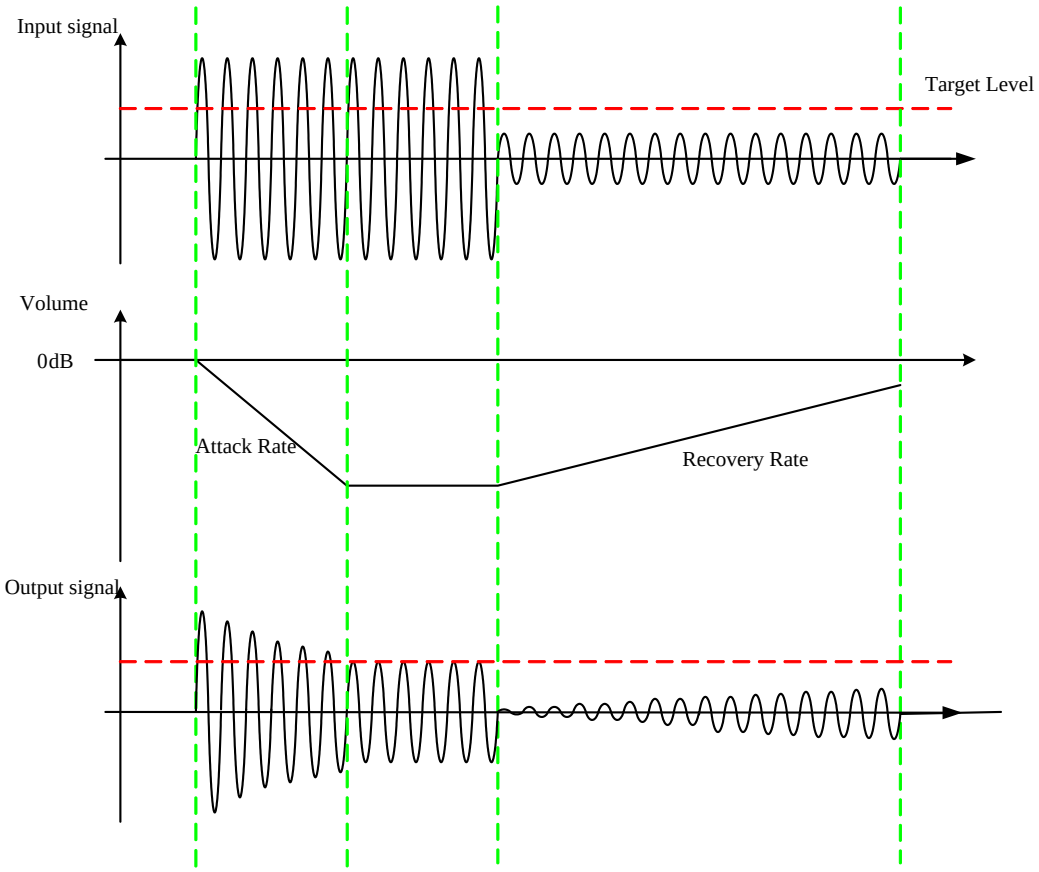


Figure 24. DRC/AGC for Playback/Recording Mode

Noise Gate Mode:

The Noise Gate Function is use to reduce the noise floor for DAC path or ADC path. When input signal is below noise gate level, the input signal will be reduced by DRC/AGC volume in order to suppress the background noise. The reducing level can be set by register. And when input signal is above noise gate, the input signal will be boosted to target level.

Fine tune parameters:

- Noise Gate Threshold: -36 ~ -82.5dB, 1.5dB/step, MX-B6[4:0]
- Noise Gate Attack Rate: T=(4*2^n)/sample rate, n = PR-06[4:0]
- Noise Gate Recovery Rate: T=(4*2^n)/sample rate, n = PR-02[12:8]
- Reducing Noise Level: 0 ~ 45dB, 3dB/step, MX-B6[15:12]

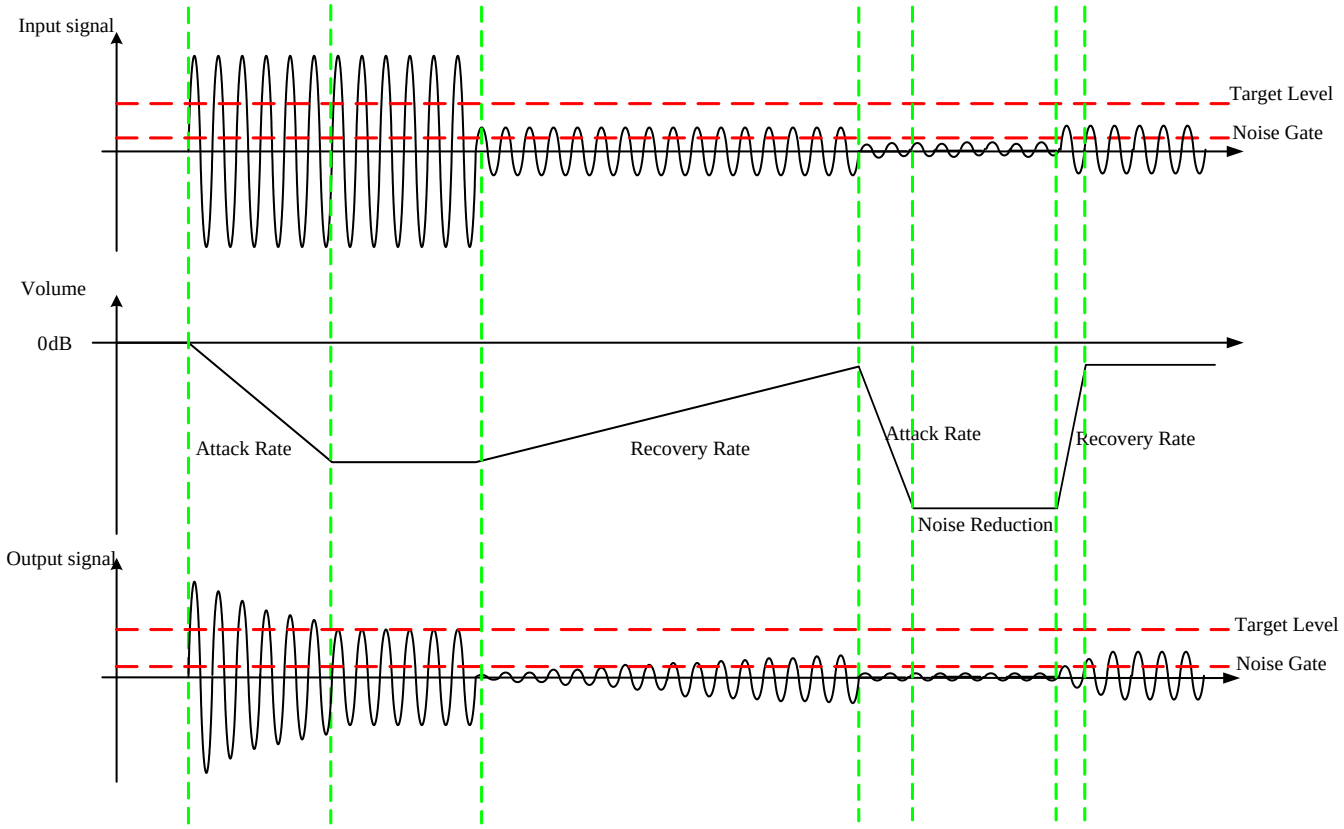


Figure 25. DRC/AGC for Noise Gate Mode

8.12. SounzReal™ Post-Processing

The Realtek's SounzReal™ post-processing is composed of:

- TruTreble
- BassBack

8.13. Equalizer Block

The equalizer block cascades 7 bands of equalizer to each channel to tailor the frequency characteristics of embedded speaker system according to user preferences and to emulate environment sound. The 7 bands equalizer includes two high pass filters, three band pass filters, one low pass filter and one biquad filter. One high pass filter cascaded in the front end is used to drop low frequency tone, The tone has a large amplitude and may damage a mini speaker. The high pass filter can be used to adjust Treble strength with gain control. One low pass filter with gain control can adjust the Bass strength. Three bands of band pass filters are used to emulate environment sounds, e.g., 'Pub', 'Live', 'Rock',… etc.. The gain, center frequency and bandwidth of each filter are all programmable. One biquad filter can switch to high-pass, low-pass or band-pass filter by register settings.

8.14. Wind Noise Reduction Filter

The wind filter is implemented by a high pass filter equalizer. The wind filter is mainly for ADC recording used. The cut-off freqnecy of wind filter is programmable and is varied accroding to different sample rate. The filter is used to remove DC offset at normal condition, and to remove wind noise at application mode.

There are three wind filters for three ADC filters:

Stereo 1 ADC Wind Filter => MX-D3 & MX-D4

Mono ADC Wind Filter => MX-EC & MX-ED

Stereo 2 ADC Wind Filter => MX-EE & MX-EF

Wind filter setting procedure (For Stereo 1 ADC Filter):

Step1: Disable wind filter – MX-D3[15]

Step2: Select filter coarse coefficient – MX-D3[14:12] and MX-D3[10:8]

Step3: Select filter fine coefficient – MX-D4[13:8] and MX-D4[5:0]

Step4: Enable wind filter – MX-D3[15]

The following table (Table 13.) is shown the Fc with sample rate selection.
For the formula of Fc calculation is also shown as:

$Fc = (Fs * \tan^{-1}(a/(2-a))) / \pi$

Where:
Sample rate = 8K/12K/16K (MX-D3[14:12] and [10:8]), $a = 2^{-6} + n * 2^{-6}$ (n is MX-D4[13:8] & MX-D4[5:0])
Sample rate = 24K/32K (MX-D3[14:12] and [10:8]), $a = 2^{-7} + n * 2^{-7}$ (n is MX-D4[13:8] & MX-D4[5:0])
Sample rate = 44.1K/48L (MX-D3[14:12] and [10:8]), $a = 2^{-8} + n * 2^{-8}$ (n is MX-D4[13:8] & MX-D4[5:0])
Sample rate = 88.2K/96L (MX-D3[14:12] and [10:8]), $a = 2^{-9} + n * 2^{-9}$ (n is MX-D4[13:8] & MX-D4[5:0])
Sample rate = 176.4K/192L (MX-D3[14:12] and [10:8]), $a = 2^{-10} + n * 2^{-10}$ (n is MX-D4[13:8] & MX-D4[5:0])

Table 13. Sample Rate with filter coefficient for Wind Filter

PR-6E[11:6]	L & R Channel Sample Rate Setting				
n	8K	16K	32K	44.1K	48K
000000’b, 0	20.0	40.1	39.9	27.4	29.8
000001’b, 1	40.4	80.8	80.2	55.0	59.9
000010’b, 2	61.1	122.2	120.7	82.7	90.0
000011’b, 3	82.1	164.2	161.6	110.5	120.3
000100’b, 4	103.4	206.9	202.8	138.4	150.6
000101’b, 5	125.1	250.2	244.4	166.4	181.1
000110’b, 6	147.1	294.3	286.2	194.5	211.7
000111’b, 7	169.5	339.0	328.4	222.7	242.5
001000’b, 8	192.2	384.4	371.0	251.1	273.3
001001’b, 9	215.2	430.5	413.8	279.5	304.3
001010’b, 10	238.7	477.4	457.0	308.1	335.4
001011’b, 11	262.4	524.9	500.5	336.8	366.6
001100’b, 12	286.6	573.2	544.4	365.6	397.9
001101’b, 13	311.1	622.3	588.6	394.5	429.4
001110’b, 14	336.0	672.1	633.2	423.5	460.9
001111’b, 15	361.3	722.6	678.1	452.6	492.6
010000’b, 16	386.9	773.9	723.3	481.9	524.5
010001’b, 17	413.0	826.0	768.9	511.2	556.4
010010’b, 18	439.4	878.9	814.9	540.7	588.5
010011’b, 19	466.2	932.5	861.2	570.3	620.7
010100’b, 20	493.5	987.0	907.8	600.0	653.0
010101’b, 21	521.1	1042.2	954.9	629.8	685.5
010110’b, 22	549.1	1098.2	1002.2	659.7	718.1
010111’b, 23	577.5	1155.0	1050.0	689.8	750.8
011000’b, 24	606.3	1212.7	1098.1	719.9	783.6
011001’b, 25	635.5	1271.1	1146.6	750.2	816.6
011010’b, 26	665.1	1330.3	1195.5	780.6	849.6
011011’b, 27	695.2	1390.4	1244.7	811.1	882.9

PR-6E[11:6]	L & R Channel Sample Rate Setting				
n	8K	16K	32K	44.1K	48K
011100’b, 28	725.6	1451.2	1294.3	841.8	916.2
011101’b, 29	756.4	1512.9	1344.3	872.5	949.7
011110’b, 30	787.6	1575.3	1394.7	903.4	983.3
011111’b, 31	819.3	1638.6	1445.4	934.4	1017.0
100000’b, 32	851.3	1702.7	1496.5	965.5	1050.9
100001’b, 33	883.7	1767.5	1548.0	996.8	1084.9
100010’b, 34	916.6	1822.3	1599.9	1028.1	1119.0
100011’b, 35	949.8	1899.6	1652.2	1059.6	1153.3
100100’b, 36	983.3	1966.7	1704.9	1091.2	1187.7
100101’b, 37	1017.3	2034.7	1757.9	1122.9	1222.2
100110’b, 38	1051.6	2103.3	1811.4	1154.8	1256.9
100111’b, 39	1086.3	2172.7	1865.2	1186.7	1291.7
101000’b, 40	1121.4	2242.9	1919.5	1218.8	1326.6
101001’b, 41	1156.8	2313.7	1974.1	1251.0	1361.7
101010’b, 42	1192.6	2385.2	2029.1	1283.4	1396.9
101011’b, 43	1228.7	2457.4	2084.6	1315.8	1432.2
101100’b, 44	1265.1	2530.2	2140.4	1348.4	1467.7
101101’b, 45	1301.8	2603.6	2196.6	1381.1	1503.3
101110’b, 46	1338.8	2677.7	2253.3	1414.0	1539.0
101111’b, 47	1376.1	2752.3	2310.3	1447.0	1574.9
110000’b, 48	1413.7	2827.5	2367.7	1480.0	1610.9
110001’b, 49	1451.5	2903.1	2425.5	1513.3	1647.1
110010’b, 50	1489.6	2979.3	2483.8	1546.6	1683.4
110011’b, 51	1528.0	3056.0	2542.4	1580.1	1719.8
110100’b, 52	1566.5	3133.1	2601.5	1613.7	1756.4
110101’b, 53	1605.3	3210.6	2660.9	1647.4	1793.1
110110’b, 54	1644.2	3288.4	2720.8	1681.3	1830.0
110111’b, 55	1683.3	3366.6	2781.0	1715.3	1867.0
111000’b, 56	1722.5	3445.1	2841.7	1749.4	1904.1
111001’b, 57	1761.9	3523.9	2902.7	1783.6	1941.4
111010’b, 58	1801.4	3602.9	2964.2	1818.0	1978.8
111011’b, 59	1841.0	3682.1	3026.1	1852.5	2016.3
111100’b, 60	1880.7	3761.4	3088.3	1887.1	2054.0
111101’b, 61	1920.4	3840.8	3151.0	1921.9	2091.9
111110’b, 62	1960.2	3920.4	3214.1	1956.8	2129.9
111111’b, 63	2000.0	4000.0	3277.5	1991.8	2168.0

8.15. I²C Control Interface

I²C is a 2-wire (SCL/SDA) half-duplex serial communication interface, supporting only slave mode. SCL is used for clock and SDA is for data. SCL clock supports up to 400KHz rate and SDA data is a open drain structure. The input has built-in spike filter and can remove less than 50ns spike at SCL and SDA.

8.15.1. Address Setting

Table 14. Address Setting (0x38h)

(MSB)			BIT				(LSB)
0	0	1	1	1	0	0	R/W

8.15.2. Complete Data Transfer

Data Transfer over I²C Control Interface

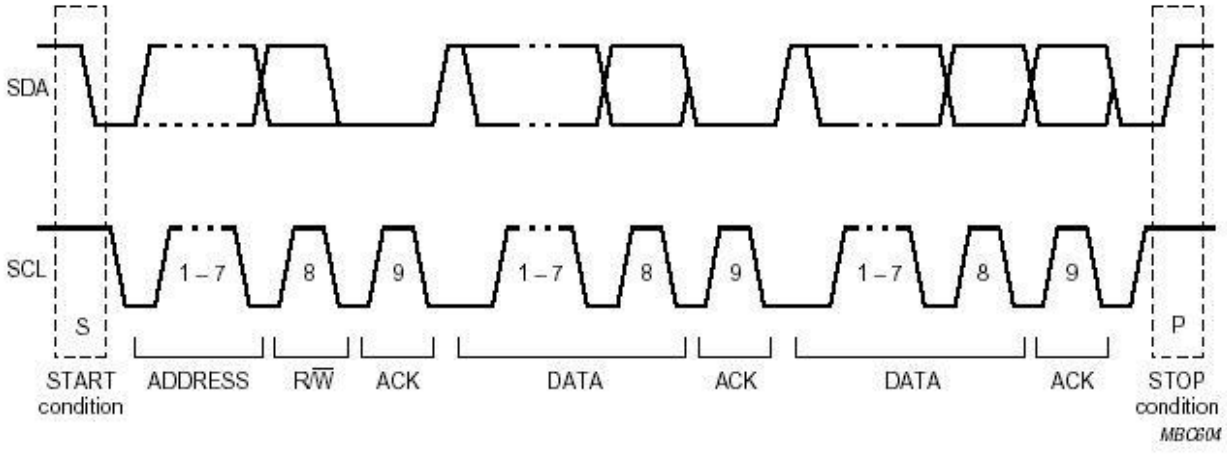
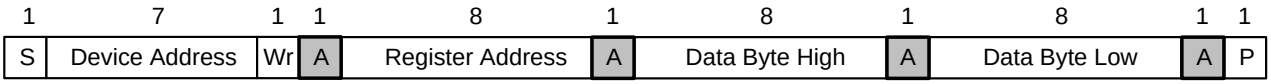


Figure 26. Data Transfer Over I²C Control Interface

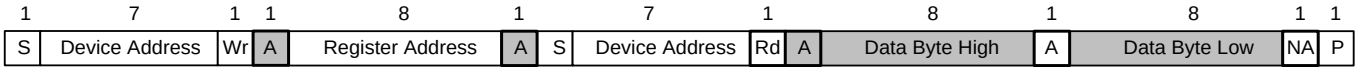
Write WORD Protocol

Table 15. Write WORD Protocol



Read WORD Protocol

Table 16. Read WORD Protocol



S: Start Condition
Slave Address: 7-bit Device Address
Wr: 0 for Write Command
Rd: 1 for Read Command
Command Code: 8-bit Register Address

A: 0 for ACK, 1 for NACK
Data Byte: 16-bit Mixer data
□: Master-to-Slave
□: Slave-to-Master

8.16. GPIO, Interrupt and Jack Detection

The ALC5672 supports six GPIOs – GPIO1/GPIO2/GPIO3/GPIO4/GPIO5/GPIO6. For GPIO function, the GPIO can be configured to input or output. For input type, the internal circuit can read pin status and report to register table. For output type, the internal circuit can drive this pin to high or low to control external device. In GPIO function, the pin polarity can be controlled by register at output type.

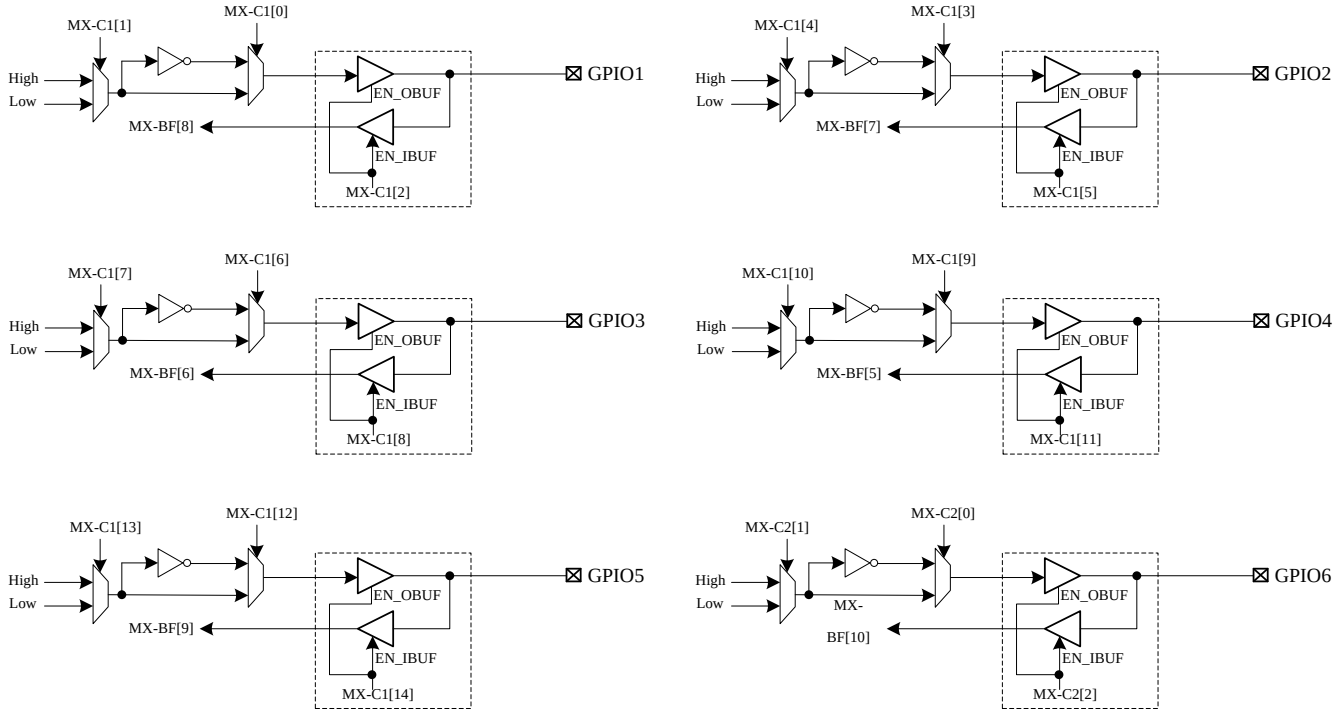
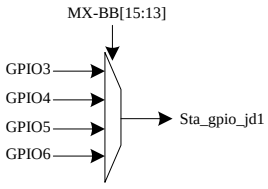


Figure 27. GPIO Function Block

For the jack detection function, there are four GPIOs (GPIO3/4/5/6) can be configured as jack detection pins and also have JD1 and JD2 can as jack detection pin. For GPIO jack detection pin source selection is controlled by MX-BB[15:13]. It's JD status is sta_gpio_jd1 – MX-BF[4]. For JD1, it can detect two ports. Which JD statuses are sta_jd1_1 – MX-BF[12] & sta_jd1_2 – MX-BF[13]. For JD2, it can detect one port. Which JD status is sta_jd2 – MX-BF[14].



For IRQ function as shown at Figure 24, the IRQ output source can be selected from JD1 Status, JD2 Status, GPIO JD Status, InLine Command Status, VAD Status and MICBIAS1 Over-Current Status. When either status is trigged, the GPIO will output a flag as interrupt signal.

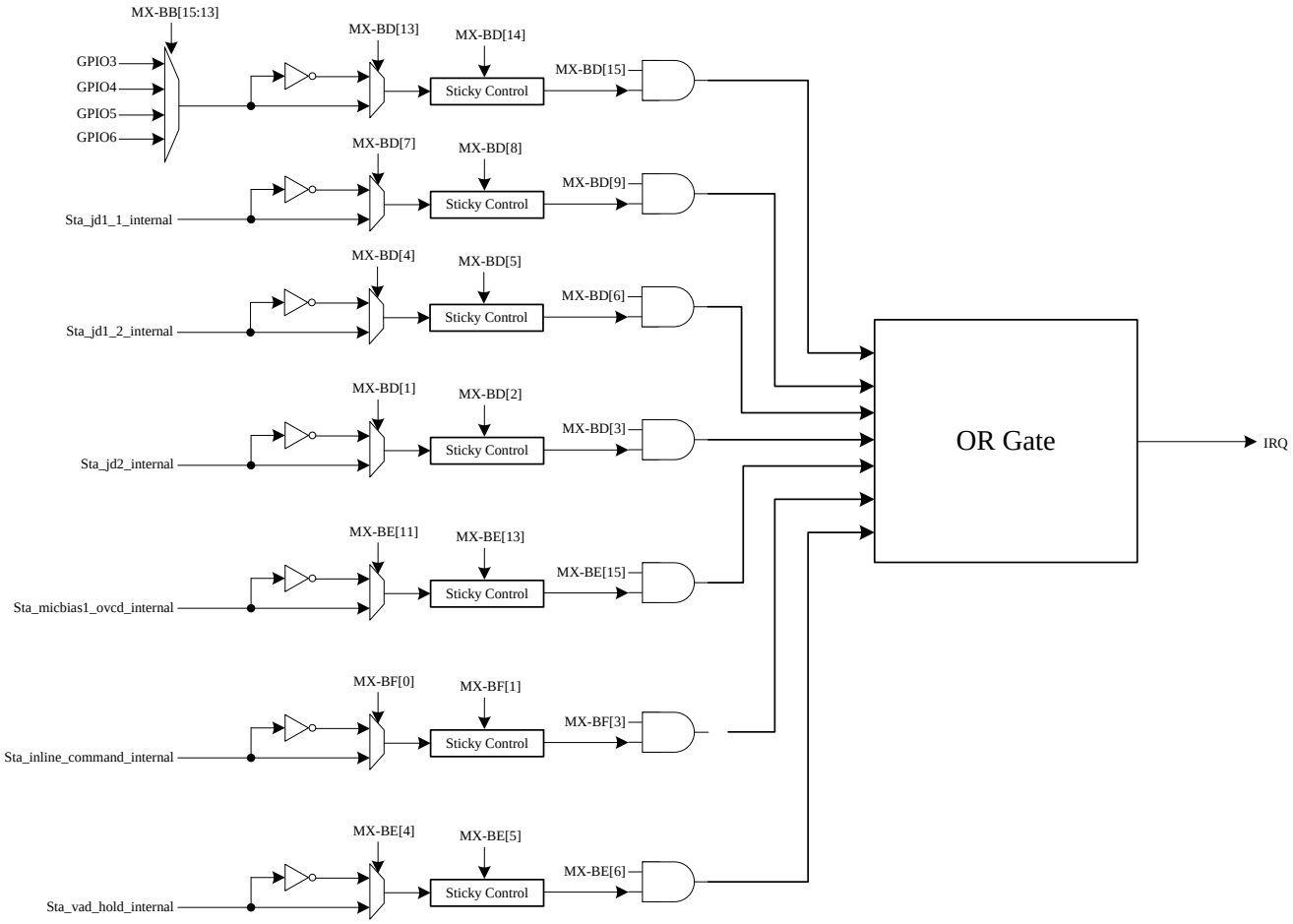
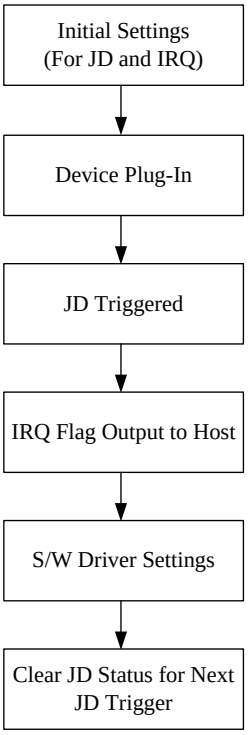


Figure 28. IRQ Function Block

In general, the IRQ output needs to combine with JD function. When JD is trigger, IRQ will output a flag to host to notice S/W driver. The S/W driver will do some settings by system design. The behavior flow chard as following:



The MICBIAS supports short current detection function. When MICBIAS circuit detects over-current happen, MICBIAS circuit will generate an over-current flag. The flag can generate an interrupt signal to notice host and let S/W do follow-up processes.

The jack detect function can be used to turn-on or turn-off the related output ports. When jack detect pin is trigged, the selected output ports will be turn-on or turn-off. For example on HP and SPK auto switch when JD is trigger.

Setting procedure:

1. Select JD status source: use sta_jd1_1 as JD source. MX-F8[2:0] = 001’b & MX-F9[11:9] = 001’b
2. Set JD status polarity for HP and SPK
   MX-BB[11:10] = 10’b, JD status low to trigger HPO
   MX-BB[9:6] = 1111’b, JD status high to trigger SPK
3. When JD status is low, HP_OUT is un-mute and SPK is mute.
   When JD status is low go high, HP is mute and SPK is un-mute.

Note: For HP and SPK port switch function, driver need to turn-on DAC to HP path and DAC to SPK path first.

8.17. Power Management

ALC5672 detailed Power Management control registers are supported in MX-61h, 62h, 63h, 64h, 65h and 66h. Each particular block will only be active when each bit MX-61h, 62h, 63h, 64h, 65h and 66h is set to enable.

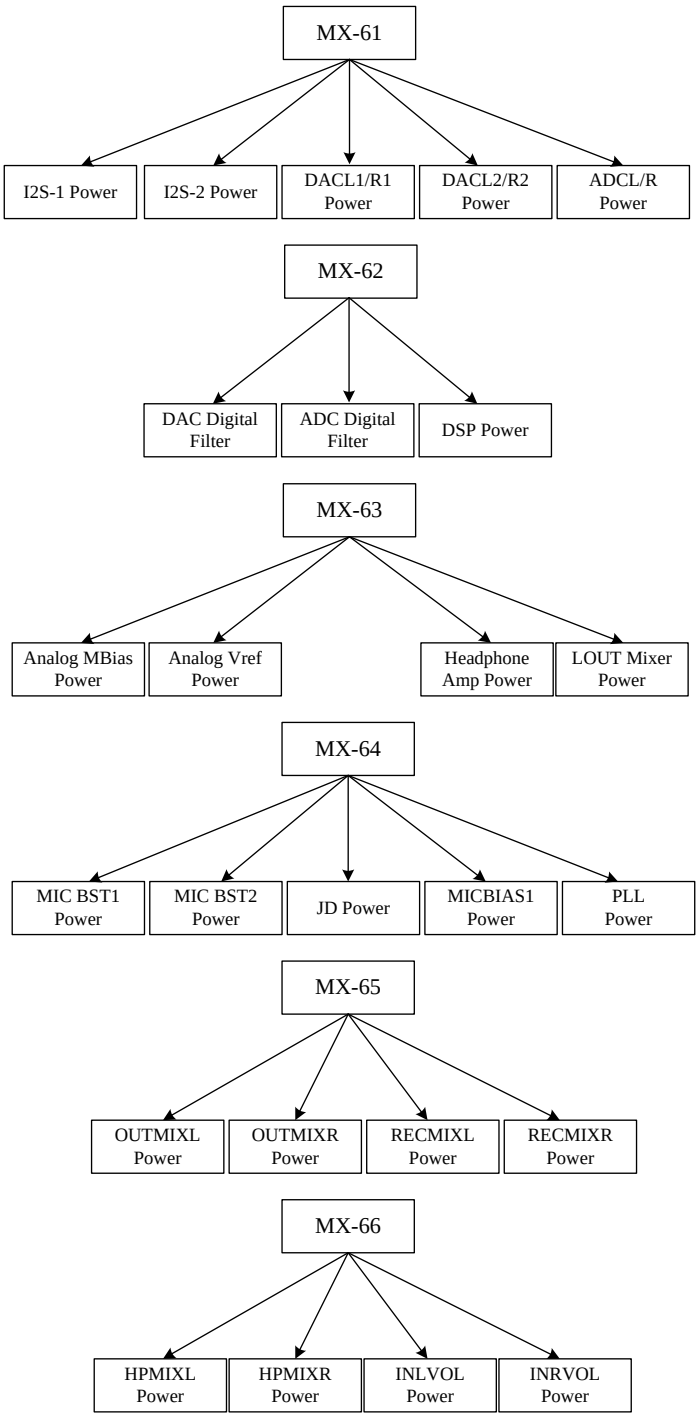


Figure 29. Power Management

8.18. Gen.3 Voice DSP Function

The on-chip Voice Processor provides microphone beam-forming with voice tracking to allow for acoustic echo cancellation, far-field pickup, stationary and non-stationary noise suppression, and voice recognition rate enhancement.

Acoustic Echo Cancellation:

The voice DSP suppresses echo effectively under all occasions, and the performance of which could be easily optimized for different types of acoustics set-up and applications for tablet computers. The AEC performs robustly under prolonged double talk periods and provides a face-to-face like conversation in full-duplex without any cut-off, drop-out, howling, voice level pumping, and annoying echoes.

Noise Suppression:

The advanced noise suppression is specifically designed for tablets to benefit users that invoke voice communication applications on these devices. Ambient noise pickup is reduced by the advanced microphone array beam-forming which could run in 2- or 3- microphone configurations. The technology further reduces both stationary noise and non-stationary noises, and enhances user experiences in video and voice chats. Noise reduction is available on both downstream and upstream signals and is highly effectively against hums, fan-noises, tones, background babbles, and a variety of unwanted interferences.

48kHz Stereo Recording with Far-Field Pickup

The vioce DSP provides specific pure 48kHz audio recording with FFP technology. It can suppress stationary noise for each channel with 24kHz bandwidth. Far-Field Pickup technology is also considered in this mode for long distance audio catch up with high signal to noise ratio. The dual feature sculpture the tablet computer to be a real stereo recording device with stationary noise suppression for long distance range.

Voice Recognition Rate Enhancement

The advanced voice processing could be configured to run in Voice Recognition Rate Enhancement mode which would perform beam-forming, acoustic echo cancellation and other processing in a way that helps to improve recognition rates in poor signal-to-noise conditions for the common commercial voice recognition engines.

Advanced Beam-Forming

The advanced beam-forming algorithm performs Voice Tracking which could follow the incidence angle of the talkers' voice and hence reduces background noise pick-up and reverberations. It also allows for exceptional widened talking angle in handheld mode to accommodate for a wide variety of user holding positions, and avoids any annoying voice drop-outs and fade-outs.

9. Registers List

ALC5672 register map as shown as following and accessing unimplemented registers, will return a 0.

9.1. Register Map

Table 17. Register Map

Type	Name	Description	Register Address	Reset State
Reset	S/W Reset	S/W Reset & Device ID	MX-00h	0x0004'h
	HPOUT	Headphone Output Volume & Mute/Un-Mute	MX-02h	0x8888'h
	LOUT	Line Output Volume & Mute/Un-Mute	MX-03h	0x8888'h
	IN1	IN1 Control 1	MX-0Ah	0x0001'h
	IN1	IN1 Control 2	MX-0Bh	0x0827'h
	IN1	IN1 Control 3	MX-0Ch	0x0000'h
	IN2	IN2 Mode and Gain Boost Control	MX-0Eh	0x0000'h
	INL/INR	INL/INR Volume Control	MX-0Fh	0x0808'h
Digital Gain/Volume	DACL1/R1	DACL1/R1 Digital Volume Control	MX-19h	0xAFAF'h
	DACL2/R2-1	DACL2/R2 Digital Volume Control	MX-1Ah	0xAFAF'h
	DACL2/R2-2	DACL2/R2 Digital Mute/Un-Mute Control	MX-1Bh	0x0000'h
	ADC	Stereo1 ADCL/R Digital Volume & Mute/Un-Mute Control	MX-1Ch	0x2F2F'h
	ADC	Mono ADCL/R Digital Path Volume Control	MX-1Dh	0x2F2F'h
	ADC	ADC Boost Gain for DMIC	MX-1Eh	0x0000'h
	ADC	Stereo2 ADCL/R Digital Volume & Mute/Un-Mute Control	MX-1Fh	0x2F2F'h
	ADC	ADC Boost Gain for DMIC	MX-20h	0x0000'h
Digital Mixer	ADC	Stereo2 ADC Digital Mixer Control	MX-26h	0x7860'h
	ADC	Stereo1 ADC Digital Mixer Control	MX-27h	0x7860'h
	ADC	Mono ADC Digital Mixer Control	MX-28h	0x7871'h
	ADC	ADC to DAC Digital Mixer Control	MX-29h	0x8080'h
	DAC	DAC Stereo Digital Mixer Control	MX-2Ah	0x5656'h
	DAC	DAC Mono Digital Mixer Control	MX-2Bh	0x5454'h
	DAC	DAC Stereo to Mono Mixer Control	MX-2Ch	0xAAA0'h
	Voice DSP	Voice DSP Path Control	MX-2Dh	0x0000'h
	Voice DSP	Voice DSP Volume Control	MX-2Eh	0x2F2F'h
	Copy Mode	ADC/DAC Data Copy Mode Control	MX-2Fh	0x1002'h
Speaker		Speaker Control 1	MX-31h	0x5F00'h
Input Mixer	RECMIXL-1	RECMIXL Gain Control	MX-3Bh	0x0000'h
	RECMIXL-2	RECMIXL Gain & Selection Control	MX-3Ch	0x007F'h
	RECMIXR-1	RECMIXR Gain Control	MX-3Dh	0x0000'h
	RECMIXR-2	RECMIXR Gain & Selection Control	MX-3Eh	0x007F'h
Output Mixer	HPOMIX	HPOMIX Gain & Selection Control	MX-45h	0x600F'h
	OUTMIXL	OUTMIXL Selection Control	MX-4Fh	0x0073'h
	OUTMIXR	OUTMIXR Selection Control	MX-52h	0x00D3'h
	LOUTMIX	LOUTMIX Gain & Selection Control	MX-53h	0xF000'h
Power Management	Management -1	I2S & DAC & ADC Power Control	MX-61h	0x0000'h

Type	Name	Description	Register Address	Reset State
	Management -2	Digital Filter & DSP & SPK Power Control	MX-62h	0x0000'h
	Management -3	VREF & MBias & LOUTMIX & HP Power Control	MX-63h	0x00C0'h
	Management -4	MICBST & MICBIAS & PLL & JD Power Control	MX-64h	0x0000'h
	Management -5	OUTMIX & RECMIX Power Control	MX-65h	0x0000'h
	Management -6	MICBIAS & OUTVOL & HPOVOL & INVOL Power Control	MX-66h	0x0000'h
PR Register	PR Index	PR Register Index	MX-6Ah	0x0000'h
	PR Data	PR Register Data	Mx-6Ch	0x0000'h
Digital Interface	I2S1 Port Ctrl	I2S-1 Interface Control	MX-70h	0x8000'h
	I2S2 Port Ctrl	I2S-2 Interface Control	MX-71h	0x8000'h
	ADC/DAC Clock	ADC/DAC Clock Control	MX-73h	0x1114'h
	ADC/DAC HPF	ADC/DAC HPF Control	MX-74h	0x0E00'h
Digital MIC		Digital Microphone Control	MX-75h	0x1505'h
		Digital Microphone Control	MX-76h	0x0015'h
TDM		TDM Interface Control	MX-77h	0x0C00'h
		TDM Interface Control	MX-78h	0x4000'h
		TDM Interface Control	MX-79h	0x0123'h
Global Clock	Clock	DSP Clock Control	MX-7Fh	0x1100'h
	Clock	Global Clock Control	MX-80h	0x0000'h
	PLL	PLL Control 1	MX-81h	0x0000'h
	PLL	PLL Control 2	MX-82h	0x0000'h
	ASRC	ASRC Control 1	MX-83h	0x0000'h
	ASRC	ASRC Control 2	MX-84h	0x0000'h
	ASRC	ASRC Control 3	MX-85h	0x0000'h
	ASRC	ASRC Control 4	MX-8Ah	0x0000'h
	ASRC	ASRC Control 5	MX-8Ch	0x0007'h
HP Amp	HP	HP Output De-Pop Control 1	MX-8Eh	0x0004'h
		HP Output De-Pop Control 2	MX-8Fh	0x1100'h
MICBIAS	MICBIAS	MICBIAS Control	MX-93h	0x0000'h
EQ	ADC EQ	ADC EQ Control 1	MX-AE	0x6000'h
	ADC EQ	ADC EQ Control 2	MX-AF	0x0000'h
	DAC EQ	DAC EQ Control 1	MX-B0h	0x6000'h
	DAC EQ	DAC EQ Control 2	MX-B1h	0x0000'h
	EQ-Parameter	DAC_L EQ (LPF: a1)	PR-A4h	0x1C10'h
	EQ-Parameter	DAC_L EQ (LPF: H0)	PR-A5h	0x01F4'h
	EQ-Parameter	DAC_R EQ (LPF: a1)	PR-A6h	0x1C10'h
	EQ-Parameter	DAC_R EQ (LPF: H0)	PR-A7h	0x01F4'h
	EQ-Parameter	DAC_L EQ (BPF2: a1)	PR-AEh	0xC882'h
	EQ-Parameter	DAC_L EQ (BPF2: a2)	PR-AFh	0x1C10'h

Type	Name	Description	Register Address	Reset State
	EQ-Parameter	DAC_L EQ (BPF2: H0)	PR-B0h	0x01F4'h
	EQ-Parameter	DAC_R EQ (BPF2: a1)	PR-B1h	0xC882'h
	EQ-Parameter	DAC_R EQ (BPF2: a2)	PR-B2h	0x1C10'h
	EQ-Parameter	DAC_R EQ (BPF2: H0)	PR-B3h	0x01F4'h
	EQ-Parameter	DAC_L EQ (BPF3: a1)	PR-B4h	0xE904'h
	EQ-Parameter	DAC_L EQ (BPF3: a2)	PR-B5h	0x1C10'h
	EQ-Parameter	DAC_L EQ (BPF3: H0)	PR-B6h	0x01F4'h
	EQ-Parameter	DAC_R EQ (BPF3: a1)	PR-B7h	0xE904'h
	EQ-Parameter	DAC_R EQ (BPF3: a2)	PR-B8h	0x1C10'h
	EQ-Parameter	DAC_R EQ (BPF3: H0)	PR-B9h	0x01F4'h
	EQ-Parameter	DAC_L EQ (BPF4: a1)	PR-BAh	0xE904'h
	EQ-Parameter	DAC_L EQ (BPF4: a2)	PR-BBh	0x1C10'h
	EQ-Parameter	DAC_L EQ (BPF4: H0)	PR-BCh	0x01F4'h
	EQ-Parameter	DAC_R EQ (BPF4: a1)	PR-BDh	0xE904'h
	EQ-Parameter	DAC_R EQ (BPF4: a2)	PR-BEh	0x1C10'h
	EQ-Parameter	DAC_R EQ (BPF4: H0)	PR-BFh	0x01F4'h
	EQ-Parameter	DAC_L EQ (HPF1: a1)	PR-C0h	0x1C10'h
	EQ-Parameter	DAC_L EQ (HPF1: H0)	PR-C1h	0x01F4'h
	EQ-Parameter	DAC_R EQ (HPF1: a1)	PR-C2h	0x1C10'h
	EQ-Parameter	DAC_R EQ (HPF1: H0)	PR-C3h	0x01F4'h
	EQ-Parameter	DAC_L EQ (HPF2: a1)	PR-C4h	0x2000'h
	EQ-Parameter	DAC_L EQ (HPF2: a2)	PR-C5h	0x0000'h
	EQ-Parameter	DAC_L EQ (HPF2: H0)	PR-C6h	0x1FF1'h
	EQ-Parameter	DAC_R EQ (HPF2: a1)	PR-C7h	0x2000'h
	EQ-Parameter	DAC_R EQ (HPF2: a2)	PR-C8h	0x0000'h

Type	Name	Description	Register Address	Reset State
	EQ-Parameter	DAC_R EQ (HPF2: H0)	PR-C9h	0x1FF1'h
	EQ-Parameter	DAC_L EQ Pre-Volume Control	PR-CAh	0x0800'h
	EQ-Parameter	DAC_R EQ Pre-Volume Control	PR-CBh	0x0800'h
	EQ-Parameter	DAC_L EQ Post-Volume Control	PR-CCh	0x0800'h
	EQ-Parameter	DAC_R EQ Post-Volume Control	PR-CDh	0x0800'h
	EQ-Parameter	ADC EQ (LPF: a1)	PR-CEh	0x1C10'h
	EQ-Parameter	ADC EQ (LPF: H0)	PR-CFh	0x01F4'h
	EQ-Parameter	ADC EQ (BPF1: a1)	PR-D0h	0xE904'h
	EQ-Parameter	ADC EQ (BPF1: a2)	PR-D1h	0x1C10'h
	EQ-Parameter	ADC EQ (BPF1: H0)	PR-D2h	0x01F4'h
	EQ-Parameter	ADC EQ (BPF2: a1)	PR-D3h	0xE904'h
	EQ-Parameter	ADC EQ (BPF2: a2)	PR-D4h	0x1C10'h
	EQ-Parameter	ADC EQ (BPF2: H0)	PR-D5h	0x01F4'h
	EQ-Parameter	ADC EQ (BPF3: a1)	PR-D6h	0xE904'h
	EQ-Parameter	ADC EQ (BPF3: a2)	PR-D7h	0x1C10'h
	EQ-Parameter	ADC EQ (BPF3: H0)	PR-D8h	0x01F4'h
	EQ-Parameter	ADC EQ (BPF4: a1)	PR-D9h	0xE904'h
	EQ-Parameter	ADC EQ (BPF4: a2)	PR-DAh	0x1C10'h
	EQ-Parameter	ADC EQ (BPF4: H0)	PR-DBh	0x01F4'h
	EQ-Parameter	ADC EQ (HPF1: a1)	PR-DCh	0x1C10'h
	EQ-Parameter	ADC EQ (HPF1: H0)	PR-DDh	0x01F4'h
	EQ-Parameter	ADC EQ Pre-Volume Control	PR-E1h	0x0800'h
	EQ-Parameter	ADC EQ Post-Volume Control	PR-E2h	0x0800'h
	EQ-Parameter	DAC_L Biquad EQ (BPF1: h0-1)	PR-E5h	0x0000'h
	EQ-Parameter	DAC_L Biquad EQ (BPF1: h0-2)	PR-E6h	0x0000'h

Type	Name	Description	Register Address	Reset State
	EQ-Parameter	DAC_L Biquad EQ (BPF1: b1-1)	PR-E7h	0x0000'h
	EQ-Parameter	DAC_L Biquad EQ (BPF1: b1-2)	PR-E8h	0x0000'h
	EQ-Parameter	DAC_L Biquad EQ (BPF1: b2-1)	PR-E9h	0x0000'h
	EQ-Parameter	DAC_L Biquad EQ (BPF1: b2-2)	PR-EAh	0x0000'h
	EQ-Parameter	DAC_L Biquad EQ (BPF1: a1-1)	PR-EBh	0x0000'h
	EQ-Parameter	DAC_L Biquad EQ (BPF1: a1-2)	PR-ECh	0x0000'h
	EQ-Parameter	DAC_L Biquad EQ (BPF1: a2-1)	PR-EDh	0x0000'h
	EQ-Parameter	DAC_L Biquad EQ (BPF1: a2-2)	PR-EEh	0x0000'h
	EQ-Parameter	DAC_R Biquad EQ (BPF1: h0-1)	PR-EFh	0x0000'h
	EQ-Parameter	DAC_R Biquad EQ (BPF1: h0-2)	PR-F0h	0x0000'h
	EQ-Parameter	DAC_R Biquad EQ (BPF1: b1-1)	PR-F1h	0x0000'h
	EQ-Parameter	DAC_R Biquad EQ (BPF1: b1-2)	PR-F2h	0x0000'h
	EQ-Parameter	DAC_R Biquad EQ (BPF1: b2-1)	PR-F3h	0x0000'h
	EQ-Parameter	DAC_R Biquad EQ (BPF1: b2-2)	PR-F4h	0x0000'h
	EQ-Parameter	DAC_R Biquad EQ (BPF1: a1-1)	PR-F5h	0x0000'h
	EQ-Parameter	DAC_R Biquad EQ (BPF1: a1-2)	PR-F6h	0x0000'h
	EQ-Parameter	DAC_R Biquad EQ (BPF1: a2-1)	PR-F7h	0x0000'h
	EQ-Parameter	DAC_R Biquad EQ (BPF1: a2-2)	PR-F8h	0x0000'h
DRC/AGC	DRC/AGC	DRC/AGC Control 1	MX-B2h	0x0000'h
	DRC/AGC	DRC/AGC Control 2	MX-B3h	0x001F'h
	DRC/AGC	DRC/AGC Control 3	MX-B4h	0x2206'h
	DRC/AGC	DRC/AGC Control 4	MX-B5h	0x1F00'h
	DRC/AGC	DRC/AGC Control 5	MX-B6h	0x0000'h
	DRC/AGC	DRC/AGC Control 6	MX-B7h	0x0000'h
Jack Detection	JD	Jack Detection Control	MX-BBh	0x0000'h
	JD	Jack Detection Control	MX-F8h	0x0000'h
	JD	Jack Detection Control	MX-F9h	0x0000'h
IRQ	IRQ	IRQ Control 1	MX-BDh	0x0000'h
	IRQ	IRQ Control 2	MX-BEh	0x0000'h
	IRQ	IRQ Control 3	MX-BFh	0x0000'h
GPIO	GPIO	GPIO Control 1	MX-C0h	0x0000'h
	GPIO	GPIO Control 2	MX-C2h	0x0000'h
	GPIO	GPIO Control 3	MX-C3h	0x0000'h

Type	Name	Description	Register Address	Reset State
SounzReal™ Post-Processing	BassBack	BassBack Control	MX-CFh	0x0013'h
	TruTreble	TruTreble Control 1	MX-D0h	0x0680'h
	TruTreble	TruTreble Control 2	MX-D1h	0x1C17'h
Wind Filter	Stereo1	Stereo1 ADC Wind Filter Control 1	MX-D3h	0xAA20'h
	Stereo1	Stereo1 ADC Wind Filter Control 2	MX-D4h	0x0000'h
	Mono	Mono ADC Wind Filter Control 1	MX-ECh	0xAA20'h
	Mono	Mono ADC Wind Filter Control 2	MX-EDh	0x0000'h
	Stereo2	Stereo2 ADC Wind Filter Control 1	MX-EEh	0xAA20'h
	Stereo2	Stereo2 ADC Wind Filter Control 2	MX-EFh	0x0000'h
SVOL & ZCD	SVOL & ZCD	Soft Volume and ZCD Control 1	MX-D9h	0x0809'h
		Soft Volume and ZCD Control 2	MX-DAh	0x0000'h
InLine Command		Inline Command Control 1	MX-DBh	0x0001'h
		Inline Command Control 2	MX-DCh	0x0049'h
		Inline Command Control 3	MX-DDh	0x0003'h
Voice DSP		Voice DSP Control 1	MX-E0h	0x0000'h
		Voice DSP Control 2	MX-E1h	0x0000'h
		Voice DSP Control 3	MX-E2h	0x0000'h
		Voice DSP Control 4	MX-E3h	0x0000'h
		Voice DSP Control 5	MX-E4h	0x0000'h
		Voice DSP Control 6	MX-E5h	0x0000'h
General Control		General Control 1	MX-FAh	0x0090'h
		ADC/DAC RESET Control	PR-3D	0x2808'h
Vendor ID	ID	Vendor ID	MX-FEh	0x10EC'h

9.2. MX-00h: S/W Reset & Device ID

Default: 0004’h

Table 18. MX-00h: S/W Reset

Port Name	Bits	Read/Write	Reset State	Description
Reserved	15:3	R	0’h	Reserved
Device_id	2:1	R	2’h	ALC5672
Reserved	0	R	0’h	Reserved

Note: Writes to this register will reset all registers to their default values.

9.3. MX-02h: Headphone Output Control

Default: 8888’h

Table 19. MX-02h: Headphone Output Control

Name	Bits	Read/Write	Reset State	Description
mu_hpo_l	15	R/W	1’h	Mute Control for Left Headphone Output Port (HPOL) 0’b: Un-Mute 1’b: Mute
Reserved	14	R	0’h	Reserved
vol_hpol	13:8	R/W	8’h	Left Headphone Channel Volume Control (HPOVOLL) ❶ 00’h: +12dB … 08’h: 0dB … 27’h: -46.5dB, with 1.5dB/step
mu_hpo_r	7	R/W	1’h	Mute Control Right Headphone Output Port (HPOR) 0’b: Un-Mute 1’b: Mute
Reserved	6	R	0’h	Reserved

Name	Bits	Read/Write	Reset State	Description
Vol_hpor	5:0	R/W	8'h	Right Headphone Channel Volume Control (HPOVOLR)❶ 00'h: +12dB … 08'h: 0dB … 27'h: -46.5dB, with 1.5dB/step

❶Volume Table

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	12	16	10	-12	32	20	-36
1	1	10.5	17	11	-13.5	33	21	-37.5
2	2	9	18	12	-15	34	22	-39
3	3	7.5	19	13	-16.5	35	23	-40.5
4	4	6	20	14	-18	36	24	-42
5	5	4.5	21	15	-19.5	37	25	-43.5
6	6	3	22	16	-21	38	26	-45
7	7	1.5	23	17	-22.5	39	27	-46.5
8	8	0	24	18	-24			
9	9	-1.5	25	19	-25.5			
10	A	-3	26	1A	-27			
11	B	-4.5	27	1B	-28.5			
12	C	-6	28	1C	-30			
13	D	-7.5	29	1D	-31.5			
14	E	-9	30	1E	-33			
15	F	-10.5	31	1F	-34.5			

9.4. MX-03h: LINE Output Control

Default: 8888'h

Table 20. MX-03h: LINE Output Control

Name	Bits	Read/Write	Reset State	Description
Mu_lout_l	15	R/W	1'h	Mute Control for Left Line Output Port(LOUTL) 0'b: Un-Mute 1'b: Mute
En_dfo1	14	R/W	0'h	LOUT Differential Mode Control 0'b: Disable (Single-ended mode) 1'b: Enable (Differential mode)
Vol_outl	13:8	R/W	08'h	Left Output Volume Control (OUTVOLL) ❶ 00'h: +12dB … 08'h: 0dB … 27'h: -46.5dB, with 1.5dB/step
Mu_lout_r	7	R/W	1'h	Mute Control for Right Line Output Port (LOUTR) 0'b: Un-Mute 1'b: Mute
Reserved	6	R	0'h	Reserved
Vol_outr	5:0	R/W	08'h	Right Output Volume Control ❶ 00'h: +12dB … 08'h: 0dB … 27'h: -46.5dB, with 1.5dB/step

❶Volume Table

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	12	16	10	-12	32	20	-36
1	1	10.5	17	11	-13.5	33	21	-37.5
2	2	9	18	12	-15	34	22	-39
3	3	7.5	19	13	-16.5	35	23	-40.5
4	4	6	20	14	-18	36	24	-42
5	5	4.5	21	15	-19.5	37	25	-43.5
6	6	3	22	16	-21	38	26	-45
7	7	1.5	23	17	-22.5	39	27	-46.5
8	8	0	24	18	-24			
9	9	-1.5	25	19	-25.5			
10	A	-3	26	1A	-27			
11	B	-4.5	27	1B	-28.5			

12	C	-6	28	1C	-30			
13	D	-7.5	29	1D	-31.5			
14	E	-9	30	1E	-33			
15	F	-10.5	31	1F	-34.5			

9.5. MX-0Ah: IN1 Port Control - 1

Default: 0001'h

Table 21. MX-0Dh: IN1 Input Control - 1

Name	Bits	Read/Write	Reset State	Description
Sel_bst1	15:12	R/W	0'h	IN1 Boost Control (BST1) 0000'b: Bypass 0001'b: +20dB 0010'b: +24dB 0011'b: +30dB 0100'b: +35dB 0101'b: +40dB 0110'b: +44dB 0111'b: +50dB 1000'b: +52dB Others : Reserved
reserved	11:3	R/W	0'h	Reserved
En_bst1	2	R/W	0'h	IN1 Port Enable Control 0'b: Disable 1'b: Enable
reserved	1:0	R/W	1'h	Reserved

9.6. MX-0Bh: IN1 Port Control - 2

Default: 0827’h

Table 22. MX-0Bh: IN1 Input Control - 2

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R	0’h	Reserved
Manual_tri_in1	12	R/W	0’h	Manual Trigger For IN1 Port 0’b: Low trigger 1’b: High trigger
Capless_gat_en	11	R/W	1’h	Capless Power Gating with IN1 Control 0’b: Register control 1’b: Auto mode
reserved	10:8	R/W	0’h	Reserved
Reg_mode	7	R/W	1’h	IN1 Port Mode Control 0’b: Auto mode 1’b: Manual mode
reserved	6:0	R/W	27’h	Reserved

9.7. MX-0Ch: IN1 Port Control - 3

Default: 0000’h

Table 23. MX-0Ch: IN1 Input Control - 3

Name	Bits	Read/Write	Reset State	Description
Reserved	15:3	R	0’h	Reserved
In1_result	2:0	R	0’h	IN1 Port Final Status 001’b: Type1 010’b: Type2 100’b: Type3

9.8. MX-0Eh: IN2 Input Control

Default: 0000’h

Table 24. MX-0Eh: IN2 Input Control

Name	Bits	Read/Write	Reset State	Description
Sel_bst2	15:12	R/W	0’h	IN2 Boost Control (BST2) 0000’b: Bypass 0001’b: +20dB 0010’b: +24dB 0011’b: +30dB 0100’b: +35dB 0101’b: +40dB 0110’b: +44dB 0111’b: +50dB 1000’b: +52dB Others : Reserved
Reserved	11:8	R/W	0’h	Reserved
En_in2_df	7	R/W	0’h	IN2 Input Mode Control 0’b: Single Ended Mode 1’b: Differential Mode
Reserved	6:0	R	0’h	Reserved

9.9. MX-0Fh: INL & INR Volume Control

Default: 0808’h

Table 25. MX-0Fh: INL & INR Volume Control

Name	Bits	Read/Write	Reset State	Description
reserved	15:13	R	0’h	Reserved
Vol_inl	12:8	R/W	8’h	INL Channel Volume Control ❶ 00’h: +12dB … 08’h: 0dB … 1F’h: -34.5dB, with 1.5dB/step
Reserved	7:5	R	0’h	Reserved
Vol_inr	4:0	R/W	8’h	INR Channel Volume Control ❶ 00’h: +12dB … 08’h: 0dB … 1F’h: -34.5dB, with 1.5dB/step

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	12	16	10	-12
1	1	10.5	17	11	-13.5
2	2	9	18	12	-15
3	3	7.5	19	13	-16.5
4	4	6	20	14	-18
5	5	4.5	21	15	-19.5
6	6	3	22	16	-21
7	7	1.5	23	17	-22.5
8	8	0	24	18	-24
9	9	-1.5	25	19	-25.5
10	A	-3	26	1A	-27
11	B	-4.5	27	1B	-28.5
12	C	-6	28	1C	-30
13	D	-7.5	29	1D	-31.5
14	E	-9	30	1E	-33
15	F	-10.5	31	1F	-34.5

9.10. MX-19h: DACL1/R1 Digital Volume

Default: AFAF'h

Table 26. MX-19h: DACL1/R1 Digital Volume

Name	Bits	Read/Write	Reset State	Description
vol_dac1_l	15:8	R/W	AF'h	DAC1 Left Channel Digital Volume❶ 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step
vol_dac1_r	7:0	R/W	AF'h	DAC1 Right Channel Digital Volume❶ 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step

9.11. MX-1Ah: DACL2/R2 Digital Volume

Default: AFAF'h

Table 27. MX-1Ah: DACL2/R2 Digital Volume

Name	Bits	Read/Write	Reset State	Description
vol_dac2_l	15:8	R/W	AF'h	DAC2 Left Channel Digital Volume❶ 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step
vol_dac2_r	7:0	R/W	AF'h	DAC2 Right Channel Digital Volume❶ 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-65.625	53	35	-45.75	106	6A	-25.875	159	9F	-6	212	D4	
1	1	-65.25	54	36	-45.375	107	6B	-25.5	160	A0	-5.625	213	D5	
2	2	-64.875	55	37	-45	108	6C	-25.125	161	A1	-5.25	214	D6	
3	3	-64.5	56	38	-44.625	109	6D	-24.75	162	A2	-4.875	215	D7	
4	4	-64.125	57	39	-44.25	110	6E	-24.375	163	A3	-4.5	216	D8	
5	5	-63.75	58	3A	-43.875	111	6F	-24	164	A4	-4.125	217	D9	
6	6	-63.375	59	3B	-43.5	112	70	-23.625	165	A5	-3.75	218	DA	
7	7	-63	60	3C	-43.125	113	71	-23.25	166	A6	-3.375	219	DB	
8	8	-62.625	61	3D	-42.75	114	72	-22.875	167	A7	-3	220	DC	
9	9	-62.25	62	3E	-42.375	115	73	-22.5	168	A8	-2.625	221	DD	
10	A	-61.875	63	3F	-42	116	74	-22.125	169	A9	-2.25	222	DE	
11	B	-61.5	64	40	-41.625	117	75	-21.75	170	AA	-1.875	223	DF	
12	C	-61.125	65	41	-41.25	118	76	-21.375	171	AB	-1.5	224	E0	
13	D	-60.75	66	42	-40.875	119	77	-21	172	AC	-1.125	225	E1	
14	E	-60.375	67	43	-40.5	120	78	-20.625	173	AD	-0.75	226	E2	
15	F	-60	68	44	-40.125	121	79	-20.25	174	AE	-0.375	227	E3	
16	10	-59.625	69	45	-39.75	122	7A	-19.875	175	AF	0	228	E4	
17	11	-59.25	70	46	-39.375	123	7B	-19.5	176	B0		229	E5	
18	12	-58.875	71	47	-39	124	7C	-19.125	177	B1		230	E6	
19	13	-58.5	72	48	-38.625	125	7D	-18.75	178	B2		231	E7	
20	14	-58.125	73	49	-38.25	126	7E	-18.375	179	B3		232	E8	
21	15	-57.75	74	4A	-37.875	127	7F	-18	180	B4		233	E9	

22	16	-57.375	75	4B	-37.5	128	80	-17.625	181	B5		234	EA	
23	17	-57	76	4C	-37.125	129	81	-17.25	182	B6		235	EB	
24	18	-56.625	77	4D	-36.75	130	82	-16.875	183	B7		236	EC	
25	19	-56.25	78	4E	-36.375	131	83	-16.5	184	B8		237	ED	
26	1A	-55.875	79	4F	-36	132	84	-16.125	185	B9		238	EE	
27	1B	-55.5	80	50	-35.625	133	85	-15.75	186	BA		239	EF	
28	1C	-55.125	81	51	-35.25	134	86	-15.375	187	BB		240	F0	
29	1D	-54.75	82	52	-34.875	135	87	-15	188	BC		241	F1	
30	1E	-54.375	83	53	-34.5	136	88	-14.625	189	BD		242	F2	
31	1F	-54	84	54	-34.125	137	89	-14.25	190	BE		243	F3	
32	20	-53.625	85	55	-33.75	138	8A	-13.875	191	BF		244	F4	
33	21	-53.25	86	56	-33.375	139	8B	-13.5	192	C0		245	F5	
34	22	-52.875	87	57	-33	140	8C	-13.125	193	C1		246	F6	
35	23	-52.5	88	58	-32.625	141	8D	-12.75	194	C2		247	F7	
36	24	-52.125	89	59	-32.25	142	8E	-12.375	195	C3		248	F8	
37	25	-51.75	90	5A	-31.875	143	8F	-12	196	C4		249	F9	
38	26	-51.375	91	5B	-31.5	144	90	-11.625	197	C5		250	FA	
39	27	-51	92	5C	-31.125	145	91	-11.25	198	C6		251	FB	
40	28	-50.625	93	5D	-30.75	146	92	-10.875	199	C7		252	FC	
41	29	-50.25	94	5E	-30.375	147	93	-10.5	200	C8		253	FD	
42	2A	-49.875	95	5F	-30	148	94	-10.125	201	C9		254	FE	
43	2B	-49.5	96	60	-29.625	149	95	-9.75	202	CA		255	FF	
44	2C	-49.125	97	61	-29.25	150	96	-9.375	203	CB				
45	2D	-48.75	98	62	-28.875	151	97	-9	204	CC				
46	2E	-48.375	99	63	-28.5	152	98	-8.625	205	CD				
47	2F	-48	100	64	-28.125	153	99	-8.25	206	CE				
48	30	-47.625	101	65	-27.75	154	9A	-7.875	207	CF				
49	31	-47.25	102	66	-27.375	155	9B	-7.5	208	D0				
50	32	-46.875	103	67	-27	156	9C	-7.125	209	D1				
51	33	-46.5	104	68	-26.625	157	9D	-6.75	210	D2				
52	34	-46.125	105	69	-26.25	158	9E	-6.375	211	D3				

9.12. MX-1Bh: DACL2/R2 Mute/Un-Mute Control

Default: 0000’h

Table 28. MX-1Bh: DACL2/R2 Mute/Un-Mute Control

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0’h	Reserved
Mu_dac2_l	13	R/W	0’h	Mute Control for Left DAC2 Volume 0’b: Un-Mute 1’b: Mute
Mu_dac2_r	12	R/W	0’h	Mute Control for Right DAC2 Volume 0’b: Un-Mute 1’b: Mute
reserved	11:7	R	0’h	Reserved
Sel_dacl2	6:4	R/W	1’h	Select DACL2 Data Source 000’b: IF1_DAC2_L 001’b: IF2_DAC_L 010’b: Reserved 011’b: TxDC_DAC_L 100’b: Reserved 101’b: VAD_ADC Others: Reserved
reserved	3	R	0’h	Reserved
Sel_dacr2	2:0	R/W	1’h	Select DACR2 Data Source 000’b: IF1_DAC2_R 001’b: IF2_DAC_R 010’b: Reserved 011’b: TxDC_DAC_R 100’b: TxDP_DAC_L Others: Reserved

9.13. MX-1Ch: Stereo1 ADC Digital Volume Control

Default: 2F2F'h

Table 29. MX-1Ch: Stereo1 ADC Digital Volume Control

Name	Bits	Read/Write	Reset State	Description
Mu_adc_vol_l	15	R/W	0'h	Mute Control for Stereo1 ADC Left Volume Channel 0'b: Un-Mute 1'b: Mute
Ad_gain_l	14:8	R/W	2F'h	Stereo1 ADC Left Channel Volume Control 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step
Mu_adc_vol_r	7	R/W	0'h	Mute Control for Stereo1 ADC Right Volume Channel 0'b: Un-Mute 1'b: Mute
Ad_gain_r	6:0	R/W	2F'h	Stereo1 ADC Right Channel Volume Control 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step

9.14. MX-1Dh: Mono ADC Digital Volume Control

Default: 2F2F'h

Table 30. MX-1Dh: Mono ADC Digital Volume Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	Reserved
Mono_ad_gain_l	14:8	R/W	2F'h	Mono ADC Left Channel Volume Control ❶ 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step

reserved	7	R	0'h	Reserved
Mono_ad_gain_r	6:0	R/W	2F'h	Mono ADC Right Channel Volume Control ❶ 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-17.625	26	1A	-7.875	52	34	1.875	78	4E	11.625	104	68	21.375
1	1	-17.25	27	1B	-7.5	53	35	2.25	79	4F	12	105	69	21.75
2	2	-16.875	28	1C	-7.125	54	36	2.625	80	50	12.375	106	6A	22.125
3	3	-16.5	29	1D	-6.75	55	37	3	81	51	12.75	107	6B	22.5
4	4	-16.125	30	1E	-6.375	56	38	3.375	82	52	13.125	108	6C	22.875
5	5	-15.75	31	1F	-6	57	39	3.75	83	53	13.5	109	6D	23.25
6	6	-15.375	32	20	-5.625	58	3A	4.125	84	54	13.875	110	6E	23.625
7	7	-15	33	21	-5.25	59	3B	4.5	85	55	14.25	111	6F	24
8	8	-14.625	34	22	-4.875	60	3C	4.875	86	56	14.625	112	70	24.375
9	9	-14.25	35	23	-4.5	61	3D	5.25	87	57	15	113	71	24.75
10	A	-13.875	36	24	-4.125	62	3E	5.625	88	58	15.375	114	72	25.125
11	B	-13.5	37	25	-3.75	63	3F	6	89	59	15.75	115	73	25.5
12	C	-13.125	38	26	-3.375	64	40	6.375	90	5A	16.125	116	74	25.875
13	D	-12.75	39	27	-3	65	41	6.75	91	5B	16.5	117	75	26.25
14	E	-12.375	40	28	-2.625	66	42	7.125	92	5C	16.875	118	76	26.625
15	F	-12	41	29	-2.25	67	43	7.5	93	5D	17.25	119	77	27
16	10	-11.625	42	2A	-1.875	68	44	7.875	94	5E	17.625	120	78	27.375
17	11	-11.25	43	2B	-1.5	69	45	8.25	95	5F	18	121	79	27.75
18	12	-10.875	44	2C	-1.125	70	46	8.625	96	60	18.375	122	7A	28.125
19	13	-10.5	45	2D	-0.75	71	47	9	97	61	18.75	123	7B	28.5
20	14	-10.125	46	2E	-0.375	72	48	9.375	98	62	19.125	124	7C	28.875
21	15	-9.75	47	2F	0	73	49	9.75	99	63	19.5	125	7D	29.25
22	16	-9.375	48	30	0.375	74	4A	10.125	100	64	19.875	126	7E	29.625
23	17	-9	49	31	0.75	75	4B	10.5	101	65	20.25	127	7F	30
24	18	-8.625	50	32	1.125	76	4C	10.875	102	66	20.625			
25	19	-8.25	51	33	1.5	77	4D	11.25	103	67	21			

9.15. MX-1Eh: ADC Digital Boost Gain Control

Default: 0000’h

Table 31. MX-1Eh: ADC Digital Boost Gain Control

Name	Bits	Read/Write	Reset State	Description
Stereo1_ad_boost_gain_l	15:14	R/W	0’h	Stereo1 ADC Left Channel Digital Boost Gain 00’b: 0dB 01’b: 12dB 10’b: 24dB 11’b: 36dB
Stereo1_ad_boost_gain_r	13:12	R/W	0’h	Stereo1 ADC Right Channel Digital Boost Gain 00’b: 0dB 01’b: 12dB 10’b: 24dB 11’b: 36dB
Stereo1_ad_comp_gain	11:10	R/W	0’h	Stereo1 ADC Compensation Gain 00’b: 0dB 01’b: 1dB 10’b: 2dB 11’b: 3dB
Stereo2_ad_boost_gain_l	9:8	R/W	0’h	Stereo2 ADC Left Channel Digital Boost Gain 00’b: 0dB 01’b: 12dB 10’b: 24dB 11’b: 36dB
Stereo2_ad_boost_gain_r	7:6	R/W	0’h	Stereo2 ADC Right Channel Digital Boost Gain 00’b: 0dB 01’b: 12dB 10’b: 24dB 11’b: 36dB
Stereo2_ad_comp_gain	5:4	R/W	0’h	Stereo2 ADC Compensation Gain 00’b: 0dB 01’b: 1dB 10’b: 2dB 11’b: 3dB
reserved	3:0	R/W	0’h	Reserved

9.16. MX-1Fh: Stereo2 ADC Digital Volume Control

Default: 2F2F'h

Table 32. MX-1Fh: Stereo2 ADC Digital Volume Control

Name	Bits	Read/Write	Reset State	Description
Mu_adc2_vol_l	15	R/W	0'h	Mute Control for Stereo2 ADC Left Volume Channel 0'b: Un-Mute 1'b: Mute
Ad2_gain_l	14:8	R/W	2F'h	Stereo2 ADC Left Channel Volume Control 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step
Mu_adc2_vol_r	7	R/W	0'h	Mute Control for Stereo2 ADC Right Volume Channel 0'b: Un-Mute 1'b: Mute
Ad2_gain_r	6:0	R/W	2F'h	Stereo2 ADC Right Channel Volume Control 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step

9.17. MX-20h: Mono ADC Digital Boost Gain Control

Default: 0000'h

Table 33. MX-20h: Mono ADC Digital Boost Gain Control

Name	Bits	Read/Write	Reset State	Description
mono_ad_boost_gain_l	15:14	R/W	0'h	Mono ADC Left Channel Digital Boost Gain 00'b: 0dB 01'b: 12dB 10'b: 24dB 11'b: 36dB

mono_ad_boost_gain_r	13:12	R/W	0'h	Mono ADC Right Channel Digital Boost Gain 00'b: 0dB 01'b: 12dB 10'b: 24dB 11'b: 36dB
mono_ad_comp_gain	11:10	R/W	0'h	Mono ADC Compensation Gain 00'b: 0dB 01'b: 1dB 10'b: 2dB 11'b: 3dB
Reserved	9:0	R	0'h	Reserved

9.18. MX-26h: Stereo2 ADC Digital Mixer Control

Default: 7860'h

Table 34. MX-26h: Stereo2 ADC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
Sel_stereo2_lr_mix	15	R/W	0'h	Mixing Control for Stereo2 ADC Left channel 0'b: L 1'b: L+R
mu_stereo2_adcl1	14	R/W	1'h	Mute Source1 to Stereo2 ADC Left Channel 0'b:UnMute 1'b:Mute
mu_stereo2_adcl2	13	R/W	1'h	Mute Source2 to Stereo2 ADC Left Channel 0'b:UnMute 1'b:Mute
sel_stereo2_adc1	12	R/W	1'h	Select Stereo2 ADC L/R Channel Source 1 0'b: DAC_MIXL / DAC_MIXR 1'b: ADC1
sel_stereo2_adc2	11	R/W	1'h	Select Stereo2 ADC L/R Channel Source 2 0'b: DAC_MIXL / DAC_MIXR 1'b: DMIC1/DMIC2/DMIC3
Reserved	10	R/W	0'h	Reserved
Sel_stereo2_dmic	9:8	R/W	0'h	Select Stereo2 DMIC Source 00'b: DMIC1 01'b: DMIC2 10'b: DMIC3 11'b: Reserved
reserved	7	R	0'h	Reserved
mu_stereo2_adcr1	6	R/W	1'h	Mute Source1 to Stereo2 ADC Right Channel 0'b:UnMute 1'b:Mute

mu_stereo2_adcr2	5	R/W	1'h	Mute Source2 to Stereo2 ADC Right Channel 0'b:UnMute 1'b:Mute
reserved	4:0	R	0'h	reserved

9.19. MX-27h: Stereo1 ADC Digital Mixer Control

Default: 7860'h

Table 35. MX-27h: Stereo1 ADC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	Reserved
mu_stereo1_adcl1	14	R/W	1'h	Mute Source 1 to Stereo1 ADC Left Channel 0'b:UnMute 1'b:Mute
mu_stereo1_adcl2	13	R/W	1'h	Mute Source 2 to Stereo1 ADC Left Channel 0'b:UnMute 1'b:Mute
sel_stereo1_adc1	12	R/W	1'h	Select Stereo1 ADC L/R Channel Source 1 0'b: DAC_MIXL / DAC_MIXR 1'b: ADC1
sel_stereo1_adc2	11	R/W	1'h	Select Stereo1 ADC L/R Channel Source 2 0'b: DAC_MIXL / DAC_MIXR 1'b: DMIC1/DMIC2/DMIC3
reserved	10	R/W	0'h	Reserved
Sel_stereo1_dmic	9:8	R/W	0'h	Select Stereo1 DMIC Source 00'b: DMIC1 01'b: DMIC2 10'b: DMIC3 11'b: Reserved
reserved	7	R	0'h	Reserved
mu_stereo1_adcr1	6	R/W	1'h	Mute Source 1 to Stereo1 ADC Right Channel 0'b:UnMute 1'b:Mute
mu_stereo1_adcr2	5	R/W	1'h	Mute Source 2 to Stereo1 ADC Right Channel 0'b:UnMute 1'b:Mute
reserved	4:0	R	0'h	reserved

9.20. MX-28h: Mono ADC Digital Mixer Control

Default: 7871’h

Table 36. MX-28h: Mono ADC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0’h	Reserved
mu_mono_adcl1	14	R/W	1’h	Mute Source 1 to Mono ADC Left channel 0’b:UnMute 1’b:Mute
mu_mono_adcl2	13	R/W	1’h	Mute Source 2 to Mono ADC Left channel 0’b:UnMute 1’b:Mute
sel_mono_adcl1	12	R/W	1’h	Select Mono ADC Left channel source 1 0’b: Mono_DAC_Mixer_L 1’b: ADC1
sel_mono_adcl2	11	R/W	1’h	Select Mono ADC Left channel source 2 0’b: Mono_DAC_Mixer_L 1’b: DMIC1_L or DMIC2_L or DMIC3_L
reserved	10	R/W	0’h	Reserved
Sel_mono_dmic_l	9:8	R/W	0’h	Select Mono Left Channel DMIC Source 00’b: DMIC1_L 01’b: DMIC2_L 10’b: DMIC3_L 11’b: Reserved
reserved	7	R	0’h	Reserved
mu_mono_adcr1	6	R/W	1’h	Mute Source 1 to Mono ADC Right channel 0’b:UnMute 1’b:Mute
mu_mono_adcr2	5	R/W	1’h	Mute Source 2 to Mono ADC Right channel 0’b:UnMute 1’b:Mute
sel_mono_adcr1	4	R/W	1’h	Select Mono ADC Right channel source 1 0’b: Mono_DAC_Mixer_R 1’b: ADC2
sel_mono_adcr2	3	R/W	0’h	Select Mono ADC Right channel source 2 0’b: Mono_DAC_Mixer_R 1’b: DMIC1_R or DMIC2_R or DMIC3_R
reserved	2	R/W	0’h	Reserved
Sel_mono_dmic_r	1:0	R/W	1’h	Select Mono Right Channel DMIC Source 00’b: DMIC1_R 01’b: DMIC2_R 10’b: DMIC3_R 11’b: Reserved

9.21. MX-29h: Stereo ADC to DAC Digital Mixer Control

Default: 8080’h

Table 37. MX-29h: Stereo ADC to DAC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
Mu_stereo1_adc_mixer_l	15	R/W	1’h	Mute Stereo1 ADC to DAC1 Left Channel 0’b:UnMute 1’b:Mute
Mu_dac1_l	14	R/W	0’h	Mute IF1 DAC Left Channel 0’b:UnMute 1’b:Mute
reserved	13:12	R	0’h	Reserved
Sel_dacr1	11:10	R/W	0’h	DACR1 Source Selection 00’b: IF1_DAC1_R 01’b: IF2_DAC_R 10’b: Reserved 11’b: Reserved
Sel_dacl1	9:8	R/W	0’h	DACL1 Source Selection 00’b: IF1_DAC1_L 01’b: IF2_DAC_L 10’b: Reserved 11’b: Reserved
Mu_stereo1_adc_mixer_r	7	R/W	1’h	Mute Stereo1 ADC to DAC1 Right Channel 0’b:UnMute 1’b:Mute
Mu_dac1_r	6	R/W	0’h	Mute IF1 DAC Right Channel 0’b:UnMute 1’b:Mute
reserved	5:0	R	0’h	reserved

9.22. MX-2Ah: Stereo DAC Digital Mixer Control

Default: 5656’h

Table 38. MX-2Ah: Stereo DAC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0’h	Reserved
mu_stereo_dacl1_mixl	14	R/W	1’h	Mute Stereo DAC1 Left channel 0’b:UnMute 1’b:Mute
gain_dacl1_to_stereo_l	13	R/W	0’h	Gain Control for DACL1 to Stereo Left Mixer 0’b: 0dB 1’b: -6dB
mu_stereo_dacl2_mixl	12	R/W	1’h	Mute Stereo DAC2 Left channel 0’b:UnMute 1’b:Mute
gain_dacl2_to_stereo_l	11	R/W	0’h	Gain Control for DACL2 to Stereo Left Mixer 0’b: 0dB 1’b: -6dB

Name	Bits	Read/Write	Reset State	Description
reserved	10	R/W	1'h	Reserved
mu_stereo_dacr1_mixl	9	R/W	1'h	Mute Stereo DAC1 Right channel to Left Mixer 0'b:UnMute 1'b:Mute
gain_dacr1_to_stereo_l	8	R/W	0'h	Gain Control for DACR1 to Stereo Left Mixer 0'b: 0dB 1'b: -6dB
reserved	7	R	0'h	reserved
mu_stereo_dacr1_mixr	6	R/W	1'h	Mute Stereo DAC1 Right channel 0'b:UnMute 1'b:Mute
gain_dacr1_to_stereo_r	5	R/W	0'h	Gain Control for DACR1 to Stereo Right Mixer 0'b: 0dB 1'b: -6dB
mu_stereo_dacr2_mixr	4	R/W	1'h	Mute Stereo DAC2 Right channel 0'b:UnMute 1'b:Mute
gain_dacr2_to_stereo_r	3	R/W	0'h	Gain Control for DACR2 to Stereo Right Mixer 0'b: 0dB 1'b: -6dB
Reserved	2	R/W	1'h	Reserved
mu_stereo_dacl1_mixr	1	R/W	1'h	Mute Stereo DAC1 Left channel to Right Mixer 0'b:UnMute 1'b:Mute
gain_dacl1_to_stereo_r	0	R/W	0'h	Gain Control for DACL1 to Stereo Right Mixer 0'b: 0dB 1'b: -6dB

9.23. MX-2Bh: Mono DAC Digital Mixer Control

Default: 5454'h

Table 39. MX-2Bh: Mono DAC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	Reserved
mu_mono_dacl1_mixl	14	R/W	1'h	Mute DAC1 Left channel to Mono DAC Left Mixer 0'b:UnMute 1'b:Mute
gain_mono_l_dacl1	13	R/W	0'h	Gain Control for DAC1 Left channel to Mono DAC Left Mixer 0'b: 0dB 1'b: -6dB
mu_mono_dacl2_mixl	12	R/W	1'h	Mute DAC2 Left channel to Mono DAC Left Mixer 0'b:UnMute 1'b:Mute
gain_mono_l_dacl2	11	R/W	0'h	Gain Control for DAC2 Left channel to Mono DAC Left Mixer 0'b: 0dB 1'b: -6dB

Name	Bits	Read/Write	Reset State	Description
mu_mono_dacr2_mixl	10	R/W	1'h	Mute DAC2 Right channel to Mono DAC Left Mixer 0'b:UnMute 1'b:Mute
gain_mono_l_dacr2	9	R/W	0'h	Gain Control for DAC2 Right channel to Mono DAC Left Mixer 0'b: 0dB 1'b: -6dB
reserved	8:7	R	0'h	reserved
mu_mono_dacr1_mixr	6	R/W	1'h	Mute DAC1 Right channel to Mono DAC Right Mixer 0'b:UnMute 1'b:Mute
gain_mono_r_dacr1	5	R/W	0'h	Gain Control for DAC1 Right channel to Mono DAC Right Mixer 0'b: 0dB 1'b: -6dB
mu_mono_dacr2_mixr	4	R/W	1'h	Mute DAC2 Right channel to Mono DAC Right Mixer 0'b:UnMute 1'b:Mute
gain_mono_r_dacr2	3	R/W	0'h	Gain Control for DAC2 Right channel to Mono DAC Right Mixer 0'b: 0dB 1'b: -6dB
mu_mono_dacl2_mixr	2	R/W	1'h	Mute DAC2 Left channel to Mono DAC Right Mixer 0'b:UnMute 1'b:Mute
gain_mono_r_dacl2	1	R/W	0'h	Gain Control for DAC2 Left channel to Mono DAC Right Mixer 0'b: 0dB 1'b: -6dB
reserved	0	R	0'h	reserved

9.24. MX-2Ch: DAC Digital Mixer Control

Default: AAA0'h

Table 40. MX-2Ch: DAC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
Mu_stereomixl_to_dacmixl	15	R/W	1'h	Mute Stereo_DAC_Mixer_L to DAC_MIXL 0'b:UnMute 1'b:Mute
gain_stereomixl_to_dacmixl	14	R/W	0'h	Gain Control for Stereo_DAC_Mixer_L to DAC_MIXL 0'b: 0dB 1'b: -6dB
Mu_dacl2_to_dacmixl	13	R/W	1'h	Mute DACL2 to DAC_MIXL 0'b:UnMute 1'b:Mute
gain_dacl2_to_dacmixl	12	R/W	0'h	Gain Control for DACL2 to DAC_MIXL 0'b: 0dB 1'b: -6dB

Name	Bits	Read/Write	Reset State	Description
Mu_stereomixr_to_dacmixr	11	R/W	1'h	Mute Stereo_DAC_Mixer_R to DAC_MIXR 0'b:UnMute 1'b:Mute
gain_stereomixr_to_dacmixr	10	R/W	0'h	Gain Control for Stereo_DAC_Mixer_R to DAC_MIXR 0'b: 0dB 1'b: -6dB
Mu_dacr2_to_dacmixr	9	R/W	1'h	Mute DACR2 to DAC_MIXR 0'b:UnMute 1'b:Mute
gain_dacr2_to_dacmixr	8	R/W	0'h	Gain Control for DACR2 to DAC_MIXR 0'b: 0dB 1'b: -6dB
Mu_dacr2_to_dacmixl	7	R/W	1'h	Mute DACR2 to DAC_MIXL 0'b:UnMute 1'b:Mute
gain_dacr2_to_dacmixl	6	R/W	0'h	Gain Control for DACR2 to DAC_MIXL 0'b: 0dB 1'b: -6dB
Mu_dacl2_to_dacmixr	5	R/W	1'h	Mute DACL2 to DAC_MIXR 0'b:UnMute 1'b:Mute
gain_dacl2_to_dacmixr	4	R/W	0'h	Gain Control for DACL2 to DAC_MIXR 0'b: 0dB 1'b: -6dB
reserved	3:0	R	0'h	Reserved

9.25. MX-2Dh: Voice DSP Path Control 1

Default: 0000'h

Table 41. MX-2Dh: Voice DSP Path Control 1

Name	Bits	Read/Write	Reset State	Description
Sel_rxdp_in	15:13	R/W	0'h	RxDP Input Selection 000'b: IF2_DAC_L/R 001'b: IF1_DAC2_L/R 010'b: Stereo1_ADC_Mixer_L/R 011'b: Stereo2_ADC_Mixer_L/R 100'b: Mono_ADC_Mixer_L 101'b: Mono_ADC_Mixer_R 110'b: DACL1/R1 (After EQ/ALC/ SounzReal™) 111'b: Reserved
Sel_src_to_rxdp	12:11	R/W	0'h	Select SRC to RxDP 00'b: Bypass 01'b: /2 10'b: /3 11'b: Reserved
Reserved	10	R	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
Sel_txdp_data	9:8	R/W	0'h	TxDP Output Data Swap 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
Sel_txdc_data	7:6	R/W	0'h	TxDC Output Data Swap 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
Sel_src_to_txdp	5:4	R/W	0'h	Select SRC to TxDP 00'b: Bypass (Stereo signal) 01'b: /2 (Mono signal) 10'b: /3 (Mono signal) 11'b: Reserved
Sel_tdm_txdp_slot	3:2	R/W	0'h	TXDP TDM Channel Slot Selection to Stereo Channel 00'b: Slot 0/1 01'b: Slot 2/3 10'b: Slot 4/5 11'b: Slot 6/7
Sel_dsp_ul_bypass	1	R/W	0'h	Select DSP Uplink Bypass 0'b: Pass DSP 1'b: Bypass DSP
Sel_dsp_dl_bypass	0	R/W	0'h	Select DSP Downlink Bypass 0'b: Pass DSP 1'b: Bypass DSP

9.26. MX-2Eh: Voice DSP Volume Control

Default: 2F2F'h

Table 42. MX-2Eh: Voice DSP Volume Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R	0'h	Reserved
Vol_txdp_l	14:8	R/W	2F'h	Mono ADC left channel digital volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB, 0.375dB/Step
Reserved	7	R	0'h	Reserved
Vol_txdp_r	6:0	R/W	2F'h	Mono ADC right channel digital volume in 0.375 dB step 00'h: -17.625dB 2F'h: 0dB 7F'h: 30dB, 0.375dB/Step

9.27. MX-2Fh: Interface DAC/ADC Data Control

Default: 1002’h

Table 43. MX-2Fh: Interface DAC/ADC Data Control

Name	Bits	Read/Write	Reset State	Description
Sel_if1_adc2_data_in	15	R/W	0’h	Select Interface1 ADC2 Data Input 0’b: IF_ADC2 1’b: VAD_ADC
Sel_if2_adc_data_in	14:12	R/W	1’h	Select Interface2 ADC Data Input 000’b: IF_ADC1 001’b: IF_ADC2 010’b: Reserved 011’b: TxDC_DAC 100’b: TxDP_ADC 101’b: VAD_ADC 110’b: Reserved 111’b: Reserved
sel_if2_dac_data	11:10	R/W	0’h	Select Interface2 DAC Data Swap 00’b: L/R 01’b: R/L 10’b: L/L 11’b: R/R
sel_if2_adc_data	9:8	R/W	0’h	Select Interface2 ADC Data Swap 00’b: L/R 01’b: R/L 10’b: L/L 11’b: R/R
reserved	7:0	R	2’h	Reserved

9.28. MX-31h: Speaker Control 1

Default: 5F00’h

Table 44. MX-31h: Speaker Control 1

Name	Bits	Read/Write	Reset State	Description
sel_spk_l	15	R/W	0’h	Select Speaker Left channel source 0’b: Mono_DAC_MIXL 1’b: Stereo_DAC_MIXL
mu_spk_l	14	R/W	1’h	Mute Speaker Left channel data 0’b: UnMute 1’b: Mute
sel_spk_r	13	R/W	0’h	Select Speaker Right channel source 0’b: Mono_DAC_MIXR 1’b: Stereo_DAC_MIXR
mu_spk_r	12	R/W	1’h	Mute Speaker Right channel data 0’b: UnMute 1’b: Mute

Name	Bits	Read/Write	Reset State	Description
Reserved	11:0	R	F00’h	Reserved

9.29. MX-3Bh: RECMIXL Control 1

Default: 0000’h

Table 45. MX-3Bh: RECMIXL Control 1

Name	Bits	Read/Write	Reset State	Description
reserved	15:13	R/W	0’h	Reserved
gain_inl_recmixl	12:10	R/W	0’h	Gain Control for INL1 to REC Left Mixer 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB
reserved	9:7	R/W	0’h	Reserved
gain_bst2_recmixl	6:4	R/W	0’h	Gain Control for Boost 2 to REC Left Mixer 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB
reserved	3:0	R	0’h	reserved

9.30. MX-3Ch: RECMIXL Control 2

Default: 007F’h

Table 46. MX-3Ch: RECMIXL Control 2

Name	Bits	Read/Write	Reset State	Description
gain_bst1_recmixl	15:13	R/W	0’h	Gain Control for Boost 1 to REC Left Mixer 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB
reserved	12:6	R	1’h	Reserved
Mu_inl_recmixl	5	R/W	1’h	INL1 to RECMIXL Mute Control 0’b : Un-Mute 1’b: Mute (-∞ dB)
reserved	4	R/W	1’h	Reserved
Mu_bst2_recmixl	3	R/W	1’h	MIC BST2 to RECMIXL Mute Control 0’b : Un-Mute 1’b: Mute (-∞ dB)
reserved	2	R/W	1’h	Reserved
Mu_bst1_recmixl	1	R/W	1’h	MIC BST1 to RECMIXL Mute Control 0’b : Un-Mute 1’b: Mute (-∞ dB)
reserved	0	R/W	1’h	Reserved

9.31. MX-3Dh: RECMIXR Control 1

Default: 0000’h

Table 47. MX-3Dh: RECMIXR Control 1

Name	Bits	Read/Write	Reset State	Description
reserved	15:13	R/W	0’h	Reserved
gain_inr_recmixr	12:10	R/W	0’h	Gain Control for INR1 to REC Right Mixer 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB
reserved	9:7	R/W	0’h	Reserved
gain_bst2_recmixr	6:4	R/W	0’h	Gain Control for Boost 2 to REC Right Mixer 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB
reserved	3:0	R	0’h	reserved

9.32. MX-3Eh: RECMIXR Control 2

Default: 007F’h

Table 48. MX-3Eh: RECMIXR Control 2

Name	Bits	Read/Write	Reset State	Description
gain_bst1_recmixr	15:13	R/W	0’h	Gain Control for Boost 1 to REC Right Mixer 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB
reserved	12:6	R	1’h	Reserved
Mu_inr_recmixr	5	R/W	1’h	INR1 to RECMIXR Mute Control 0’b : Un-Mute 1’b: Mute (-∞ dB)
reserved	4	R/W	1’h	Reserved
Mu_bst2_recmixr	3	R/W	1’h	MIC BST2 to RECMIXR Mute Control 0’b : Un-Mute 1’b: Mute (-∞ dB)
reserved	2	R/W	1’h	Reserved
Mu_bst1_recmixr	1	R/W	1’h	MIC BST1 to RECMIXR Mute Control 0’b : Un-Mute 1’b: Mute (-∞ dB)
reserved	0	R/W	1’h	Reserved

9.33. MX-45h: HPOMIX Control

Default: 600F'h

Table 49. MX-45h: HPOMIX Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	Reserved
Mu_dac1_hpo	14	R/W	1'h	DAC1 to HPO Mute Control 0'b: Un-Mute 1'b: Mute (-∞ dB)
Mu_hpvol_hpo	13	R/W	1'h	HPOVOL to HPO Mute Control 0'b: Un-Mute 1'b: Mute (-∞ dB)
En_bst_hp	12	R/W	0'h	HPO Gain Control 0'b: 0dB 1'b: -6dB
reserved	11:4	R	0'h	Reserved
Mu_inr1_hpmixr	3	R/W	1'h	INR to HPMIXR Mute Control 0'b: Un-Mute 1'b: Mute (-∞ dB)
Mu_dacr1_hpomixr	2	R/W	1'h	DACR1 to HPMIXR Mute Control 0'b : Un-Mute 1'b: Mute (-∞ dB)
Mu_inl1_hpomixl	1	R/W	1'h	INL to HPMIXL Mute Control 0'b : Un-Mute 1'b: Mute (-∞ dB)
Mu_dacl1_hpomixl	0	R/W	1'h	DACL1 to HPMIXL Mute Control 0'b : Un-Mute 1'b: Mute (-∞ dB)

9.34. MX-4Fh: OUTMIXL Control

Default: 0073'h

Table 50. MX-4Fh: OUTMIXL Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:6	R	1'h	reserved
Mu_bst1_outmixl1	5	R/W	1'h	Mute Control for BST1 to OUTMIXL1 0'b: Un-Mute 1'b: Mute (-∞ dB)
Mu_inl_outmixl1	4	R/W	1'h	Mute Control for INL1 to OUTMIXL1 0'b: Un-Mute 1'b: Mute (-∞ dB)
Reserved	3:2	R	0'h	reserved
Mu_dacl2_outmixl1	1	R/W	1'h	Mute Control for DACL2 to OUTMIXL1 0'b: Un-Mute 1'b: Mute (-∞ dB)

Name	Bits	Read/Write	Reset State	Description
Mu_dacl1_outmixl1	0	R/W	1'h	Mute Control for DACL1 to OUTMIXL1 0'b: Un-Mute 1'b: Mute (-∞ dB)

9.35. MX-52h: OUTMIXR Control

Default: 00D3'h

Table 51. MX-52h: OUTMIXR Control 3

Name	Bits	Read/Write	Reset State	Description
reserved	15:7	R	1'h	reserved
Mu_bst2_outmixr1	6	R/W	1'h	Mute Control for BST2 to OUTMIXR1 0'b: Un-Mute 1'b: Mute (-∞ dB)
reserved	5	R	0'h	reserved
Mu_inr_outmixr1	4	R/W	1'h	Mute Control for INR1 to OUTMIXR1 0'b: Un-Mute 1'b: Mute (-∞ dB)
reserved	3:2	R	0'h	reserved
Mu_dacr2_outmixr1	1	R/W	1'h	Mute Control for DACR2 to OUTMIXR1 0'b: Un-Mute 1'b: Mute (-∞ dB)
Mu_dacr1_outmixr1	0	R/W	1'h	Mute Control for DACR1 to OUTMIXR1 0'b: Un-Mute 1'b: Mute (-∞ dB)

9.36. MX-53h: LOUTMIX Control

Default: F000'h

Table 52. MX-53h: LOUTMIX Control

Name	Bits	Read/Write	Reset State	Description
mu_dacl1_lout1	15	R/W	1'h	Mute DACL1 to LOUT1 Mixer 0'b: Un-Mute 1'b: Mute (-∞ dB)
mu_dacr1_lout1	14	R/W	1'h	Mute DACR1 to LOUT1 Mixer 0'b: Un-Mute 1'b: Mute (-∞ dB)
mu_outmixl1_lout1	13	R/W	1'h	Mute Output Left Volume 1 to LOUT1 Mixer 0'b: Un-Mute 1'b: Mute (-∞ dB)
mu_outmixr1_lout1	12	R/W	1'h	Mute Output Right Volume 1 to LOUT1 Mixer 0'b: Un-Mute 1'b: Mute (-∞ dB)

Name	Bits	Read/Write	Reset State	Description
bst_lout1	11	R/W	0'h	Gain Control for ALL path to LOUT1 Mixer 0'b: 0dB 1'b: -6dB
reserved	10:0	R	0'h	Reserved

9.37. MX-61h: Power Management Control 1

Default: 0000'h

Table 53. MX-61h: Power Management Control 1

Name	Bits	Read/Write	Reset State	Description
En_i2s1	15	R/W	0'h	I2S1 Digital Interface Power Control 0'b: Power Down 1'b: Power On
En_i2s2	14	R/W	0'h	I2S2 Digital Interface Power Control 0'b: Power Down 1'b: Power On
reserved	13	R/W	0'h	Reserved
Pow_dac_l_1	12	R/W	0'h	Analog DACL1 Power Control 0'b: Power Down 1'b: Power On
Pow_dac_r_1	11	R/W	0'h	Analog DACR1 Power Control 0'b: Power Down 1'b: Power On
reserved	10:8	R	0'h	Reserved
Pow_dac_l_2	7	R/W	0'h	Analog DACL2 Power Control 0'b: Power Down 1'b: Power On
Pow_dac_r_2	6	R/W	0'h	Analog DACR2 Power Control 0'b: Power Down 1'b: Power On
reserved	5:3	R	0'h	Reserved
Pow_adc_l	2	R/W	0'h	Analog ADCL Power Control 0'b: Power Down 1'b: Power On
Pow_adc_r	1	R/W	0'h	Analog ADCR Power Control 0'b: Power Down 1'b: Power On
reserved	0	R	0'h	Reserved

9.38. MX-62h: Power Management Control 2

Default: 0000’h

Table 54. MX-62h: Power Management Control 2

Name	Bits	Read/Write	Reset State	Description
Pow_adc_stereo_filter	15	R/W	0’h	Stereo1 ADC Digital Filter Power Control 0’b: Power Down 1’b: Power On
Pow_adc_monol_filter	14	R/W	0’h	Mono ADC_L Digital Filter Power Control 0’b: Power Down 1’b: Power On
Pow_adc_monor_filter	13	R/W	0’h	Mono ADC_R Digital Filter Power Control 0’b: Power Down 1’b: Power On
Pow_i2s_dsp	12	R/W	0’h	I2S Interface for DSP Power Control 0’b: Power Down 1’b: Power On
pow_dac_stereo1_filter	11	R/W	0’h	Power on DAC stereo1 filter 0’b: Power Down 1’b: Power On
pow_dac_monol_filter	10	R/W	0’h	Power on DAC mono left filter 0’b: Power Down 1’b: Power On
pow_dac_monor_filter	9	R/W	0’h	Power on DAC mono right filter 0’b: Power Down 1’b: Power On
pow_adc_stereo2_filter	8	R/W	0’h	Power on ADC stereo2 filter 0’b: Power Down 1’b: Power On
Pow_spk	7	R/W	0’h	Power on Speaker 0’b: Power down 1’b: Power on
reserved	6:0	R	0’h	Reserved

9.39. MX-63h: Power Management Control 3

Default: 00C0’h

Table 55. MX-63h: Power Management Control 3

Name	Bits	Read/Write	Reset State	Description
Pow_vref1	15	R/W	0’h	VREF1 Power Control 0’b: Power Down 1’b: Power On
En_fastb1	14	R/W	0’h	VREF1 Fast Mode Control 0’b: Fast VREF 1’b: Slow VREF, (For good analog performance)

Name	Bits	Read/Write	Reset State	Description
Pow_main_bias	13	R/W	0’h	MBIAS Power Control 0’b: Power Down 1’b: Power On
Pow_lout	12	R/W	0’h	LOUTMIX Power Control 0’b: Power Down 1’b: Power On
Pow_bg_bias	11	R/W	0’h	MBIAS Bandgap Power Control 0’b: Power Down 1’b: Power On
reserved	10:8	R	0’h	Reserved
En_l_hp	7	R/W	1’h	Left Headphone Amp Power Control 0’b: Power Down 1’b: Power On
En_r_hp	6	R/W	1’h	Right Headphone Amp Power Control 0’b: Power Down 1’b: Power On
En_amp_hp	5	R/W	0’h	Improve HP Amp Driving 0’b: Disable 1’b: Enable
Pow_vref2	4	R/W	0’h	VREF2 Power Control 0’b: Power Down 1’b: Power On
En_fastb2	3	R/W	0’h	VREF2 Fast Mode Control 0’b: Fast VREF 1’b: Slow VREF, (For good analog performance)
Dvo_ldo	2:0	R/W	3’h	Selection of the LDO output 000’b: Reserved 001’b: Reserved 010’b: 1.0V 011’b: 1.2V 100’b: 1.25V 101’b: 1.3V 110’b: 1.35V 111’b: 1.4V

9.40. MX-64h: Power Management Control 4

Default: 0000’h

Table 56. MX-64h: Power Management Control 4

Name	Bits	Read/Write	Reset State	Description
Pow_bst1_1	15	R/W	0’h	MIC BST1 Power Control 1 0’b: Power Down 1’b: Power On
reserved	14	R/W	0’h	reserved
Pow_bst2_1	13	R/W	0’h	MIC BST2 Power Control 1 0’b: Power Down 1’b: Power On

Name	Bits	Read/Write	Reset State	Description
reserved	12	R/W	0'h	reserved
Pow_micbias1_1	11	R/W	0'h	MICBIAS1 Power Control 1 0'b: Power Down 1'b: Power On
reserved	10	R/W	0'h	reserved
Pow_pll	9	R/W	0'h	PLL Power Control 0'b: Power Down 1'b: Power On
reserved	8:7	R	0'h	Reserved
Pow_bst1_2	6	R/W	0'h	MIC BST1 Power Control 2 0'b: Power Down 1'b: Power On
reserved	5	R	0'h	Reserved
Pow_bst2_2	4	R/W	0'h	MIC BST2 Power Control 2 0'b: Power Down 1'b: Power On
reserved	3	R	0'h	Reserved
Pow_jd1	2	R/W	0'h	JD1 Power Control 0'b: Power Down 1'b: Power On
Pow_jd2	1	R/W	0'h	JD2 Power Control 0'b: Power Down 1'b: Power On
reserved	0	R	0'h	Reserved

9.41. MX-65h: Power Management Control 5

Default: 0000'h

Table 57. MX-65h: Power Management Control 5

Name	Bits	Read/Write	Reset State	Description
Pow_outmixl	15	R/W	0'h	OUTMIXL & VOL Power Control 0'b: Power Down 1'b: Power On
Pow_outmixr	14	R/W	0'h	OUTMIXR & VOL Power Control 0'b: Power Down 1'b: Power On
reserved	13:12	R	0'h	Reserved
Pow_recmixl	11	R/W	0'h	RECMIXL Power Control 0'b: Power Down 1'b: Power On
Pow_recmixr	10	R/W	0'h	RECMIXR Power Control 0'b: Power Down 1'b: Power On
reserved	9:0	R	0'h	Reserved

9.42. MX-66h: Power Management Control 6

Default: 0000’h

Table 58. MX-66h: Power Management Control 6

Name	Bits	Read/Write	Reset State	Description
reserved	15:12	R	0’h	Reserved
Pow_hpovoll	11	R/W	0’h	HPMIXL & VOL Power Control 0’b: Power Down 1’b: Power On
Pow_hpovolr	10	R/W	0’h	HPMIXR & VOL Power Control 0’b: Power Down 1’b: Power On
Pow_inlvol	9	R/W	0’h	INLVOL Power Control 0’b: Power Down 1’b: Power On
Pow_inrvol	8	R/W	0’h	INRVOL Power Control 0’b: Power Down 1’b: Power On
reserved	7:6	R	0’h	Reserved
Pow_mic_in_det	5	R/W	0’h	MIC_IN_DET Power Control 0’b: Power Down 1’b: Power On
reserved	4:1	R	0’h	Reserved
Pow_micbias1_2	0	R/W	0’h	MICBIAS1 Power Control 2 0’b: Power Down 1’b: Power On

9.43. MX-6Ah: Private Register Index

Default: 0000’h

Table 59. MX-6Ah: Private Register Index

Name	Bits	Read/Write	Reset State	Description
reserved	15:8	R	0’h	reserved
Pr_index	7:0	R/W	0’h	PR Register Index

9.44. MX-6Ch: Private Register Data

Default: 0000’h

Table 60. MX-6Ch: Private Register Data

Name	Bits	Read/Write	Reset State	Description
Pr_data	15:0	R/W	0’h	PR Register Data

9.45. MX-70h: I2S1 Digital Interface Control

Default: 8000’h

Table61. MX-70h: I2S1 Digital Interface Control

Name	Bits	Read/Write	Reset State	Description
Sel_i2s1_ms	15	R/W	1’h	I2S1 Digital Interface Mode Control 0’b: Master Mode 1’b: Slave Mode
reserved	14:12	R	0’h	Reserved
en_i2s1_out_comp	11:10	R/W	0’h	I2S1 Output Data Compress (For ADCDAT1 Output) 00’b: OFF 01’b: µ law 10’b: A law 11’b: Reserved
en_i2s1_in_comp	9:8	R/W	0’h	I2S1 Input Data Compress (For DACDAT1 Input) 00’b: OFF 01’b: µ law 10’b: A law 11’b: Reserved
Inv_i2s1_bclk	7	R/W	0’h	I2S1 BCLK Polarity Control 0’b: Normal 1’b: Invert
reserved	6:4	R	0’h	Reserved
sel_i2s1_len	3:2	R/W	0’h	I2S1 Data Length Selection 00’b: 16 bits 01’b: 20 bits 10’b: 24 bits 11’b: 8 bits
sel_i2s1_format	1:0	R/W	0’h	I2S1 PCM Data Format Selection 00’b: I^2S format 01’b: Left justified 10’b: PCM Mode A (LRCK One Plus at Master Mode) 11’b: PCM Mode B (LRCK One Plus at Master Mode)

9.46. MX-71h: I2S2 Digital Interface Control

Default: 8000’h

Table 62. MX-71h: I2S2 Digital Interface Control

Name	Bits	Read/Write	Reset State	Description
Sel_i2s2_ms	15	R/W	1’h	I2S2 Digital Interface Mode Control 0’b: Master Mode 1’b: Slave Mode
reserved	14:12	R	0’h	Reserved
en_i2s2_out_comp	11:10	R/W	0’h	I2S2 Output Data Compress (For ADCDAT2 Output) 00’b: OFF 01’b: µ law 10’b: A law 11’b: Reserved
en_i2s2_in_comp	9:8	R/W	0’h	I2S2 Input Data Compress (For DACDAT2 Input) 00’b: OFF 01’b: µ law 10’b: A law 11’b: Reserved
inv_i2s2_bclk	7	R/W	0’h	I2S2 BCLK Polarity Control 0’b: Normal 1’b: Invert
reserved	6:4	R	0’h	Reserved
sel_i2s2_len	3:2	R/W	0’h	I2S2 Data Length Selection 00’b: 16 bits 01’b: 20 bits 10’b: 24 bits 11’b: 8bits
sel_i2s2_format	1:0	R/W	0’h	I2S2 PCM Data Format Selection 00’b: I^2S format 01’b: Left justified 10’b: PCM Mode A (LRCK One Plus at Master Mode) 11’b: PCM Mode B (LRCK One Plus at Master Mode)

9.47. MX-73h: ADC/DAC Clock Control

Default: 1114’h

Table 63. MX-73h: ADC/DAC Clock Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0’h	Reserved

Name	Bits	Read/Write	Reset State	Description
sel_i2s_pre_div1	14:12	R/W	1'h	I2S Clock Pre-Divider 1 000'b: ÷ 1 001'b: ÷ 2 010'b: ÷ 3 011'b: ÷ 4 100'b: ÷ 6 101'b: ÷ 8 110'b: ÷ 12 111'b: ÷ 16
sel_i2s_bclk_ms2	11	R/W	0'h	I2S2 Master Mode Clock Relative of BCLK and LRCK 0'b: 16Bits (32FS) 1'b: 32Bits (64FS)
sel_i2s_pre_div2	10:8	R/W	1'h	I2S Pre-Divider 2 000'b: ÷ 1 001'b: ÷ 2 010'b: ÷ 3 011'b: ÷ 4 100'b: ÷ 6 101'b: ÷ 8 110'b: ÷ 12 111'b: ÷ 16
reserved	7:4	R/W	1'h	Reserved
sel_dac_osr	3:2	R/W	1'h	Stereo DAC Over Sample Rate Select 00'b: 128Fs 01'b: 64Fs 10'b: 32Fs 11'b: Reserved
sel_adc_osr	1:0	R/W	0'h	Stereo ADC Over Sample Rate Select 00'b: 128Fs 01'b: 64Fs 10'b: 32Fs 11'b: Reserved

9.48. MX-74h: ADC/DAC HPF Control

Default: 0E00'h

Table 64. MX-74h: ADC/DAC HPF Control

Name	Bits	Read/Write	Reset State	Description
reserved	15:12	R	0'h	Reserved
Dehpf_en	11	R/W	1'h	Enable Stereo/Mono DAC High Pass Filter 0'b: Disable 1'b: Enable
Adhpf_en	10	R/W	1'h	Enable Stereo1/2 ADC High Pass Filter 0'b: Disable 1'b: Enable
Mono_adhpf_en	9	R/W	1'h	Enable Mono ADC High Pass Filter 0'b: Disable 1'b: Enable

Name	Bits	Read/Write	Reset State	Description
Reserved	8:0	R	0'h	Reserved

9.49. MX-75h: Digital Microphone Control 1

Default: 1505'h

Table 65. MX-75h: Digital Microphone Control 1

Name	Bits	Read/Write	Reset State	Description
en_dmic1	15	R/W	0'h	Enable DMIC1 Interface 0'b: Disable 1'b: Enable (Output DMIC clock)
en_dmic2	14	R/W	0'h	Enable DMIC2 Interface 0'b: Disable 1'b: Enable (Output DMIC clock)
sel_dmic_l_edge_stereo1	13	R/W	0'h	Stereo1 ADC Filter DMIC Left Channel Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_r_edge_stereo1	12	R/W	1'h	Stereo1 ADC Filter DMIC Right Channel Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
reserved	11	R/W	0'h	Reserved
Dmic2_data_pin_share	10	R/W	1'h	Select the Pin share of DMIC2_DATA 0'b:GPIO8 1'b:IN3N
sel_dmic_l_edge_stereo2	9	R/W	0'h	Stereo2 ADC Filter DMIC Left Channel Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_r_edge_stereo2	8	R/W	1'h	Stereo2 ADC Filter DMIC Right Channel Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_clk	7:5	R/W	0'h	DMIC Clock Rate Control 000'b: 256*fs/2 001'b: 256*fs/3 010'b: 256*fs/4 011'b: 256*fs/6 100'b: 256*fs/8 101'b: 256*fs/12
en_dmic3	4	R/W	0'h	Enable DMIC3 Interface 0'b: Disable 1'b: Enable (Output DMIC clock)

Name	Bits	Read/Write	Reset State	Description
sel_dmic_l_edge_mono	3	R/W	0'h	Mono ADC Filter DMIC Left Channel Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic_r_edge_mono	2	R/W	1'h	Mono ADC Filter DMIC Right Channel Source Control (Synchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
dmic1_data_pin_share	1:0	R/W	1'h	Select the Pin share of DMIC1_DATA 00'b: GPIO6 01'b: IN2P 10'b: Reserved 11'b: Reserved

9.50. MX-76h: Digital Microphone Control 2

Default: 0015'h

Table 66. MX-76h: Digital Microphone Control 2

Name	Bits	Read/Write	Reset State	Description
Reserved	15:8	R	0'h	Reserved
Dmic3_data_pin_share	7:6	R/W	0'h	Select the Pin share of DMIC3_DATA 00'b: Reserved 01'b: Reserved 10'b: GPIO5 (DACDAT2) 11'b: Reserved
sel_dmic3_lpf_l_edge	5	R/W	0'h	DMIC3 Data Left Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic3_lpf_r_edge	4	R/W	1'h	DMIC3 Data Right Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic2_lpf_l_edge	3	R/W	0'h	DMIC2 Data Left Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic2_lpf_r_edge	2	R/W	1'h	DMIC2 Data Right Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic1_lpf_l_edge	1	R/W	0'h	DMIC1 Data Left Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge

Name	Bits	Read/Write	Reset State	Description
sel_dmic1_lpf_r_edge	0	R/W	1'h	DMIC1 Data Right Channel Source Control (Asynchronous Mode) 0'b: Latch from falling edge 1'b: Latch from rising edge

9.51. MX-77h: TDM Interface Control 1

Default: 0C00'h

Table 67. MX-77h: TDM Interface Control 1

Name	Bits	Read/Write	Reset State	Description
reserved	15	R/W	0'h	Reserved
mode_sel	14	R/W	0'h	I2S / TDM Mode Control 0'b: Normal I2S Mode 1'b: TDM Mode
Tdmslot_sel	13:12	R/W	0'h	TDM Channel Number Select 00'b: 2ch 01'b: 4ch 10'b: 6ch 11'b: 8ch
Channel_length	11:10	R/W	3'h	TDM Channel Length 00'b: 16bit (For Slave Mode and Master Mode) 01'b: 20bit (For Slave Mode) 10'b: 24bit (For Slave Mode) 11'b: 32bit (For Slave Mode and Master Mode)
rx_adc_data_sel	9	R/W	0'h	ADC Data to ADCDAT Data Location 0'b: 1L/1R/2L/2R/3L/3R/4L/4R 1'b: 2L/2R/1L/1R/4L/4R/3L/3R
reserved	8	R	0'h	Reserved
sel_i2s_rx_ch2	7:6	R/W	0'h	Data Swap for Slot0/1 in ADCDAT1 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
sel_i2s_rx_ch4	5:4	R/W	0'h	Data Swap for Slot2/3 in ADCDAT1 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
sel_i2s_rx_ch6	3:2	R/W	0'h	Data Swap for Slot4/5 in ADCDAT1 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R

Name	Bits	Read/Write	Reset State	Description
sel_i2s_rx_ch8	1:0	R/W	0’h	Data Swap for Slot6/7 in ADCDAT1 00’b: L/R 01’b: R/L 10’b: L/L 11’b: R/R

9.52. MX-78h: TDM Interface Control 2

Default: 4000’h

Table 68. MX-78h: TDM Interface Control 2

Name	Bits	Read/Write	Reset State	Description
sel_i2s_lrck_polarity	15	R/W	0’h	TDM Interface LRCK Polarity Inverter 0’b: Normal 1’b: Invert
reserved	14:12	R/W	4’h	Reserved
lrck_pulse_sel	11	R/W	0’h	LRCK Pulse Width Select (Master Mode Only) 0’b: One BCLK width 1’b: One channel slot width
reserved	10:8	R/W	0’h	Reserved
mute_tdm2_outl	7	R/W	0’h	IF1_ADC1 Left Data Mute/Un-mute Control 0’b : Un-Mute 1’b : Mute
mute_tdm2_outr	6	R/W	0’h	IF1_ADC1 Right Data Mute/Un-mute Control 0’b : Un-Mute 1’b : Mute
mute_tdm4_outl	5	R/W	0’h	IF1_ADC2 Left Data Mute/Un-mute Control 0’b : Un-Mute 1’b : Mute
mute_tdm4_outr	4	R/W	0’h	IF1_ADC2 Right Data Mute/Un-mute Control 0’b : Un-Mute 1’b : Mute
mute_tdm6_outl	3	R/W	0’h	IF1_ADC3 Left Data Mute/Un-mute Control 0’b : Un-Mute 1’b : Mute
mute_tdm6_outr	2	R/W	0’h	IF1_ADC3 Right Data Mute/Un-mute Control 0’b : Un-Mute 1’b : Mute
mute_tdm8_outl	1	R/W	0’h	IF1_ADC4 Left Data Mute/Un-mute Control 0’b : Un-Mute 1’b : Mute

Name	Bits	Read/Write	Reset State	Description
mute_tdm8_outr	0	R/W	0'h	IF1_ADC4 Right Data Mute/Un-mute Control 0'b : Un-Mute 1'b : Mute

9.53. MX-79h: TDM Interface Control 3

Default: 0123'h

Table 69. MX-79h: TDM Interface Control 3

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R	0'h	Reserved
sel_i2s_tx_l_ch2	14:12	R/W	0'h	IF1_DAC1_L Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
Reserved	11	R	0'h	Reserved
sel_i2s_tx_r_ch2	10:8	R/W	1'h	IF1_DAC1_R Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
Reserved	7	R	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
sel_i2s_tx_l_ch4	6:4	R/W	2'h	IF1_DAC2_L Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
Reserved	3	R	0'h	Reserved
sel_i2s_tx_r_ch4	2:0	R/W	3'h	IF1_DAC2_R Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7

9.54. MX-7Fh: Clock Control 1

Default: 1100'h

Table 70. MX-7Fh: Clock Control 1

Name	Bits	Read/Write	Reset State	Description
Reserved	15:4	R	110'h	Reserved
sel_dsp_asrc0	3:0	R/W	0'h	Select the Clock Source for DSP 0000'b: clk_sys 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: Reserved 0100'b: Reserved 0101'b: clk_sys2 Others: Reserved

9.55. MX-80h: Global Clock Control

Default: 0000’h

Table 71. MX-80h: Global Clock Control

Name	Bits	Read/Write	Reset State	Description
sel_sysclk1	15:14	R/W	0’h	System Clock Source MUX Control 00’b: MCLK 01’b: PLL 10’b: Internal Clock 11’b: Reserved
sel_pll_sour	13:11	R/W	0’h	PLL Source Selection 000’b: From MCLK 001’b: From BCLK1 010’b: From BCLK2 Others: Reserved
reserved	10:4	R	0’h	Reserved
sel_pll_pre_div	3	R/W	0’h	PLL Pre-Divider 0’b: ÷ 1 1’b: ÷ 2
reserved	2:0	R	0’h	Reserved

9.56. MX-81h: PLL Control 1

Default: 0000’h

Table 72. MX-81h: PLL Control 1

Name	Bits	Read/Write	Reset State	Description
Pll_n_code	15:7	R/W	0’h	PLL N[8:0] Code 000000000’b: Div 2 000000001’b: Div 3 … 111111111’b: Div 513
Reserved	6:5	R	0’h	Reserved
Pll_k_code	4:0	R/W	0’h	PLL K[4:0] Code 00000’b: Div 2 00001’b: Div 3 … 11111’b: Div 33

9.57. MX-82h: PLL Control 2

Default: 0000’h

Table 73. MX-82h: PLL Control 2

Name	Bits	Read/Write	Reset State	Description
Pll_m_code	15:12	R/W	0’h	PLL M[3:0] Code 0000’b: Div 2 0001’b: Div 3 … 1111’b: Div 17
Pll_m_bypass	11	R/W	0’h	Bypass PLL M Code 0’b : No bypass 1’b : Bypass
Reserved	10:0	R	0’h	Reserved

9.58. MX-83h: ASRC Control 1

Default: 0000’h

Table 74. MX-83h: ASRC Control 1

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R	0’h	Reserved
En_i2s2_asrc	12	R/W	0’h	Enable I2S2 ASRC Function 0’b: Disable 1’b: Enable
En_i2s1_asrc	11	R/W	0’h	Enable I2S1 ASRC Function 0’b: Disable 1’b: Enable
Sel_stereo_dac_mode	10	R/W	0’h	Enable DAC ASRC for Stereo DAC 0’b : Disable 1’b : Enable
Sel_mono_dac_l_mode	9	R/W	0’h	Enable DAC ASRC for mono left path 0’b : Disable 1’b : Enable
Sel_mono_dac_r_mode	8	R/W	0’h	Enable DAC ASRC for mono right path 0’b : Disable 1’b : Enable
en_dmic_asrc_stereo1	7	R/W	0’h	Enable DMIC ASRC for stereo1 path 0’b : Disable 1’b : Enable

Name	Bits	Read/Write	Reset State	Description
en_dmic_asrc_stereo2	6	R/W	0'h	Enable DMIC ASRC for stereo2 path 0'b : Disable 1'b : Enable
en_dmic_asrc_monol	5	R/W	0'h	Enable DMIC ASRC for mono left path 0'b : Disable 1'b : Enable
en_dmic_asrc_monor	4	R/W	0'h	Enable DMIC ASRC for mono right path 0'b : Disable 1'b : Enable
en_adc_asrc_stereo1	3	R/W	0'h	Enable ADC ASRC for stereo1 path 0'b : Disable 1'b : Enable
en_adc_asrc_stereo2	2	R/W	0'h	Enable ADC ASRC for stereo2 path 0'b : Disable 1'b : Enable
en_adc_asrc_monol	1	R/W	0'h	Enable ADC ASRC for mono left path 0'b : Disable 1'b : Enable
en_adc_asrc_monor	0	R/W	0'h	Enable ADC ASRC for mono right path 0'b : Disable 1'b : Enable

9.59. MX-84h: ASRC Control 2

Default: 0000'h

Table 75. MX-84h: ASRC Control 2

Name	Bits	Read/Write	Reset State	Description
sel_da_filter_stereo_asrc	15:12	R/W	0'h	Select the ASRC Clock Source for DA Stereo Filter 0000'b : CLK_sys 0001'b : clk_i2s1_asrc 0010'b : clk_i2s2_asrc 0011'b : Reserved 0100'b : Reserved 0101'b : clk_sys2 Others: Reserved
sel_da_filter_monol_asrc	11:8	R/W	0'h	Select the ASRC Clock Source for DA Mono Left Filter 0000'b: clk_sysy_div_out 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: Reserved 0100'b: Reserved 0101'b: clk_sys2 Others: Reserved

Name	Bits	Read/Write	Reset State	Description
sel_da_filter_monor_asrc	7:4	R/W	0'h	Select the ASRC Clock Source for DA Mono Right Filter 0000'b: clk_sysy_div_out 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: Reserved 0100'b: Reserved 0101'b: clk_sys2 Others: Reserved
sel_ad_filter_stereo1_asrc	3:0	R/W	0'h	Select the ASRC Clock Source for AD Stereo1 Filter 0000'b: clk_sysy_div_out 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: Reserved 0100'b: Reserved 0101'b: clk_sys2 Others: Reserved

9.60. MX-85h: ASRC Control 3

Default: 0000'h

Table 76. MX-85h: ASRC Control 3

Name	Bits	Read/Write	Reset State	Description
sel_up_filter_asrc	15:12	R/W	0'h	Select the ASRC Clock Source for Up Sample Rate Filter 0000'b: clk_sysy_div_out 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: Reserved 0100'b: Reserved 0101'b: clk_sys2 Others: Reserved
sel_down_filter_asrc	11:8	R/W	0'h	Select the ASRC Clock Source for Down Sample Rate Filter 0000'b: clk_sysy_div_out 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: Reserved 0100'b: Reserved 0101'b: clk_sys2 Others: Reserved

Name	Bits	Read/Write	Reset State	Description
sel_ad_filter_monol_asrc	7:4	R/W	0'h	Select the ASRC Clock Source for AD Mono Left Filter 0000'b: clk_sysy_div_out 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: Reserved 0100'b: Reserved 0101'b: clk_sys2 Others: Reserved
sel_ad_filter_monor_asrc	3:0	R/W	0'h	Select the ASRC Clock Source for AD Mono Right Filter 0000'b: clk_sysy_div_out 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: Reserved 0100'b: Reserved 0101'b: clk_sys2 Others: Reserved

9.61. MX-8Ah: ASRC Control 4

Default: 0000'h

Table 77. MX-8Ah: ASRC Control 4

Name	Bits	Read/Write	Reset State	Description
i2s1_asrc_prediv	15:14	R/W	0'h	Set the I2S1 Clock Division for ASRC Mode 00'b: div1 01'b: div2 10'b: div3 11'b: reserved
sel_i2s1_asrc	13:12	R/W	0'h	Select the ASRC source of ASRC 00'b: ASRC1 01'b: ASRC2 10'b: Reserved 11'b: Reserved
i2s2_asrc_prediv	11:10	R/W	0'h	Set the I2S2 Clock Division for ASRC Mode 00'b: div1 01'b: div2 10'b: div3 11'b: Reserved
sel_i2s2_asrc	9:8	R/W	0'h	Select the ASRC Source of I2S2 00'b: ASRC1 01'b: ASRC2 10'b: Reserved 11'b: Reserved
reserved	7:0	R/W	0'h	Reserved

9.62. MX-8Ch: ASRC Control 5

Default: 0007'h

Table 78. MX-8Ch: ASRC Control 5

Name	Bits	Read/Write	Reset State	Description
sel_ad_filter_stereo2_asrc	15:12	R/W	0'h	Select the ASRC Clock Source for AD Stereo2 Filter 0000'b: clk_sysy_div_out 0001'b: clk_i2s1_asrc 0010'b: clk_i2s2_asrc 0011'b: Reserved 0100'b: Reserved 0101'b: clk_sys2 Others: Reserved
reserved	11:0	R/W	7'h	Reserved

9.63. MX-8Eh: HP Amp Control 1

Default: 0004'h

Table 79. MX-8Eh: HP Amp Control 1

Name	Bits	Read/Write	Reset State	Description
Smttrig_hp	15	R/W	0'h	Enable Softgen Trigger for Soft Mute Depop 0'b: Disable 1'b: Enable
reserved	14:10	R/W	0'h	Reserved
En_smt_l_hp	9	R/W	0'h	Enable HP_L Mute/Un-Mute Depop 0'b: Disbale 1'b: Enable
En_smt_r_hp	8	R/W	0'h	Enable HP_R Mute/Un-Mute Depop 0'b: Disbale 1'b: Enable
Pdn_hp	7	R/W	0'h	Capless Depop Power Down Control 0'b: Disbale 1'b: Enable
Softgen_rstn	6	R/W	0'h	Reset Softgen to Initialize SOFTP=1 0'b: Disbale 1'b: Reset
Softgen_rstp	5	R/W	0'h	Reset Softgen to Initialize SOFTP=0 0'b: Disbale 1'b: Reset
En_out_hp	4	R/W	0'h	Enable Headphone Output 0'b: Disable 1'b: Enable

Name	Bits	Read/Write	Reset State	Description
Pow_pump_hp	3	R/W	0'h	Charge Pump Power Control 0'b: Power Down 1'b: Power On
En_softgen_hp	2	R/W	1'h	Power On Soft Generator 0'b: Power down 1'b: Power on
reserved	1	R/W	0'h	Reserved
Pow_capless	0	R/W	0'h	HP Amp All Power On Control 0'b: Power Down 1'b: Power On

9.64. MX-8Fh: HP Amp Control 2

Default: 1100'h

Table 80. MX-8Fh: HP Amp Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0'h	Reserved
Depop_mode_hp	13	R/W	0'h	Select HP Depop Mode 0'b: Depop mode 1 1'b: Depop mode 2
reserved	12:7	R/W	22'h	Reserved
En_depop_mode1	6	R/W	0'h	HP Depop Mode 1 Control 0'b: Disbale 1'b: Enable
reserved	5:0	R/W	0'h	Reserved

9.65. MX-93h: MICBIAS Control

Default: 0000'h

Table 81. MX-93h: MICBIAS Control

Name	Bits	Read/Write	Reset State	Description
Sel_micbias1	15	R/W	0'h	MICBIAS1 Output Voltage Control 0'b: 0.9 * MICVDD 1'b: 0.75 * MICVDD
reserved	14:12	R/W	0'h	Reserved
Pow_mic1_ovcd	11	R/W	0'h	MICBIAS1 Short Current Detector Control 0'b: Disable 1'b: Enable
Mic1_ovcd_th_sel	10:9	R/W	0'h	MICBIAS1 Short Current Detector Threshold 00'b: 640uA 01'b: 1280uA 1x'b: 1920uA Note: tolerance is 200uA
reserved	8:6	R/W	0'h	reserved

Name	Bits	Read/Write	Reset State	Description
Ckn_micbias	5	R/W	0’h	MICBIAS Clock Power 0’b: Disable 1’b: Enable
Pow_clk_int	4	R/W	0’h	Internal Clock Power 0’b: Disable 1’b: Enable
Sel_irq_debounce	3	R/W	0’h	Select IRQ De-bounce Clock 0’b: MCLK 1’b: Internal clock
reserved	2:0	R	0’h	reserved

9.66. MX-AEh: ADC Path EQ Control 1

Default: 6000’h

Table 82. MX-AEh: ADC Path EQ Control 1

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R	0’h	Reserved
ad_eq_param_update	14	R/W	1’h	ADC Path EQ Parameter Update Control 0’b: Busy (Waiting for cross) 1’b: Stand-by Write “1” to update parameter
Reserved	13:6	R/W	80’h	Reserved
Ad_eq_hpf1_status	5	R	0’h	ADC Path EQ High Pass Filter (HPF1) Status. 0’b: Normal 1’b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Ad_eq_bpf4_status	4	R	0’h	ADC Path EQ Band-4 (BP4) Status. 0’b: Normal 1’b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Ad_eq_bpf3_status	3	R	0’h	ADC Path EQ Band-3 (BP3) Status. 0’b: Normal 1’b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.

Name	Bits	Read/Write	Reset State	Description
Ad_eq_bpf2_status	2	R	0'h	ADC Path EQ Band-2 (BP2) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Ad_eq_bpf1_status	1	R	0'h	ADC Path EQ Band-1 (BP1) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Ad_eq_lpf_status	0	R	0'h	ADC Path EQ Low Pass Filter (LPF) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.

9.67. MX-AFh: ADC Path EQ Control 2

Default: 0000'h

Table 83. MX-AFh: ADC Path EQ Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:9	R	0'h	Reserved
ad_eq_lpf_tpy	8	R/W	0'h	ADC Path 1st EQ Low Pass Filter Mode Control (LPF) 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)
ad_eq_hpf1_tpy	7	R/W	0'h	ADC Path 1st EQ High Pass Filter1 Mode Control (HPF1) 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
Reserved	6	R	0'h	Reserved
ad_eq_hpf1_en	5	R/W	0'h	ADC Path EQ 1st High Pass Filter (HPF1) Control. 0'b: Disabled (bypass) and reset 1'b: Enabled
ad_eq_bpf4_en	4	R/W	0'h	ADC Path 2nd EQ Band-4 (BP4) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Ad_eq_bpf3_en	3	R/W	0'h	ADC Path 2nd EQ Band-3 (BP3) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.

Name	Bits	Read/Write	Reset State	Description
Ad_eq_bpf2_en	2	R/W	0'h	ADC Path 2nd EQ Band-2 (BP2) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Ad_eq_bpf1_en	1	R/W	0'h	ADC Path 2nd EQ Band-1 (BP1) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Ad_eq_lpf_en	0	R/W	0'h	ADC Path 1st EQ Low Pass Filter (LPF) Filter Control. 0'b: Disabled and reset 1'b: Enabled.

9.68. MX-B0h: DAC Path EQ Control 1

Default: 6000'h

Table 84. MX-B0h: DAC Path EQ Control 1

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	Reserved
Da_eq_param_update	14	R/W	1'h	DAC Path EQ parameter update control 0'b: Busy (Waiting for cross) 1'b: Stand-by Write "1" to update parameter
reserved	13:8	R/W	20'h	Reserved
Da_eq_lpf1_status	7	R	0'h	DAC Path EQ Low Pass Filter (LPF2) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Da_eq_hpf2_status	6	R	0'h	DAC Path EQ High Pass Filter (HPF2) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Da_eq_hpf1_status	5	R	0'h	DAC Path EQ High Pass Filter (HPF1) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.

Name	Bits	Read/Write	Reset State	Description
Da_eq_bpf4_status	4	R	0'h	DAC Path EQ Band-4 (BP4) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Da_eq_bpf3_status	3	R	0'h	DAC Path EQ Band-3 (BP3) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Da_eq_bpf2_status	2	R	0'h	DAC Path EQ Band-2 (BP2) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Eq_biquad_wclr	1	R	0'h	DAC Path EQ Band-1 (Biquad Type) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
Reserved	0	R	0'h	Reserved

9.69. MX-B1h: EQ Control 2

Default: 0000'h

Table 85. MX-B1h: EQ Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0'h	Reserved
Da_eq_lpf1_tpy_r	13	R/W	0'h	DAC Path Right Channel 1st EQ Low Pass Filter Mode Control (LPF2) 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)
Da_eq_lpf1_tpy_l	12	R/W	0'h	DAC Path Left Channel 1st EQ Low Pass Filter Mode Control (LPF2) 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)
Reserved	11:10	R	0'h	Reserved
Da_eq_hpf1_tpy_r	9	R/W	0'h	DAC Path Right Channel 1st EQ High Pass Filter1 Mode Control 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
Da_eq_hpf1_tpy_l	8	R/W	0'h	DAC Path Left Channel 1st EQ High Pass Filter1 Mode Control 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)

Name	Bits	Read/Write	Reset State	Description
Da_eq_lpf1_en	7	R/W	0'h	DAC Path 1st EQ Low Pass Filter (LPF2) Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Da_eq_hpf2_en	6	R/W	0'h	DAC Path EQ 2nd High Pass Butterworth Filter (HPF) Control. 0'b: Disabled (bypass) and reset 1'b: Enabled
Da_eq_hpf1_en	5	R/W	0'h	DAC Path EQ 1st High Pass Filter (HPF1) Control. 0'b: Disabled (bypass) and reset 1'b: Enabled
Da_eq_bpf4_en	4	R/W	0'h	DAC Path 2nd EQ Band-4 (BP4) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Da_eq_bpf3_en	3	R/W	0'h	DAC Path 2nd EQ Band-3 (BP3) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Da_eq_bpf2_en	2	R/W	0'h	DAC Path 2nd EQ Band-2 (BP2) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Eq_biquad_en	1	R/W	0'h	DAC Path 2nd EQ Band-1 (Biquad Type) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Reserved	0	R	0'h	Reserved

9.70. MX-B2h: DRC Control 1

Default: 0000'h

Table 86. MX-B2h: DRC Control 1

Name	Bits	Read/Write	Reset State	Description
Reserved	15:7	R	0'h	Reserved
Alc_thmin_fast_rc_en	6	R/W	0'h	DRC THMIN Mode Fast Recover Control 0'b: Disable fast recover 1'b: Enable fast recover
Alc_thmin	5:0	R/W	0'h	DRC THMIN Mode Threshold Level Control 00'h: -60dB 01'h: -60.75dB 02'h: -61.5dB … 2E'h: -94.5dB, 0.75dB/Step

9.71. MX-B3h: DRC Control 2

Default: 001F'h

Table 87. MX-B3h: DRC Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	Reserved
Alc_noise_gate_ht	14:12	R/W	0'h	ALC Noise Gate Hold Time Control 000'b: 0 sample 001'b: 128 samples 010'b: 256 samples … 111'b: 896 samples
alc_ft_boost	11:6	R/W	0'h	ALC Digital Pre-BOOST (0.75dB/step) 00'h= 0dB 01'h= 0.75dB 02'h= 1.5dB 03'h= 2.25dB … 27'h= 29.25dBFS Others: Reserved
alc_bk_gain_r	5:0	R/W	1f'h	ALC Right Channel Digital Post-BOOST (0.375dB/step) 00'h= -11.625dB … 3F'h= 12dB

9.72. MX-B4h: DRC Control 3

Default: 2206'h

Table 88. MX-B4h: DRC Control 3

Name	Bits	Read/Write	Reset State	Description
sel_drc_agc	15:14	R/W	0'h	DRC Enable Control 00'b: Disable DRC 01'b: Enable DRC to DAC Path 10'b: Disable DRC 11'b: Enable DRC to ADC Path
update_drc_agc_param	13	R	1'h	Update DRC Parameter Write 1'b to update all DRC parameter
sel_drc_agc_atk	12:8	R/W	2'h	Select DRC attack rate (0.375dB/TU)❶ 00'h: 83 uSec 01'h: 0.167 mSec … 10'h: 5.46 Sec Others: Reserved

Name	Bits	Read/Write	Reset State	Description
Drc_agc_rate_sel	7:5	R/W	0'h	DRC Rate Control for Sample Rate Change❸ 001'b: 48kHz 010'b: 96kHz 011'b: 192kHz 101'b: 44.1kHz 110'b: 88.2kHz 111'b: 176.4kHz Others: Reserved
sel_rc_rate	4:0	R/W	6'h	Select DRC recovery rate (0.375dB/TU)❷ 00'h: 83 uSec 01'h: 0.167 mSec … 10'h: 5.46 Sec Others: Reserved

❶ attack time=(4*2^n)/Sample_Rate, n=MX-B4[12:8], default=0.33mS
❷ recovery time=(4*2^n)/Sample_Rate, n= MX-B4 [4:0], default=5.3mS
❸ When change I2S's sample rate, the DRC/AGC rate control is need to be changed same with I2S's sample rate. When change the DRC/AGC rate, the parameter of DRC/AGC isn't need be modified.
When I2S's sample rate is below 48kHz, that need to set the DRC/AGC rate to 48kHz and re-calculate the DRC/AGC's parameter by I2S's sample rate.

9.73. MX-B5h: DRC Control 4

Default: 1F00'h

Table 89. MX-B5h: DRC Control 4

Name	Bits	Read/Write	Reset State	Description
Alc_drc_ratio_sel2	15:14	R/W	0'h	DRC Compression-2 Ratio Selection 00'b: 1:1 01'b: 1:2 10'b: 1:4 11'b: 1:8
sel_drc_agc_post_bst	13:8	R/W	1f'h	DRC Digital Post-Boost Gain (0.375dB/step)❶ 00'h= -11.625dB … 3F'h= 12dB Others: Reserved

Name	Bits	Read/Write	Reset State	Description
En_drc_agc_compress	7	R/W	0'h	DRC Compression Function Control 0'b: Disable 1'b: Enable
Sel_ratio	6:5	R/W	0'h	DRC Compression Ratio Selection 00'b: 1:1 01'b: 1:2 10'b: 1:4 11'b: 1:8
Alc_noise_gate_drop_en	4	R/W	0'h	DRC Noise Gate Drop Mode Control 0'b: Disable 1'b: Enable
Reserved	3:2	R	0'h	Reserved
noise_gate_ratio_sel	1:0	R/W	0'h	DRC Expansion Ratio Control when Noise Gate is Enabled 00'b: 1:1 01'b: 2:1 10'b: 4:1 11'b: 8:1

❶Gain table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-11.625	16	10	-5.625	32	20	0.375	48	30	6.375	64	40	
1	1	-11.25	17	11	-5.25	33	21	0.75	49	31	6.75	65	41	
2	2	-10.875	18	12	-4.875	34	22	1.125	50	32	7.125	66	42	
3	3	-10.5	19	13	-4.5	35	23	1.5	51	33	7.5	67	43	
4	4	-10.125	20	14	-4.125	36	24	1.875	52	34	7.875	68	44	
5	5	-9.75	21	15	-3.75	37	25	2.25	53	35	8.25	69	45	
6	6	-9.375	22	16	-3.375	38	26	2.625	54	36	8.625	70	46	
7	7	-9	23	17	-3	39	27	3	55	37	9	71	47	
8	8	-8.625	24	18	-2.625	40	28	3.375	56	38	9.375	72	48	
9	9	-8.25	25	19	-2.25	41	29	3.75	57	39	9.75	73	49	
10	A	-7.875	26	1A	-1.875	42	2A	4.125	58	3A	10.125	74	4A	
11	B	-7.5	27	1B	-1.5	43	2B	4.5	59	3B	10.5	75	4B	
12	C	-7.125	28	1C	-1.125	44	2C	4.875	60	3C	10.875	76	4C	
13	D	-6.75	29	1D	-0.75	45	2D	5.25	61	3D	11.25			
14	E	-6.375	30	1E	-0.375	46	2E	5.625	62	3E	11.625			
15	F	-6	31	1F	0	47	2F	6	63	3F	12			

9.74. MX-B6h: DRC Control 5

Default: 0000’h

Table 90. MX-B6h: DRC Control 5

Name	Bits	Read/Write	Reset State	Description
Noise_gate_boost	15:12	R/W	0’h	Select Compensation Gain When Signal is Below Noise Gate 0’h: 0dB 1’h: 3dB 2’h: 6dB … E’h: 42dB F’h: 45dB
Reserved	11:7	R	0’h	Reserved
en_drc_agc_noise_gate	6	R/W	0’h	Enable Noise Gate function 0’b: Diaable 1’b: Enable
En_drc_agc_noise_gate_hold	5	R/W	0’h	Enable Noise Gate Hold Data Function 0’b: Disable 1’b: Enable
sel_drc_agc_noise_th	4:0	R/W	0’h	Noise Gate Threshold (-1.5dB/step) 00’h: -24dBFS 01’h: -25.5dBFS …….. 1F’h: -70.5 dBFS

9.75. MX-B7h: DRC Control 6

Default: 0000’h

Table 91. MX-B7h: DRC Control 6

Name	Bits	Read/Write	Reset State	Description
Reserved	15:12	R	0’h	Reserved

Name	Bits	Read/Write	Reset State	Description
alc_thmax2	11:6	R/W	0'h	DRC Limiter Threshold 2 Control (0.75dB/step) 00'h= 0dBFS 01'h= -0.75dBFS 02'h= -1.5dBFS 03'h= -2.25dBFS …….. 1F'h= -45dBFS
alc_thmax	5:0	R/W	0'h	DRC Limiter Threshold Control (0.375dB/step) 00'h= 0dBFS 01'h= -0.375dBFS 02'h= -0.75dBFS 03'h= -1.125dBFS …….. 1F'h= -23.625dBFS

9.76. MX-BBh: Jack Detection Control 1

Default: 0000'h

Table 92. MX-BBh: Jack Detection Control 1

Name	Bits	Read/Write	Reset State	Description
sel_gpio_jd1	15:13	R/W	0'h	GPIO Jack Detect – 1 Source Selection 000'b: OFF 001'b: GPIO3 010'b: GPIO4 011'b: GPIO5 100'b: GPIO6 101'b: Reserved 110'b: Reserved 111'b: Reserved
reserved	12	R	0'h	reserved
en_jd_hpo	11	R/W	0'h	Enable jack detect trigger HPOUT 0'b: Disable 1'b: Enable

Name	Bits	Read/Write	Reset State	Description
polarity_jd_tri_hpo	10	R/W	0'h	Select jack detect polarity trigger HPOUT 0'b: Low trigger 1'b: High trigger
en_jd_spk_l	9	R/W	0'h	Enable jack detect trigger SPK_L 0'b: Disable 1'b: Enable
polarity_jd_tri_spk_l	8	R/W	0'h	Select jack detect polarity trigger SPK_L 0'b: Low trigger 1'b: High trigger
en_jd_spk_r	7	R/W	0'h	Enable jack detect trigger SPK_R 0'b: Disable 1'b: Enable
polarity_jd_tri_spk_r	6	R/W	0'h	Select jack detect polarity trigger SPK_R 0'b: Low trigger 1'b: High trigger
Reserved	5:4	R/W	0'h	Reserved
en_jd_lout1	3	R/W	0'h	Enable jack detect trigger LOUT1 0'b: Disable 1'b: Enable
polarity_jd_tri_lout1	2	R/W	0'h	Select jack detect polarity trigger LOUT1 0'b: Low trigger 1'b: High trigger
Reserved	1:0	R	0'h	Reserved

9.77. MX-BDh: IRQ Control 1

Default: 0000'h

Table 93. MX-BDh: IRQ Control 1

Name	Bits	Read/Write	Reset State	Description
en_irq_gpio_jd1	15	R/W	0'h	IRQ Output Source Configure of GPIO Jack Detection 1 Status 0'b: bypass 1'b: Normal
en_gpio_jd1_sticky	14	R/W	0'h	Sticky Control for GPIO Jack Detect 1 0'b: Disable 1'b: Enable
inv_gpio_jd1	13	R/W	0'h	GPIO Jack Detection 1 Status Polarity 0'b: Normal 1'b: Output Invert
reserved	12:10	R/W	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
en_irq_jd1_1	9	R/W	0'h	IRQ Output Source Configure of JD1_1 Jack Detection Status 0'b: bypass 1'b: Normal
en_jd1_1_sticky	8	R/W	0'h	Sticky Control for JD1_1 Jack Detect 0'b: Disable 1'b: Enable
inv_jd1_1	7	R/W	0'h	JD1_1 Jack Detection Status Polarity 0'b: Normal 1'b: Output Invert
en_irq_jd1_2	6	R/W	0'h	IRQ Output Source Configure of JD1_2 Jack Detection Status 0'b: bypass 1'b: Normal
en_jd1_2_sticky	5	R/W	0'h	Sticky Control for JD1_2 Jack Detect 0'b: Disable 1'b: Enable
inv_jd1_2	4	R/W	0'h	JD1_2 Jack Detection Status Polarity 0'b: Normal 1'b: Output Invert
en_irq_jd2	3	R/W	0'h	IRQ Output Source Configure of JD2 Jack Detection Status 0'b: bypass 1'b: Normal
en_jd2_sticky	2	R/W	0'h	Sticky Control for JD2 Jack Detect 0'b: Disable 1'b: Enable
inv_jd2	1	R/W	0'h	JD2 Jack Detection Status Polarity 0'b: Normal 1'b: Output Invert
reserved	0	R	0'h	Reserved

9.78. MX-BEh: IRQ Control 2

Default: 0000'h

Table 94. MX-BEh: IRQ Control 2

Name	Bits	Read/Write	Reset State	Description
en_irq_micbias1_ovcd	15	R/W	0'h	IRQ Output Source Configure of MICBIAS1 Over Current Status 0'b: bypass 1'b: Normal
reserved	14	R/W	0'h	Reserved
en_micbias1_ovcd_sticky	13	R/W	0'h	Sticky Control for MICBIAS1 Over Current 0'b: Disable 1'b: Enable

Name	Bits	Read/Write	Reset State	Description
reserved	12	R/W	0’h	Reserved
inv_micbias1_ovcd	11	R/W	0’h	MICBIAS1 over current status polarity 0’b: Normal 1’b: Output Invert
reserved	10	R/W	0’h	Reserved
Sta_micbias1_ovcd	9	R	0’h	MICBIAS1 over current status Read: return status of each status pin Write: Write ‘0’ to clear stick bit
reserved	8	R/W	0’h	Reserved
sta_vad_fg_hold	7	R	0’h	Status of VAD Flag Read: Return status of Jack Detect Select output Write: Write ‘0’ to clear stick bit
en_irq_vad_fg_hold	6	R/W	0’h	IRQ output source configure of VAD Flag jack detection status 0’b: bypass 1’b: Normal
en_vad_fg_hold_sticky	5	R/W	0’h	Sticky Control for VAD Flag Jack Detect 0’b: Disable 1’b: Enable
inv_vad_fg_hold	4	R/W	0’h	VAD Flag Status Polarity 0’b: Normal 1’b: Output Invert
reserved	3:0	R/W	0’h	Reserved

9.79. MX-BFh: IRQ Control 3

Default: 0000’h

Table 95. MX-BFh: IRQ Control 3

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0’h	Reserved
sta_jd2	14	R	0’h	Status of JD2 Jack detection . Read: Return status of Jack Detect Select output Write: Write ‘0’ to clear stick bit

Name	Bits	Read/Write	Reset State	Description
sta_jd1_2	13	R	0'h	Status of JD1_2 Jack detection . Read: Return status of Jack Detect Select output Write: Write '0' to clear stick bit
sta_jd1_1	12	R	0'h	Status of JD1_1 Jack detection . Read: Return status of Jack Detect Select output Write: Write '0' to clear stick bit
reserved	11	R	0'h	Reserved
sta_gpio6	10	R	0'h	GPIO6 Pin Status Read: return status of each GPIO pin
sta_gpio5	9	R	0'h	GPIO5 Pin Status Read: return status of each GPIO pin
sta_gpio1	8	R	0'h	GPIO1 Pin Status Read: return status of each GPIO pin
sta_gpio2	7	R	0'h	GPIO2 Pin Status Read: return status of each GPIO pin
sta_gpio3	6	R	0'h	GPIO3 Pin Status Read: return status of each GPIO pin
sta_gpio4	5	R	0'h	GPIO4 Pin Status Read: return status of each GPIO pin
sta_gpio_jd1	4	R	0'h	Status of GPIO Jack detection 1 Read: Return status of Jack Detect Select output Write: Write '0' to clear stick bit
en_irq_inline	3	R/W	0'h	IRQ Output Source Configure of InLine Command Status 0'b: bypass 1'b: Normal
sta_inline	2	R	0'h	Status of InLine Command Trigger Read: Return status of InLine Command Trigger Write: Write '0' to clear stick bit
en_inline_sticky	1	R/W	0'h	Sticky Control for InLine Command 0'b: Disable 1'b: Enable
inv_inline	0	R/W	0'h	InLine Command Status Polarity 0'b: Normal 1'b: Output Invert

9.80. MX-C0h: GPIO Control 1

Default: 0000’h

Table 96. MX-C0h: GPIO Control 1

Name	Bits	Read/Write	Reset State	Description
sel_gpio1_type	15	R/W	0’h	GPIO1 Pin Function Select 0’b: GPIO1 1’b: IRQ output
sel_gpio2_type	14	R/W	0’h	GPIO2 Pin Function Select 0’b: GPIO2 1’b: DMIC1_SCL
Reserved	13:9	R/W	0’h	Reserved
Sel_i2s2_pin	8	R/W	0’h	I2S-2 Pin Function Selection 0’b: I2S function pins 1’b: GPIO function pins
sel_gpio5_type	7	R/W	0’h	GPIO5 Pin Function Select 0’b: GPIO5 1’b: DMIC3_SDA
sel_gpio6_type	6	R/W	0’h	GPIO6 Pin Function Select 0’b: GPIO6 1’b: DMIC1_SDA
Reserved	5:0	R/W	0’h	Reserved

9.81. MX-C1h: GPIO Control 2

Default: 0000’h

Table 97. MX-C1h: GPIO Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15	R/W	0’h	Reserved
sel_gpio5	14	R/W	0’h	GPIO5 Pin Configuration 0’b: Input 1’b: Output
sel_gpio5_logic	13	R/W	0’h	GPIO5 Output Pin Control 0’b: Drive Low 1’b: Drive High
inv_gpio5	12	R/W	0’h	GPIO5 Pin Polarity 0’b: Normal 1’b: Output Invert
sel_gpio4	11	R/W	0’h	GPIO4 Pin Configuration 0’b: Input 1’b: Output
sel_gpio4_logic	10	R/W	0’h	GPIO4 Output Pin Control 0’b: Drive Low 1’b: Drive High

Name	Bits	Read/Write	Reset State	Description
inv_gpio4	9	R/W	0'h	GPIO4 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio3	8	R/W	0'h	GPIO3 Pin Configuration 0'b: Input 1'b: Output
sel_gpio3_logic	7	R/W	0'h	GPIO3 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio3	6	R/W	0'h	GPIO3 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio2	5	R/W	0'h	GPIO2 Pin Configuration 0'b: Input 1'b: Output
sel_gpio2_logic	4	R/W	0'h	GPIO2 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio2	3	R/W	0'h	GPIO2 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio1	2	R/W	0'h	GPIO1 Pin Configuration 0'b: Input 1'b: Output
sel_gpio1_logic	1	R/W	0'h	GPIO1 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio1	0	R/W	0'h	GPIO1 Pin Polarity 0'b: Normal 1'b: Output Invert

9.82. MX-C2h: GPIO Control 3

Default: 0000'h

Table 98. MX-C2h: GPIO Control 3

Name	Bits	Read/Write	Reset State	Description
reserved	15:3	R/W	0'h	Reserved
sel_gpio6	2	R/W	0'h	GPIO6 Pin Configuration 0'b: Input 1'b: Output
sel_gpio6_logic	1	R/W	0'h	GPIO6 Output Pin Control 0'b: Drive Low 1'b: Drive High

Name	Bits	Read/Write	Reset State	Description
inv_gpio6	0	R/W	0'h	GPIO6 Pin Polarity 0'b: Normal 1'b: Output Invert

9.83. MX-CFh: SounzReal™ BassBack Control

Default: 0013'h

Table 99. MX-CFh: SounzReal™ BassBack Control

Name	Bits	Read/Write	Reset State	Description
En_bb	15	R/W	0'h	Enable BassBack Function 0'b: Disable 1'b: Enable
Sel_bb_coef	14:12	R/W	0'h	Select Control for BassBack Coefficient Type 000'b: Type A 001'b: Type B 010'b: Type C 011'b: Type D 1xx'b: Reserved
Reserved	11:6	R	0'h	Reserved
Bb_boost_gain	5:0	R/W	13'h	Select Control BassBack Boost Gain 000001'b: 1.5dB 000010'b: 3dB …… 010011'b: 24dB …… 011111'b: 42dB, with 1.5dB/Step

9.84. MX-D0h: SounzReal™ TruTreble Control 1

Default: 0680'h

Table 100. MX-D0h: SounzReal™ TruTreble Control 1

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R/W	0'h	Reserved
En_mp	13	R/W	0'h	Enable TruTreble Function 0'b: Disable 1'b: Enable

Name	Bits	Read/Write	Reset State	Description
Mp_eg	12:8	R/W	6'h	TruTreble Enhanced Gain Control ❶ 00000'b: -11.625dB 00001'b: -10.5dB ……. 00110'b: -3dB ..... 10100'b: 7.5dB
reserved	7:0	R/W	80'h	Reserved

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Eg	Enhanced Gain	Eg	Enhanced Gain
1	-11.625dB	11	2.25 dB
2	-10.5 dB	12	3 dB
3	-9 dB	13	3.75 dB
4	-6.75 dB	14	4.5 dB
5	-4.5 dB	15	4.875 dB
6	-3 dB	16	5.625 dB
7	-1.875 dB	17	6 dB
8	-0.375 dB	18	6.375 dB
9	0.375 dB	19	7.125 dB
10	1.5 dB	20	7.5 dB

9.85. MX-D1h: SounzReal™ TruTreble Control 2

Default: 1C17'h

Table 101. MX-D1h: SounzReal™ l TruTreble Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0'h	Reserved
mp_hp_wt	13	R/W	0'h	Select The Harmonic Weighting 0'b: a = 1/4(default) 1'b: a = 1/2
mp_og	12:8	R/W	1C'h	Select The Origin Signal Gain 00000'b: -5.8125dB 00001'b: -5.625dB … 10111'b: -0.5625 dB ... 11111'b: 12dB, with 0.1875dB/Step
reserved	7:6	R	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
mp_hg	5:0	R/W	17'h	Select High Frequency Harmonic Gain (0.375 /step) 000000'b: -11.625dB 000001'b: -11.25dB … 010111'b: -3dB ... 111111'b: 12dB, with 0.375dB/Step

9.86. MX-D3h: Stereo1 ADC Wind Filter Control 1

Default: A220'h

Table 102. MX-D3h: Stereo1 ADC Wind Filter Control 1

Name	Bits	Read/Write	Reset State	Description
adj_hpf_2nd_en_stereo1	15	R/W	1'h	Stereo1 ADC Wind Filter Enable Control 0'b : Disable and bypass 1'b : Enable
adj_hpf_coef_l_sel_stereo1	14:12	R/W	2'h	Stereo1 ADC Wind Filter Left Channel Coefficient Coarse Selection 000'b : fs=8k, fc = 20~2000Hz fs=12k, fc = 30~3000Hz fs=16k, fc = 40~4000Hz 001'b : fs=24k, fc = 30~2458Hz fs=32k, fc = 40~3278Hz 010'b : fs=44.1k, fc = 28~1992Hz fs=48k, fc = 30~2168Hz 011'b : fs=88.2k, fc = 28~1869Hz fs=96k, fc = 30~2034Hz 100'b : fs=176.4k, fc = 27~1811Hz fs=192k, fc = 30~1971Hz Others: Reserved
Reserved	11	R	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
adj_hpf_coef_r_sel_stereo1	10:8	R/W	2'h	Stereo1 ADC Wind Filter Right Channel Coefficient Coarse Selection 000'b : fs=8k, fc = 20~2000Hz fs=12k, fc = 30~3000Hz fs=16k, fc = 40~4000Hz 001'b : fs=24k, fc = 30~2458Hz fs=32k, fc = 40~3278Hz 010'b : fs=44.1k, fc = 28~1992Hz fs=48k, fc = 30~2168Hz 011'b : fs=88.2k, fc = 28~1869Hz fs=96k, fc = 30~2034Hz 100'b : fs=176.4k, fc = 27~1811Hz fs=192k, fc = 30~1971Hz Others: Reserved
reserved	7:0	R/W	20'h	Reserved

9.87. MX-D4h: Stereo1 ADC Wind Filter Control 2

Default: 0000'h

Table 103. MX-D4h: Stereo1 ADC Wind Filter Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0'h	Reserved
adj_hpf_coef_l_num_stereo1	13:8	R/W	0'h	Stereo1 ADC Wind Filter Right Channel Coefficient Fine Selection (0~63)
reserved	7:6	R	0'h	Reserved
adj_hpf_coef_r_num_stereo1	5:0	R/W	0'h	Stereo1 ADC Wind Filter Left Channel Coefficient Fine Selection (0~63)

9.88. MX-D9h: Soft Volume & ZCD Control 1

Default: 0809'h

Table 104. MX-D9h: Soft Volume & ZCD Control 1

Name	Bits	Read/Write	Reset State	Description
en_softvol	15	R/W	0'h	Digital Soft Volume Delay Control 0'b: Disable 1'b: Enable

Name	Bits	Read/Write	Reset State	Description
reserved	14	R/W	0’h	Reserved
en_o_svol	13	R/W	0’h	OUTVOLL/R Soft Volume Delay Control 0’b: Disable 1’b: Enable
en_hpo_svol	12	R/W	0’h	HPOVOLL/R Soft Volume Delay Control 0’b: Disable 1’b: Enable
en_zcd_digital	11	R/W	1’h	Digital Volume Zero Crossing Detection Control 0’b: Disable 1’b: Enable
pow_zcd	10	R/W	0’h	Power On Zero Crossing 0’b: Power Down 1’b: Power On
reserved	9:4	R	0’h	Reserved
sel_svol	3:0	R/W	9’h	Soft Volume Change Delay Time 0000: 1 SVSYNC 0001: 2 SVSYNC 0010: 4 SVSYNC 0011: 8 SVSYNC 0100: 16 SVSYNC 0101: 32 SVSYNC 0110: 64 SVSYNC 0111: 128 SVSYNC 1000: 256 SVSYNC 1001: 512 SVSYNC 1010: 1024 SVSYNC Others: Reserved Note: SVSYNC=1/Fs, Step:-1.5dBFS

9.89. MX-DAh: Soft Volume & ZCD Control 2

Default: 0000’h

Table 105. MX-DAh: Soft Volume & ZCD Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:7	R/W	0’h	Reserved
en_zcd_outmixr	6	R/W	0’h	OUTMIXR ZCD Control 0’b: Disable 1’b: Enable
en_zcd_outmixl	5	R/W	0’h	OUTMIXL ZCD Control 0’b: Disable 1’b: Enable
en_zcd_hpmixr	4	R/W	0’h	HPMIXR ZCD Control 0’b: Disable 1’b: Enable

Name	Bits	Read/Write	Reset State	Description
en_zcd_hpmixl	3	R/W	0'h	HPMIXL ZCD Control 0'b: Disable 1'b: Enable
reserved	2	R/W	0'h	Reserved
en_zcd_recmixr	1	R/W	0'h	RECMIXR ZCD Control 0'b: Disable 1'b: Enable
en_zcd_recmixl	0	R/W	0'h	RECMIXL ZCD Control 0'b: Disable 1'b: Enable

9.90. MX-DBh: Inline Command Control 1

Default: 0001'h

Table 106. MX-DBh: Inline Command Control 1

Name	Bits	Read/Write	Reset State	Description
sta_one_up_button	15	R	0'h	Status of One Click Command for Up Button Write "1" to clear it
sta_double_up_button	14	R	0'h	Status of Double Click Command for Up Button Write "1" to clear it
sta_hold_up_button	13	R	0'h	Status of Hold Command for Up Button Write "1" to clear it
sta_one_center_button	12	R	0'h	Status of One Click Command for Center Button Write "1" to clear it
sta_double_center_button	11	R	0'h	Status of Double Click Command for Center Button Write "1" to clear it
sta_hold_center_button	10	R	0'h	Status of Hold Command for Center Button Write "1" to clear it
sta_one_down_button	9	R	0'h	Status of One Click Command for Down Button Write "1" to clear it
sta_double_down_button	8	R	0'h	Status of Double Click Command for Down Button Write "1" to clear it
sta_hold_down_button	7	R	0'h	Status of Hold Command for Down Button Write "1" to clear it
En_inline	6	R/W	0'h	Enable InLine Command 0'b: Disable 1'b: Enable
reserved	5	R	0'h	Reserved
Sel_clk_mic	4:3	R/W	0'h	Select InLine Command Debounce Clock 00'b: OSC/2^17 01'b: OSC/2^16 10'b: OSC/2^15 11'b: OSC/2^14

Name	Bits	Read/Write	Reset State	Description
Mic_in_det_0_th	2:0	R/W	1'h	MIC Input Voltage Threshold Control (CMP0) 000'b: 0.09V 001'b: 0.12V 010'b: 0.15V 011'b: 0.18V 100'b: 0.17V 101'b: 0.23V 110'b: 0.29V 111'b: 0.34V

9.91. MX-DCh: Inline Command Control 2

Default: 0049'h

Table 107. MX-DCh: Inline Command Control 2

Name	Bits	Read/Write	Reset State	Description
en_inline_vol	15	R/W	0'h	Enable Inline Command Direct to Control Digital Volume 0'b: Disable 1'b: Enable
sel_inline_ctl_if	14	R/W	0'h	Select The Inline Command Control Path 0'b: IF1 DAC Volume/Mute(Un-Mute) 1'b: IF2 DAC Volume/Mute(Un-Mute)
Conti_hold_up	13	R/W	0'h	Select Hold Command Behavior for Up Button 0'b: One pulse trigger 1'b: Continue pulse trigger
Conti_hold_center	12	R/W	0'h	Select Hold Command Behavior for Center Button 0'b: One pulse trigger 1'b: Continue pulse trigger
Conti_hold_down	11	R/W	0'h	Select Hold Command Behavior for Down Button 0'b: One pulse trigger 1'b: Continue pulse trigger
in_det_window	10:0	R/W	49'h	Inline Command Click Window Control MX-DB[4:3]=00'b => (1/OSC)*16384*n MX-DB[4:3]=01'b => (1/OSC)*8192*n MX-DB[4:3]=10'b => (1/OSC)*4096*n MX-DB[4:3]=11'b => (1/OSC)*2048*n (n=0~127)

9.92. MX-DDh: Inline Command Control 3

Default: 0009’h

Table 108. MX-DDh: Inline Command Control 3

Name	Bits	Read/Write	Reset State	Description
Reserved	15:6	R	0’h	Reserved
Mic_in_det_1_th	5:3	R/W	1’h	MIC Input Voltage Threshold Control (CMP1) 000’b: 0.36V 001’b: 0.39V 010’b: 0.42V 011’b: 0.45V 100’b: 0.68V 101’b: 0.74V 110’b: 0.80V 111’b: 0.86V
Mic_in_det_2_th	2:0	R/W	1’h	MIC Input Voltage Threshold Control (CMP2) 000’b: 0.69V 001’b: 0.71V 010’b: 0.74V 011’b: 0.77V 100’b: 1.31V 101’b: 1.37V 110’b: 1.43V 111’b: 1.48V

9.93. MX-E0h: Voice DSP Control 1

Default: 0000’h

Table 109. MX-E0h: Voice DSP Control 1

Name	Bits	Read/Write	Reset State	Description
Aec_cmd	15:8	R/W	0’h	Voice DSP Command
dsp_clk_sel	7:6	R/W	0’h	Voice DSP Control Interface Clock Select 00’b: SYSCLK/3/16 01’b: SYSCLK/4/16 10’b: SYSCLK/6/16 11’b: SYSCLK/8/16
Aec_busy	5	R	0’h	Voice DSP R/W Busy 0’b: Normal 1’b: Busy
Sel_dsp_cmd	4	R/W	0’h	Voice DSP R/W Command 0’b: Write 1’b: Read

Name	Bits	Read/Write	Reset State	Description
Sel_dsp_data_len	3:2	R/W	0'h	Voice DSP Control Interface Data Length 00'b: 0 byte 01'b: 1 byte 10'b: 2 byte 11'b: 3 byte
Sel_dsp_addr_len	1	R/W	0'h	Voice DSP Control Interface Address Length 0'b: 8 bit 1'b: 16 bit
Aec_cmd_start	0	R/W	0'h	Write "1" to start Voice DSP Control Interface Command

9.94. MX-E1h: Voice DSP Control 2

Default: 0000'h

Table 110. MX-E1h: Voice DSP Control 2

Name	Bits	Read/Write	Reset State	Description
Aec_addr	15:0	R/W	0'h	Voice DSP Address

9.95. MX-E2h: Voice DSP Control 3

Default: 0000'h

Table 111. MX-E2h: Voice DSP Control 3

Name	Bits	Read/Write	Reset State	Description
Aec_write_data	15:0	R/W	0'h	Voice DSP Write Data

9.96. MX-E3h: Voice DSP Control 4

Default: 0000'h

Table 112. MX-E3h: Voice DSP Control 4

Name	Bits	Read/Write	Reset State	Description
Reserved	15:8	R	0'h	Reserved
Aec_write_data2	7:0	R/W	0'h	Voice DSP Write Data

9.97. MX-E4h: Voice DSP Control 5

Default: 0000’h

Table 113. MX-E4h: Voice DSP Control 5

Name	Bits	Read/Write	Reset State	Description
read_data_aec	15:0	R	0’h	Voice DSP Read Data

9.98. MX-E5h: Voice DSP Control 6

Default: 0000’h

Table 114. MX-E5h: Voice DSP Control 6

Name	Bits	Read/Write	Reset State	Description
Reserved	15:8	R	0’h	Reserved
read_data_aec2	7:0	R	0’h	Voice DSP Read Data

9.99. MX-ECh: Mono ADC Wind Filter Control 1

Default: A200’h

Table 115. MX-ECh: Mono ADC Wind Filter Control 1

Name	Bits	Read/Write	Reset State	Description
adj_hpf_2nd_en_mono	15	R/W	1’h	Mono ADC Wind Filter Enable Control 0’b : Disable and bypass 1’b : Enable
adj_hpf_coef_l_sel_mono	14:12	R/W	2’h	Mono ADC Wind Filter Left Channel Coefficient Coarse Selection 000’b : fs=8k, fc = 20~2000Hz fs=12k, fc = 30~3000Hz fs=16k, fc = 40~4000Hz 001’b : fs=24k, fc = 30~2458Hz fs=32k, fc = 40~3278Hz 010’b : fs=44.1k, fc = 28~1992Hz fs=48k, fc = 30~2168Hz 011’b : fs=88.2k, fc = 28~1869Hz fs=96k, fc = 30~2034Hz 100’b : fs=176.4k, fc = 27~1811Hz fs=192k, fc = 30~1971Hz Others: Reserved
Reserved	11	R	0’h	Reserved
adj_hpf_coef_r_sel_mono	10:8	R/W	2’h	Mono ADC Wind Filter Right Channel Coefficient Coarse Selection 000’b : fs=8k, fc = 20~2000Hz fs=12k, fc = 30~3000Hz fs=16k, fc = 40~4000Hz 001’b : fs=24k, fc = 30~2458Hz fs=32k, fc = 40~3278Hz 010’b : fs=44.1k, fc = 28~1992Hz fs=48k, fc = 30~2168Hz 011’b : fs=88.2k, fc = 28~1869Hz fs=96k, fc = 30~2034Hz 100’b : fs=176.4k, fc = 27~1811Hz fs=192k, fc = 30~1971Hz Others: Reserved
reserved	7:0	R	0’h	Reserved

9.100. MX-EDh: Mono ADC Wind Filter Control 2

Default: 0000’h

Table 116. MX-EDh: Mono ADC Wind Filter Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0’h	Reserved
adj_hpf_coef_l_num_mono	13:8	R/W	0’h	Mono ADC Wind Filter Right Channel Coefficient Fine Selection (0~63)
Reserved	7:6	R	0’h	Reserved
adj_hpf_coef_r_num_mono	5:0	R/W	0’h	Mono ADC Wind Filter Left Channel Coefficient Fine Selection (0~63)

9.101. MX-EEh: Stereo2 ADC Wind Filter Control 1

Default: A200’h

Table 117. MX-EEh: Stereo2 ADC Wind Filter Control 1

Name	Bits	Read/Write	Reset State	Description
adj_hpf_2nd_en_stereo2	15	R/W	1’h	Stereo2 ADC Wind Filter Enable Control 0’b : Disable and bypass 1’b : Enable
adj_hpf_coef_l_sel_stereo2	14:12	R/W	2’h	Stereo2 ADC Wind Filter Left Channel Coefficient Coarse Selection 000’b : fs=8k, fc = 20~2000Hz fs=12k, fc = 30~3000Hz fs=16k, fc = 40~4000Hz 001’b : fs=24k, fc = 30~2458Hz fs=32k, fc = 40~3278Hz 010’b : fs=44.1k, fc = 28~1992Hz fs=48k, fc = 30~2168Hz 011’b : fs=88.2k, fc = 28~1869Hz fs=96k, fc = 30~2034Hz 100’b : fs=176.4k, fc = 27~1811Hz fs=192k, fc = 30~1971Hz Others: Reserved
Reserved	11	R	0’h	Reserved

Name	Bits	Read/Write	Reset State	Description
adj_hpf_coef_r_sel_stereo2	10:8	R/W	2'h	Stereo2 ADC Wind Filter Right Channel Coefficient Coarse Selection 000'b : fs=8k, fc = 20~2000Hz fs=12k, fc = 30~3000Hz fs=16k, fc = 40~4000Hz 001'b : fs=24k, fc = 30~2458Hz fs=32k, fc = 40~3278Hz 010'b : fs=44.1k, fc = 28~1992Hz fs=48k, fc = 30~2168Hz 011'b : fs=88.2k, fc = 28~1869Hz fs=96k, fc = 30~2034Hz 100'b : fs=176.4k, fc = 27~1811Hz fs=192k, fc = 30~1971Hz Others: Reserved
reserved	7:0	R	0'h	Reserved

9.102. MX-EFh: Stereo2 ADC Wind Filter Control 2

Default: 0000'h

Table 118. MX-EFh: Stereo2 ADC Wind Filter Control 2

Name	Bits	Read/Write	Reset State	Description
Reserved	15:14	R	0'h	Reserved
adj_hpf_coef_l_num_stereo2	13:8	R/W	0'h	Stereo2 ADC Wind Filter Right Channel Coefficient Fine Selection (0~63)
Reserved	7:6	R	0'h	Reserved
adj_hpf_coef_r_num_stereo2	5:0	R/W	0'h	Stereo2 ADC Wind Filter Left Channel Coefficient Fine Selection (0~63)

9.103. MX-F8h: Jack Detection Control

Default: 0000’h

Table 119. MX-F8h: Jack Detection Control

Name	Bits	Read/Write	Reset State	Description
reserved	15:8	R	0’h	Reserved
en_jd_combo_jack	7	R/W	0’h	Enable Jack Detect to Trigger Combo Jack 0’b: Disable 1’b: Enable
polarity_jd_tri_cbj	6	R/W	0’h	Select Jack Detect Polarity to Trigger Combo Jack 0’b: Low trigger 1’b: High trigger
Sel_jd_trigger_cbj	5:3	R/W	0’h	JD Trigger Source Selection for Combo Jack 000’b: From sta_gpio_jd1 001’b: From sta_jd1_1 010’b: From sta_jd1_2 011’b: From sta_jd2 100’b: Reserved 101’b: Reserved 110’b: From MX0B[12] Others: Reserved
Sel_jd_trigger_hpo	2:0	R/W	0’h	JD Trigger Source Selection for HPO 000’b: From sta_gpio_jd1 001’b: From sta_jd1_1 010’b: From sta_jd1_2 011’b: From sta_jd2 100’b: Reserved 101’b: Reserved Others: Reserved

9.104. MX-F9h: Jack Detection Control

Default: 0000’h

Table 120. MX-F9h: Jack Detection Control

Name	Bits	Read/Write	Reset State	Description
reserved	15:12	R	0’h	Reserved
Sel_jd_trigger_spk	11:9	R/W	0’h	JD Trigger Source Selection for SPK_OUT 000’b: From sta_gpio_jd1 001’b: From sta_jd1_1 010’b: From sta_jd1_2 011’b: From sta_jd2 100’b: Reserved 101’b: Reserved Others: Reserved
Reserved	8:6	R	0’h	Reserved

Name	Bits	Read/Write	Reset State	Description
Sel_jd_trigger_lout1	5:3	R/W	0'h	JD Trigger Source Selection for LOUT1 000'b: From sta_gpio_jd1 001'b: From sta_jd1_1 010'b: From sta_jd1_2 011'b: From sta_jd2 100'b: Reserved 101'b: Reserved Others: Reserved
Reserved	2:0	R/W	0'h	Reserved

9.105. MX-FAh: General Control 1

Default: 0090'h

Table 121. MX-FAh: General Control 1

Name	Bits	Read/Write	Reset State	Description
Reserved	15:14	R/W	0'h	Reserved
Rst_dsp	13	R/W	0'h	Voice DSP Reset Control 0'b: Normal 1'b: Reset
Sel_if1_adc1_data_in1	12	R/W	0'h	Selection-1 for IF1 ADC1 Input Data 0'b: IF_ADC1 1'b: IF_ADC3
Sel_if1_adc1_data_in2	11	R/W	0'h	Selection-2 for IF1 ADC1 Input Data 0'b: IF_ADC1 or IF1_ADC3 1'b: TxDP_ADC
Sel_if1_adc2_data_in1	10	R/W	0'h	Selection for IF1 ADC2 Input Data 0'b: IF_ADC2 or VAD_ADC 1'b: TxDP_ADC
Reserved	9:4	R/W	9'h	Reserved
En_detect_clk_sys	3	R/W	0'h	Enable MCLK Detection and Auto Switch to RC Clock When MCLK is Remove 0'b: Disable 1'b: Enable
Reserved	2:1	R	0'h	Reserved
digital_gate_ctrl	0	R/W	0'h	Enable MCLK Gating Control 0'b: Disable 1'b: Enable

9.106. PR-3Dh: ADC/DAC RESET Control

Default: 2808’h

Table 122. PR-3Dh: ADC/DAC RESET Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R/W	1’h	Reserved
En_ckgen_adc	12	R/W	0’h	Enable ADC Clock Generator 0’b: Disable 1’b: Enable
Reserved	11:10	R/W	2’h	Reserved
En_ckgen_dac	9	R/W	0’h	Enable DAC Clock Generator 0’b: Disable 1’b: Enable
Reserved	8:0	R/W	8’h	Reserved

9.107. PR-A4h: DAC_L EQ (LPF:a1)

Default: 1C10’h

Table 123. PR-A4h: DAC_L EQ (LPF2:a1)

Name	Bits	Read/Write	Reset State	Description
lpf_a1	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.108. PR-A5h: DAC_L EQ (LPF:H0)

Default: 01F4’h

Table 124. PR-A5h: DAC_L EQ (LPF2:H0)

Name	Bits	Read/Write	Reset State	Description
lpf_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.109. PR-A6h: DAC_R EQ (LPF:a1)

Default: 1C10’h

Table 125. PR-A6h: DAC_R EQ (LPF2:a1)

Name	Bits	Read/Write	Reset State	Description
lpf_a1	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.110. PR-A7h: DAC_R EQ (LPF:H0)

Default: 01F4’h

Table 126. PR-A7h: DAC_R EQ (LPF:H0)

Name	Bits	Read/Write	Reset State	Description
lpf_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.111. PR-AEh: DAC_L EQ (BPF2:a1)

Default: C882’h

Table 127. PR-AEh: DAC_L EQ (BPF2:a1)

Name	Bits	Read/Write	Reset State	Description
Bpf2_a1	15:0	R/W	C882’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.112. PR-AFh: DAC_L EQ (BPF2:a2)

Default: 1C10’h

Table 128. PR-AFh: DAC_L EQ (BPF2:a2)

Name	Bits	Read/Write	Reset State	Description
Bpf2_a2	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

9.113. PR-B0h: DAC_L EQ (BPF2:H0)

Default: 01F4’h

Table 129. PR-B0h: DAC_L EQ (BPF2:H0)

Name	Bits	Read/Write	Reset State	Description
Bpf2_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.114. PR-B1h: DAC_R EQ (BPF2:a1)

Default: C882’h

Table 130. PR-B1h: DAC_R EQ (BPF2:a1)

Name	Bits	Read/Write	Reset State	Description
Bpf2_a1	15:0	R/W	C882’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.115. PR-B2h: DAC_R EQ (BPF2:a2)

Default: 1C10’h

Table 131. PR-B2h: DAC_R EQ (BPF2:a2)

Name	Bits	Read/Write	Reset State	Description
Bpf2_a2	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

9.116. PR-B3h: DAC_R EQ (BPF2:H0)

Default: 01F4’h

Table 132. PR-B3h: DAC_R EQ (BPF2:H0)

Name	Bits	Read/Write	Reset State	Description
Bpf2_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.117. PR-B4h: DAC_L EQ (BPF3:a1)

Default: E904’h

Table 133. PR-B4h: DAC_L EQ (BPF3:a1)

Name	Bits	Read/Write	Reset State	Description
Bpf3_a1	15:0	R/W	E904’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.118. PR-B5h: DAC_L EQ (BPF3:a2)

Default: 1C10’h

Table 134. PR-B5h: DAC_L EQ (BPF3:a2)

Name	Bits	Read/Write	Reset State	Description
Bpf3_a2	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

9.119. PR-B6h: DAC_L EQ (BPF3:H0)

Default: 01F4’h

Table 135. PR-B6h: DAC_L EQ (BPF3:H0)

Name	Bits	Read/Write	Reset State	Description
Bpf3_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.120. PR-B7h: DAC_R EQ (BPF3:a1)

Default: E904’h

Table 136. PR-B7h: DAC_R EQ (BPF3:a1)

Name	Bits	Read/Write	Reset State	Description
Bpf3_a1	15:0	R/W	E904’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.121. PR-B8h: DAC_R EQ (BPF3:a2)

Default: 1C10’h

Table 137. PR-B8h: DAC_R EQ (BPF3:a2)

Name	Bits	Read/Write	Reset State	Description
Bpf3_a2	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

9.122. PR-B9h: DAC_R EQ (BPF3:H0)

Default: 01F4’h

Table 138. PR-B9h: DAC_R EQ (BPF3:H0)

Name	Bits	Read/Write	Reset State	Description
Bpf3_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.123. PR-BAh: DAC_L EQ (BPF4:a1)

Default: E904’h

Table 139. PR-BAh: DAC_L EQ (BPF4:a1)

Name	Bits	Read/Write	Reset State	Description
Bpf4_a1	15:0	R/W	E904’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.124. PR-BBh: DAC_L EQ (BPF4:a2)

Default: 1C10’h

Table 140. PR-BBh: DAC_L EQ (BPF4:a2)

Name	Bits	Read/Write	Reset State	Description
Bpf4_a2	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

9.125. PR-BCh: DAC_L EQ (BPF4:H0)

Default: 01F4’h

Table 141. PR-BCh: DAC_L EQ (BPF4:H0)

Name	Bits	Read/Write	Reset State	Description
Bpf4_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.126. PR-BDh: DAC_R EQ (BPF4:a1)

Default: E904’h

Table 142. PR-BDh: DAC_R EQ (BPF4:a1)

Name	Bits	Read/Write	Reset State	Description
Bpf4_a1	15:0	R/W	E904’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.127. PR-BEh: DAC_R EQ (BPF4:a2)

Default: 1C10’h

Table 143. PR-BEh: DAC_R EQ (BPF4:a2)

Name	Bits	Read/Write	Reset State	Description
Bpf4_a2	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

9.128. PR-BFh: DAC_R EQ (BPF4:H0)

Default: 01F4’h

Table 144. PR-BFh: DAC_R EQ (BPF4:H0)

Name	Bits	Read/Write	Reset State	Description
Bpf4_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.129. PR-C0h: DAC_L EQ (HPF1:a1)

Default: 1C10’h

Table 145. PR-C0h: DAC_L EQ (HPF1:a1)

Name	Bits	Read/Write	Reset State	Description
Hpf1_a1	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.130. PR-C1h: DAC_L EQ (HPF1:H0)

Default: 01F4’h

Table 146. PR-C1h: DAC_L EQ (HPF1:H0)

Name	Bits	Read/Write	Reset State	Description
Hpf1_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.131. PR-C2h: DAC_R EQ (HPF1:a1)

Default: 1C10’h

Table 147. PR-C2h: DAC_R EQ (HPF1:a1)

Name	Bits	Read/Write	Reset State	Description
Hpf1_a1	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.132. PR-C3h: DAC_R EQ (HPF1:H0)

Default: 01F4’h

Table 147. PR-C3h: DAC_R EQ (HPF1:H0)

Name	Bits	Read/Write	Reset State	Description
Hpf1_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.133. PR-C4h: DAC_L EQ (HPF2:a1)

Default: 2000’h

Table 149. PR-C4h: DAC_L EQ (HPF2:a1)

Name	Bits	Read/Write	Reset State	Description
Hpf2_a1	15:0	R/W	2000’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.134. PR-C5h: DAC_L EQ (HPF2:a2)

Default: 0000’h

Table 150. PR-C5h: DAC_L EQ (HPF2:a2)

Name	Bits	Read/Write	Reset State	Description
Hpf2_a2	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

9.135. PR-C6h: DAC_L EQ (HPF2:H0)

Default: 1FF1’h

Table 151. PR-C6h: DAC_L EQ (HPF2:H0)

Name	Bits	Read/Write	Reset State	Description
Hpf2_h0	15:0	R/W	1FF1’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.136. PR-C7h: DAC_R EQ (HPF2:a1)

Default: 2000’h

Table 152. PR-C7h: DAC_R EQ (HPF2:a1)

Name	Bits	Read/Write	Reset State	Description
Hpf2_a1	15:0	R/W	2000’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.137. PR-C8h: DAC_R EQ (HPF2:a2)

Default: 0000’h

Table 153. PR-C8h: DAC_R EQ (HPF2:a2)

Name	Bits	Read/Write	Reset State	Description
Hpf2_a2	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

9.138. PR-C9h: DAC_R EQ (HPF2:H0)

Default: 1FF1’h

Table 154. PR-C9h: DAC_R EQ (HPF2:H0)

Name	Bits	Read/Write	Reset State	Description
Hpf2_h0	15:0	R/W	1FF1’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.139. PR-CAh: DAC_L EQ Pre-Volume Control

Default: 0800’h

Table 155. PR-CAh: DAC_L EQ Pre-Volume Control

Name	Bits	Read/Write	Reset State	Description
Da_eq_pre_vol_l	15:0	R/W	0800’h	DAC Left Channel EQ Pre-Volume Control 2’s Complement in 5.11 Format. (Default is 0dB) The range is from -16 ~ 15.99, pre-gain should be in 0 ~ 15.99 [+24dB ~ -66dB]

9.140. PR-CBh: DAC_R EQ Pre-Volume Control

Default: 0800’h

Table 156. PR-CBh: DAC_R EQ Pre-Volume Control

Name	Bits	Read/Write	Reset State	Description
Da_eq_pre_vol_l	15:0	R/W	0800’h	DAC Right Channel EQ Pre-Volume Control 2’s Complement in 5.11 Format. (Default is 0dB) The range is from -16 ~ 15.99, pre-gain should be in 0 ~ 15.99 [+24dB ~ -66dB]

9.141. PR-CCh: DAC_L EQ Post-Volume Control

Default: 0800’h

Table 157. PR-CCh: DAC_L EQ Post-Volume Control

Name	Bits	Read/Write	Reset State	Description
Da_eq_post_vol_l	15:0	R/W	0800’h	DAC Left Channel EQ Post-Volume Control 2’s Complement in 5.11 Format. (Default is 0dB) The range is from -16 ~ 15.99, pre-gain should be in 0 ~ 15.99 [+24dB ~ -66dB]

9.142. PR-CDh: DAC_R EQ Post-Volume Control

Default: 0800’h

Table 158. PR-CDh: DAC_R EQ Post-Volume Control

Name	Bits	Read/Write	Reset State	Description
Da_eq_post_vol_l	15:0	R/W	0800’h	DAC Right Channel EQ Post-Volume Control 2’s Complement in 5.11 Format. (Default is 0dB) The range is from -16 ~ 15.99, pre-gain should be in 0 ~ 15.99 [+24dB ~ -66dB]

9.143. PR-CEh: ADC EQ (LPF:a1)

Default: 1C10’h

Table 159. PR-CEh: ADC EQ (LPF:a1)

Name	Bits	Read/Write	Reset State	Description
ad_eq_lpf_a1	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.144. PR-CFh: ADC EQ (LPF:H0)

Default: 01F4’h

Table 160. PR-CFh: ADC EQ (LPF:H0)

Name	Bits	Read/Write	Reset State	Description
ad_eq_lpf_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.145. PR-D0h: ADC EQ (BPF1:a1)

Default: E904’h

Table 161. PR-D0h: ADC EQ (BPF1:a1)

Name	Bits	Read/Write	Reset State	Description
ad_eq_Bpf1_a1	15:0	R/W	E904’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.146. PR-D1h: ADC EQ (BPF1:a2)

Default: 1C10’h

Table 162. PR-D1h: ADC EQ (BPF1:a2)

Name	Bits	Read/Write	Reset State	Description
Ad_eq_Bpf1_a2	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

9.147. PR-D2h: ADC EQ (BPF1:H0)

Default: 01F4’h

Table 163. PR-D2h: ADC EQ (BPF1:H0)

Name	Bits	Read/Write	Reset State	Description
ad_eq_Bpf1_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.148. PR-D3h: ADC EQ (BPF2:a1)

Default: E904’h

Table 164. PR-D3h: ADC EQ (BPF2:a1)

Name	Bits	Read/Write	Reset State	Description
ad_eq_Bpf2_a1	15:0	R/W	E904’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.149. PR-D4h: ADC EQ (BPF2:a2)

Default: 1C10’h

Table 165. PR-D4h: ADC EQ (BPF2:a2)

Name	Bits	Read/Write	Reset State	Description
Ad_eq_Bpf2_a2	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

9.150. PR-D5h: ADC EQ (BPF2:H0)

Default: 01F4’h

Table 166. PR-D5h: ADC EQ (BPF2:H0)

Name	Bits	Read/Write	Reset State	Description
ad_eq_Bpf2_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.151. PR-D6h: ADC EQ (BPF3:a1)

Default: E904’h

Table 167. PR-D6h: ADC EQ (BPF3:a1)

Name	Bits	Read/Write	Reset State	Description
ad_eq_Bpf3_a1	15:0	R/W	E904’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.152. PR-D7h: ADC EQ (BPF3:a2)

Default: 1C10’h

Table 168. PR-D7h: ADC EQ (BPF3:a2)

Name	Bits	Read/Write	Reset State	Description
Ad_eq_Bpf3_a2	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

9.153. PR-D8h: ADC EQ (BPF3:H0)

Default: 01F4’h

Table 169. PR-D8h: ADC EQ (BPF3:H0)

Name	Bits	Read/Write	Reset State	Description
ad_eq_Bpf3_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.154. PR-D9h: ADC EQ (BPF4:a1)

Default: E904’h

Table 170. PR-D9h: ADC EQ (BPF4:a1)

Name	Bits	Read/Write	Reset State	Description
ad_eq_Bpf4_a1	15:0	R/W	E904’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.155. PR-DAh: ADC EQ (BPF4:a2)

Default: 1C10’h

Table 171. PR-DAh: ADC EQ (BPF4:a2)

Name	Bits	Read/Write	Reset State	Description
Ad_eq_Bpf4_a2	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

9.156. PR-DBh: ADC EQ (BPF4:H0)

Default: 01F4’h

Table 172. PR-DBh: ADC EQ (BPF4:H0)

Name	Bits	Read/Write	Reset State	Description
ad_eq_Bpf4_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.157. PR-DCh: ADC EQ (HPF1:a1)

Default: 1C10’h

Table 173. PR-DCh: ADC EQ (HPF1:a1)

Name	Bits	Read/Write	Reset State	Description
Ad_eq_hpf1_a1	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

9.158. PR-DDh: ADC EQ (HPF1:H0)

Default: 01F4’h

Table 174. PR-DDh: ADC EQ (HPF1:H0)

Name	Bits	Read/Write	Reset State	Description
ad_eq_hpf1_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

9.159. PR-E1h: ADC EQ Pre-Volume Control

Default: 0800’h

Table 175. PR-E1h: ADC EQ Pre-Volume Control

Name	Bits	Read/Write	Reset State	Description
ad_eq_pre_vol	15:0	R/W	0800’h	ADC Left Channel EQ Pre-Volume Control 2’s Complement in 5.11 Format. (Default is 0dB) The range is from -16 ~ 15.99, pre-gain should be in 0 ~ 15.99 [+24dB ~ -66dB]

9.160. PR-E2h: ADC EQ Post-Volume Control

Default: 0800’h

Table 176. PR-E2h: ADC EQ Post-Volume Control

Name	Bits	Read/Write	Reset State	Description
Ad_eq_post_vol	15:0	R/W	0800’h	ADC Left Channel EQ Post-Volume Control 2’s Complement in 5.11 Format. (Default is 0dB) The range is from -16 ~ 15.99, pre-gain should be in 0 ~ 15.99 [+24dB ~ -66dB]

9.161. PR-E5h: DAC_L Biquad EQ (BPF1:h0-1)

Default: 0000’h

Table 177. PR-E5h: DAC_L Biquad EQ (BPF1:h0-1)

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R	0’h	Reserved
Eq_biquad_h0_l_msb	12:0	R/W	0’h	2’s complement in 4.25 format. (The range is from –8~7.99)

9.162. PR-E6h: DAC_L Biquad EQ (BPF1:h0-2)

Default: 0000’h

Table 178. PR-E6h: DAC_L Biquad EQ (BPF1:h0-2)

Name	Bits	Read/Write	Reset State	Description
Eq_biquad_h0_l_lsb	15:0	R/W	0’h	2’s complement in 4.25 format. (The range is from –8~7.99)

9.163. PR-E7h: DAC_L Biquad EQ (BPF1:b1-1)

Default: 0000’h

Table 179. PR-E7h: DAC_L Biquad EQ (BPF1:b1-1)

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R	0’h	Reserved
Eq_biquad_b1_l_msb	12:0	R/W	0’h	2’s complement in 4.25 format. (The range is from –8~7.99)

9.164. PR-E8h: DAC_L Biquad EQ (BPF1:b1-2)

Default: 0000’h

Table 180. PR-E8h: DAC_L Biquad EQ (BPF1:b1-2)

Name	Bits	Read/Write	Reset State	Description
Eq_biquad_b1_l_lsb	15:0	R/W	0’h	2’s complement in 4.25 format. (The range is from –8~7.99)

9.165. PR-E9h: DAC_L Biquad EQ (BPF1:b2-1)

Default: 0000’h

Table 181. PR-E9h: DAC_L Biquad EQ (BPF1:b2-1)

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R	0’h	Reserved
Eq_biquad_b2_l_msb	12:0	R/W	0’h	2’s complement in 4.25 format. (The range is from –8~7.99)

9.166. PR-EAh: DAC_L Biquad EQ (BPF1:b2-2)

Default: 0000’h

Table 182. PR-EAh: DAC_L Biquad EQ (BPF1:b2-2)

Name	Bits	Read/Write	Reset State	Description
Eq_biquad_b2_l_lsb	15:0	R/W	0’h	2’s complement in 4.25 format. (The range is from –8~7.99)

9.167. PR-EBh: DAC_L Biquad EQ (BPF1:a1-1)

Default: 0000’h

Table 183. PR-EBh: DAC_L Biquad EQ (BPF1:a1-1)

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R	0’h	Reserved
Eq_biquad_a1_l_msb	12:0	R/W	0’h	2’s complement in 4.25 format. (The range is from –8~7.99)

9.168. PR-ECh: DAC_L Biquad EQ (BPF1:a1-2)

Default: 0000’h

Table 184. PR-ECh: DAC_L Biquad EQ (BPF1:a1-2)

Name	Bits	Read/Write	Reset State	Description
Eq_biquad_a1_l_lsb	15:0	R/W	0’h	2’s complement in 4.25 format. (The range is from –8~7.99)

9.169. PR-EDh: DAC_L Biquad EQ (BPF1:a2-1)

Default: 0000’h

Table 185. PR-EDh: DAC_L Biquad EQ (BPF1:a2-1)

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R	0’h	Reserved

Name	Bits	Read/Write	Reset State	Description
Eq_biquad_a2_l_msb	12:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

9.170. PR-EEh: DAC_L Biquad EQ (BPF1:a2-2)

Default: 0000'h

Table 186. PR-EEh: DAC_L Biquad EQ (BPF1:a2-2)

Name	Bits	Read/Write	Reset State	Description
Eq_biquad_a2_l_lsb	15:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

9.171. PR-EFh: DAC_R Biquad EQ (BPF1:h0-1)

Default: 0000'h

Table 187. PR-EFh: DAC_R Biquad EQ (BPF1:h0-1)

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R	0'h	Reserved
Eq_biquad_h0_r_msb	12:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

9.172. PR-F0h: DAC_R Biquad EQ (BPF1:h0-2)

Default: 0000'h

Table 188. PR-F0h: DAC_R Biquad EQ (BPF1:h0-2)

Name	Bits	Read/Write	Reset State	Description
Eq_biquad_h0_r_lsb	15:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

9.173. PR-F1h: DAC_R Biquad EQ (BPF1:b1-1)

Default: 0000’h

Table 189. PR-F1h: DAC_R Biquad EQ (BPF1:b1-1)

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R	0’h	Reserved
Eq_biquad_b1_r_msb	12:0	R/W	0’h	2’s complement in 4.25 format. (The range is from –8~7.99)

9.174. PR-F2h: DAC_R Biquad EQ (BPF1:b1-2)

Default: 0000’h

Table 190. PR-F2h: DAC_R Biquad EQ (BPF1:b1-2)

Name	Bits	Read/Write	Reset State	Description
Eq_biquad_b1_r_lsb	15:0	R/W	0’h	2’s complement in 4.25 format. (The range is from –8~7.99)

9.175. PR-F3h: DAC_R Biquad EQ (BPF1:b2-1)

Default: 0000’h

Table 191. PR-F3h: DAC_R Biquad EQ (BPF1:b2-1)

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R	0’h	Reserved
Eq_biquad_b2_r_msb	12:0	R/W	0’h	2’s complement in 4.25 format. (The range is from –8~7.99)

9.176. PR-F4h: DAC_R Biquad EQ (BPF1:b2-2)

Default: 0000’h

Table 192. PR-F4h: DAC_R Biquad EQ (BPF1:b2-2)

Name	Bits	Read/Write	Reset State	Description
Eq_biquad_b2_r_lsb	15:0	R/W	0’h	2’s complement in 4.25 format. (The range is from –8~7.99)

9.177. PR-F5h: DAC_R Biquad EQ (BPF1:a1-1)

Default: 0000’h

Table 193. PR-F5h: DAC_R Biquad EQ (BPF1:a1-1)

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R	0’h	Reserved
Eq_biquad_a1_r_msb	12:0	R/W	0’h	2’s complement in 4.25 format. (The range is from –8~7.99)

9.178. PR-F6h: DAC_R Biquad EQ (BPF1:a1-2)

Default: 0000’h

Table 194. PR-F6h: DAC_R Biquad EQ (BPF1:a1-2)

Name	Bits	Read/Write	Reset State	Description
Eq_biquad_a1_r_lsb	15:0	R/W	0’h	2’s complement in 4.25 format. (The range is from –8~7.99)

9.179. PR-F7h: DAC_R Biquad EQ (BPF1:a2-1)

Default: 0000’h

Table 195. PR-F7h: DAC_R Biquad EQ (BPF1:a2-1)

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R	0’h	Reserved

Name	Bits	Read/Write	Reset State	Description
Eq_biquad_a2_r_msb	12:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

9.180. PR-F8h: DAC_R Biquad EQ (BPF1:a2-2)

Default: 0000'h

Table 196. PR-F8h: DAC_R Biquad EQ (BPF1:a2-2)

Name	Bits	Read/Write	Reset State	Description
Eq_biquad_a2_r_lsb	15:0	R/W	0'h	2's complement in 4.25 format. (The range is from –8~7.99)

9.181. MX-FEh: Vendor ID

Default: 10EC'h

Table 197. MX-FEh: Vendor ID

Name	Bits	Read/Write	Reset State	Description
Vendor_id	15:0	R	10EC'h	Vendor ID

10. Electrical Characteristics

10.1. DC Characteristics

10.1.1. Absolute Maximum Ratings

Table 198. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies					
Digital IO Buffer	DBVDD	-0.3	-	3.63	V
Digital Core	DCVDD	-0.3	-	1.4	V
Analog	AVDD	-0.3	-	1.98	V
Headphone	CPVDD	-0.3	-	1.98	V
Micbias	MICVDD	-0.3	-	3.63	V
Speaker	SPKVDD	-0.3	-	7[1]	V
Operating Ambient Temperature	Ta	-25	-	+85	°C
Storage Temperature	Ts	-55	-	+125	°C

Note 1: SPKVDD=5V with 3.5% duty cycle Power bouncing up to SPKVDD=7V is acceptable.

10.1.2. Recommended Operating Conditions

Table 199. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Digital IO Buffer	DBVDD	1.71	1.8	3.6	V
Digital Core	DCVDD	1.05	1.2	1.3	V
Analog	AVDD	1.71	1.8	1.9	V
Analog	DACREF	1.71	1.8	1.9	V
Headphone	CPVDD	1.71	1.8	1.9	V
Micbias	MICVDD	3.0	3.3	3.6	V
Speaker	SPKVDD[1]	3.0	3.6/5.0	5.5	V

Note 1: A 10µF Capacitor must be connected from SPKVDD to SPKGND, and should be placed as close as possible to the SPKVDD pin.

10.1.3. Static Characteristics

Table 200. Static Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Range	V_{IN}	-0.30	-	DBVDD+0.30	V
Low Level Input Voltage	V_{IL}	-	-	0.35DBVDD	V
High Level Input Voltage	V_{IH}	0.65DBVDD	-	-	V
High Level Output Voltage	V_{OH}	0.9DBVDD	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1DBVDD	V
Output Buffer High Drive Current	-	-	15	-	mA
Output Buffer Low Drive Current	-	-	14.7	-	mA
Input Buffer Pull-Up Resistor	-	125	148	180	KΩ
Input Buffer Pull-Down Resistor	-	193	225	266	KΩ

Note: DBVDD=1.8V, DCVDD=1.2V, $T_{ambient}$=40°C.

10.2. Analog Performance Characteristics

Table 201. Analog Performance Characteristics

Parameter	Min	Typ	Max	Units
Full Scale Input Voltage				
Line Inputs (Single-ended)	-	0.6	-	Vrms
MIC Inputs (Single-ended)	-	0.6	-	Vrms
MIC Inputs (Differential)	-	1.2	-	Vrms
Full Scale Output Voltage				
Line Outputs (Single-ended)	-	1.0	-	Vrms
Line Outputs (Differential)	-	1.0	-	Vrms
Headphone Amplifiers Outputs (For 10KOhm Load)	-	1.0	-	Vrms
Headphone Amplifiers Outputs (For 16Ohm Load)	-	0.7	-	Vrms
Headphone Amplifiers Outputs (For 32Ohm Load)	-	0.8	-	Vrms
Speaker Amplifiers Outputs (SPKVDD=5.0V with 4Ω Load, 1% THD+N)	-	2.9	-	Vrms
S/N Ratio				
Stereo DAC Direct to HP_L/R with 16/32/10KOhm	-	100	102	dBA
Stereo DAC Direct to SPK_OUT with 8Ohm/5V (Differential)	-	93		dBA
Line_In to Stereo ADC with 0dB (Single-end)		93	95	dBA
MIC_In to Stereo ADC with 0dB (Differential or Single-end)		93	95	dBA
MIC_In to Stereo ADC with 20dB and MICBIAS (Differential or Single-end)		TBD		dBA
MIC_In to Stereo ADC with 40dB and MICBIAS (Differential or Single-end)		TBD		dBA
MIC_In to Stereo ADC with 50dB and MICBIAS (Differential or Single-end)		TBD		dBA
Total Harmonic Distortion + Noise				
DAC Direct to HP_L/R with 16Ohm				
Po = 20mW/CH (16Ohm) (with AES17 Filter)		-81	-83	dB
Po = 20mW/CH (32Ohm) (with AES17 Filter)		-81	-83	dB
DAC Direct to HP_L/R with 10KOhm				
-3dBFS		-85		dB
DAC Direct to SPK_OUT (Differential)				
Po=1.2W (5V/8Ohm)		<1		%
Po=2.1W (5V/4Ohm)		<1		%
Po=920mW (4.2V/8Ohm)		<1		%
Po=650mW (3.6V/8Ohm)		<1		%
Line_In to Stereo ADC with 0dB (Single-end)		-84		dB
MIC_In to Stereo ADC with 0dB (Differential or Single-end)		-84		dB
MIC_In to Stereo ADC with 20dB and MICBIAS (Differential or Single-end)		TBD		dB
MIC_In to Stereo ADC with 40dB and MICBIAS (Differential		TBD		dB

Parameter	Min	Typ	Max	Units
or Single-end)				
MIC_In to Stereo ADC with 50dB and MICBIAS (Differential or Single-end)		TBD		dB
BTL Speaker Amplifier Efficiency				
(f_{IN}=1kHz, 8Ω Load, SPKVDD=5.0V, Output Power=1.5W, with LC filter, L=33uH and C=1uF)				
Class-D (Stereo Mode)	-	89	-	%
Power Consumption (Slave I2S Mode, 16-bit, SR: 44.1KHz)				
P_power down (No Clock Input)		<60		uW
P_playback (Stereo DAC to HP_OUT with 16 Ohm Load, With Clock, play silence)		<= 5.5		mW
P_playback (Stereo DAC to HP_OUT with 16 Ohm Load, With Clock, Po=1mW/CH)		<= 13		mW
P_record (LINE_IN to Stereo ADC, With Clock)		< 10		mW
Power Down Current				
I_{DDA} (Analog Block)	-	-	10	µA
I_{DDD} (Digital Block)	-	-	30	µA
MICBIAS1 Output Voltage				
Setting 1	-	0.9*MICVDD	-	V
Setting 2	-	0.75*MICVDD	-	V
MICBIAS1 Drive Current				
MICBIAS = 0.9*LDO2_O	-	4	-	mA

Note: Standard test conditions:
$T_{ambient}$=25°C
DBVDD=1.8V
DCVDD=1.2V
AVDD=1.8V
MICVDD=3.3V
CPVDD=1.8V
SPKVDD=5.0V or 4.2V or 3.6V.
1kHz input sine wave; PCM Sampling frequency=48kHz; Test bench Characterization BW: 10Hz~22kHz, 0dB attenuation
dBA: with A-Weighting

10.3. Signal Timing

10.3.1. I²C Control Interface

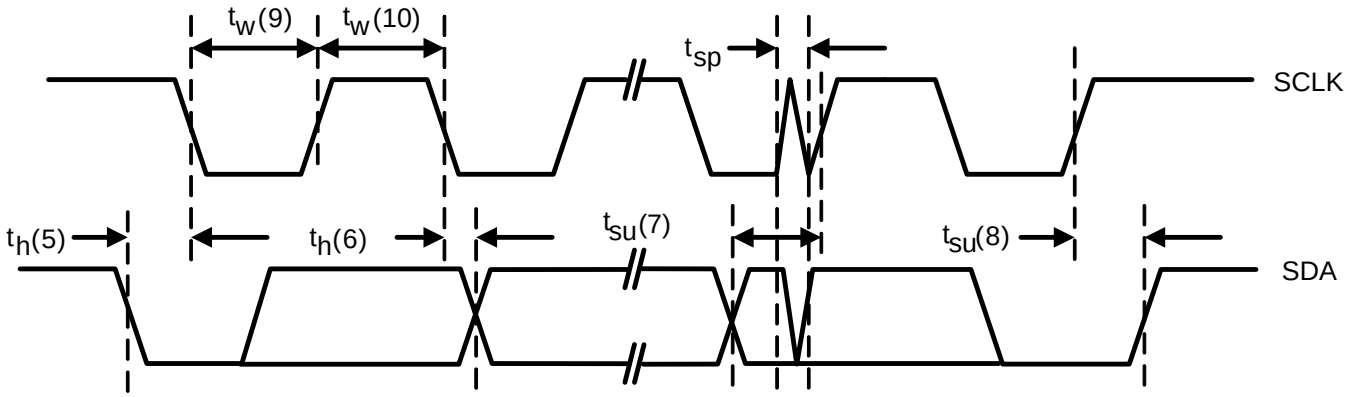


Figure 30. I²C Control Interface

Table 202. I²C Timing

Parameter	Symbol	Min	Typ	Max	Units
Clock Pulse Duration	$t_w(9)$	1.3	-	-	µs
Clock Pulse Duration	$t_w(10)$	600	-	-	ns
Clock Frequency	F	0	-	400K	Hz
Start Hold Time	$t_h(5)$	600	-	-	ns
Data Setup Time	$t_{su}(7)$	100	-	-	ns
Data Hold Time	$t_h(6)$	-	-	900	ns
Rising Time	t_r	-	-	300	ns
Falling Time	t_f	-	-	300	ns
Stop Setup Time	$t_{su}(8)$	600	-	-	ns
Pulse Width of Spikes Suppressed Input Filter	t_{sp}	0	-	50	ns

10.3.2. I²S/PCM Interface Master Mode

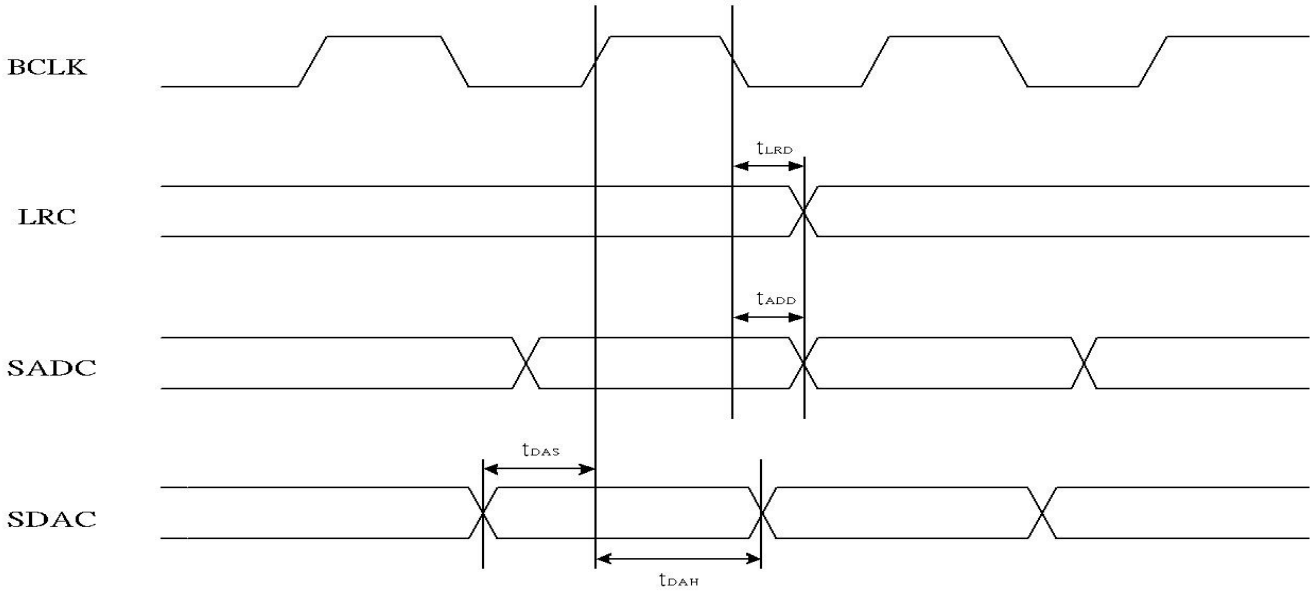


Figure 31. Timing of I²S/PCM Master Mode

Table 203. Timing of I²S/PCM Master Mode

Parameter	Symbol	Min	Typ	Max	Units
LRCK Output to BCLK Delay	t_{LRD}	-	-	30	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

10.3.3. I²S/PCM Interface Slave Mode

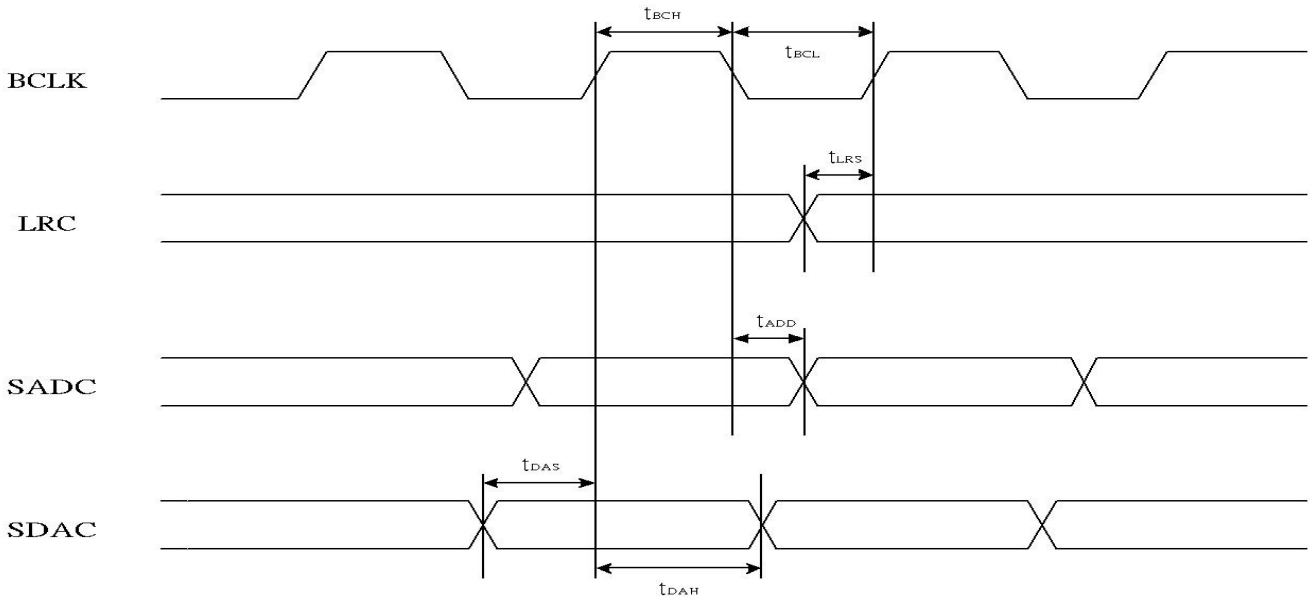


Figure 32. I²S/PCM Slave Mode Timing

Table 204. I²S/PCM Slave Mode Timing

Parameter	Symbol	Min	Typ	Max	Units
BCLK High Pulse Width	t_{BCH}	20	-	-	ns
BCLK Low Pulse Width	t_{BCL}	20	-	-	ns
LRCK Input Setup Time	t_{LRS}	30	-	-	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

10.3.4. Digital Microphone Interface

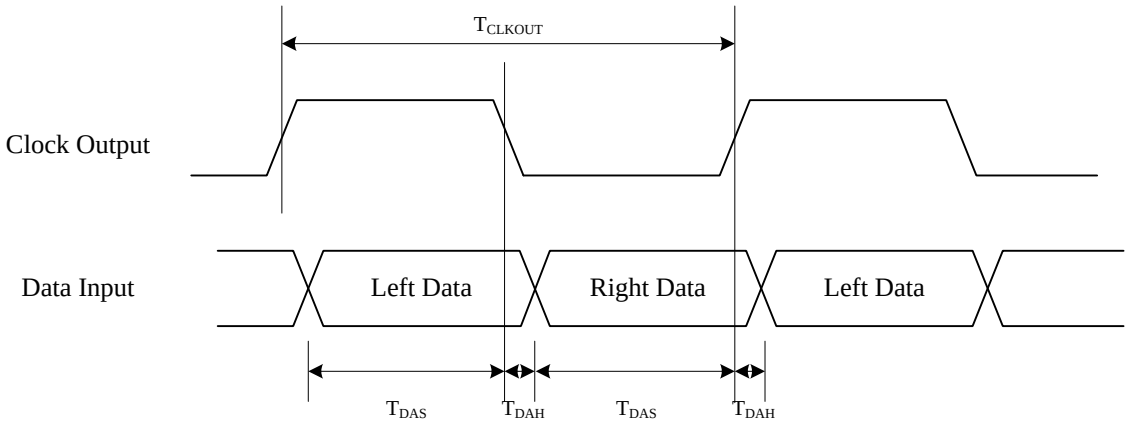
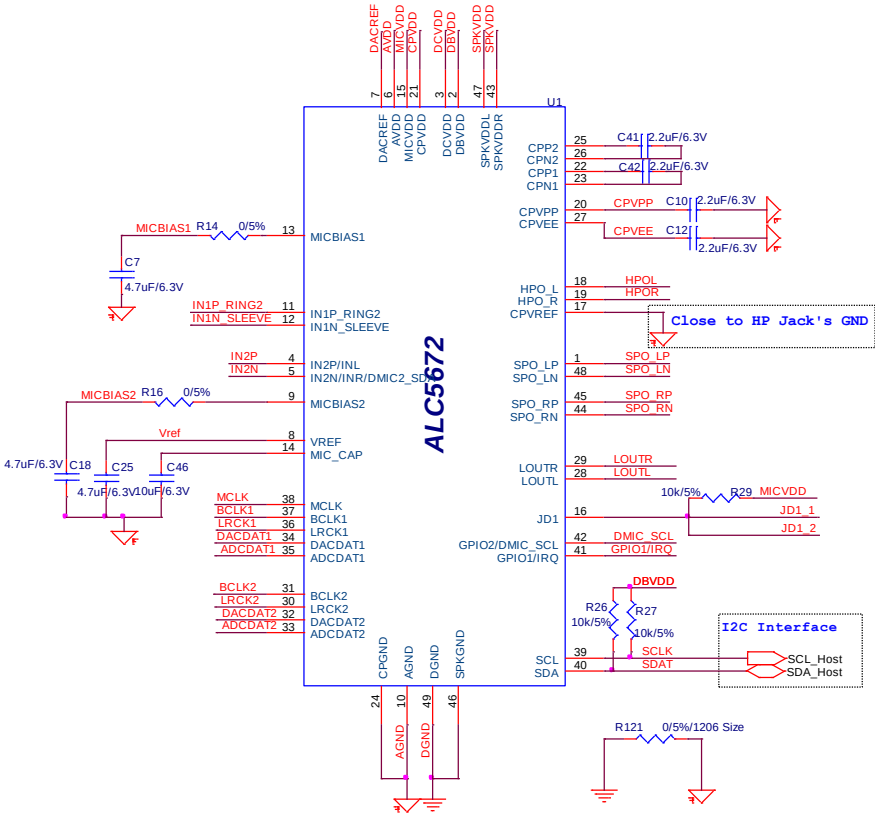


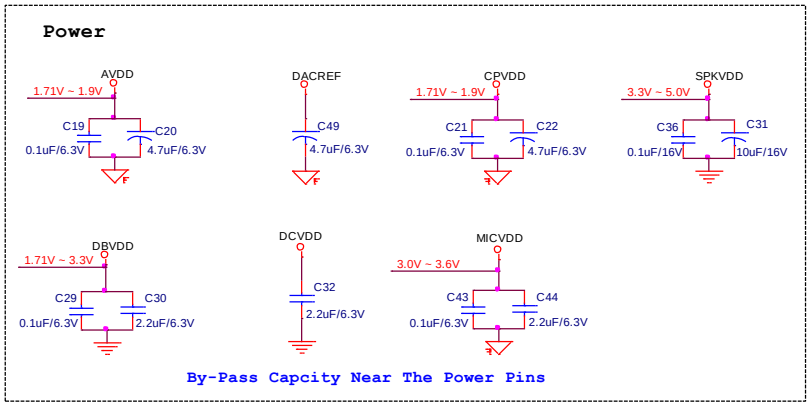
Figure 33. Digital Microphone Interface Timing

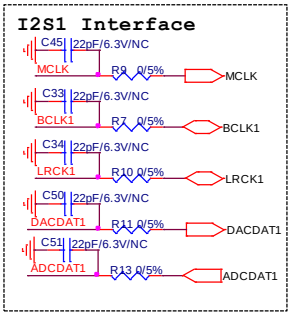
Table 205. Digital Microphone Interface Timing

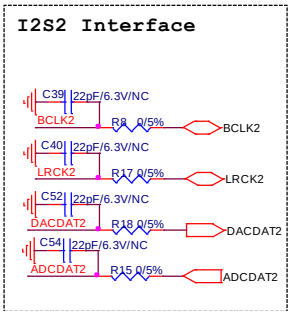
Parameter	Symbol	Min	Typ	Max	Units
Clock Output Rate	T_{CLKOUT}	300	-	-	ns
Clock Duty Cycle		45:55		55:45	
Data Input Setup Time	T_{DAS}	20	-	-	ns
Data Input Hold Time	T_{DAH}	10	-	-	ns

11. Application Circuits









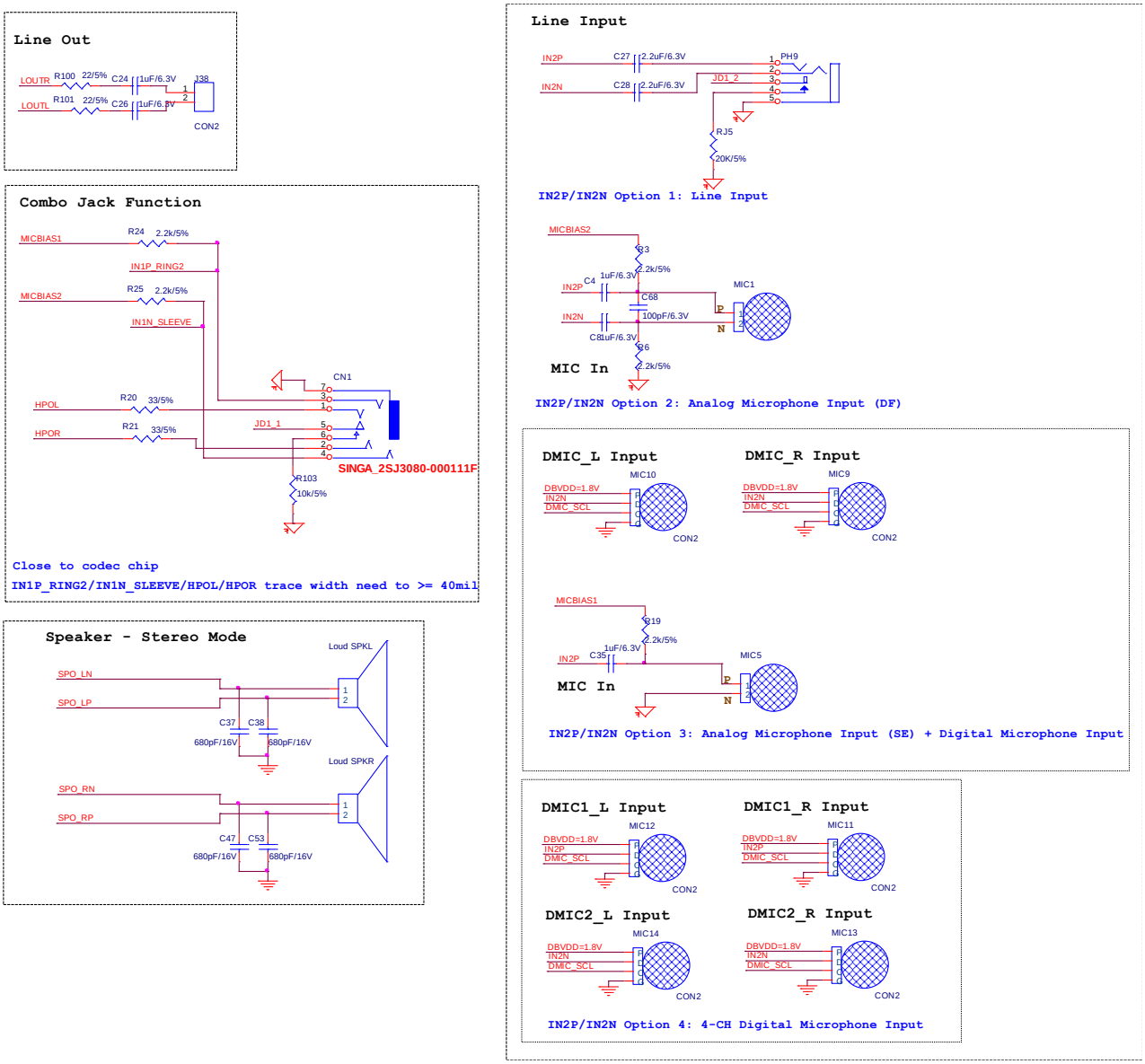
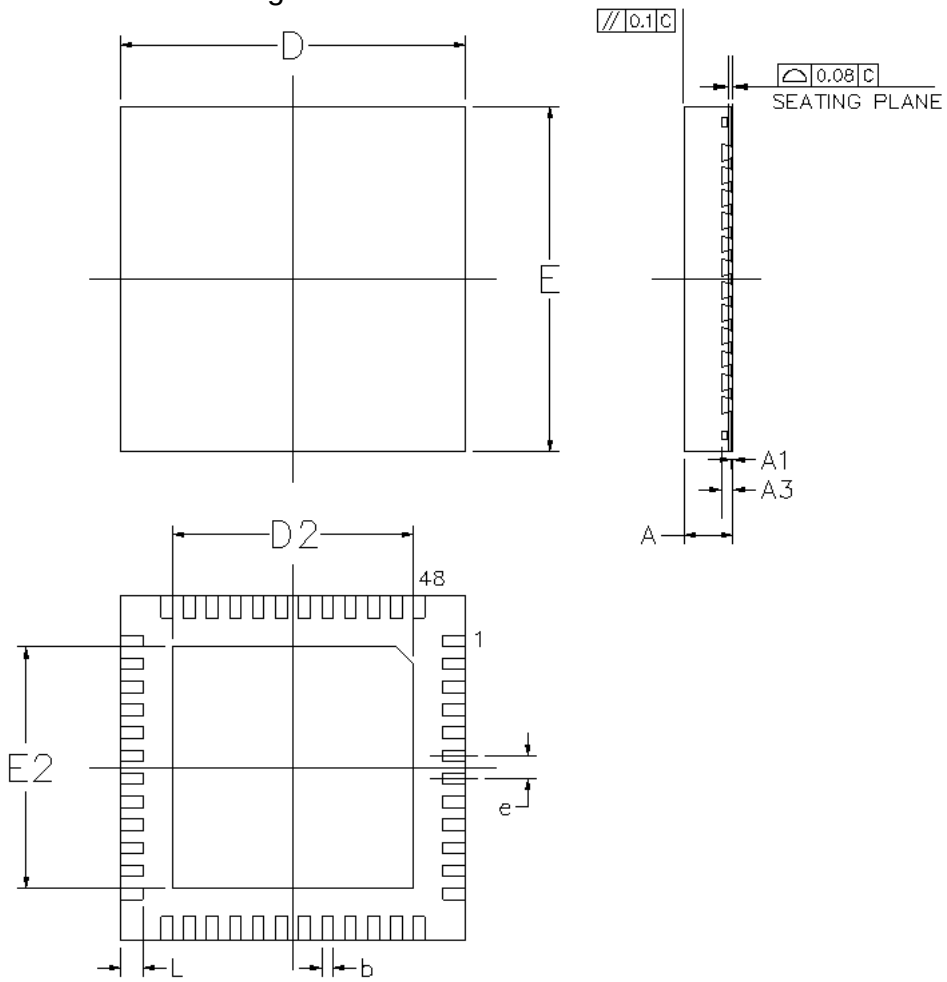


Figure 34. Application Circuit

12. Package Information

12.1. Mechanical Dimensions

Plastic Quad Flat No-Lead Package 48 Leads 6x6mm^2 Outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	6.00BSC			0.236BSC		
D2/E2	4.15	4.4	4.65	0.163	0.173	0.183
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes‥

1. CONTROLLING DIMENSION‥ MILLIMETER(mm).
2. REFERENCE DOCUMENTL‥ JEDEC MO-220.

Figure 35. Package Dimension

12.2. Package Thermal Information

Table 206. Thermal Information

Parameter	Symbol	Min	Typ	Max	Units
QFN48 (6x6) Thermal Impedance (Junction to Case)	θ_{jc}	-	8.4	-	^{o}C/W
QFN48 (6x6) Thermal Impedance (Junction to Ambient)	θ_{ja}	-	28	-	^{o}C/W

*Follow JEDEC PCB:

1. PCB Dimension (L x W): 114.3mm x 101.6mm
2. PCB Thickness: 1.6mm
3. Number of Cu Layer-PCB: 4-layers (2S2P)
4. PCB Via Number: 10
5. Air flow: 0 (m/s)

13. Ordering Information

Table 207. Ordering Information

Part Number	Package	Status
ALC5672-CG	48-Pin QFN (6mm x 6mm) in 'Green' Package (Tray)	N/A
ALC5672-CGT	48-Pin QFN (6mm x 6mm) in 'Green' Package (Tape & Reel)	N/A
ALC5672R-CG	48-Pin QFN (6mm x 6mm) in 'Green' Package (Tray)	N/A
ALC5672R-CGT	48-Pin QFN (6mm x 6mm) in 'Green' Package (Tape & Reel)	N/A

* "R" is special for certain assign project purpose, not for general purpose.

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