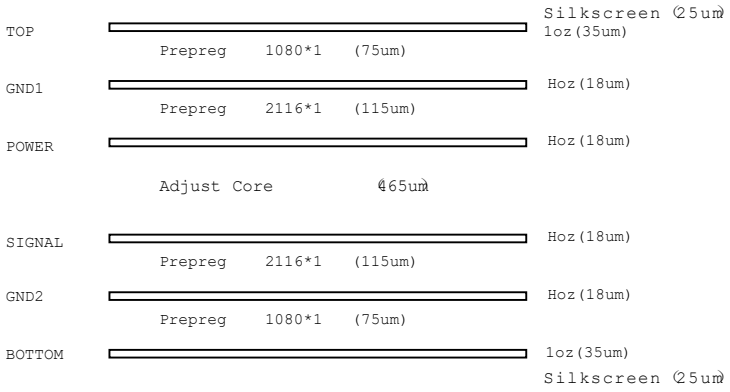
CONTENT INDEXING

6 LAYERS PCB STACK (e.g. PCB=1.0mm)



Note:

1:If the Value or option of the componert properties is DNP indicating do not mounted

Note

Option

Description

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Revision History

Version	Date	Author	Change Note	Approved
V1.0	2018.09.27	jzx	First edition	
V1.1				
V1.2				
V1.3				

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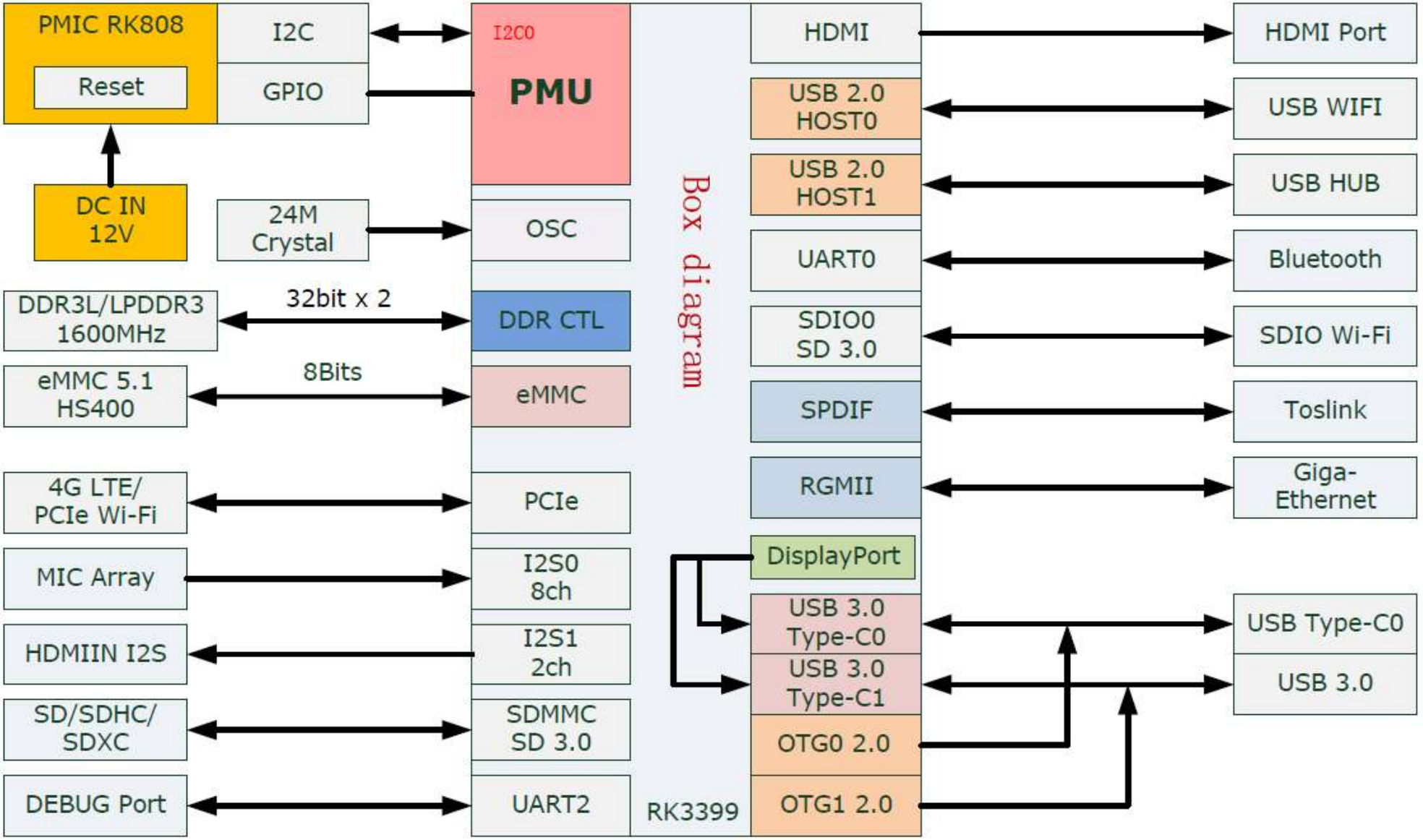

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I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_1V8	Rockchip RK808-D	0x1b	PMIC	100kHz,400KHz
					Silergy SYR837PKC	0x40	DC-DC BUCK	100kHz,400KHz,3.4MHz
					Silergy SYR838PKC	0x41	DC-DC BUCK	100kHz,400KHz,3.4MHz
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5	I2C_SDA_VIDEO I2C_SCL_VIDEO	VCC_1V8	Toshiba TC358749XBG	1F	HDMI Transmit	
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2	I2C2_SDA I2C2_SCL	VCC_3V0	2410	0X54		
					2410	0X55		
					9777	0X20		
					7719	0X44		
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4	I2C_SDA_HDMI I2C_SCL_HDMI	VCC_3V0				
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2	I2C_SDA_TYPEC I2C_SCL_TYPEC	VCC_1V8	ALC5672	0X38		
					Toshiba TC358749XBG	1F	HDMI Transmit	
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	Other pin function					
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2	RESERVE					
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2	RESERVE					

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Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUIO1	pmuio1_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLDO3
Part E	PMUIO2	pmu1830_gpio1abcd	1.8V(Default) 3.0V	VCC_1V8	RK808-D Buck4
Part I	APIO1	gmac_gpio3abc	3.3V only	VCC_1V8 VCC3V3_LAN	RK808-D Buck4
Part L	APIO2	bt656_gpio2ab	1.8V(Default) 3.0V	VCC_1V8	RK808-D VLDO3
Part G	APIO3	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	APIO4	gpio1830_gpio4cd	1.8V 3.0V(Default)	VCC_1V5 VCC_3V0	RK808-D VLDO6 RK808-D VLDO8
Part J	APIO5	audio_gpio3d_gpio4a	1.8V(Default) 3.0V	VCC_1V8	RK808-D Buck4
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V(Default)	VCCIO_SD	RK808-D VLDO4

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RK808-D Power Diagram and Sequence

PowerName	PMIC Channel	Time Slot (step 2mS)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF
VCC3V3_SYS	EX_DCDC	Slot:1	3.3V	2.0A	ON	ON
VCC_1V8	DCDC4	Slot:1	1.8V	3.0A	ON	ON
VCCA_1V8	VLDO3	Slot:1	1.8V	100mA	ON	ON
VCC_1V5	VLDO6	Slot:1	1.5V	150mA	ON	ON
VDD_LOG	EX_DCDC	Slot:1A	0.9V	1.0A	ON	ON
VCCA_0V9	EX_LDO	Slot:1A	0.9V	300mA	ON	ON
VDD_CPU_B	EX_DCDC	Slot:1A	0.9V	6.0A	ON	OFF
VDD_GPU	EX_DCDC	Slot:1A	0.9V	6.0A	ON	OFF
VCC_DDR	DCDC3	Slot:2	FB=1.0V	2.5A	ON	ON
VCC3V0_SD	EX_LDO	Slot:2	3.0V	500mA	ON	ON
VDD_CPU_L	DCDC2	Slot:3	0.9V	5.0A	ON	OFF
VDD_CENTER	DCDC1	Slot:4	0.9V	5.0A	ON	OFF
VCC_3V0	VLDO8	Slot:5	3.0V	300mA	ON	ON
VCCIO_SD	VLDO4	Slot:7	3.0V	150mA	ON	ON
VCCA1V8_HDMI	VLDO2		1.8V	150mA	OFF	ON
VCCA0V9_HDMI	VLDO7		0.9V	300mA	OFF	ON
Reserve	VSWOUT1	Slot:6		5.0A	ON	OFF
Reserve	VSWOUT2			5.0A	OFF	OFF
Reserve	VLDO1			150mA	OFF	OFF
Reserve	VLDO5			300mA	OFF	OFF
RESET		Slot:7	OD		ON	

DC Adapter 12V

VCC12V_DCIN

1110mA/23mA/TBD

SY8113B BUCK,PWM 3A,<5uA shutdown — EN always ON

SY8113B BUCK,PWM 3A,<5uA shutdown — EN always ON

VCC5V0_USB 5.1V

2440mA/48mA/TBD

SY6280AAC Switch 5V/1A,80mR 0.1uA shutdown → VBUS5V0_TYPEC → VBUS USB 3.0 Type-C0 port (VCC5V0_TYPEC0_EN)

SY6280AAC Switch 5V/1A,80mR 0.1uA shutdown → VCC5V0_HOST0 → VBUS USB 2.0 A port (VCC5V0_HOST_EN)

SY6280AAC Switch 5V/1A,80mR 0.1uA shutdown → VCC5V0_HOST1 → VBUS USB 2.0 A port (VCC5V0_HOST_EN)

SY6280AAC Switch 5V/1A,80mR 0.1uA shutdown → VCC5V0_HOST2 → VBUS USB 3.0 A port (VCC5V0_HOST_EN)

FUSB302 Type-C VCONN CC 300mA/1uA

VCC5V0_SYS 5.0V

VCC_RTC (VCC of PMIC RTC) S0/S3/S5 7.6mA/TBD/30uA

VCC_BAT 3.3V

WPM2015 P-MOSFET 1.8A,110mR@4.5V → VCC5V0_FAN (FAN_CTL_H) → VCC of Speaker AMP S0/OFF/OFF

B5819WS → VCC5V0_HDMI → VCC of HDMI Device

SY8089AAAC BUCK,PWM 2A,<1uA shutdown (PMIC_EXT_EN)

VCC3V3_SYS

PT5108E23E-30 LDO 3.0V/500mA <1uA shutdown → VCC3V0_SD (SDMMC0_PWR_H) → SD/TF Card S0/OFF/OFF TBD/TBD/TBD

TT2102 ADJ LDO 0.9V/300mA <1uA shutdown (VCC3V3_SYS) → VCCA_0V9

VCC0V9_PLL	AVDD of PLL	S0/S3/OFF	13.4mA/108uA/TBD
VCC0V9_PMUPLL	VDD of PMU PLL	S0/S3/OFF	12.3mA/160uA/TBD
VCC0V9_DDRPLL	AVDD of DDR CTRL	S0/S3/OFF	13.4mA/18uA/TBD
VCC0V9_EMMC	VDD of EMMC CTRL CORE DLL	S0/S3/OFF	3.4mA/<3mA/TBD
VCC0V9_USB	AVDD of USB phy	S0/S3/OFF	20.6mA/2.54mA/TBD
VCC0V9_PCIE	AVDD of PCIE phy	S0/S3/OFF	6.3mA/TBD/TBD

PT5108E23E-18 LDO 1.8V/500mA <1uA shutdown (EFUSE_VQPS_EN_H) → VCC_EFUSE → VCC of EFUSE User/OFF/OFF 1.7mA/TBD/TBD

VCC3V3_CC	VCC of FUSB302	S0/S3/OFF	8.6mA/<0.3mA/TBD
VCC3V3_USB	AVDD of USB phy	S0/S3/OFF	17.7mA/0.25mA/TBD
VCC3V3_EMMC	CORE VCC of EMMC FLASH	S0/S3/OFF	200mA/0.24mA/TBD
VCC3V3_WL	VCC of WIFI module	S0/OFF/OFF	
VCC3V3_WLIN	VBAT of WIFI+BT module	S0/S3/OFF	864mA/12.1mA/TBD
VCC3V3_LAN	AVCC/DVCC of ethernet phy	S0/S3/OFF	103.5mA/26.3mA/TBD
VCC3V3_MIC	VDD of MIC Array	S0/S3/OFF	
VCC3V3_SPDIF	VCC of SPDIF Driver IC	S0/S3/OFF	TBD/TBD/TBD
VCC3V3_PCIE	VCC of PCIE Device	S0/OFF/OFF	
VCC3V3_IR	VCC of IR Receiver	S0/S3/OFF	5.3mA/1.1mA/TBD
VCC3V3_HDMIIN	VCC of PCIE Device	S0/OFF/OFF	
VCC3V3_LED	Work LED	S0/S3/OFF	1.2mA/1.2mA/TBD
VCC3V3_HUB	AVDD of USB HUB	S0/S3/OFF	TBD/0.56mA/TBD

PMIC RK808 BUCK1 5A,0.7-1.5V TBD uA shutdown	VDD_CENTER	VDD of SOC center	S0/OFF/OFF	1050mA/TBD/TBD
PMIC RK808 BUCK2 5A,0.7-1.5V TBD uA shutdown	VDD_CPU_L	VDD of Quard-A53	S0/OFF/OFF	1480mA/TBD/TBD
PMIC RK808 BUCK3 2.5A,1.0-1.8V TBD uA shutdown	VCC_DDR	VDD of DDR CTRL	S0/S3/OFF	
		VDDCA/VDD2 of DDR	S0/S3/OFF	1240mA/3.5mA/TBD
		VDDQ of DDR	S0/S3/OFF	
PMIC RK808 BUCK4 3A,1.8-3.3V TBD uA shutdown	VCC_1V8	VCC1V8_EMMC → VDD of EMMC CRTL,VDDQ of EMMC FLASH IO	S0/S3/OFF	234mA/<4mA/TBD
		VCC1V8_WIFI → VDDIO of WIFI+BT module	S0/S3/OFF	10.6mA/4.25mA/TBD
		VCC1V8_IO → VDDIO/VDDPST of GPIO	S0/S3/OFF	20mA/0.3mA/TBD
		VCC1V8_DDR → VDD1 of LPDDR3	S0/S3/OFF	49.7mA/940uA/TBD uA
PMIC RK808 LDO1 150mA,1.8-3.4V TBD uA shutdown				
PMIC RK808 LDO2 150mA,1.8-3.4V TBD uA shutdown	VCCA1V8_HDMI	AVDD of HDMI/MIPI TX phy	S0/OFF/OFF	11.7mA/TBD/TBD
PMIC RK808 LDO3 100mA,0.8-2.5V TBD uA shutdown	VCCA_1V8	VCC1V8_PMUIO1 → VDDIO/VDDPST of PMUIO1	S0/S3/OFF	5mA/133uA/TBD
		VCC1V8_PMUPLL → VDD of PMU PLL	S0/S3/OFF	9.6mA/1.01mA/TBD
		VCC1V8_PLL → AVDD of PLL	S0/S3/OFF	18mA/0.3uA/TBD
		VCC1V8_USB → AVDD of USB phy	S0/S3/OFF	10.1mA/1.79mA/TBD
		VCC1V8_ADC → AVDD of SARADC	S0/S3/OFF	3.3mA/<1mA/TBD
		VCC1V8_PCIE → AVDD of PCIE phy	S0/S3/OFF	5mA/<1mA/TBD
PMIC RK808 LDO4 150mA,1.8-3.4V TBD uA shutdown	VCCIO_SD	VDDIO of SDMMC0	S0/OFF/OFF	3.4mA/TBD/TBD
PMIC RK808 LDO5 300mA,1.8-3.4V TBD uA shutdown				
PMIC RK808 LDO6 150mA,0.8-2.5V TBD uA shutdown	VCC_1V5	VDDPST of APIO2/APIO4	S0/OFF/OFF	17.4mA/TBD/TBD
PMIC RK808 LDO7 300mA,0.8-2.5V TBD uA shutdown	VCCA0V9_HDMI	AVDD of HDMI/MIPI TX phy	S0/OFF/OFF	20.5mA/TBD/TBD
PMIC RK808 LDO8 300mA,1.8-3.4V TBD uA shutdown	VCC_3V0	VDD of APIO2/APIO4/PMUIO2	S0/OFF/OFF	13.5mA/TBD/TBD
PMIC RK808 VSW1 5A,200mohm TBD uA shutdown				
PMIC RK808 VSW2 5A,200mohm TBD uA shutdown				
SYR837PKC Switch 6A,1uA shutdown (VCC_1V8)	VDD_CPU_B	VDD of Dual-A72	S0/OFF/OFF	4140mA/TBD/TBD
SYR838PKC Switch 6A,1uA shutdown (VCC_1V8)	VDD_GPU	VDD of Mali-T864	S0/OFF/OFF	3880mA/TBD/TBD
SY8088AAC BUCK,PWM 1A,<1uA shutdown (VCC_1V8)	VDD_LOG	VDD of SOC Logic	S0/S3/OFF	390mA/7.5mA/TBD

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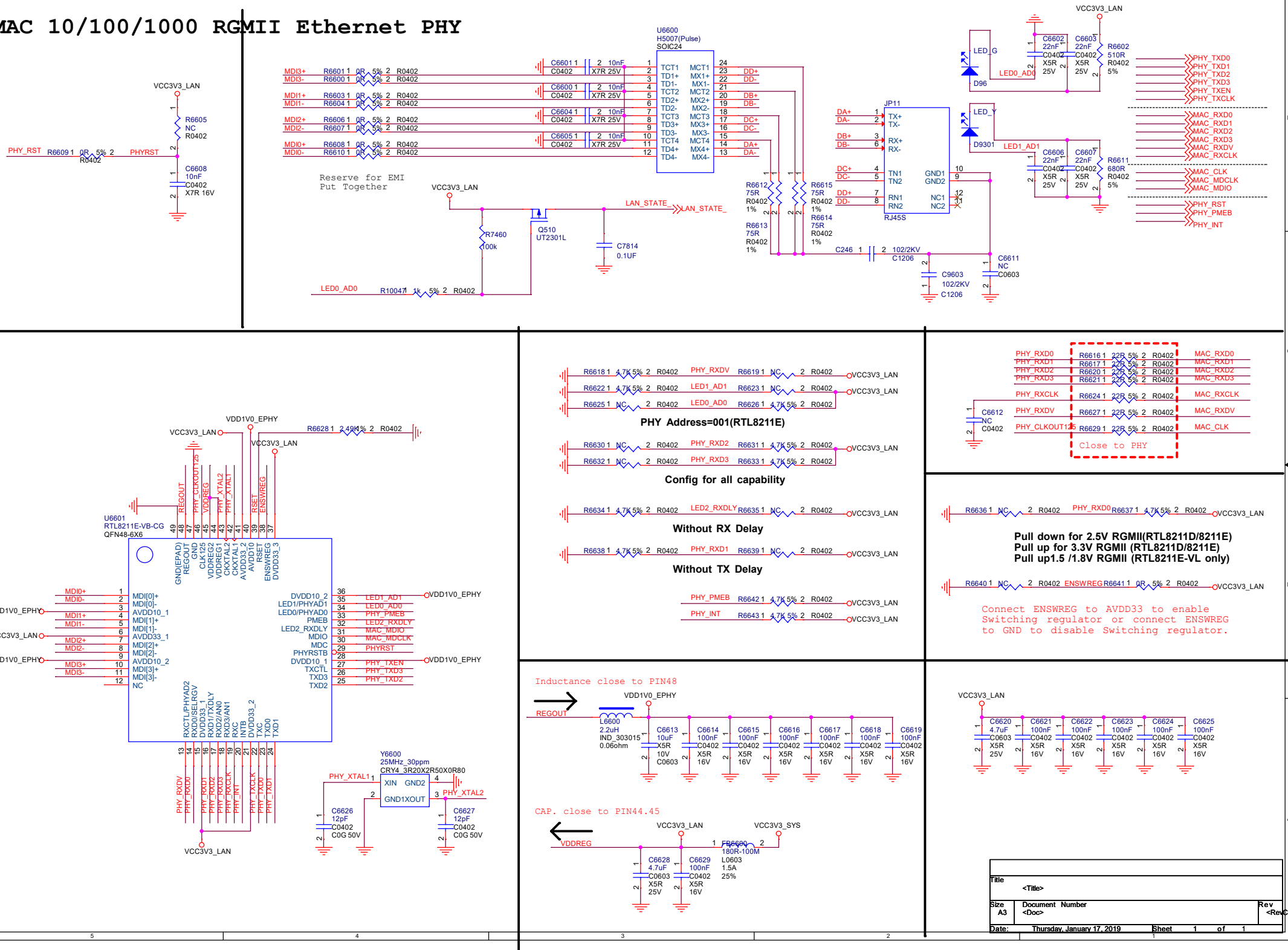
GMAC 10/100/1000 RGMII Ethernet PHY



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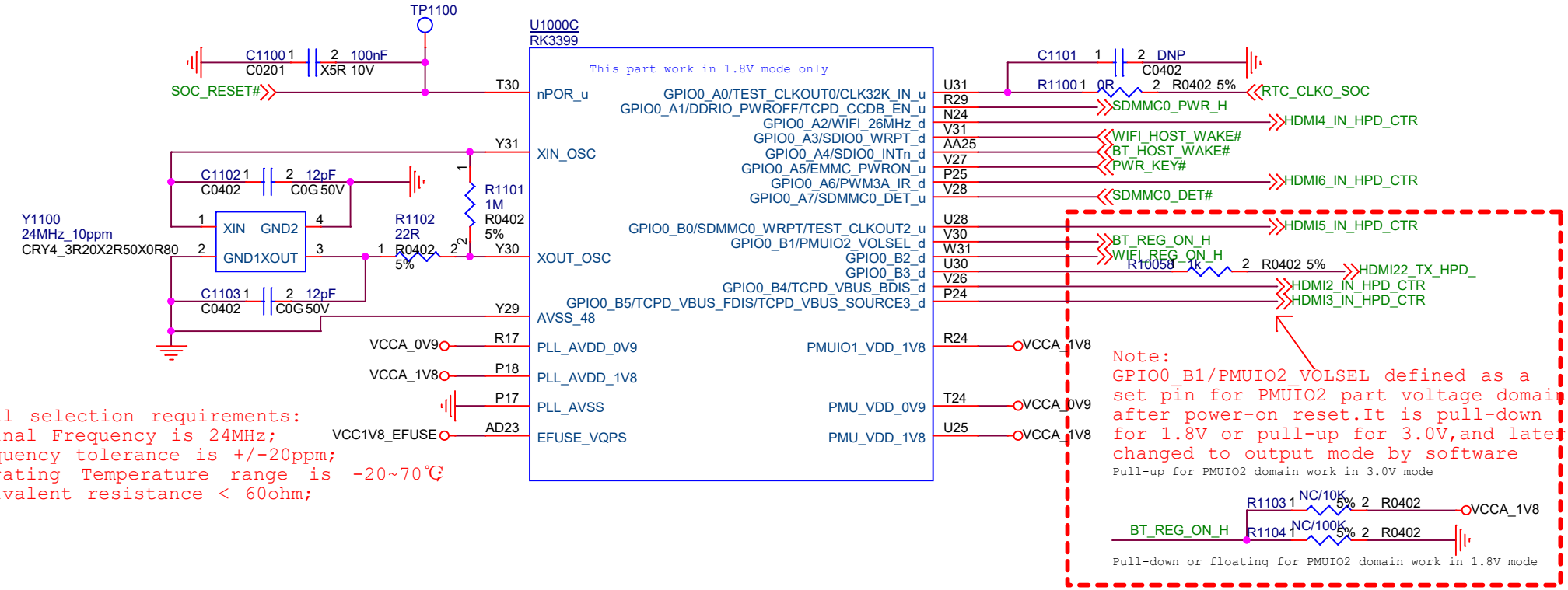
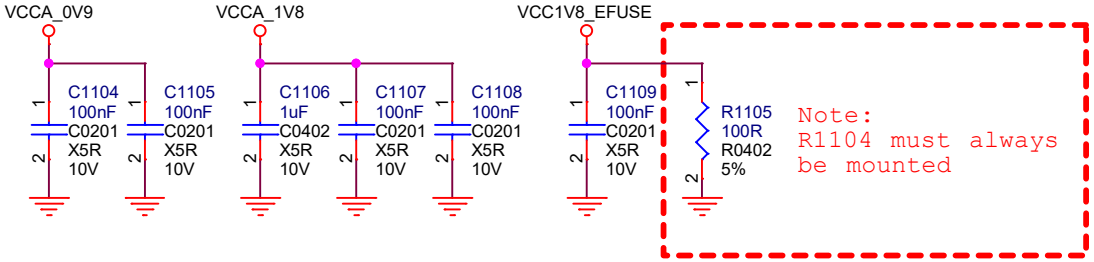
RK3399_C



Cristal selection requirements:
1.Nominal Frequency is 24MHz;
2.Frequency tolerance is +/-20ppm;
3.Operating Temperature range is -20~70℃;
4.Equivalent resistance < 60ohm;



Note:All the Power filter capacitors should be placed close to the power pins of RK3399

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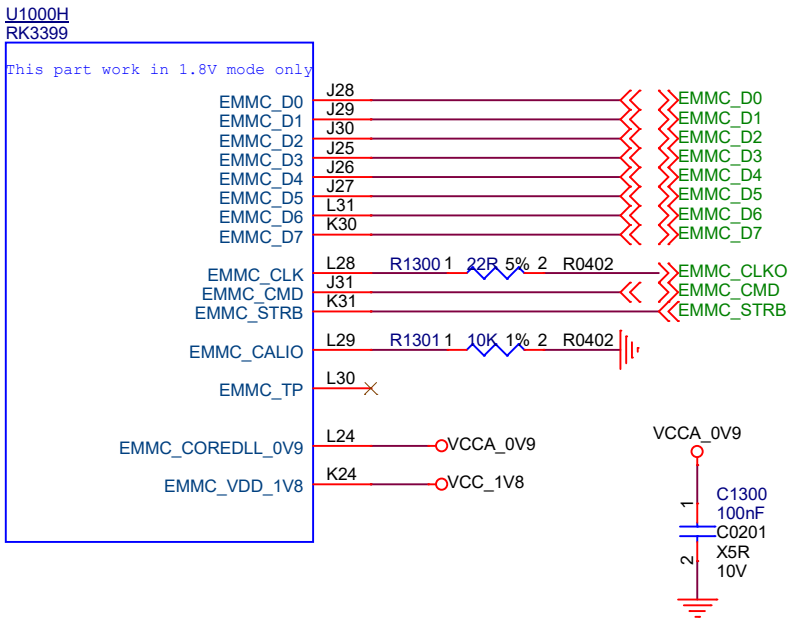
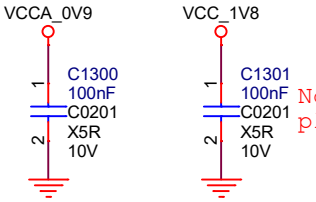
RK3399_H

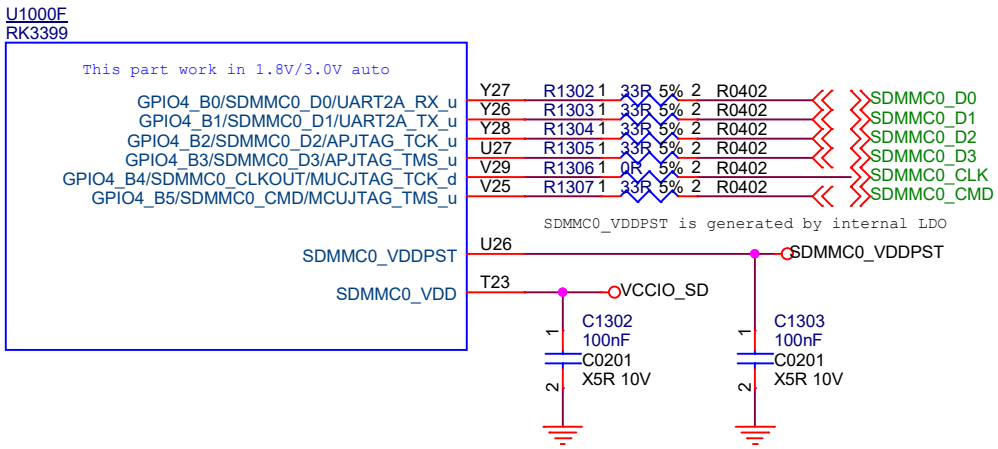




EMMC design rules:
1.Data[0:3],CMD and Strobe lines routing parallel as a group,and be isolated with other signals by GND line,the skew between group is less than 200mils;
2.Clk should be isolated with other signals by GND line;The skew between data signals is less than 20ps;
3.Max trace length < 3.93inchs;
4.Trace impedance 50ohm+/-10%;
5.The distance between other signals follows the 3W rule;
6.R1300 should be place close to RK3399;

Note:All the Power filter capacitors should be placed close to the power pins of RK3399

RK3399_F



SDMMC design rules:
1.Data[0:3] and CMD lines routing parallel as a group,and be isolated with other signals by GND line,the skew between group is less than 200mils;
2.Clk should be isolated with other signals by GND line;The skew between data signals is less than 20ps;
3.Max trace length < 3.93inchs;
4.Trace impedance 50ohm+/-10%;
5.The distance between other signals follows the 3W rule;

Note:All the Power filter capacitors should be placed close to the power pins of RK3399

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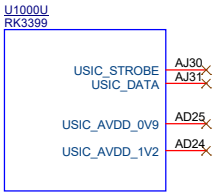
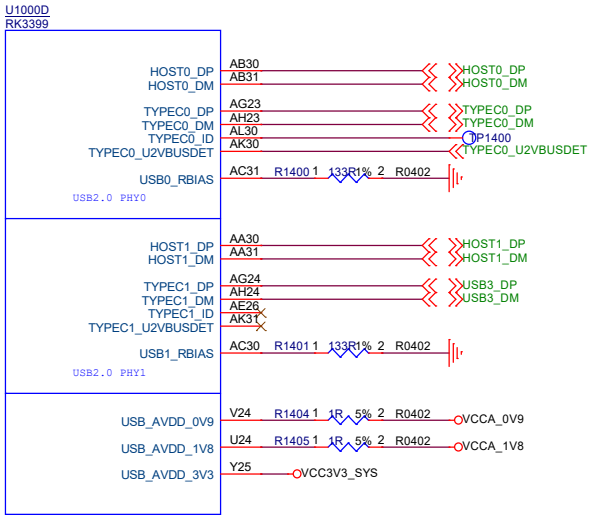
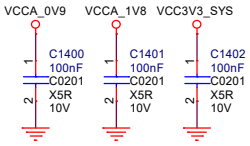
RK3399_U



RK3399_D

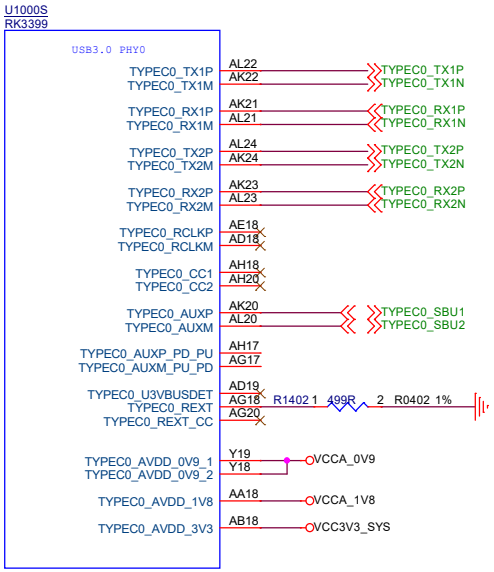


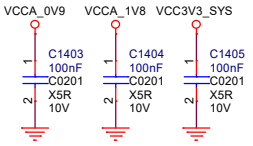


Note:All the Power filter capacitors should be placed close to the power pins of RK3399

USB2.0 design rules:
1.Max intra-pair skew < 4ps;
2.Max trace length < 6inchs;
3.Max allowed via < 6;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals follows the 3W rule;

RK3399_S

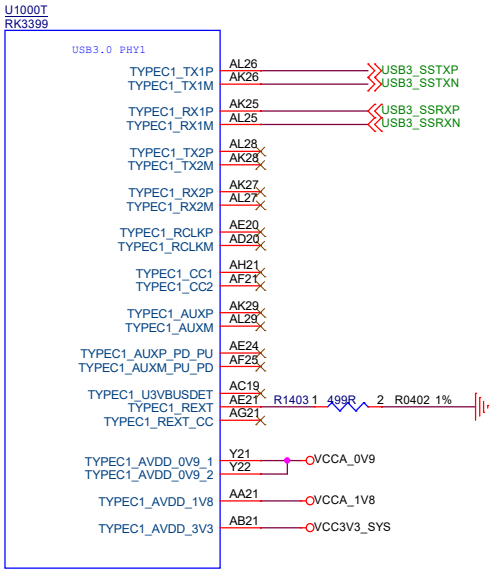




Note:All the Power filter capacitors should be placed close to the power pins of RK3399

USB3.0 design rules:
1.Max intra-pair skew < 4ps;
2.Max length skew between TX and RX < 1.6ns;
3.Max trace length < 6inchs;
4.Max allowed via < 4;
5.Trace impedance 90ohm+/-10%;
6.The distance between other signals follows the 3W rule;

RK3399_T



DP design rules:
1.Max intra-pair skew < 4ps;
2.Max trace length < 6inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals follows the 3W rule;

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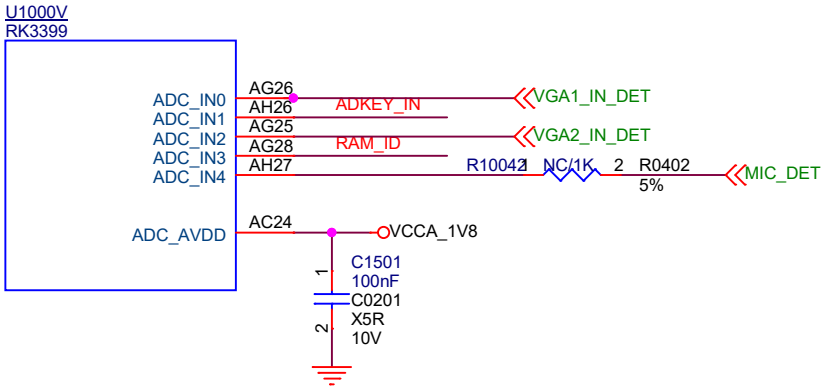
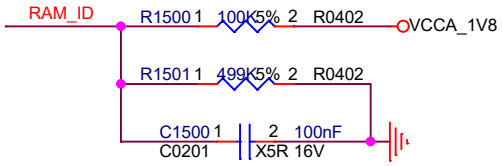
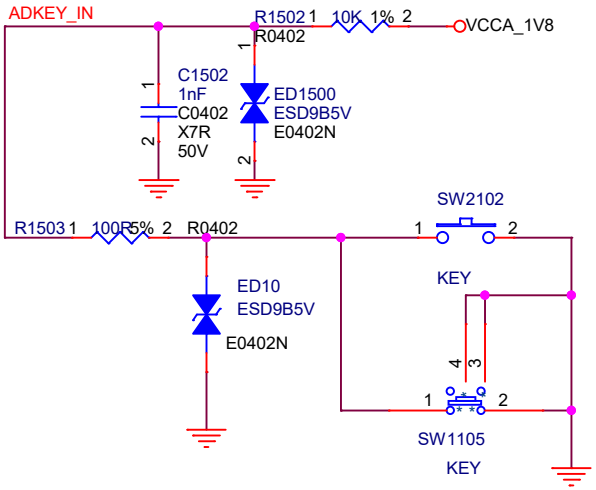
RK3399_V





Note:All the Power filter capacitors should be placed close to the power pins of RK3399

	RAM ID	R1500 PU	R1501 PD
DDR3/DDR3L	0.6V	200K	100K
LPDDR3	0.112V	150K	10K
LPDDR4	1.5V	100K	499K



Note:
1.If ADKEY_IN=0V at power-on reset,
then system will enter into Recovery mode.
2.R1503,SW1500,ED1500 can be deleted if no need at Mass Production

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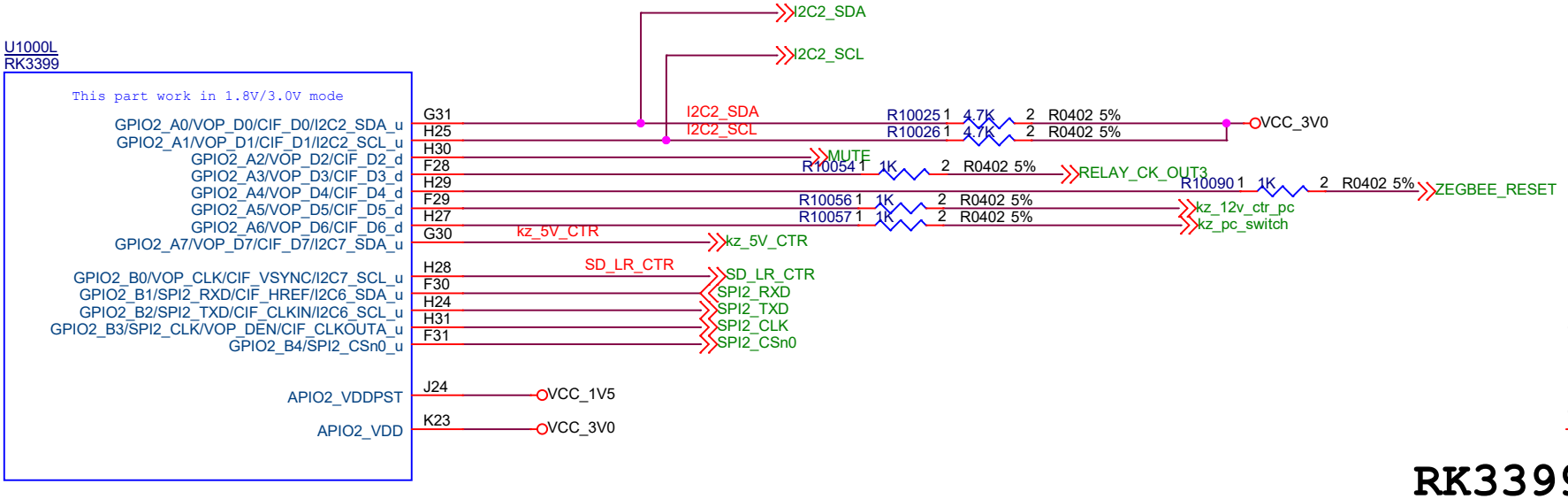
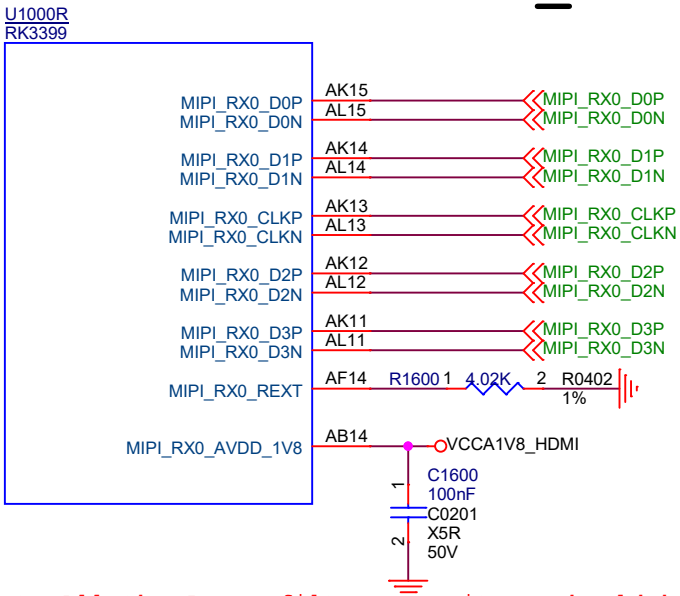
RK3399_L



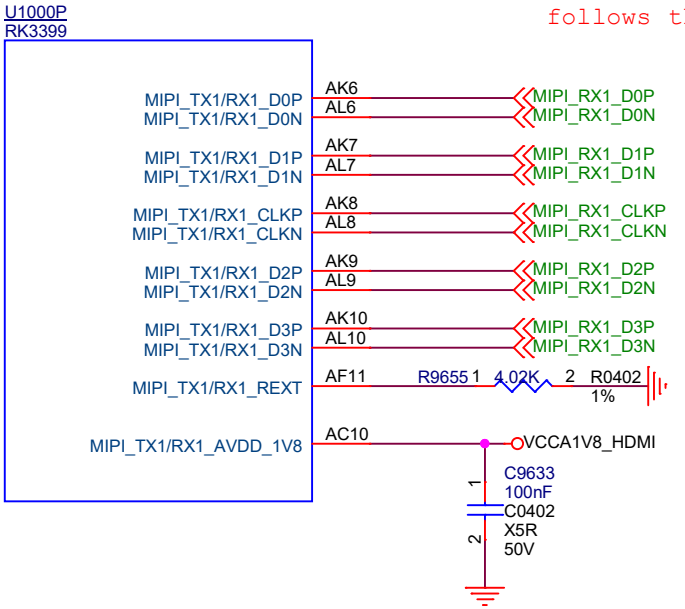
MIPI design rules:
1.Max intra-pair skew < 4ps;
2.Max length skew between clk and data < 7ps;
3.Max trace length < 7.2inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;

RK3399_R



Note:All the Power filter capacitors should be placed close to the power pins of RK3399

RK3399_P



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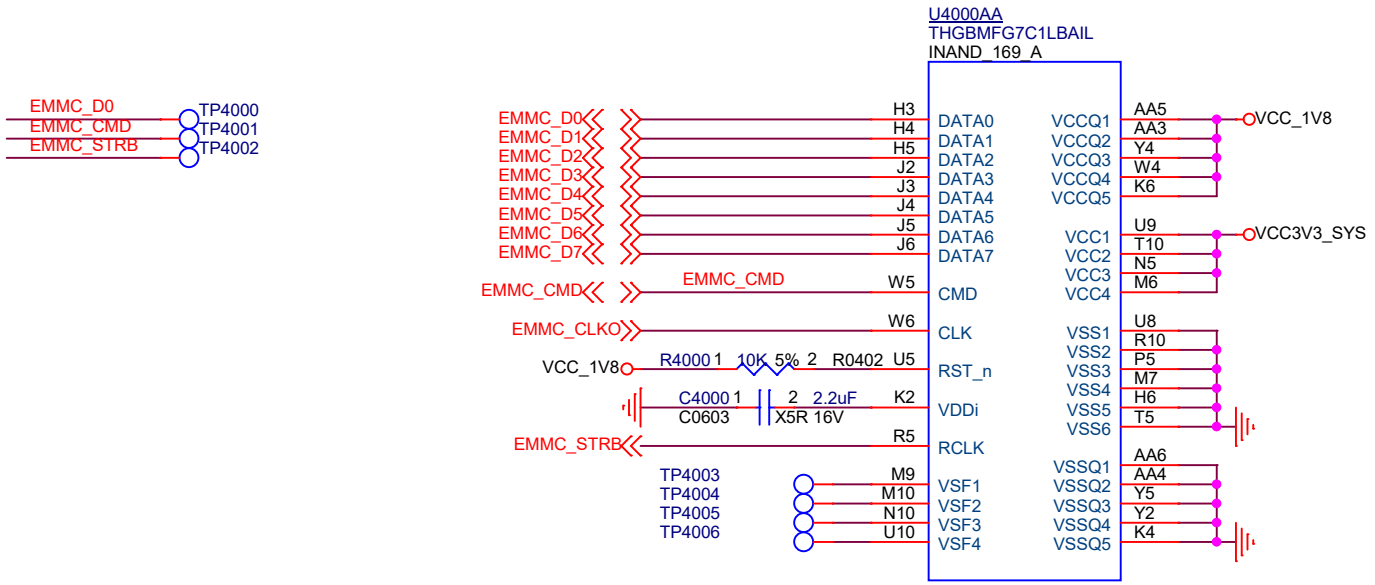
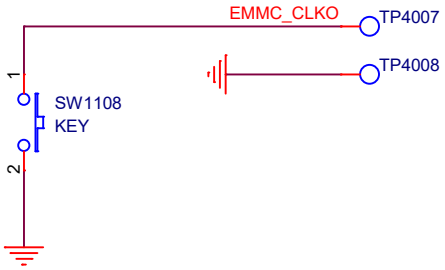
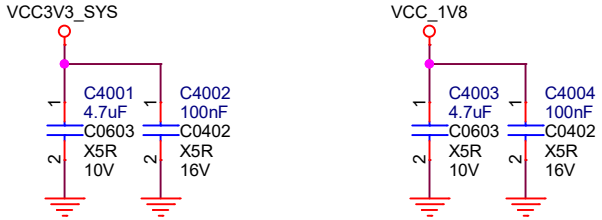
eMMC FLASH



Note:
Reserve TestPoint for firmware update.
If EMMC_CLKO=0V at power-on reset,
then system will enter into Maskrom mode.





Note:All the Power filter capacitors should be placed close to the power pins of eMMC

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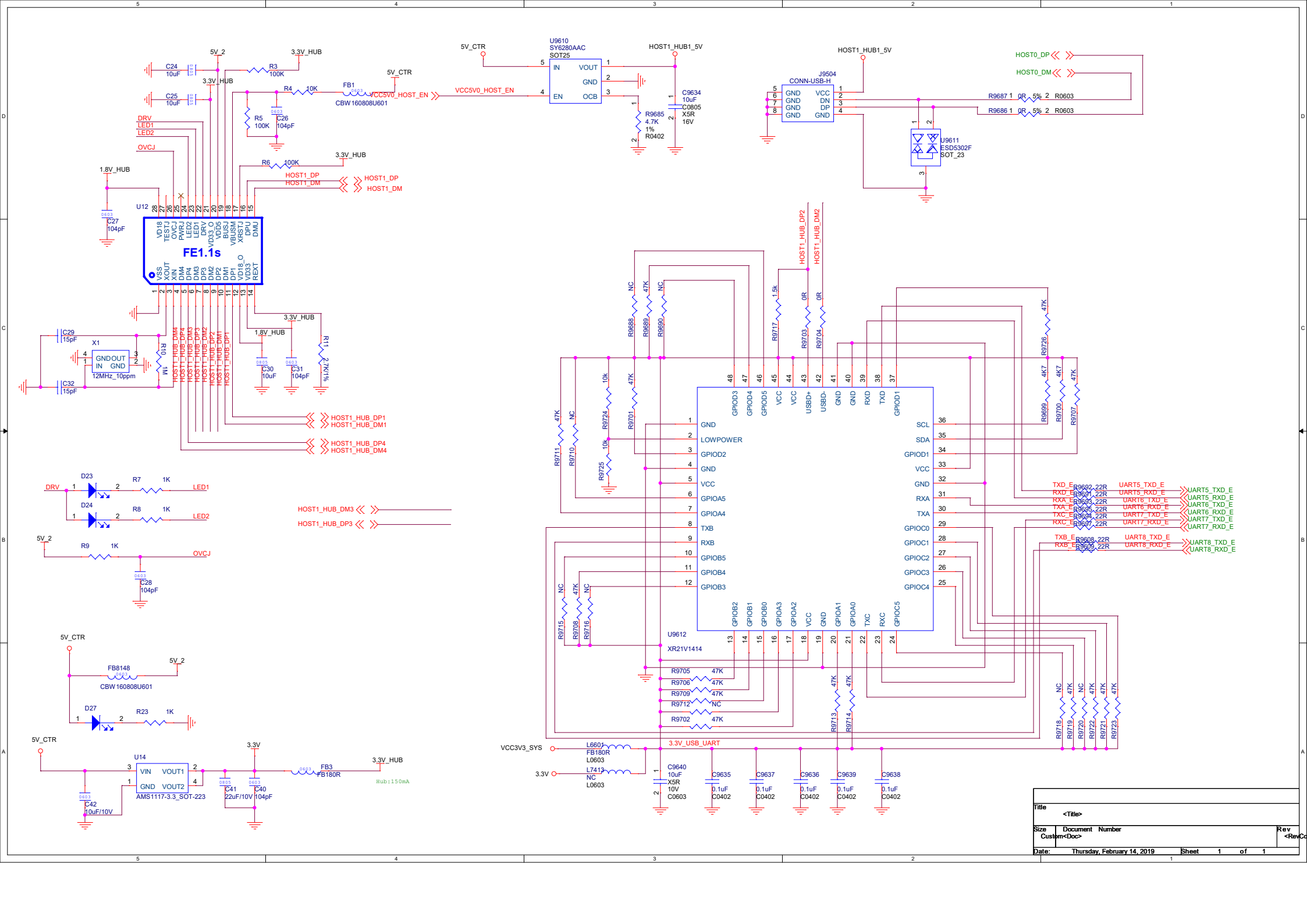
5V_2
3.3V_HUB
C24 10uF
C25 10uF
R3 100K
R4 10K
FB1 CBW160808U601
5V_CTR
VCC5V0_HOST_EN
R5 100K
C26 104pF
DRV
LED1
LED2
OVCJ
R6 100K
HOST1_DP
HOST1_DM
1.8V_HUB
U12
FE1.1s
C27 104pF
C29 15pF
X1
12MHz_10ppm
C32 15pF
R10 1M
C30 10uF
C31 104pF
R11 2.7K/1%
HOST1_HUB_DP1
HOST1_HUB_DM1
HOST1_HUB_DP4
HOST1_HUB_DM4
HOST1_HUB_DM3
HOST1_HUB_DP3
D23
D24
R7 1K
R8 1K
LED1
LED2
R9 1K
C28 104pF
5V_CTR
FB8148
CBW160808U601
D27
R23 1K
U14
AMS1117-3.3_SOT-223
C42 10uF/10V
C41 22uF/10V
C40 104pF
FB3 FB180R
Hub:150mA
U9610
SY6280AAC
SOT25
C9634 10uF
C0805
X5R
16V
R9685 4.7K 1% R0402
HOST1_HUB1_5V
J9504
CONN-USB-H
R9687 0R 5% R0603
R9686 0R 5% R0603
U9611
ESD5302F
SOT_23
HOST0_DP
HOST0_DM
U9612
XR21V1414
R9688 NC
R9689 47K
R9690 NC
R9717 1.5k
R9703 0R
R9704 0R
R9724 10k
R9701 47K
R9725 10k
R9711 47K
R9710 NC
R9715 NC
R9708 47K
R9716 NC
R9705 47K
R9706 47K
R9709 47K
R9712 NC
R9702 47K
R9726 47K
R9699 4K7
R9700 4K7
R9707 47K
R9692 22R
R9691 22R
R9693 22R
R9695 22R
R9694 22R
R9697 22R
R9698 22R
R9696 22R
UART5_TXD_E
UART5_RXD_E
UART6_TXD_E
UART6_RXD_E
UART7_TXD_E
UART7_RXD_E
UART8_TXD_E
UART8_RXD_E
R9713 47K
R9714 47K
R9718 NC
R9719 47K
R9720 NC
R9722 47K
R9721 47K
R9723 47K
3.3V_USB_UART
VCC3V3_SYS
3.3V
L6601 FB180R L0603
L7413 NC L0603
C9640 10uF X5R 10V C0603
C9635 0.1uF C0402
C9637 0.1uF C0402
C9636 0.1uF C0402
C9639 0.1uF C0402
C9638 0.1uF C0402
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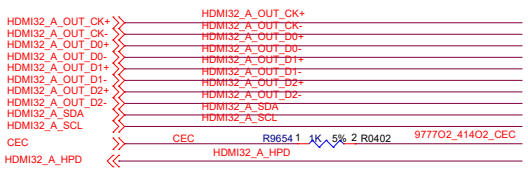
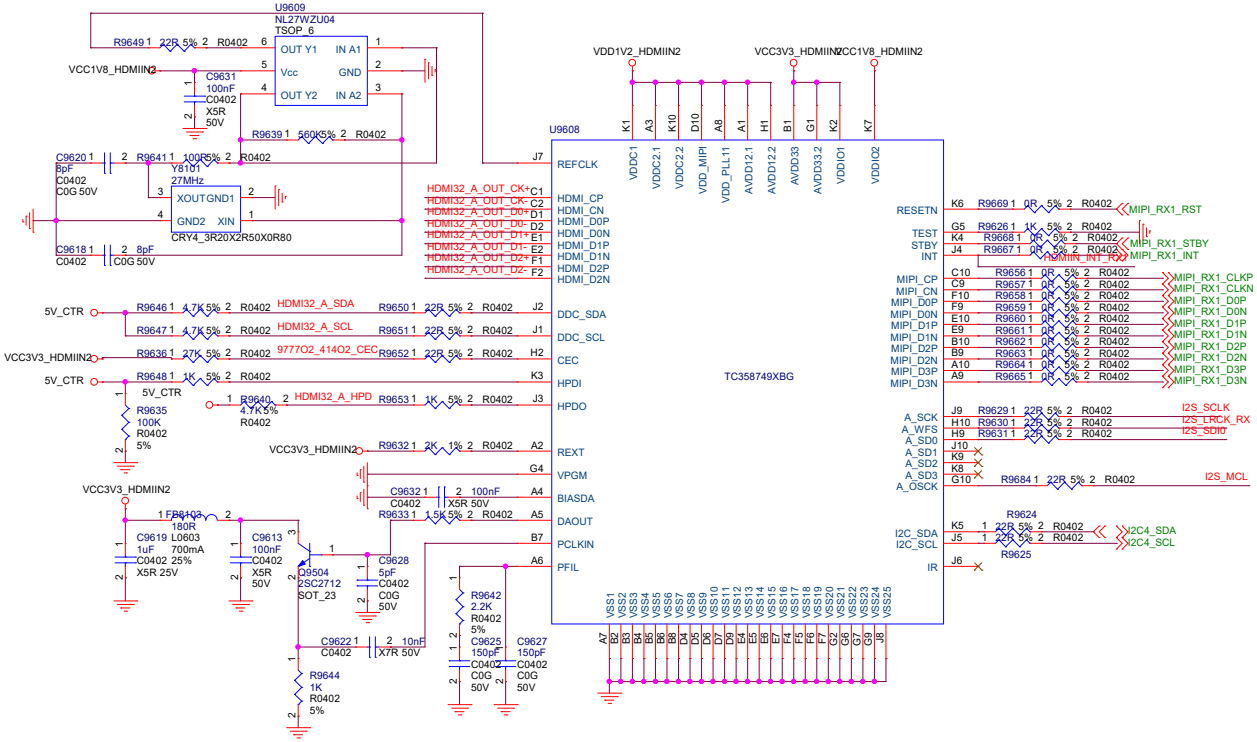
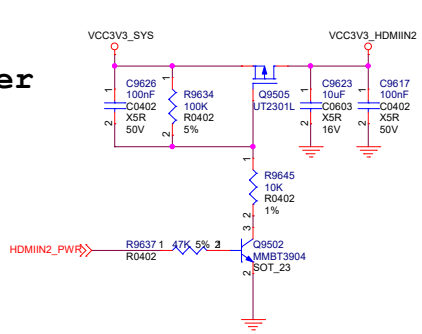
HDMI INPUT

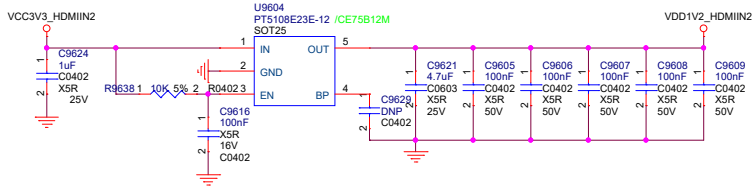


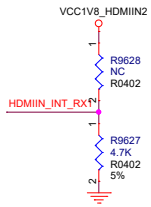
HDMI to MIPI:TC358749XBG

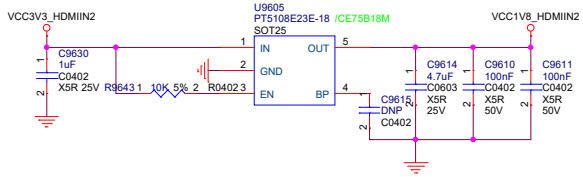


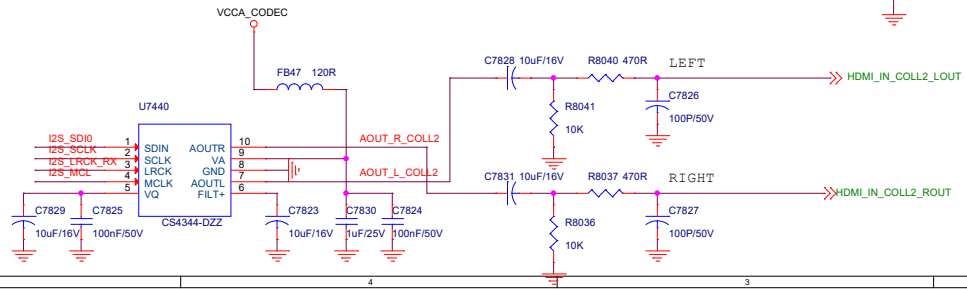
Power











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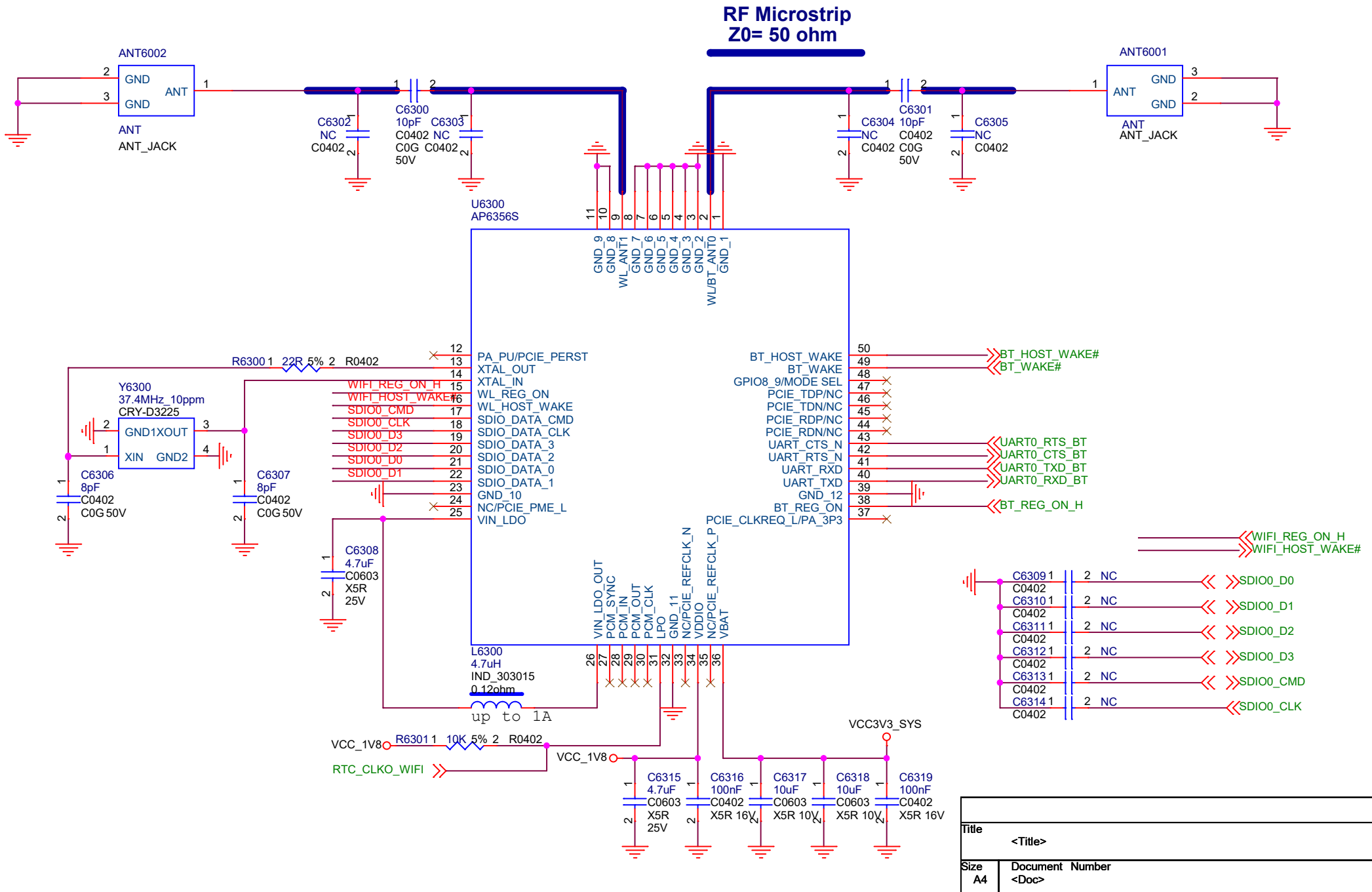
SDIO WIFI/BT MODULE-MIMO

Note:VBAT voltage range is 3.0V~4.8V,
and peak-current is at least 400mA.



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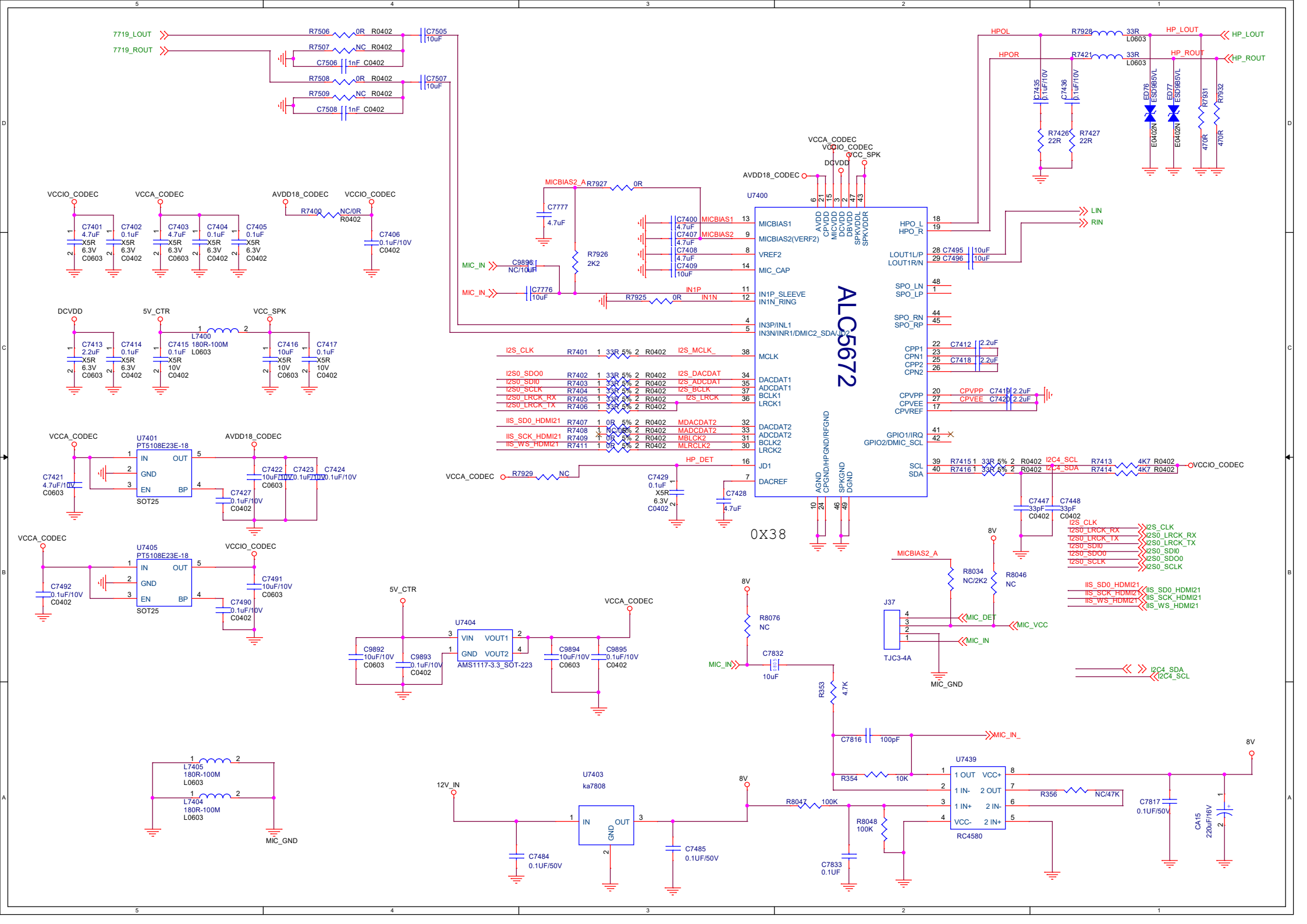
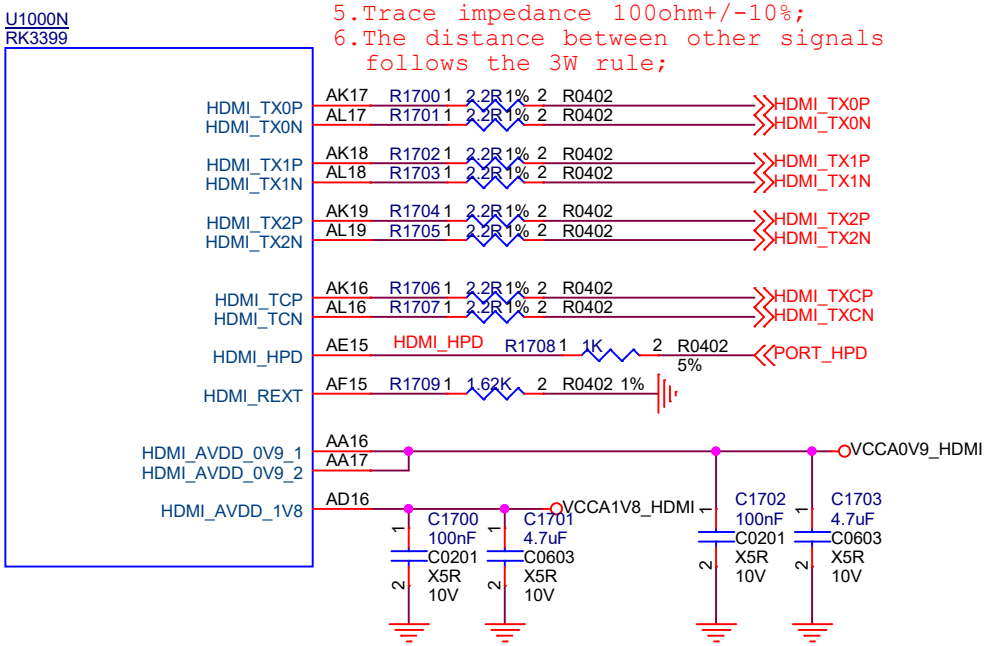

7719_LOUT
7719_ROUT
R7506 0R R0402
R7507 NC R0402
C7506 1nF C0402
R7508 0R R0402
R7509 NC R0402
C7508 1nF C0402
C7505 10uF
C7507 10uF
VCCIO_CODEC
VCCA_CODEC
AVDD18_CODEC
C7401 4.7uF X5R 6.3V C0603
C7402 0.1uF X5R 6.3V C0402
C7403 4.7uF X5R 6.3V C0603
C7404 0.1uF X5R 6.3V C0402
C7405 0.1uF X5R 6.3V C0402
R7400 NC/0R R0402
C7406 0.1uF/10V C0402
DCVDD
5V_CTR
VCC_SPK
C7413 2.2uF X5R 6.3V C0603
C7414 0.1uF X5R 6.3V C0402
L7400 180R-100M L0603
C7415 0.1uF X5R 10V C0402
C7416 10uF X5R 10V C0603
C7417 0.1uF X5R 10V C0402
U7401 PT5108E23E-18 SOT25
C7421 4.7uF/10V C0603
C7422 10uF/10V C0603
C7423 0.1uF/10V
C7424 0.1uF/10V
C7427 0.1uF/10V C0402
U7405 PT5108E23E-18 SOT25
C7492 0.1uF/10V C0402
C7491 10uF/10V C0603
C7490 0.1uF/10V C0402
L7405 180R-100M L0603
L7404 180R-100M L0603
MIC_GND
MICBIAS2_A
R7927 0R
C7777 4.7uF
R7926 2K2
MIC_IN
C9896 NC/10uF
C7776 10uF
R7925 0R
IN1P
IN1N
C7400 MICBIAS1 4.7uF
C7407 MICBIAS2 4.7uF
C7408 4.7uF
C7409 10uF
U7400
ALC5672
MICBIAS1
MICBIAS2(VERF2)
VREF2
MIC_CAP
IN1P_SLEEVE
IN1N_RING
IN3P/INL1
IN3N/INR1/DMIC2_SDA/JD2
MCLK
DACDAT1
ADCDAT1
BCLK1
LRCK1
DACDAT2
ADCDAT2
BCLK2
LRCK2
JD1
DACREF
AVDD
CPVDD
MICVDD
DCVDD
DBVDD
SPKVDDL
SPKVDDR
AGND
CPGND/HPGND/RFGND
SPKGND
DGND
I2S_CLK
R7401 33R 5% 2 R0402
I2S_MCLK_
I2S0_SDO0
I2S0_SDI0
I2S0_SCLK
I2S0_LRCK_RX
I2S0_LRCK_TX
R7402 33R 5% 2 R0402
R7403 33R 5% 2 R0402
R7404 33R 5% 2 R0402
R7405 33R 5% 2 R0402
R7406 33R 5% 2 R0402
I2S_DACDAT
I2S_ADCDAT
I2S_BCLK
I2S_LRCK
IIS_SD0_HDMI21
IIS_SCK_HDMI21
IIS_WS_HDMI21
R7407 0R 5% 2 R0402
R7408 NC/0R 5% 2 R0402
R7409 0R 5% 2 R0402
R7411 0R 5% 2 R0402
MDACDAT2
MADCDAT2
MBLCK2
MLRCLK2
HP_DET
R7929 NC
C7429 0.1uF X5R 6.3V C0402
C7428 4.7uF
0X38
HPOL
HPOR
R7928 33R L0603
R7421 33R L0603
HP_LOUT
HP_ROUT
C7435 0.1uF/10V
C7436 0.1uF/10V
R7426 22R
R7427 22R
ED76 ESD9B5VL E0402N
ED77 ESD9B5VL E0402N
R7931 470R
R7932 470R
HPO_L
HPO_R
LOUT1L/P
LOUT1R/N
C7495 10uF
C7496 10uF
LIN
RIN
SPO_LN
SPO_LP
SPO_RN
SPO_RP
CPP1
CPN1
CPP2
CPN2
C7412 2.2uF
C7418 2.2uF
CPVPP
CPVEE
CPVREF
C7419 2.2uF
C7420 2.2uF
GPIO1/IRQ
GPIO2/DMIC_SCL
SCL
SDA
R7415 33R 5% 2 R0402
R7416 33R 5% 2 R0402
I2C4_SCL
I2C4_SDA
R7413 4K7 R0402
R7414 4K7 R0402
C7447 33pF C0402
C7448 33pF C0402
I2S_CLK
I2S0_LRCK_RX
I2S0_LRCK_TX
I2S0_SDI0
I2S0_SDO0
I2S0_SCLK
IIS_SD0_HDMI21
IIS_SCK_HDMI21
IIS_WS_HDMI21
I2C4_SDA
I2C4_SCL
8V
MICBIAS2_A
R8034 NC/2K2
R8046 NC
J37
TJC3-4A
MIC_DET
MIC_VCC
MIC_IN
MIC_GND
U7404
AMS1117-3.3_SOT-223
VIN
VOUT1
VOUT2
GND
C9892 10uF/10V C0603
C9893 0.1uF/10V C0402
C9894 10uF/10V C0603
C9895 0.1uF/10V C0402
R8076 NC
C7832 10uF
R353 4.7K
C7816 100pF
MIC_IN_
U7403
ka7808
12V_IN
C7484 0.1UF/50V
C7485 0.1UF/50V
R8047 100K
R8048 100K
C7833 0.1uF
U7439
RC4580
1 OUT
VCC+
1 IN-
2 OUT
1 IN+
2 IN-
VCC-
2 IN+
R354 10K
R356 NC/47K
C7817 0.1UF/50V
CA15 220uF/16V

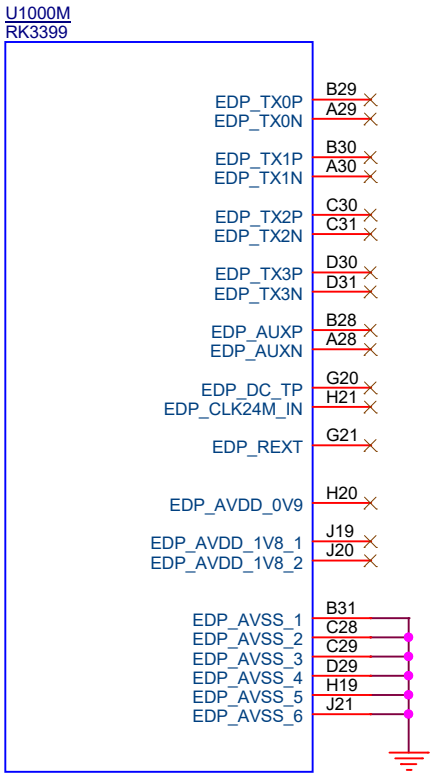
RK3399_N

HDMI design rules:
1.Max intra-pair skew < 4ps;
2.Max length skew between clk and data < 80ps;
3.Max trace length < 9.8inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;

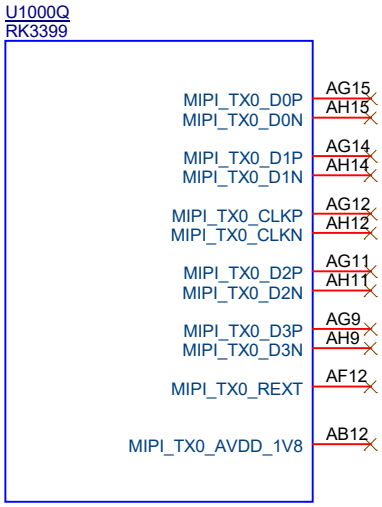


Note:All the Power filter capacitors should be placed close to the power pins of RK3399

RK3399_M



RK3399_Q



eDP design rules:
1.Max intra-pair skew <4 ps;
2.Max trace length < 6inchs;
3.Max allowed via < 4;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals follows the 3W rule;

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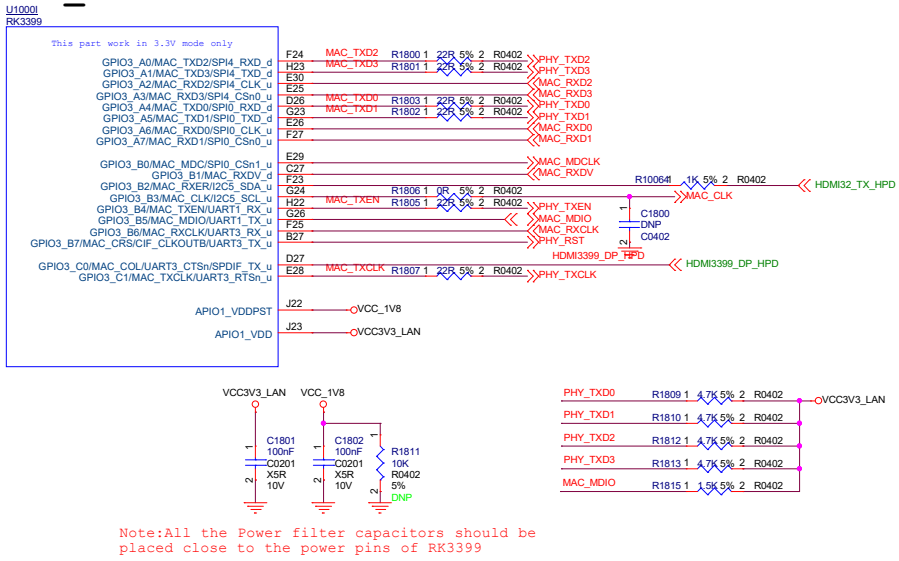
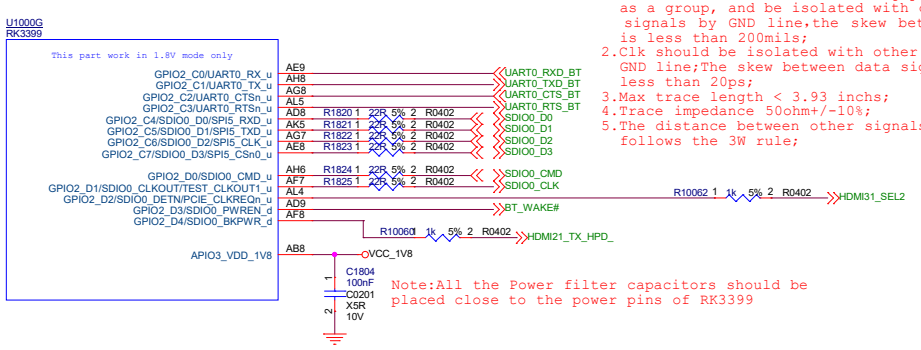
RK3399_I



Note:All the Power filter capacitors should be placed close to the power pins of RK3399

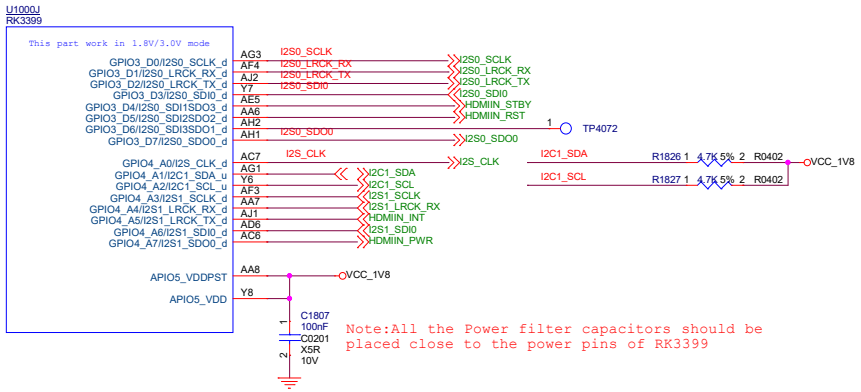
RK3399_G



SDIO design rules:
1.Data[0:3] and CMD lines routing parallel as a group, and be isolated with other signals by GND line,the skew between group is less than 200mils;
2.Clk should be isolated with other signals by GND line;The skew between data signals is less than 20ps;
3.Max trace length < 3.93 inchs;
4.Trace impedance 50ohm+/-10%;
5.The distance between other signals follows the 3W rule;

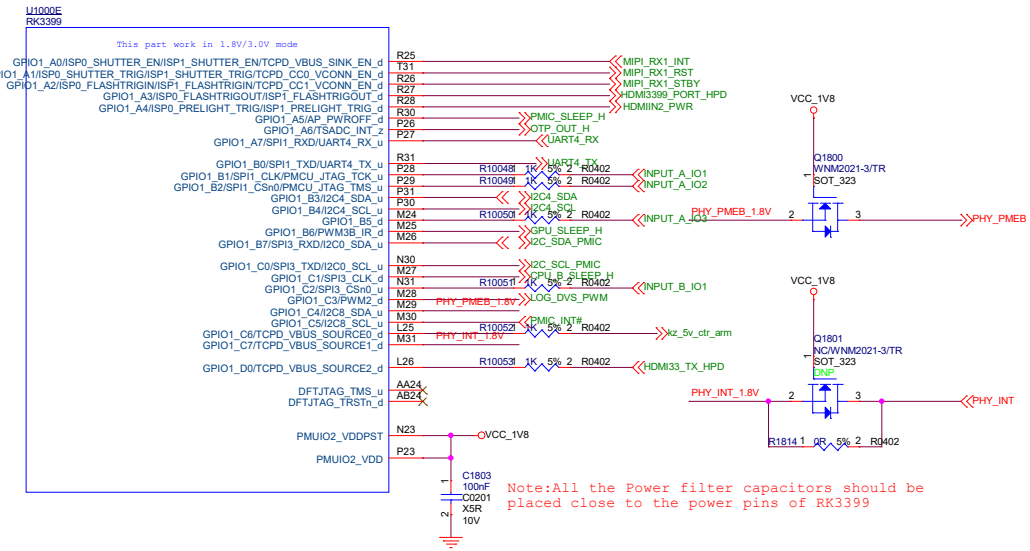
Note:All the Power filter capacitors should be placed close to the power pins of RK3399

RK3399_J

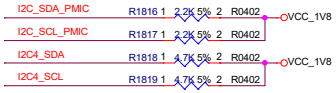


Note:All the Power filter capacitors should be placed close to the power pins of RK3399

RK3399_E



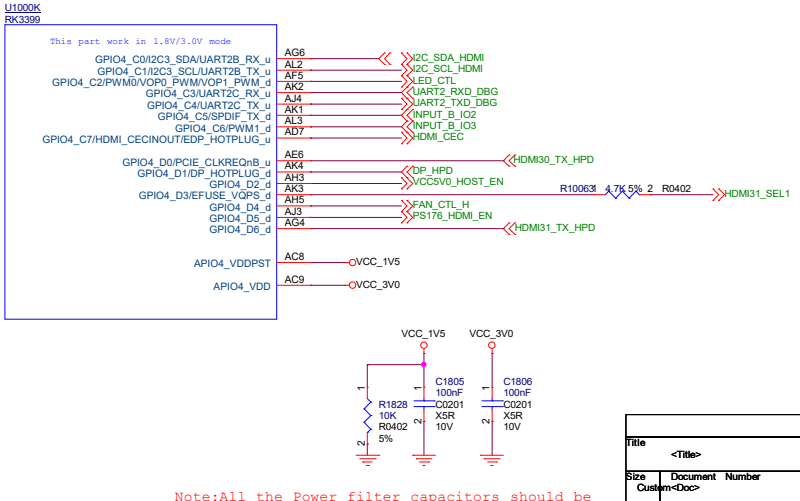
Note:All the Power filter capacitors should be placed close to the power pins of RK3399



1.8V Only	VDDPST=VDDIO=1.8V
3.3V Only	VDDPST=1.8V,VDDIO=3.3V
1.8V/3.0V mode	3.0V mode:VDDPST=1.5V,VDDIO=3.0V 1.8V mode:VDDPST=1.8V,VDDIO=1.8V

Note:All the part which support 1.8V and 3.0V mode, software config should match with hardware design.

RK3399_K



Note:All the Power filter capacitors should be placed close to the power pins of RK3399

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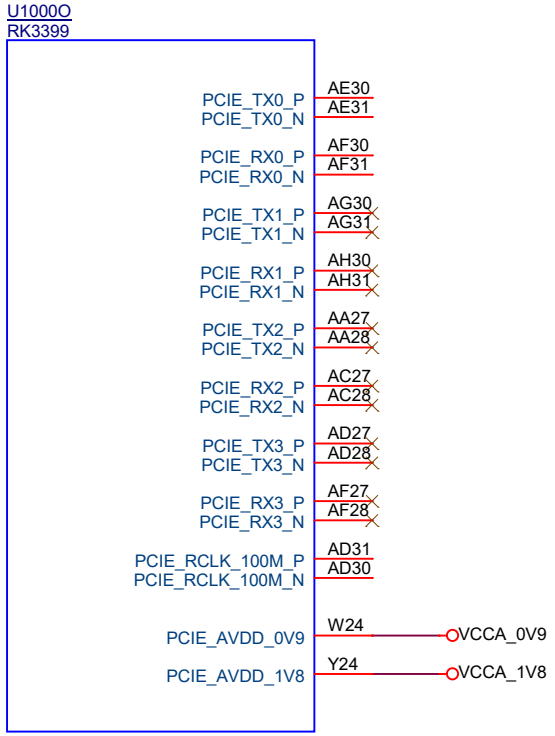
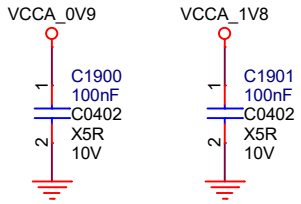
RK3399_O



PCIE design rules:
1.Max intra-pair skew < 4ps;
2.Max inter-pair skew < 1.6ns;
3.Max trace length < 14inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;



Note:All the Power filter capacitors should be placed close to the power pins of RK3399

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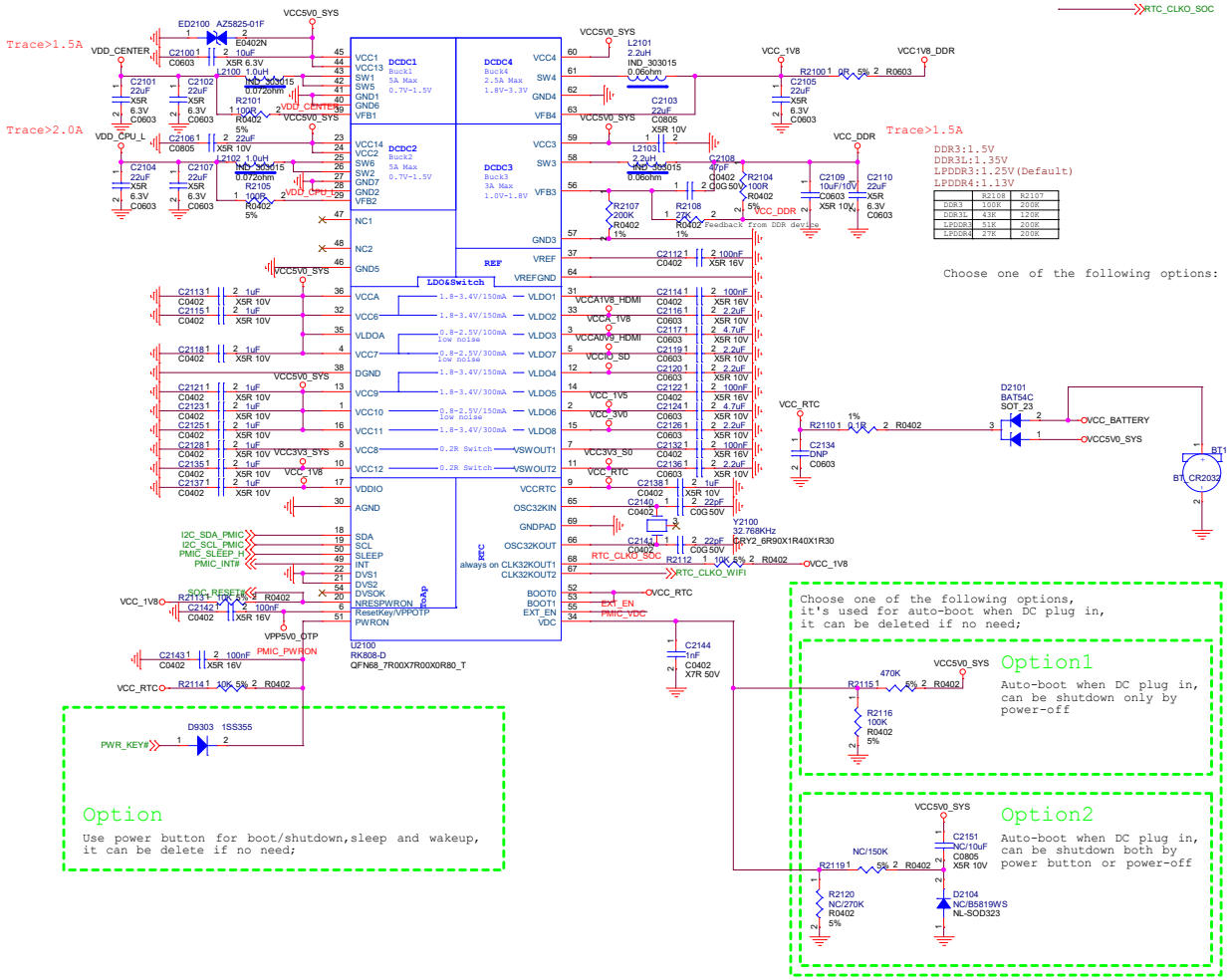
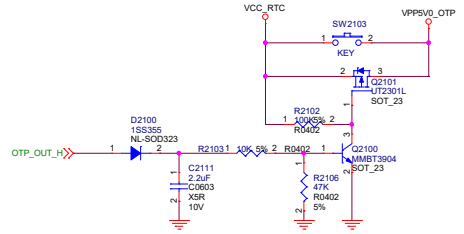
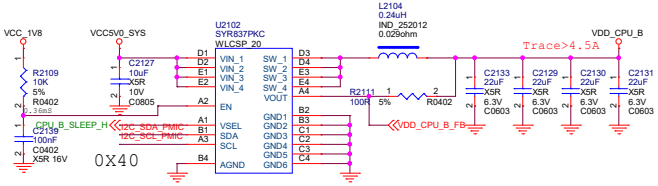
PMIC RK808-D



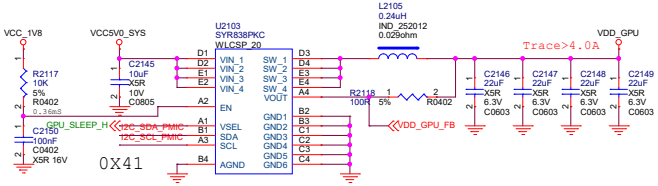
Over-temperature Protection & RESET



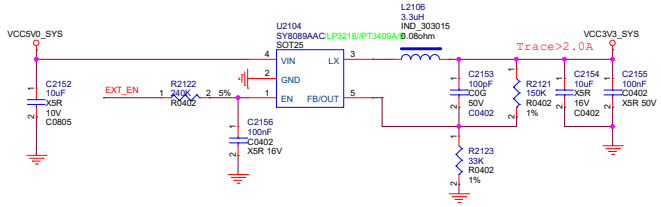
Power of VDD_CPU_B

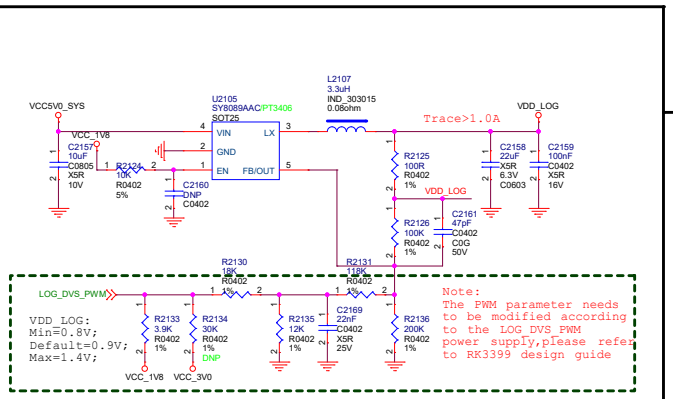


Power of VDD_GPU

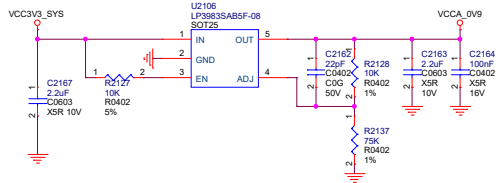


Power of VCC3V3_SYS

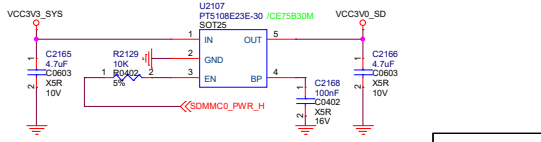




Power of VCCA_0V9



Power of VCC3V0_SD



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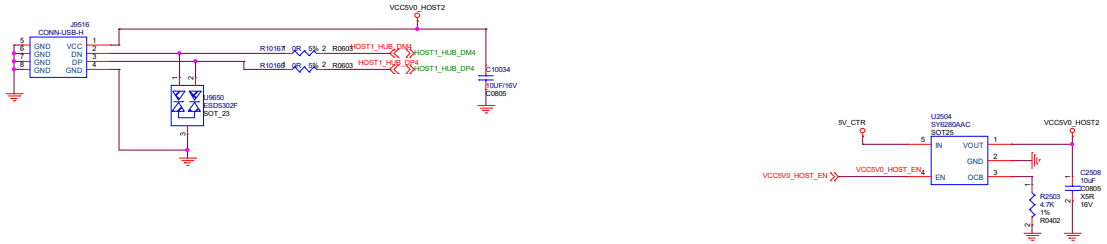
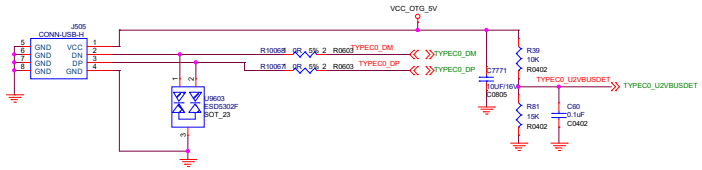
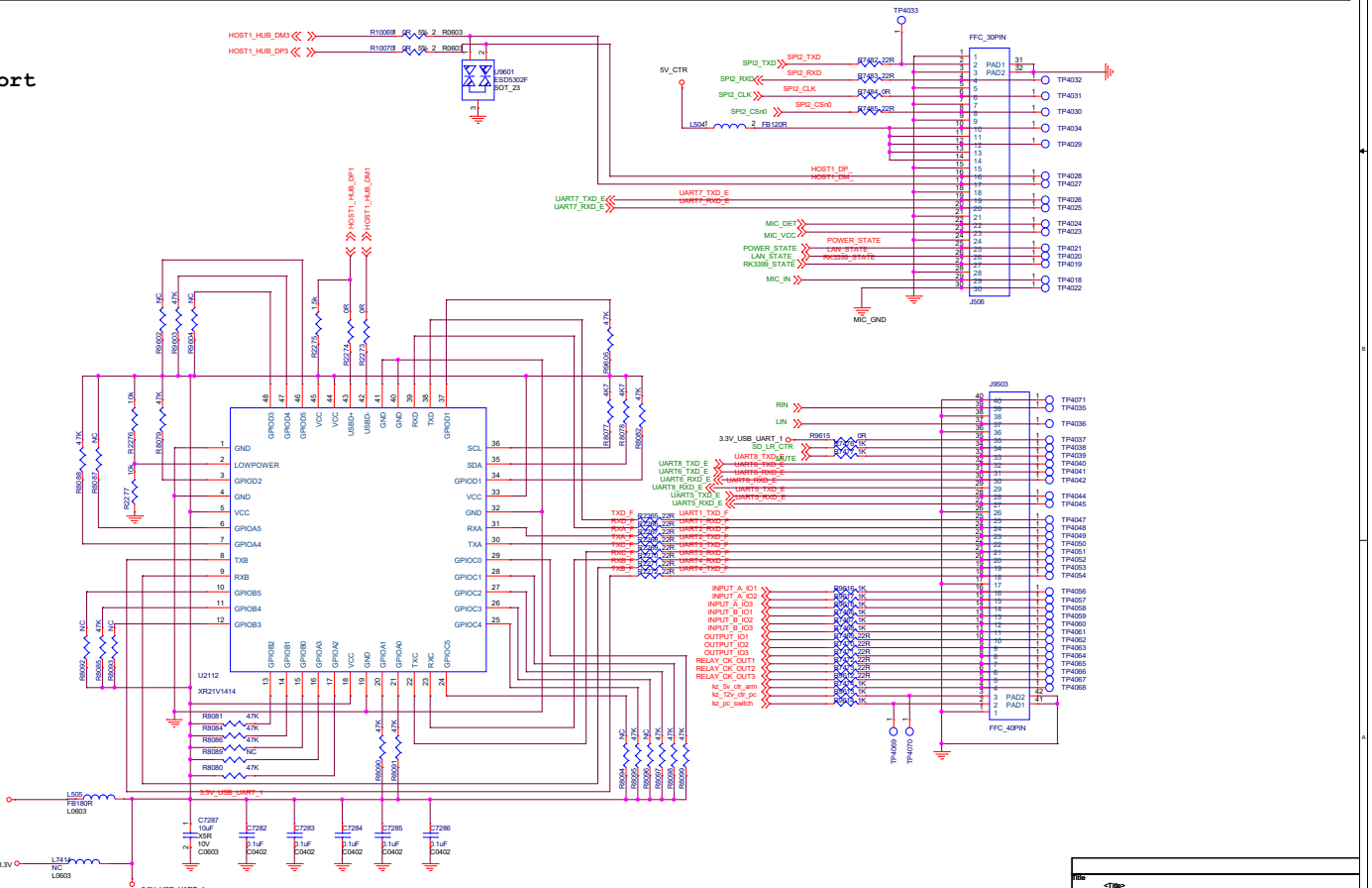




USB2.0 OTG Port



USB2.0 HOST Port

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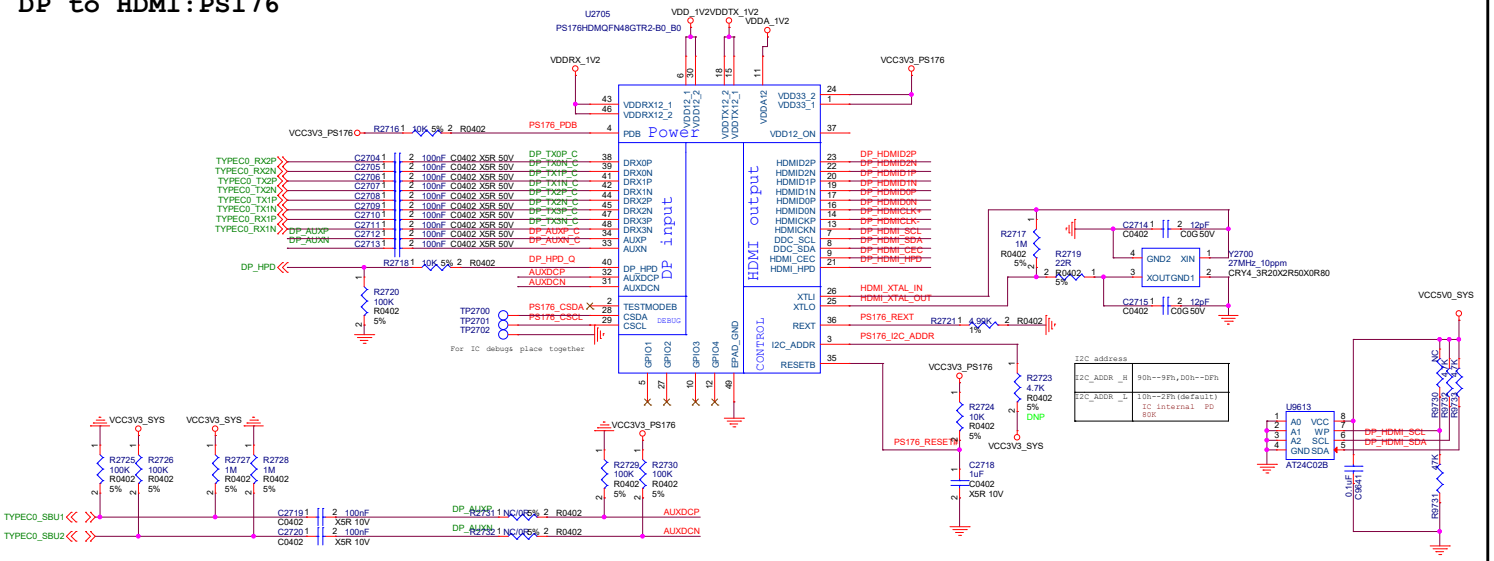
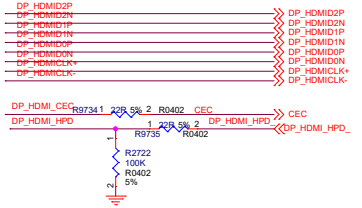
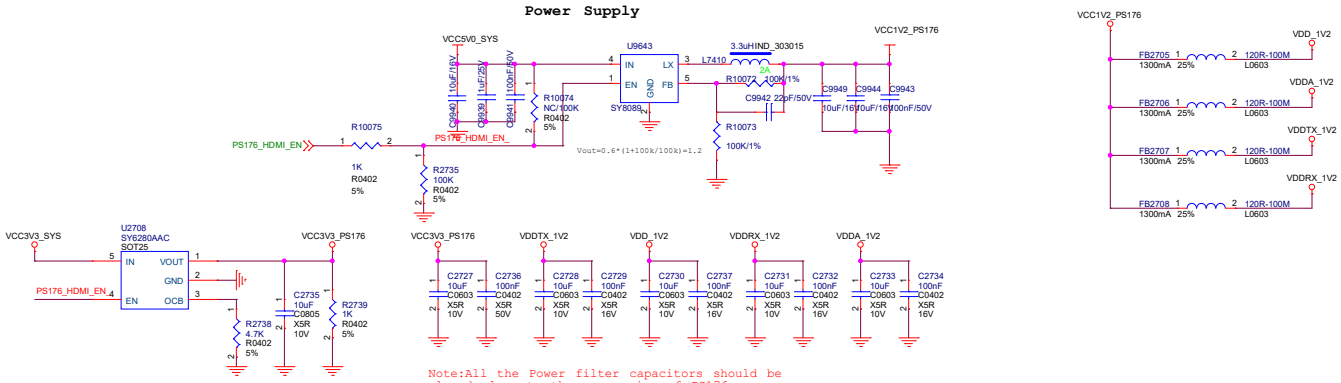
DP to HDMI:PS176



HDMI Output Port



PS176 Power



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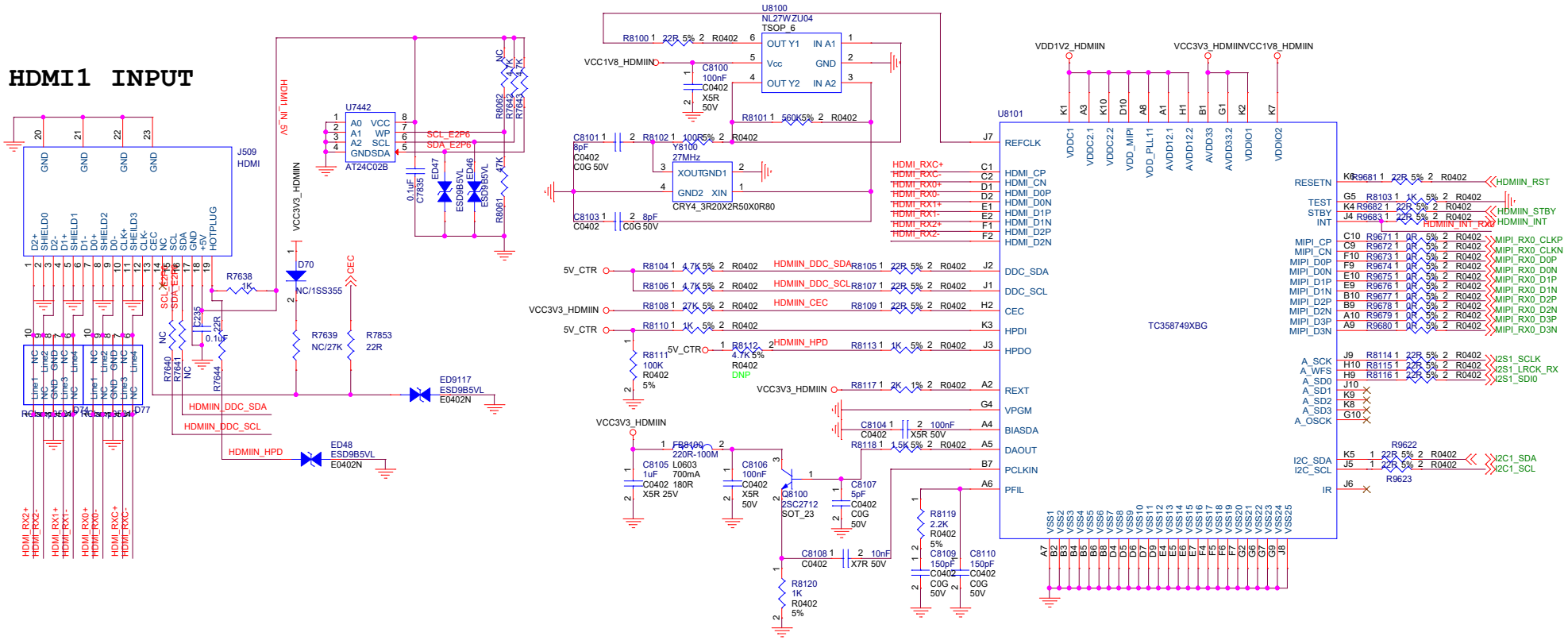
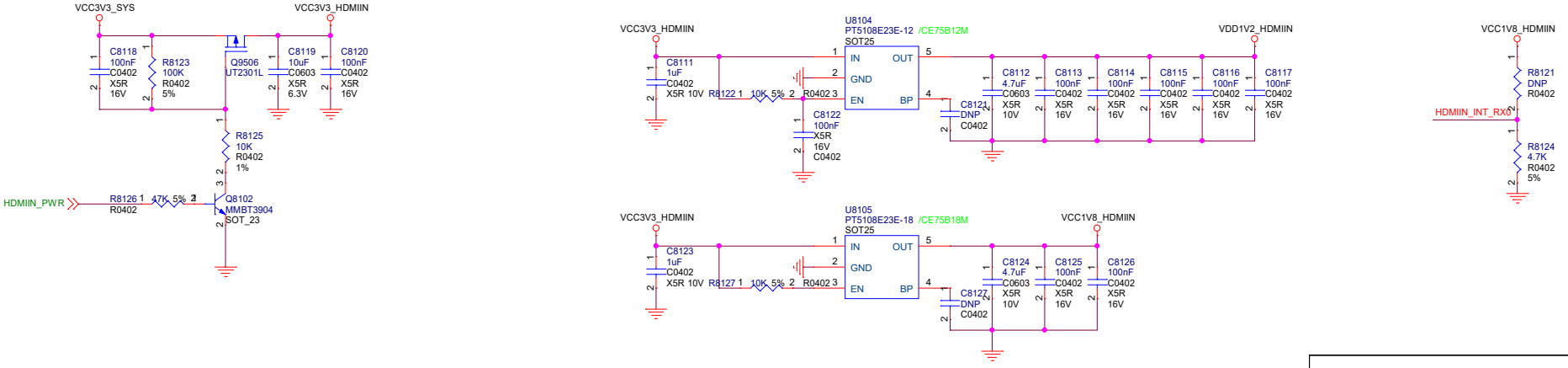
HDMI to MIPI:TC358749XBG

HDMI1 INPUT



Power



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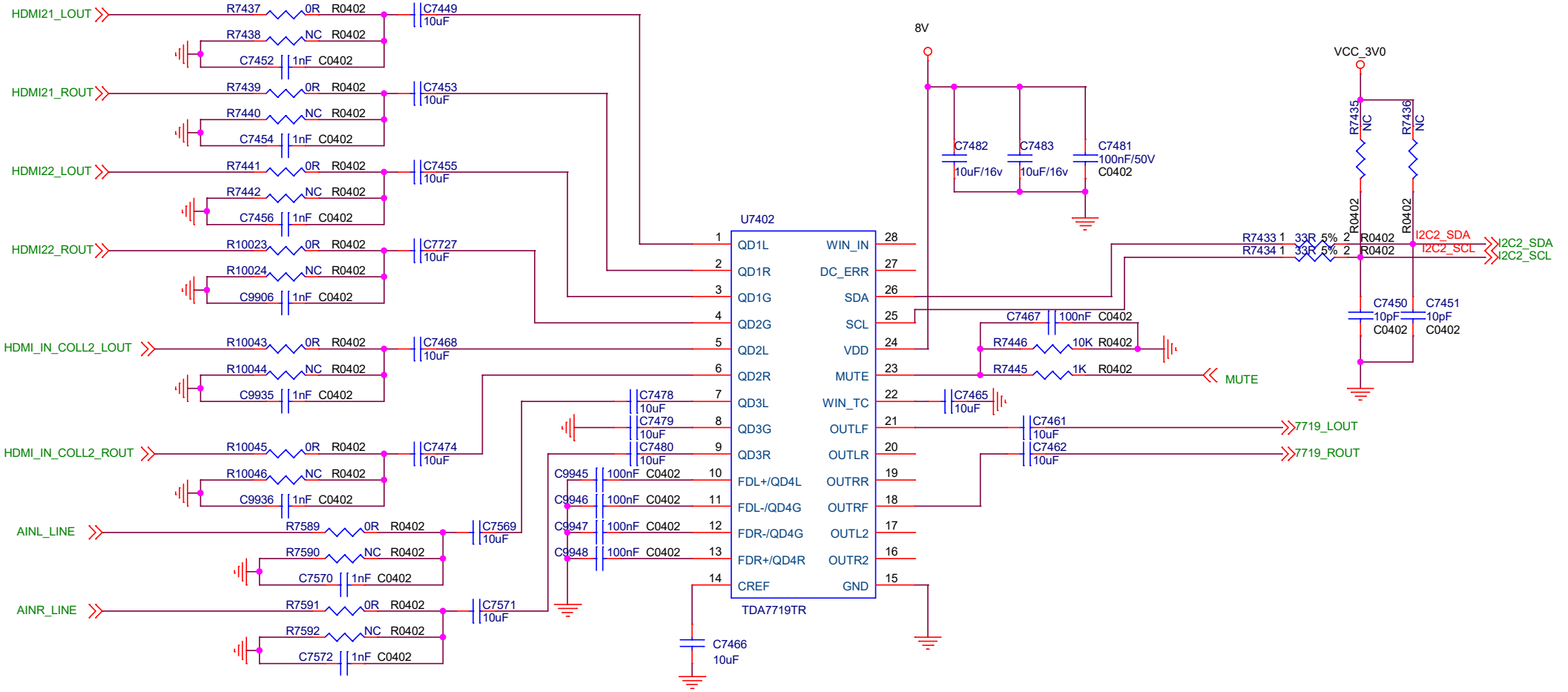

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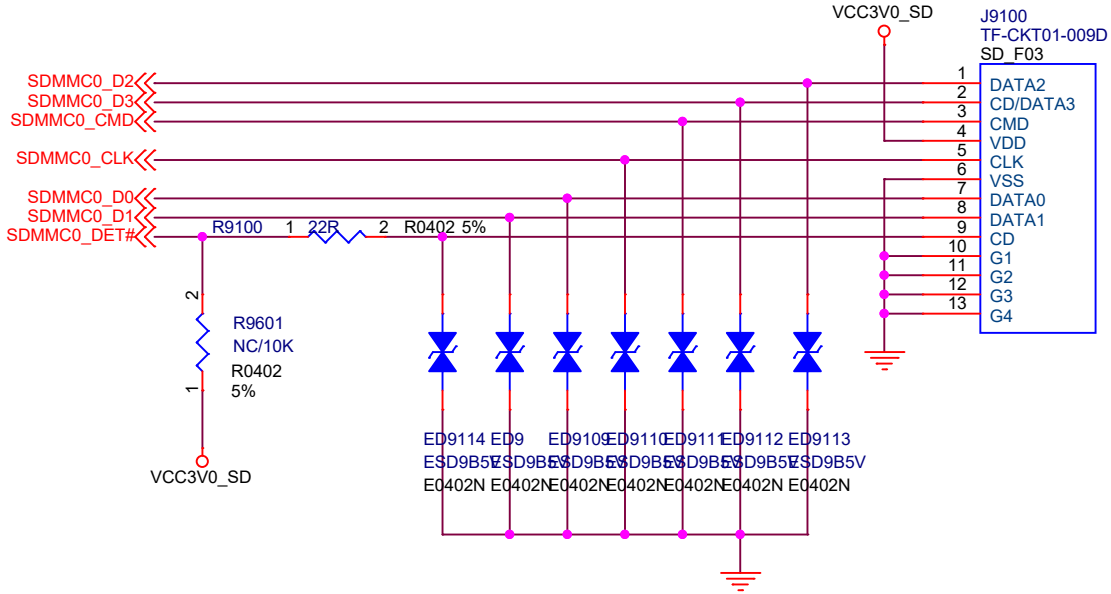
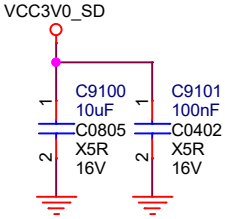
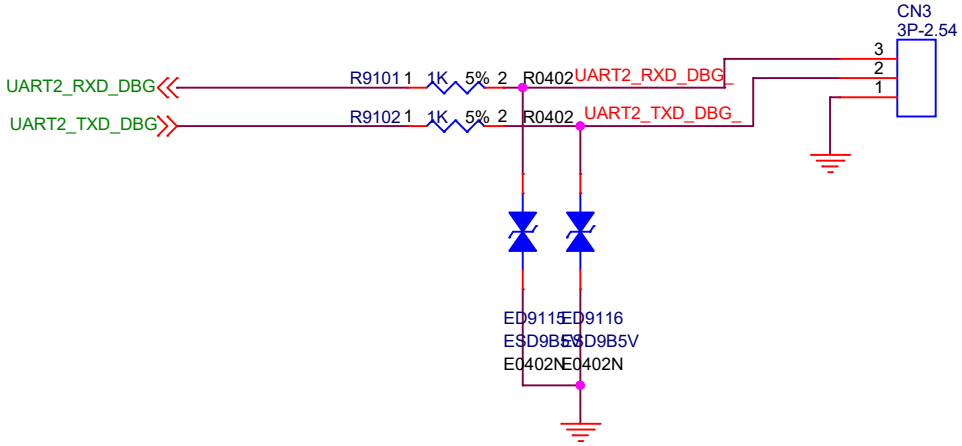
TF CARD





UART for debug



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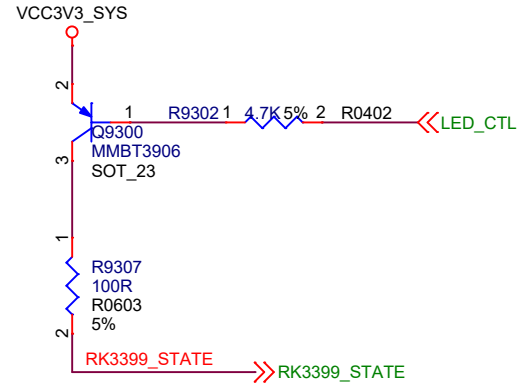
LED

Note:
Blue LED shows work states



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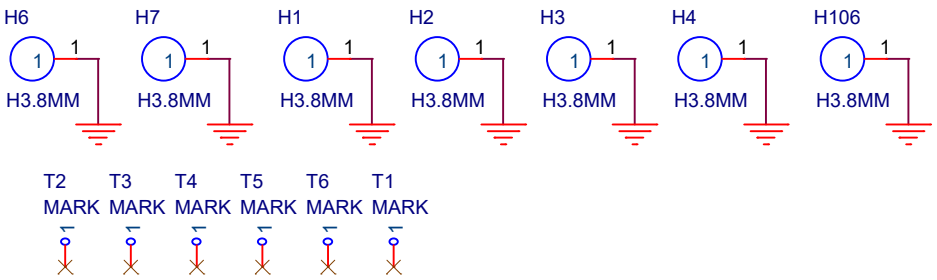
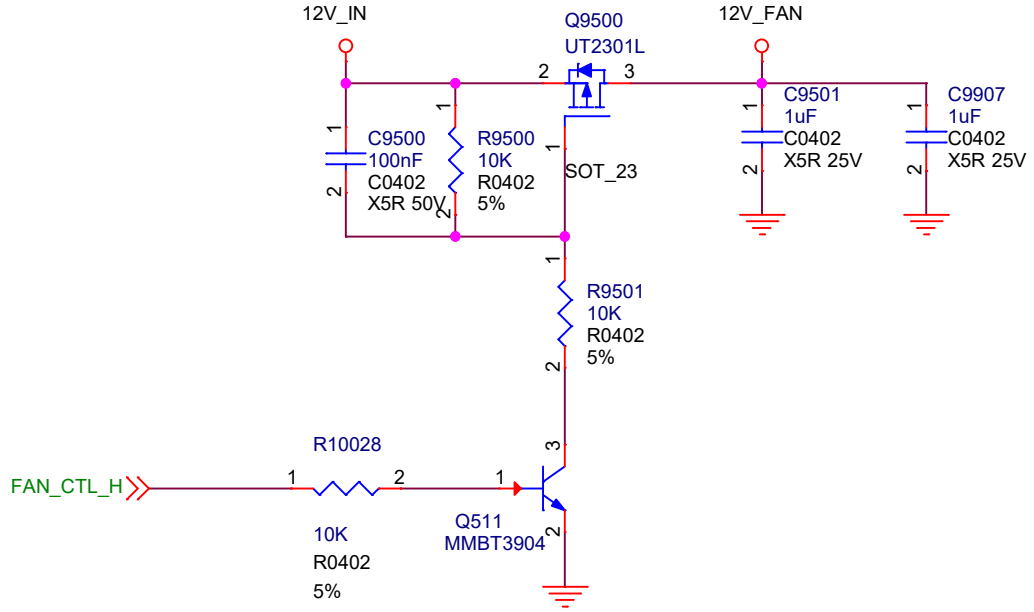
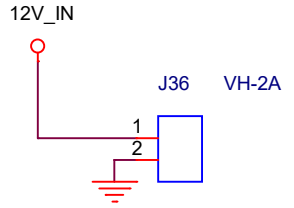
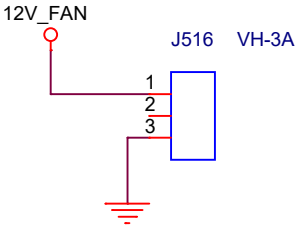
HEATSINK/FAN(option)

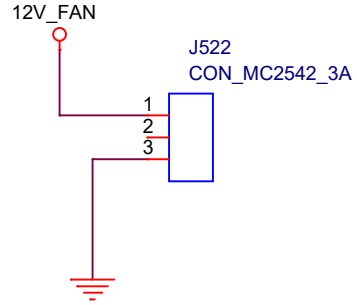
Note:Power for FAN,It can be deleted if no need.











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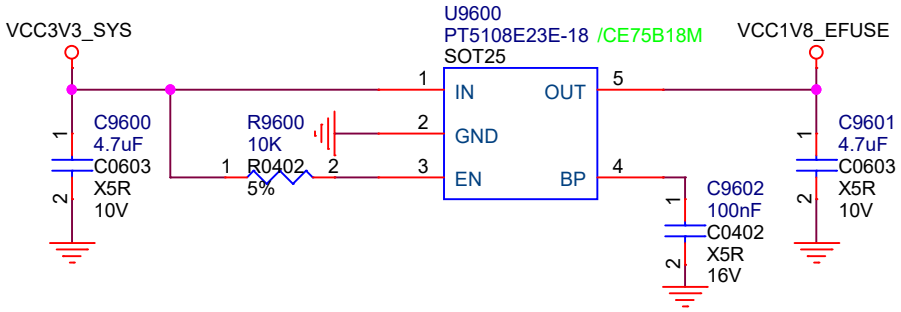
eFUSE(option)

Note:Power for eFUSE Program,it is recommended to
reserve on the tooling.It can be deleted if no need.



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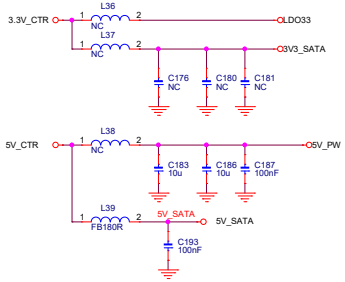
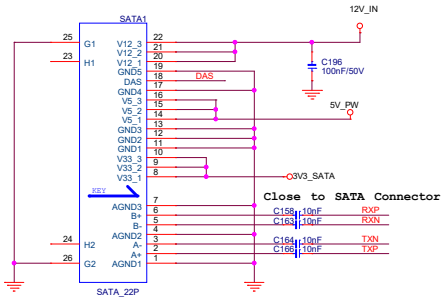
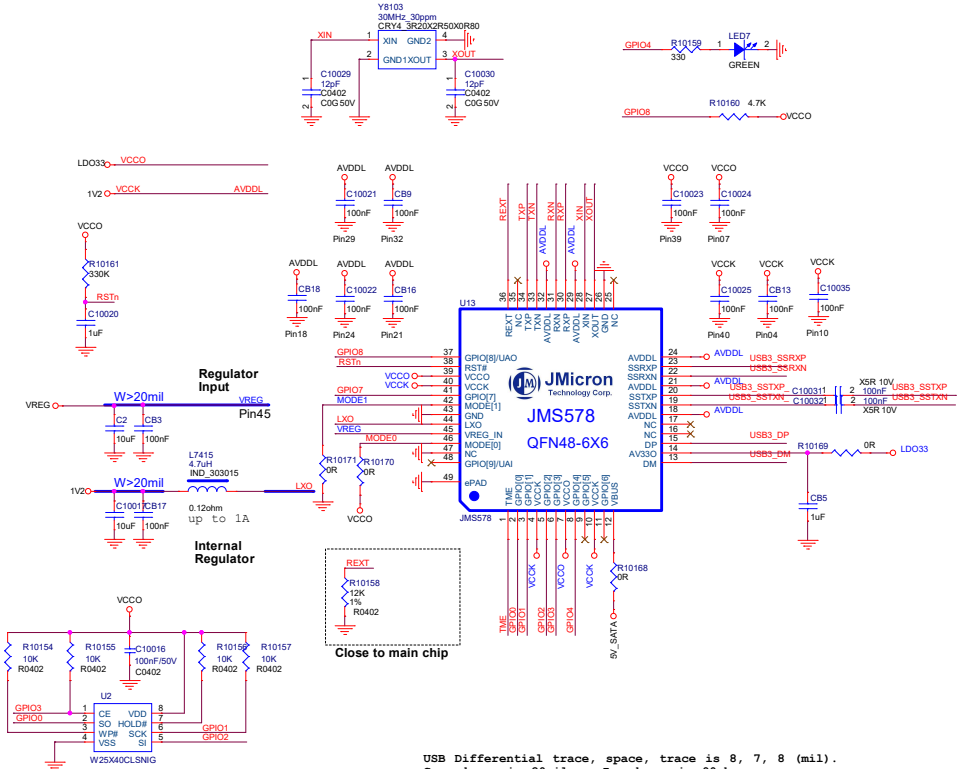


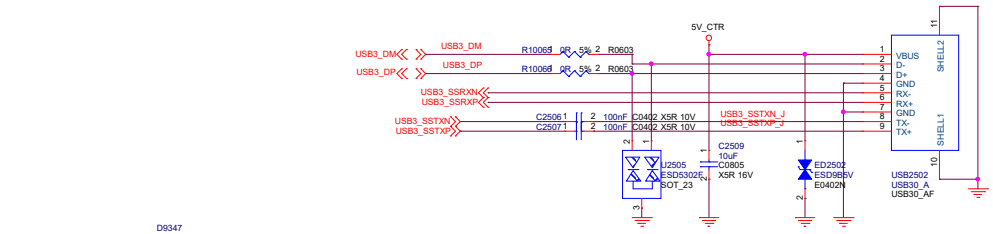


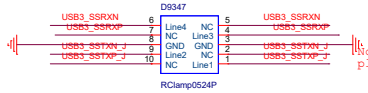
SATA Differential trace, space, trace is 5, 7, 5 (mil).
Ground gap is 20mil. Impedance is 100ohm.



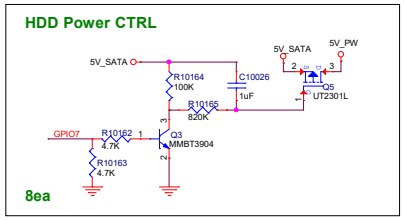
USB Differential trace, space, trace is 8, 7, 8 (mil).
Ground gap is 20mil. Impedance is 90ohm.

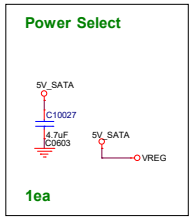
USB3.0 HOST Port

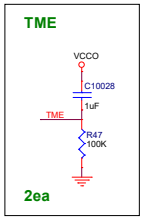


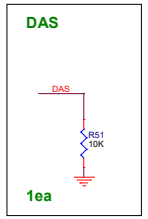


Note:All the ESD components should be placed close to the port









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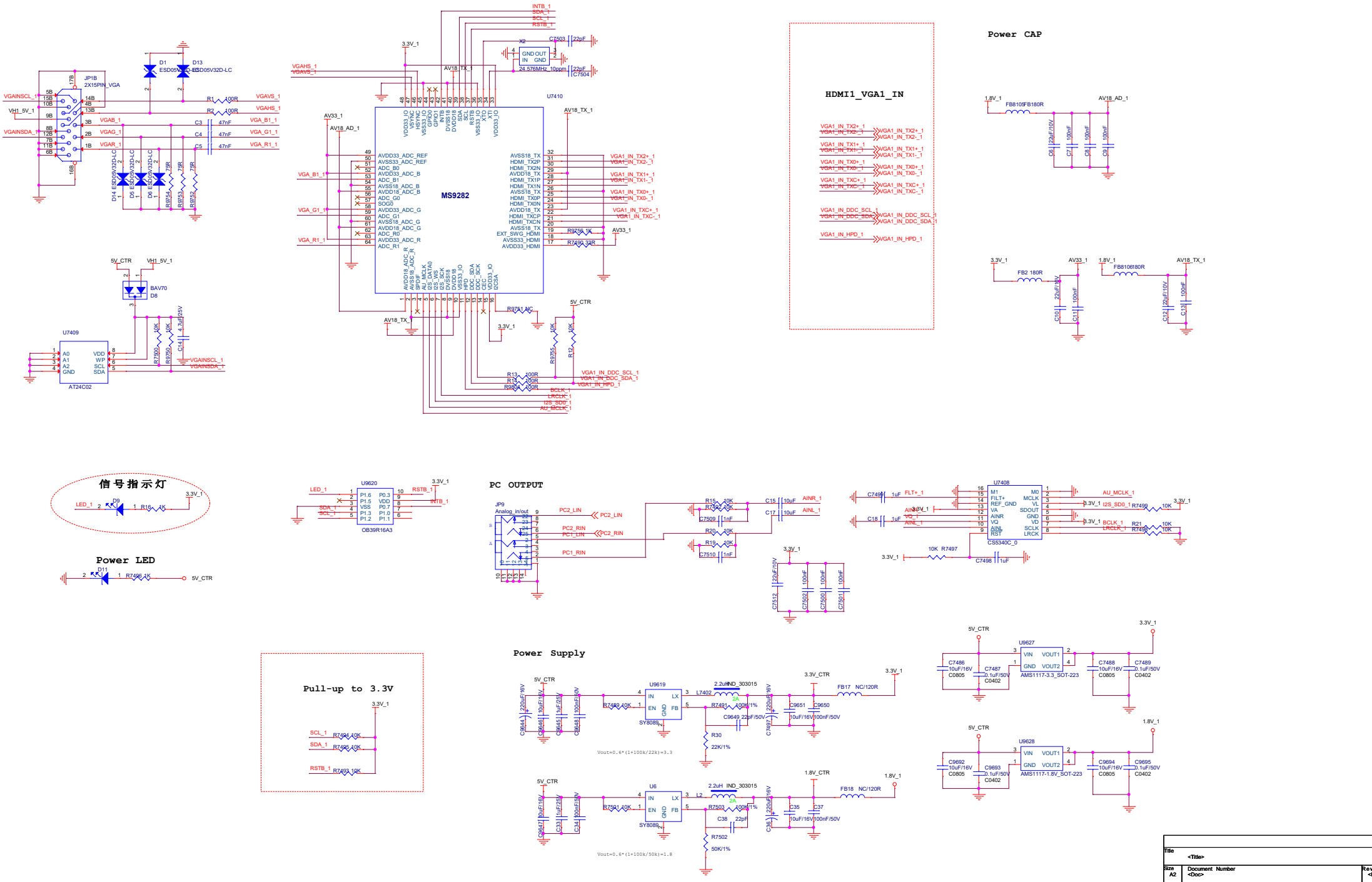

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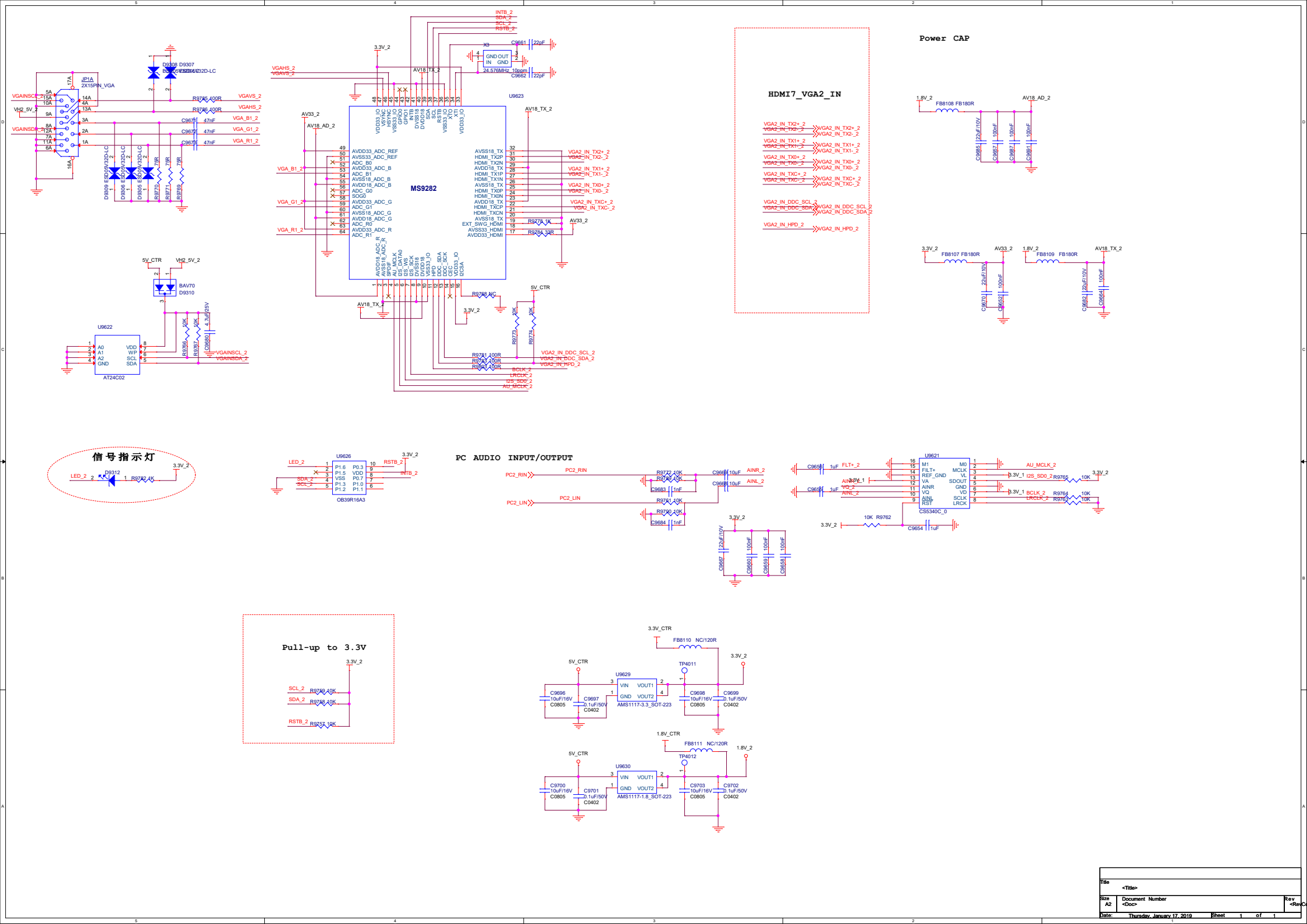
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JP1A
2X15PIN_VGA
U9622
AT24C02
U9626
OB39R16A3
U9621
CS5340C_0
U9629
AMS1117-3.3_SOT-223
U9630
AMS1117-1.8_SOT-223
信号指示灯
PC AUDIO INPUT/OUTPUT
Pull-up to 3.3V
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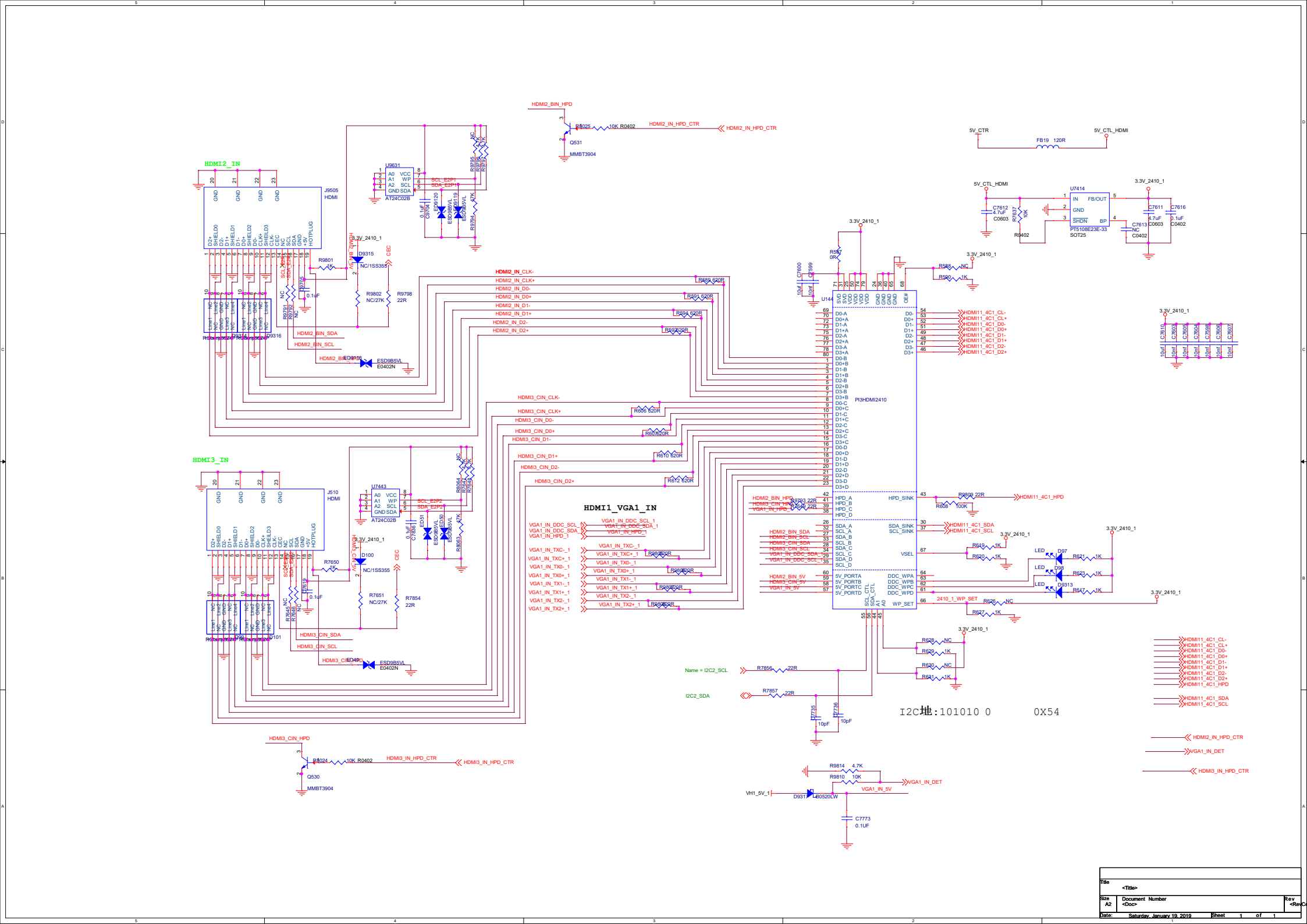
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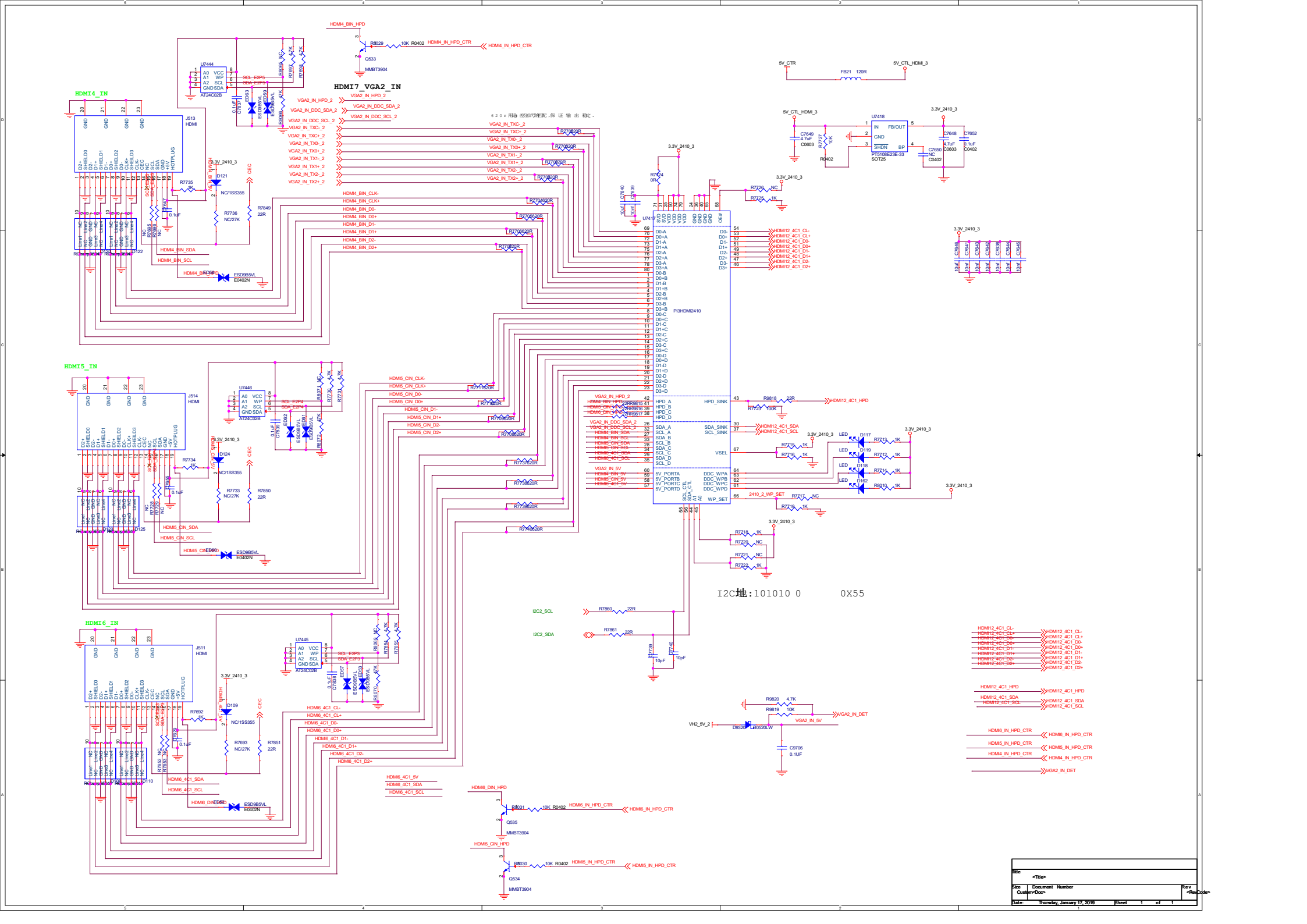
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PI3HDMI2410
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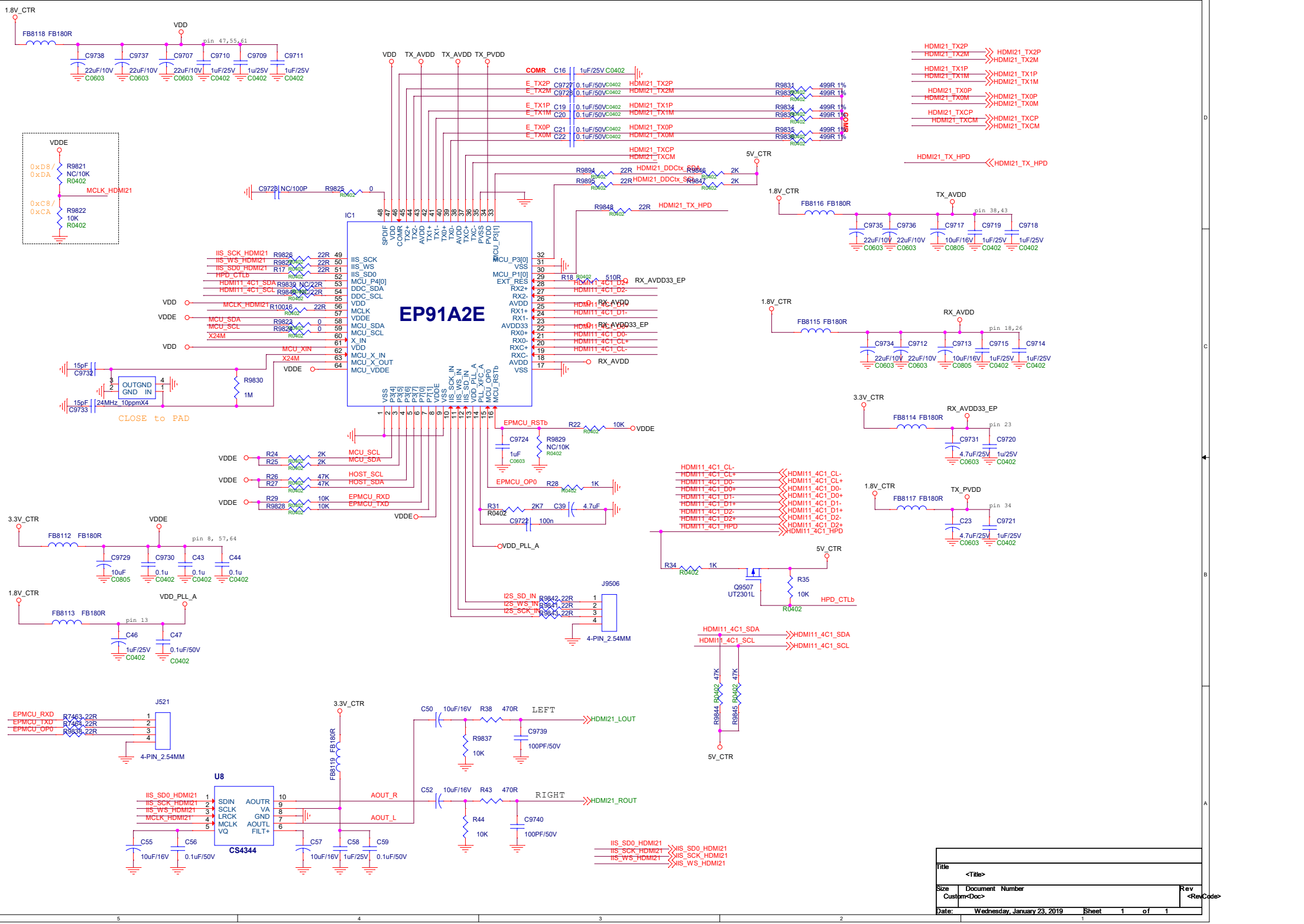
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1.8V_CTR
VDD
FB8118 FB180R
C9738 22uF/10V C0603
C9737 22uF/10V C0603
C9707 22uF/10V C0603
C9710 1uF/25V C0402
C9709 1u/25V C0402
C9711 1uF/25V C0402
pin 47,55,61
VDDE
0xD8/ 0xDA
R9821 NC/10K R0402
MCLK_HDMI21
0xC8/ 0xCA
R9822 10K R0402
TX_AVDD
TX_PVDD
COMR C16 1uF/25V C0402
E_TX2P C9727 0.1uF/50V C0402
E_TX2M C9728 0.1uF/50V C0402
E_TX1P C19 0.1uF/50V C0402
E_TX1M C20 0.1uF/50V C0402
E_TX0P C21 0.1uF/50V C0402
E_TX0M C22 0.1uF/50V C0402
HDMI21_TX2P
HDMI21_TX2M
HDMI21_TX1P
HDMI21_TX1M
HDMI21_TX0P
HDMI21_TX0M
HDMI21_TXCP
HDMI21_TXCM
R9831 499R 1%
R9832 499R 1%
R9834 499R 1%
R9833 499R 1%
R9835 499R 1%
R9836 499R 1%
5V_CTR
R9894 22R HDMI21_DDCtx_SDA
R9895 22R HDMI21_DDCtx_SCL
R9846 2K
R9847 2K
HDMI21_TX_HPD
R9848 22R HDMI21_TX_HPD
C9725 NC/100P
R9825 0
FB8116 FB180R
C9735 22uF/10V C0603
C9736 22uF/10V C0603
C9717 10uF/16V C0805
C9719 1uF/25V C0402
C9718 1uF/25V C0402
pin 38,43
IIS_SCK_HDMI21
IIS_WS_HDMI21
IIS_SD0_HDMI21
HPD_CTLb
HDMI11_4C1_SDA
HDMI11_4C1_SCL
R9826 22R
R9827 22R
R17 22R
R9839 NC/22R
R9840 NC/22R
IIS_SCK
IIS_WS
IIS_SD0
MCU_P4[0]
DDC_SDA
DDC_SCL
VDD
MCLK
VDDE
MCU_SDA
MCU_SCL
X_IN
VDD
MCU_X_IN
MCU_X_OUT
MCU_VDDE
MCU_P3[1]
MCU_P3[0]
VSS
MCU_P1[0]
EXT_RES
RX2+
RX2-
AVDD
RX1+
RX1-
AVDD33
RX0+
RX0-
RXC+
RXC-
AVDD
VSS
R18 510R
RX_AVDD33_EP
RX_AVDD
HDMI11_4C1_D2+
HDMI11_4C1_D2-
HDMI11_4C1_D1+
HDMI11_4C1_D1-
HDMI11_4C1_D0+
HDMI11_4C1_D0-
HDMI11_4C1_CL+
HDMI11_4C1_CL-
R10016 22R
R9823 0
R9824 0
MCU_XIN
X24M
15pF C9732
15pF C9733
OUTGND GND IN
24MHz_10ppmX4
CLOSE to PAD
R9830 1M
1.8V_CTR
FB8115 FB180R
C9734 22uF/10V C0603
C9712 22uF/10V C0603
C9713 10uF/16V C0805
C9715 1uF/25V C0402
C9714 1uF/25V C0402
pin 18,26
3.3V_CTR
FB8114 FB180R
C9731 4.7uF/25V C0603
C9720 1u/25V C0402
pin 23
EPMCU_RSTb
R22 10K
C9724 1uF C0603
R9829 NC/10K R0402
EPMCU_OP0
R28 1K
R31 2K7
C39 4.7uF
C9722 100n
R24 2K
R25 2K
MCU_SCL
MCU_SDA
R26 47K
R27 47K
HOST_SCL
HOST_SDA
R29 10K
R9828 10K
EPMCU_RXD
EPMCU_TXD
VDD_PLL_A
3.3V_CTR
FB8112 FB180R
C9729 10uF C0805
C9730 0.1u C0402
C43 0.1u C0402
C44 0.1u C0402
pin 8, 57,64
1.8V_CTR
FB8113 FB180R
C46 1uF/25V C0402
C47 0.1uF/50V C0402
pin 13
J9506
I2S_SD_IN
I2S_WS_IN
I2S_SCK_IN
R9842 22R
R9841 22R
R9843 22R
4-PIN_2.54MM
HDMI11_4C1_CL-
HDMI11_4C1_CL+
HDMI11_4C1_D0-
HDMI11_4C1_D0+
HDMI11_4C1_D1-
HDMI11_4C1_D1+
HDMI11_4C1_D2-
HDMI11_4C1_D2+
HDMI11_4C1_HPD
5V_CTR
R34 1K
Q9507 UT2301L
R35 10K
HPD_CTLb
R0402
1.8V_CTR
FB8117 FB180R
C23 4.7uF/25V C0603
C9721 1u/25V C0402
pin 34
HDMI11_4C1_SDA
HDMI11_4C1_SCL
R9844 47K
R9845 47K
5V_CTR
J521
EPMCU_RXD
EPMCU_TXD
EPMCU_OP0
R7463 22R
R7464 22R
R9838 22R
4-PIN_2.54MM
3.3V_CTR
FB8119 FB180R
U8
CS4344
SDIN
SCLK
LRCK
MCLK
VQ
AOUTR
VA
GND
AOUTL
FILT+
IIS_SD0_HDMI21
IIS_SCK_HDMI21
IIS_WS_HDMI21
MCLK_HDMI21
AOUT_R
AOUT_L
C50 10uF/16V
R38 470R
LEFT
HDMI21_LOUT
R9837 10K
C9739 100PF/50V
C52 10uF/16V
R43 470R
RIGHT
HDMI21_ROUT
R44 10K
C9740 100PF/50V
C55 10uF/16V
C56 0.1uF/50V
C57 10uF/16V
C58 1uF/25V
C59 0.1uF/50V
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Date: Wednesday, January 23, 2019
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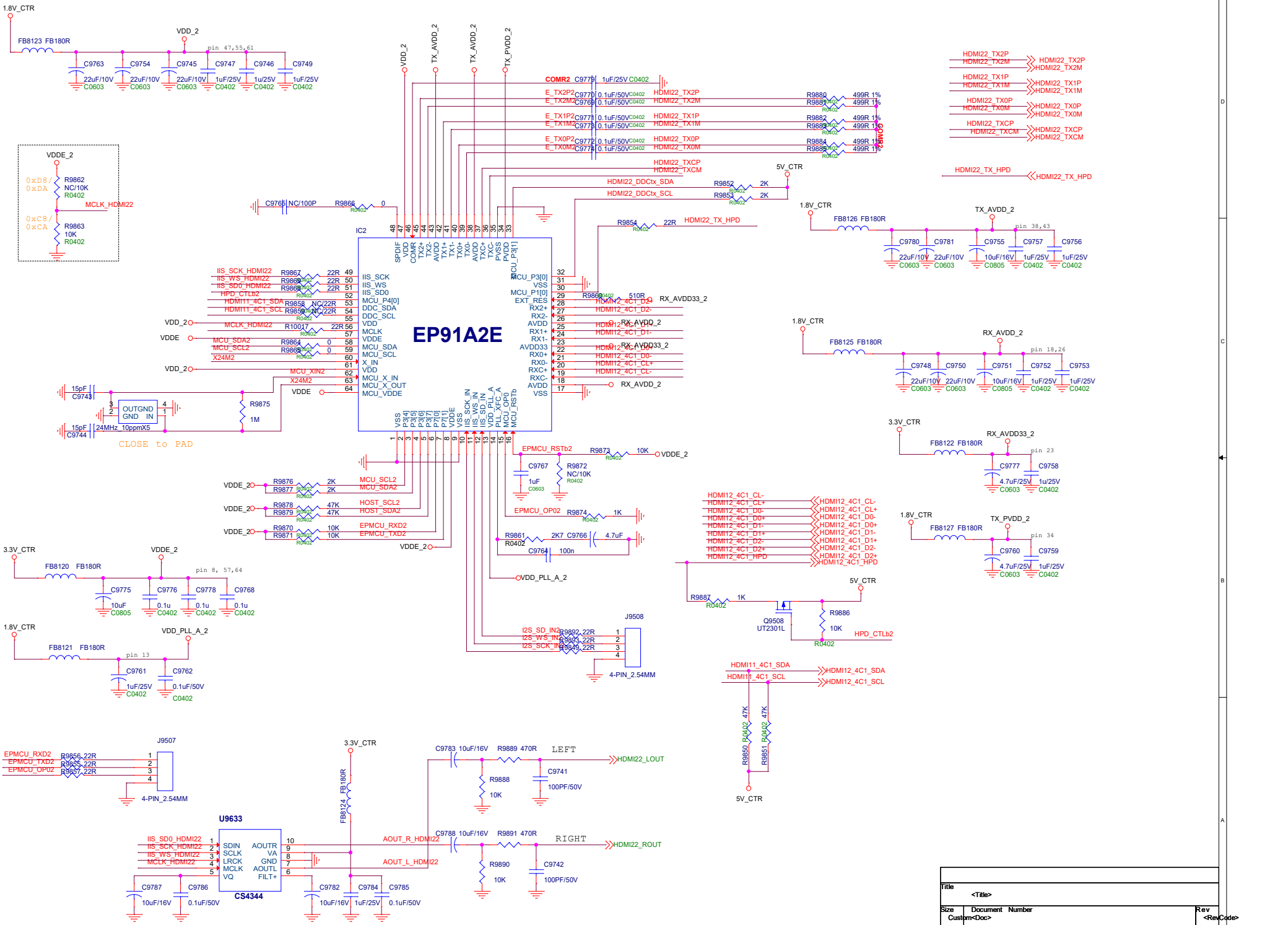
EP91A2E
IC2
1.8V_CTR
VDD_2
FB8123 FB180R
C9763 22uF/10V C0603
C9754 22uF/10V C0603
C9745 22uF/10V C0603
C9747 1uF/25V C0402
C9746 1u/25V C0402
C9749 1uF/25V C0402
pin 47,55,61
TX_AVDD_2
TX_PVDD_2
COMR2 C9779 1uF/25V C0402
E_TX2P2 C9770 0.1uF/50V C0402
E_TX2M2 C9769 0.1uF/50V C0402
E_TX1P2 C9771 0.1uF/50V C0402
E_TX1M2 C9773 0.1uF/50V C0402
E_TX0P2 C9772 0.1uF/50V C0402
E_TX0M2 C9774 0.1uF/50V C0402
HDMI22_TX2P
HDMI22_TX2M
HDMI22_TX1P
HDMI22_TX1M
HDMI22_TX0P
HDMI22_TX0M
HDMI22_TXCP
HDMI22_TXCM
R9880 499R 1%
R9881 499R 1%
R9882 499R 1%
R9883 499R 1%
R9884 499R 1%
R9885 499R 1%
COMR2
HDMI22_DDCtx_SDA
HDMI22_DDCtx_SCL
R9852 2K
R9853 2K
5V_CTR
HDMI22_TX_HPD
R9854 22R
C9765 NC/100P
R9866 0
VDDE_2
0xD8/0xDA
0xC8/0xCA
R9862 NC/10K R0402
R9863 10K R0402
MCLK_HDMI22
IIS_SCK_HDMI22
IIS_WS_HDMI22
IIS_SD0_HDMI22
HPD_CTLb2
HDMI11_4C1_SDA
HDMI11_4C1_SCL
MCLK_HDMI22
MCU_SDA2
MCU_SCL2
X24M2
MCU_XIN2
R9867 22R
R9868 22R
R9869 22R
R9858 NC/22R
R9859 NC/22R
R10017 22R
R9864 0
R9865 0
15pF C9743
15pF C9744
24MHz_10ppmX5
OUTGND GND IN
CLOSE to PAD
R9875 1M
RX_AVDD33_2
RX_AVDD_2
HDMI12_4C1_D2+
HDMI12_4C1_D2-
HDMI12_4C1_D1+
HDMI12_4C1_D1-
HDMI12_4C1_D0+
HDMI12_4C1_D0-
HDMI12_4C1_CL+
HDMI12_4C1_CL-
R9860 510R
EPMCU_RSTb2
R9873 10K
C9767 1uF
R9872 NC/10K
EPMCU_OP02
R9874 1K
R9861 2K7
C9766 4.7uF
C9764 100n
VDD_PLL_A_2
MCU_SCL2
MCU_SDA2
HOST_SCL2
HOST_SDA2
EPMCU_RXD2
EPMCU_TXD2
R9876 2K
R9877 2K
R9878 47K
R9879 47K
R9870 10K
R9871 10K
I2S_SD_IN2
I2S_WS_IN2
I2S_SCK_IN2
R9892 22R
R9893 22R
R9894 22R
J9508
4-PIN_2.54MM
3.3V_CTR
FB8120 FB180R
C9775 10uF C0805
C9776 0.1u C0402
C9778 0.1u C0402
C9768 0.1u C0402
pin 8, 57,64
FB8121 FB180R
C9761 1uF/25V C0402
C9762 0.1uF/50V C0402
pin 13
FB8126 FB180R
C9780 22uF/10V C0603
C9781 22uF/10V C0603
C9755 10uF/16V C0805
C9757 1uF/25V C0402
C9756 1uF/25V C0402
pin 38,43
FB8125 FB180R
C9748 22uF/10V C0603
C9750 22uF/10V C0603
C9751 10uF/16V C0805
C9752 1uF/25V C0402
C9753 1uF/25V C0402
pin 18,26
FB8122 FB180R
C9777 4.7uF/25V C0603
C9758 1u/25V C0402
pin 23
FB8127 FB180R
C9760 4.7uF/25V C0603
C9759 1uF/25V C0402
pin 34
HDMI12_4C1_CL-
HDMI12_4C1_CL+
HDMI12_4C1_D0-
HDMI12_4C1_D0+
HDMI12_4C1_D1-
HDMI12_4C1_D1+
HDMI12_4C1_D2-
HDMI12_4C1_D2+
HDMI12_4C1_HPD
R9887 1K
Q9508 UT2301L
R9886 10K
HPD_CTLb2
HDMI11_4C1_SDA
HDMI11_4C1_SCL
R9850 47K
R9851 47K
J9507
EPMCU_RXD2
EPMCU_TXD2
EPMCU_OP02
R9856 22R
R9855 22R
R9857 22R
4-PIN_2.54MM
U9633
CS4344
SDIN SCLK LRCK MCLK VQ
AOUTR VA GND AOUTL FILT+
IIS_SD0_HDMI22
IIS_SCK_HDMI22
IIS_WS_HDMI22
MCLK_HDMI22
AOUT_R_HDMI22
AOUT_L_HDMI22
FB8124 FB180R
C9787 10uF/16V
C9786 0.1uF/50V
C9782 10uF/16V
C9784 1uF/25V
C9785 0.1uF/50V
C9783 10uF/16V
R9889 470R
LEFT
R9888 10K
C9741 100PF/50V
HDMI22_LOUT
C9788 10uF/16V
R9891 470R
RIGHT
R9890 10K
C9742 100PF/50V
HDMI22_ROUT
Title <Title>
Size Custom<Doc>
Document Number
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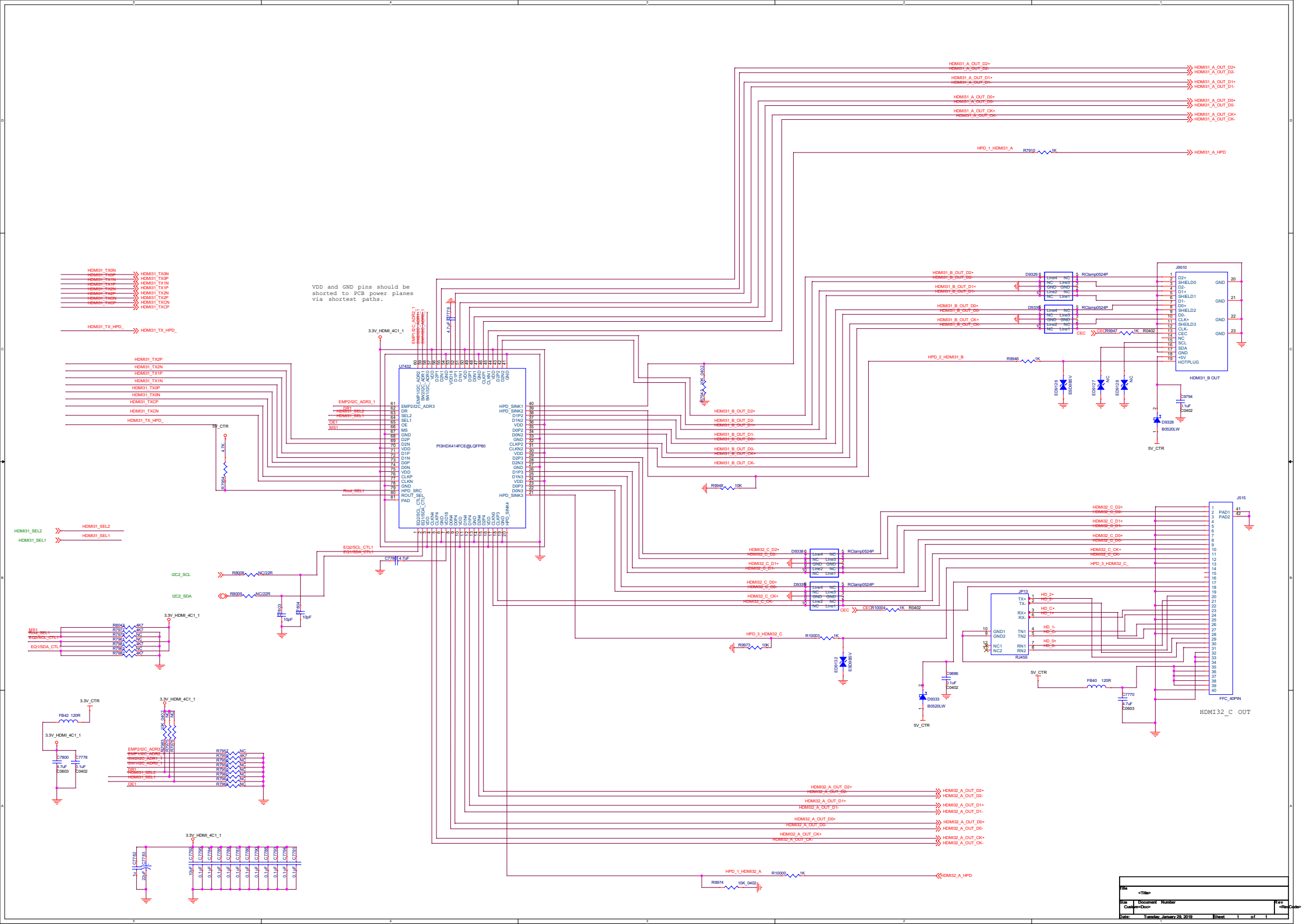
VDD and GND pins should be shorted to PCB power planes via shortest paths.
PI3HDX414FCE@LQFP80
HDMI32_C OUT
FFC_40PIN
RJ45S
HOTPLUG
HDMI31_B OUT
Title
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Size
Document Number
Rev
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Date: Tuesday, January 29, 2019
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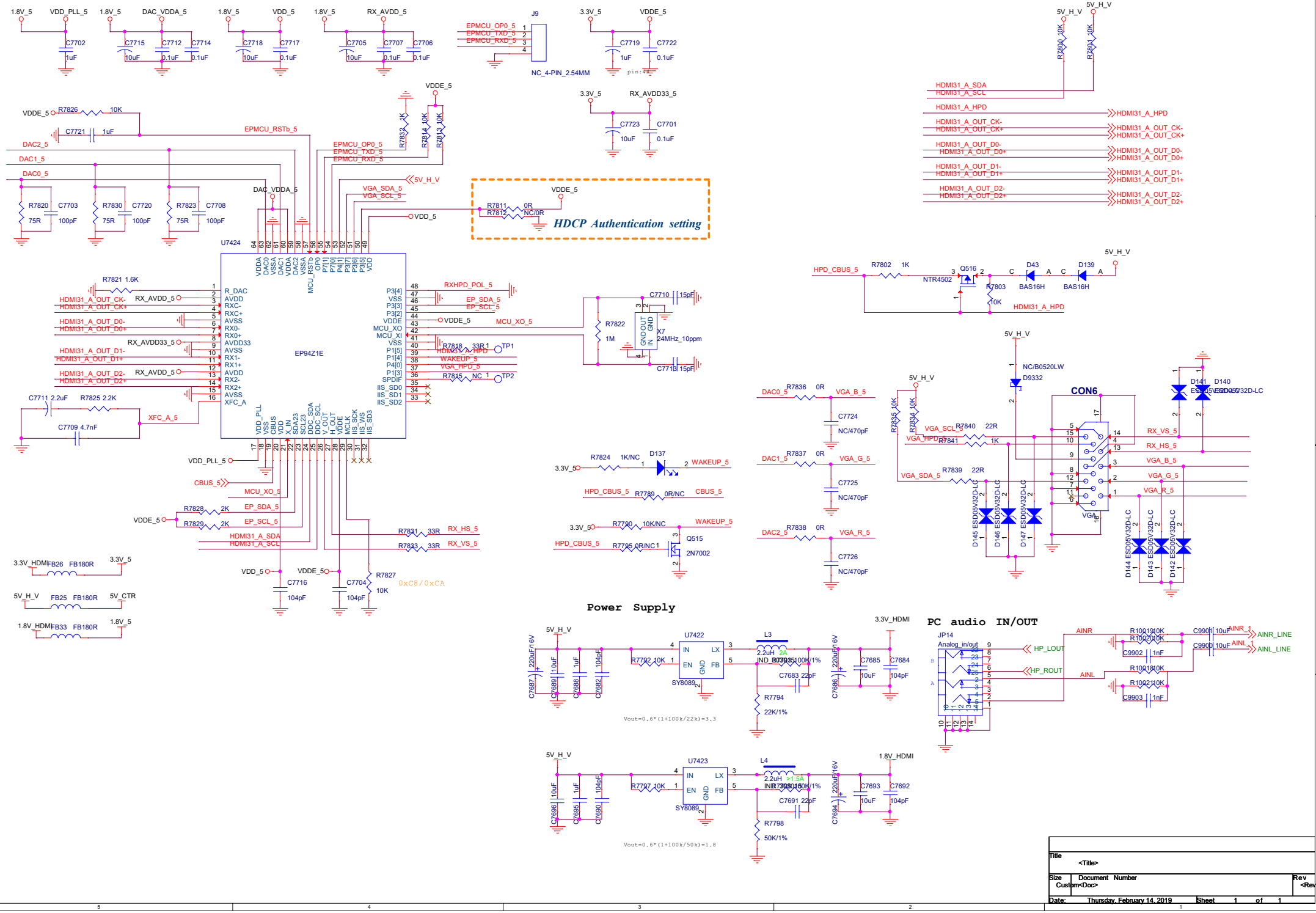
1.8V_5
VDD_PLL_5
DAC_VDDA_5
VDD_5
RX_AVDD_5
3.3V_5
VDDE_5
5V_H_V
J9
NC_4-PIN_2.54MM
EPMCU_OP0_5
EPMCU_TXD_5
EPMCU_RXD_5
EPMCU_RSTb_5
VGA_SDA_5
VGA_SCL_5
HDCP Authentication setting
U7424
EP94Z1E
R_DAC
AVDD
RXC-
RXC+
AVSS
RX0-
RX0+
AVDD33
RX1-
RX1+
AVDD
RX2-
RX2+
AVSS
XFC_A
MCU_XO_5
EP_SDA_5
EP_SCL_5
RXHPD_POL_5
WAKEUP_5
HDMI31_A_HPD
VGA_HPD_5
CBUS_5
VDD_PLL_5
HDMI31_A_SDA
HDMI31_A_SCL
RX_HS_5
RX_VS_5
HDMI31_A_OUT_CK-
HDMI31_A_OUT_CK+
HDMI31_A_OUT_D0-
HDMI31_A_OUT_D0+
HDMI31_A_OUT_D1-
HDMI31_A_OUT_D1+
HDMI31_A_OUT_D2-
HDMI31_A_OUT_D2+
CON6
Power Supply
PC audio IN/OUT
SY8089
Vout=0.6*(1+100k/22k)=3.3
Vout=0.6*(1+100k/50k)=1.8
0xC8 / 0xCA
Title
<Title>
Size
Document Number
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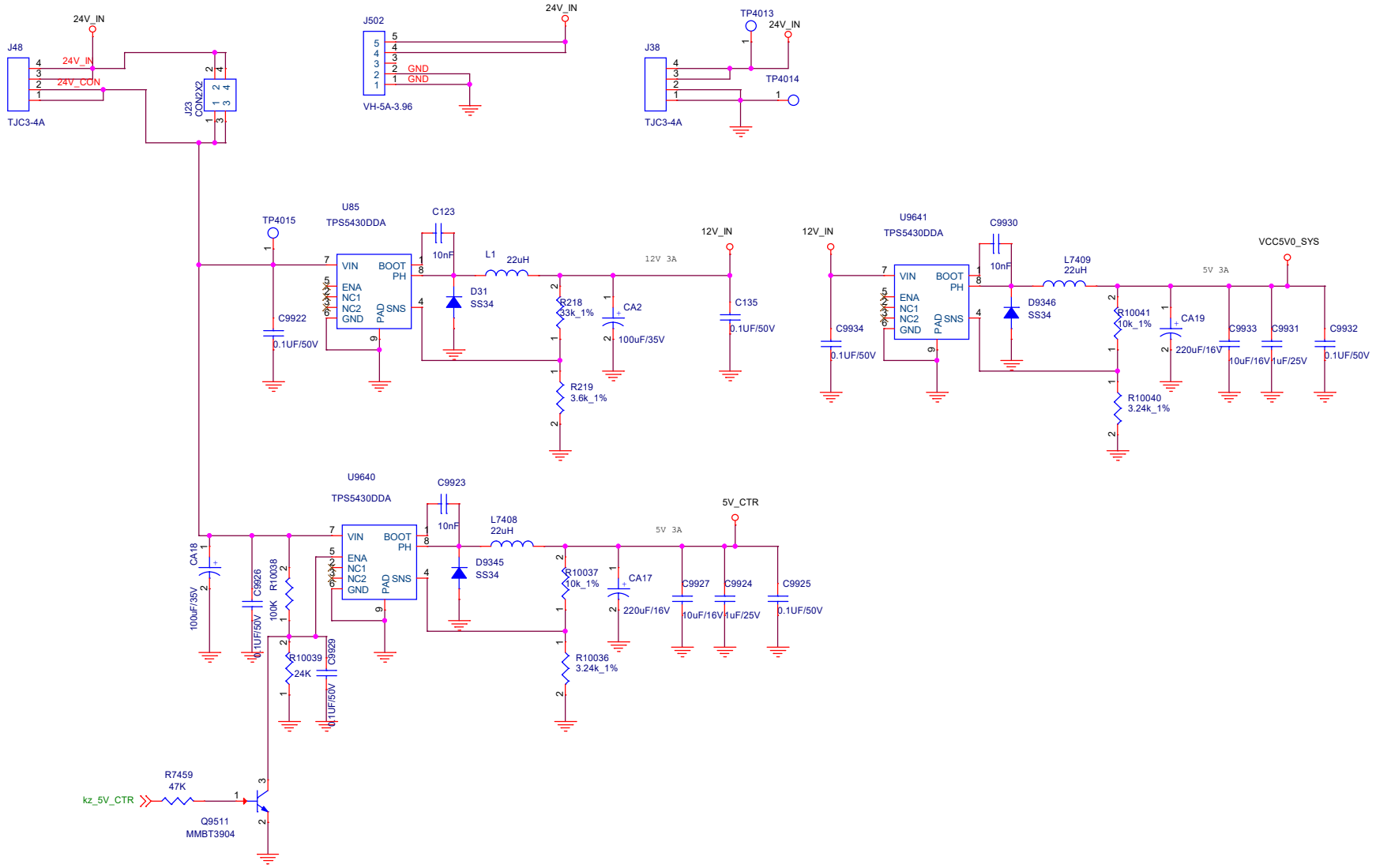

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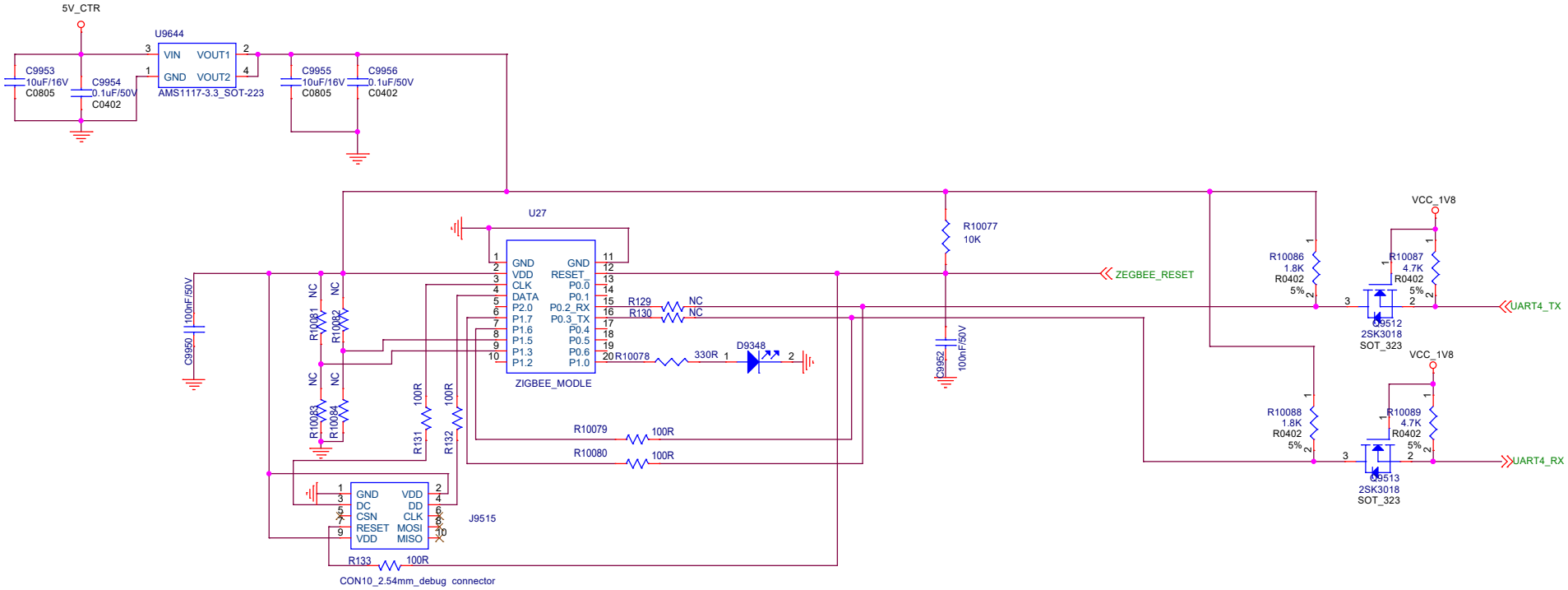
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Thursday, January 17, 2019	Sheet 1 of 1	



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Size A3	Document Number <Doc>	Rev <RevCode>
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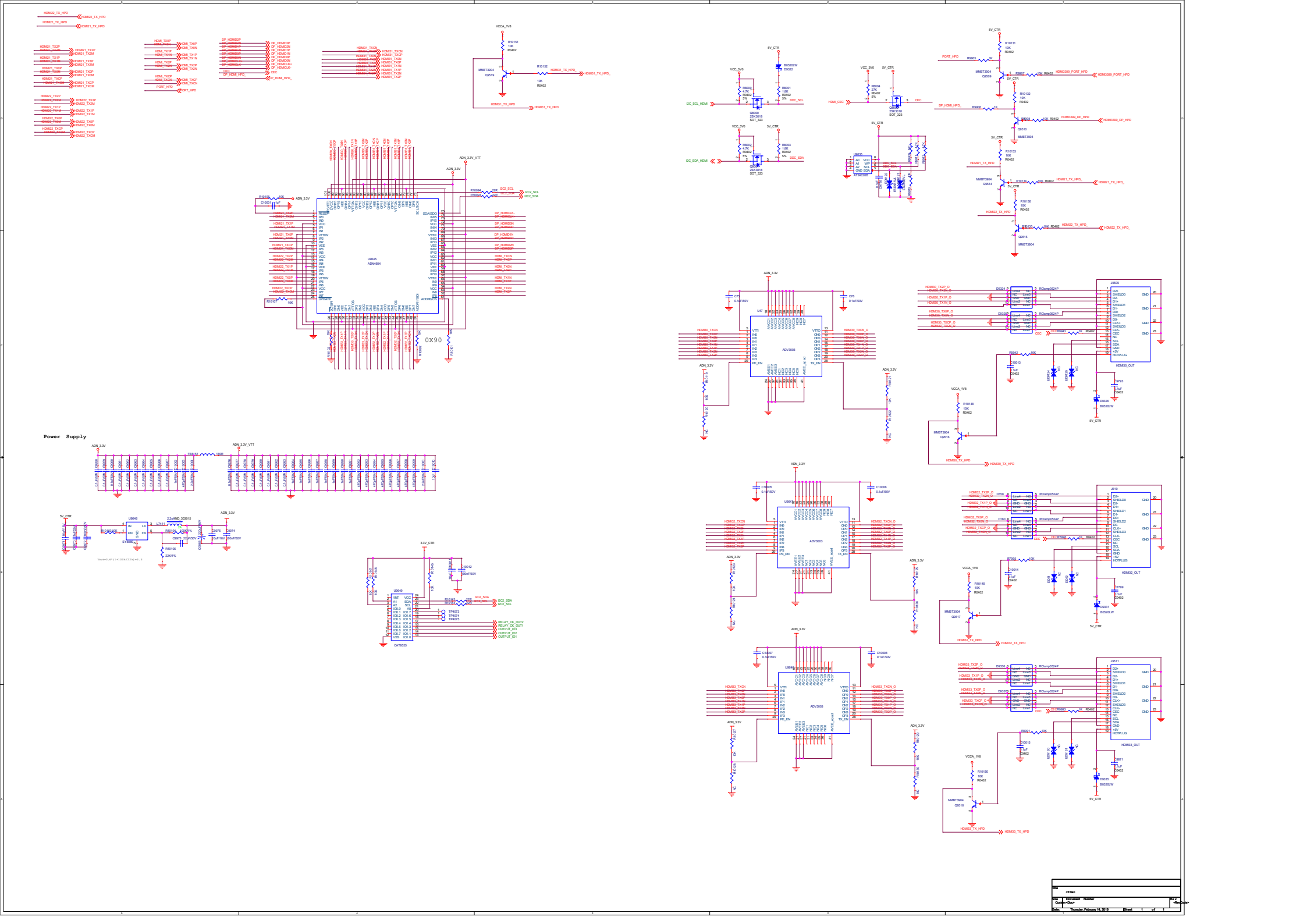
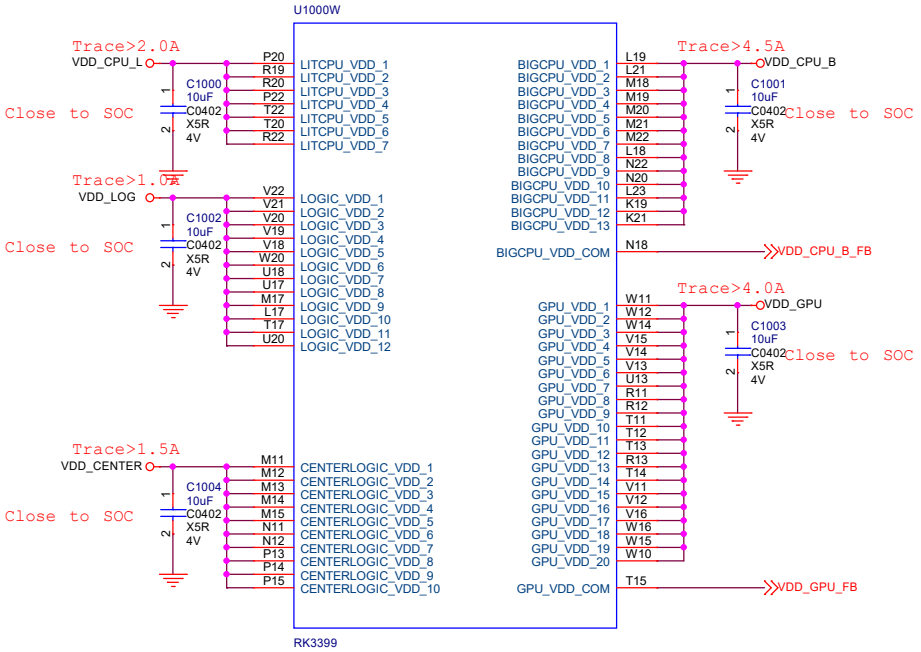
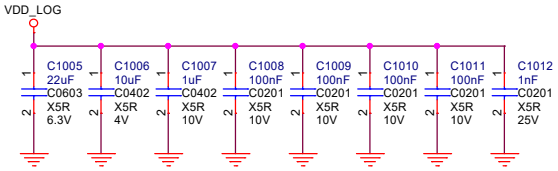
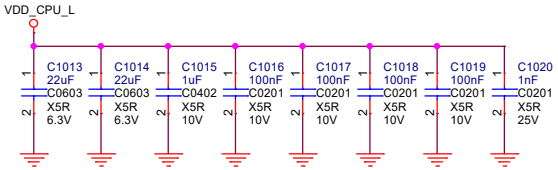
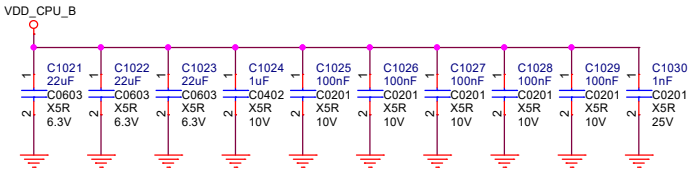

Power Supply
U6645
ADN4604
ADV3003
U6646
U6647
U6648
U6649
CAT9555
J9509
J9510
J9511
HDMI30_OUT
HDMI32_OUT
HDMI33_OUT
HDMI30_TX_HPD
HDMI32_TX_HPD
HDMI33_TX_HPD
ADN_3.3V
ADN_3.3V_VTT
VCCA_1V8
5V_CTR
3.3V_CTR

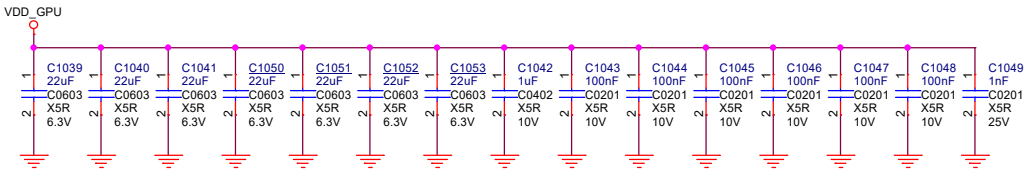


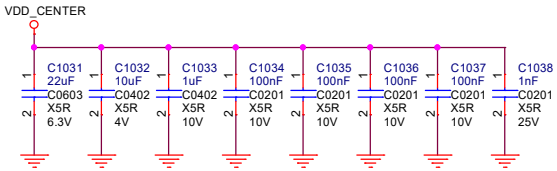
Note:All the Power filter capacitors should be placed close to the power pins of RK3400

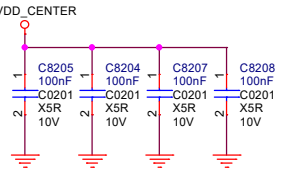


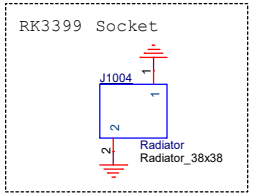


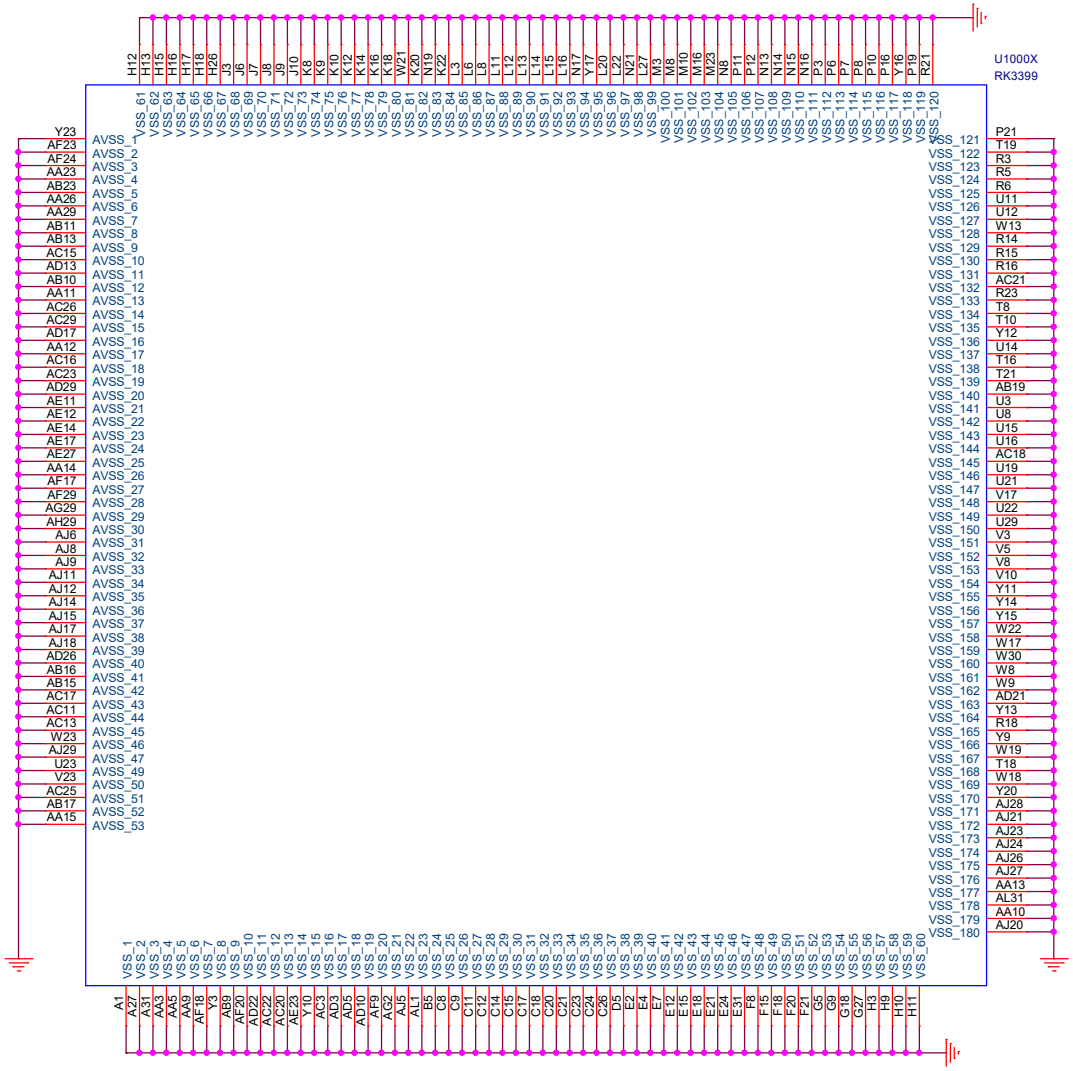












Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_box_LPDDR4_200P		
File:	<Page name>		
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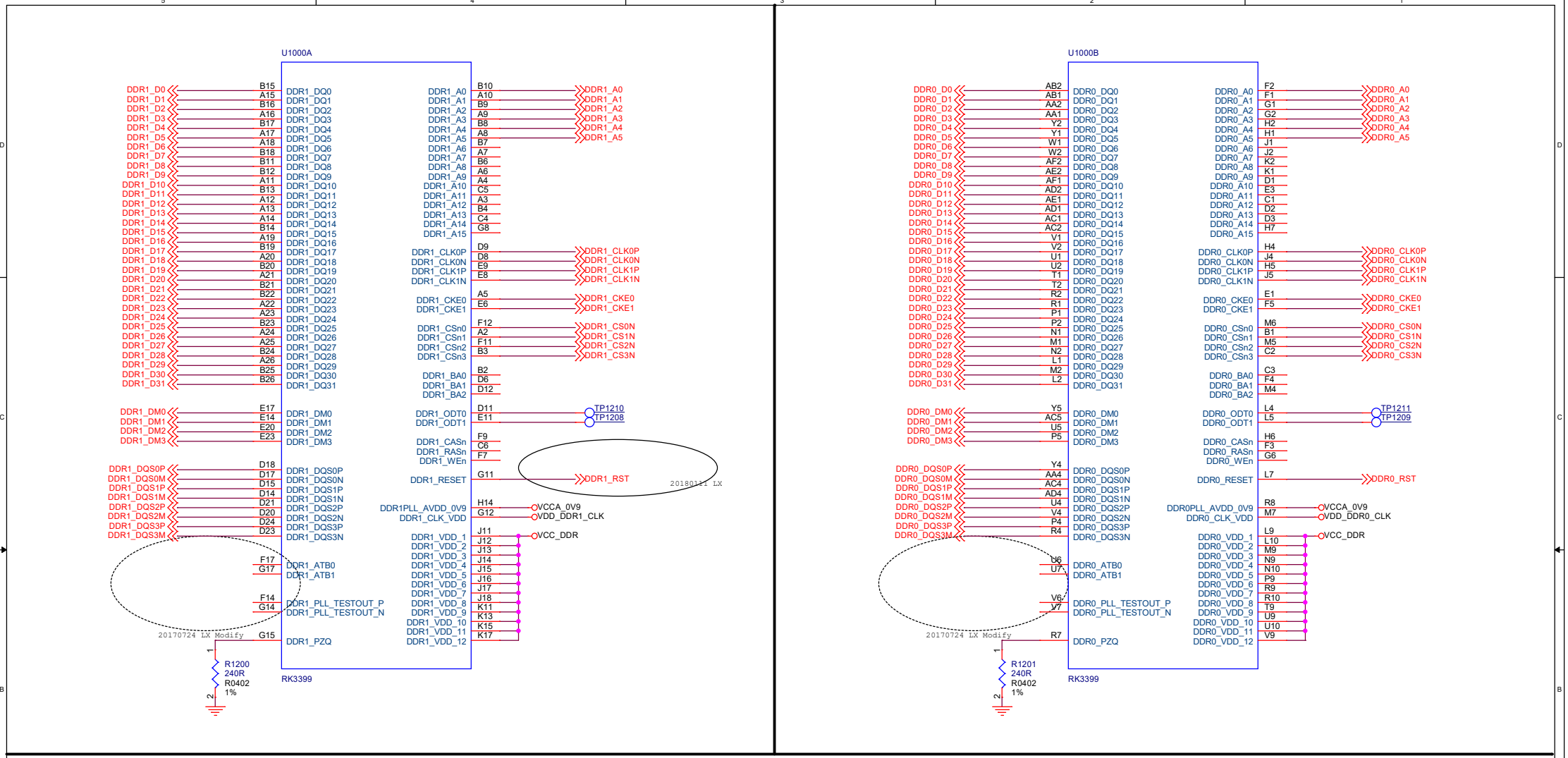
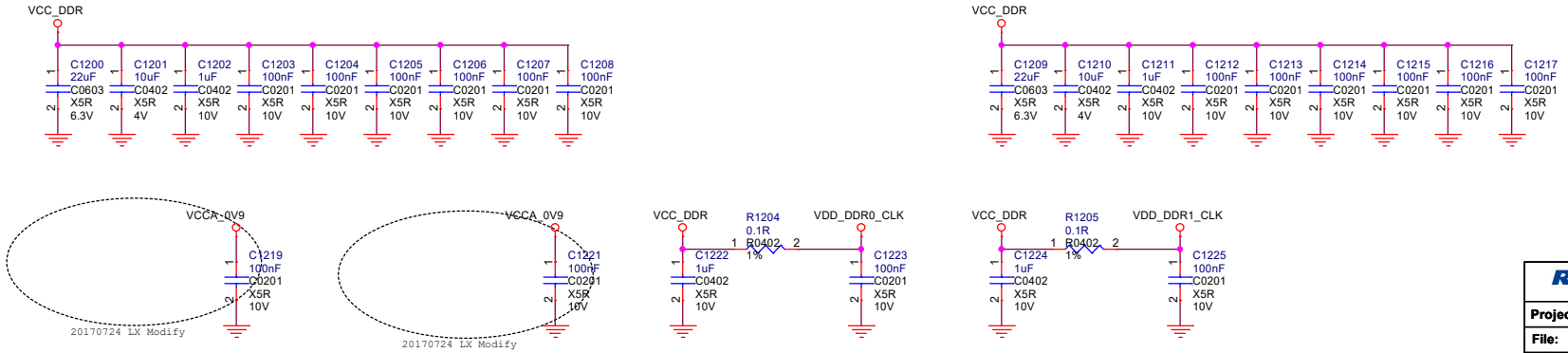
Designed by:	Linus	Sheet:	6 of 22



DDR FILTER



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_box_LPDDR4_200P		
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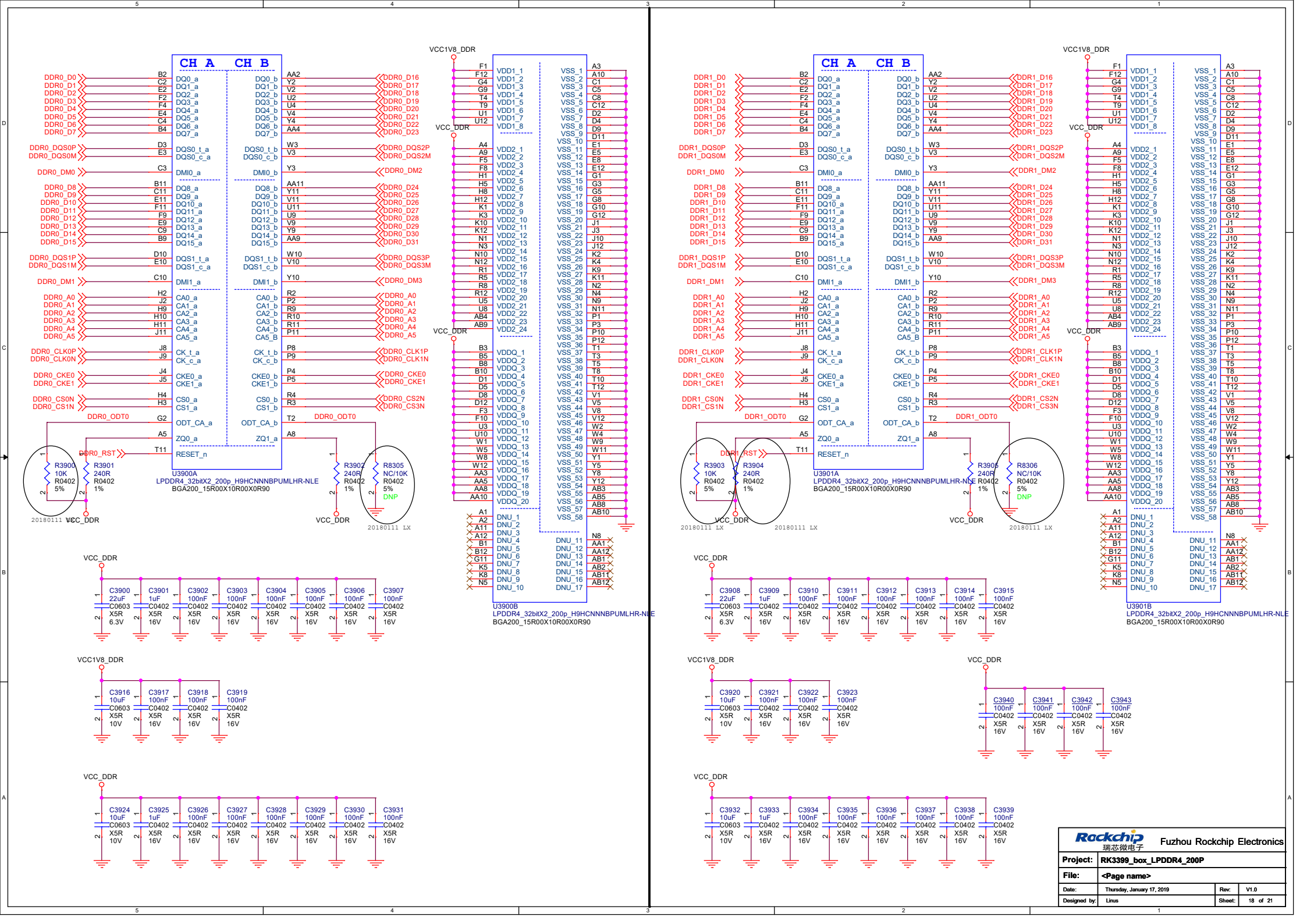
Designed by:	Linus	Sheet:	8 of 22


CH A
CH B
U3900A
LPDDR4_32bitX2_200p_H9HCNNNBPUMLHR-NLE
BGA200_15R00X10R00X0R90
U3900B
LPDDR4_32bitX2_200p_H9HCNNNBPUMLHR-NLE
BGA200_15R00X10R00X0R90
U3901A
LPDDR4_32bitX2_200p_H9HCNNNBPUMLHR-NLE
BGA200_15R00X10R00X0R90
U3901B
LPDDR4_32bitX2_200p_H9HCNNNBPUMLHR-NLE
BGA200_15R00X10R00X0R90
VCC1V8_DDR
VCC_DDR
DDR0_ODT0
DDR0_RST
DDR1_ODT0
DDR1_RST
R3900 10K R0402 5%
R3901 240R R0402 1%
R3902 240R R0402 1%
R8305 NC/10K R0402 5% DNP
R3903 10K R0402 5%
R3904 240R R0402 1%
R3905 240R R0402 1%
R8306 NC/10K R0402 5% DNP
20180111 LX
C3900 22uF C0603 X5R 6.3V
C3901 1uF C0402 X5R 16V
C3902 100nF C0402 X5R 16V
C3903 100nF C0402 X5R 16V
C3904 100nF C0402 X5R 16V
C3905 100nF C0402 X5R 16V
C3906 100nF C0402 X5R 16V
C3907 100nF C0402 X5R 16V
C3908 22uF C0603 X5R 6.3V
C3909 1uF C0402 X5R 16V
C3910 100nF C0402 X5R 16V
C3911 100nF C0402 X5R 16V
C3912 100nF C0402 X5R 16V
C3913 100nF C0402 X5R 16V
C3914 100nF C0402 X5R 16V
C3915 100nF C0402 X5R 16V
C3916 10uF C0603 X5R 10V
C3917 100nF C0402 X5R 16V
C3918 100nF C0402 X5R 16V
C3919 100nF C0402 X5R 16V
C3920 10uF C0603 X5R 10V
C3921 100nF C0402 X5R 16V
C3922 100nF C0402 X5R 16V
C3923 100nF C0402 X5R 16V
C3924 10uF C0603 X5R 10V
C3925 1uF C0402 X5R 16V
C3926 100nF C0402 X5R 16V
C3927 100nF C0402 X5R 16V
C3928 100nF C0402 X5R 16V
C3929 100nF C0402 X5R 16V
C3930 100nF C0402 X5R 16V
C3931 100nF C0402 X5R 16V
C3932 10uF C0603 X5R 10V
C3933 1uF C0402 X5R 16V
C3934 100nF C0402 X5R 16V
C3935 100nF C0402 X5R 16V
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C3937 100nF C0402 X5R 16V
C3938 100nF C0402 X5R 16V
C3939 100nF C0402 X5R 16V
C3940 100nF C0402 X5R 16V
C3941 100nF C0402 X5R 16V
C3942 100nF C0402 X5R 16V
C3943 100nF C0402 X5R 16V
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Project: RK3399_box_LPDDR4_200P
File: <Page name>
Date: Thursday, January 17, 2019
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Designed by: Linus
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