CS 2110 — Quiz 2, Group A **Answer Key**
January 2018 This quiz is worth a total of **100 points + 5 bonus points**.

You are allowed to use one sheet of scrap paper. Feel free to request scrap paper from your Teaching Assistants. **Please make sure that all of your answers are contained within the answer boxes or the fill-in lines.** Do not write your work in the answer boxes, **keep all of your work on your scrap paper**. You will **NOT** be given credit for showing work. Having anything except the answer inside the boxes or above the fill-in lines reduces autograder performance and might cause incorrect results. **Make sure to write your name, username, and answers legibly. You will not receive credit for illegible answers.**

Logic Gates

1. Fill in the following truth tables. [24]
   Hint: A XNOR B is equivalent to NOT (A XOR B).

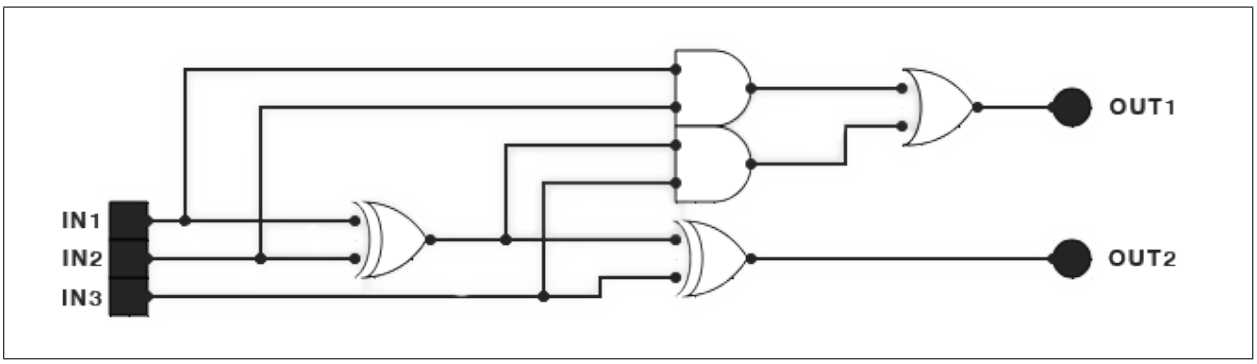
A	B	A AND B
0	0	0
0	1	0
1	0	0
1	1	1

A	B	A OR B
0	0	0
0	1	1
1	0	0
1	1	1

A	B	A XNOR B
0	0	1
0	1	0
1	0	0
1	1	1

Circuit Analysis

2. Fill in the blanks of the following truth table with respect to the circuit shown in the diagram. [32]



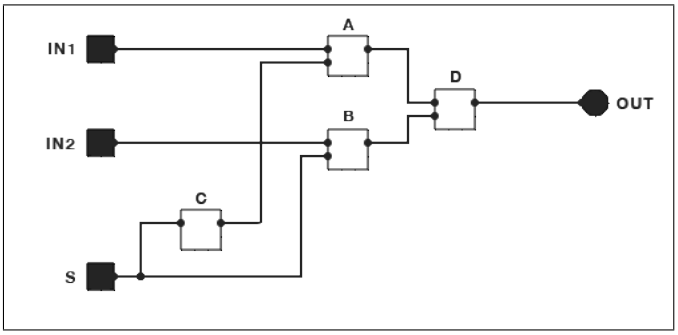
IN1	IN2	IN3	OUT1	OUT2
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Note that this is a 1-bit full adder.

Plexers

3. Answer the following questions about decoders and multiplexers.
   (a) What is the **minimum** number of select bits that a multiplexer can have if it needs to be able to select from **13** inputs? **4** [5]
   (b) What is the **maximum number of outputs** a decoder with a single 5-bit input can have? **32** [5]

4. The diagram below represents a 2-input multiplexer, with *IN1* and *IN2* as its inputs, *S* as the select bit, and *OUT* as the output.



Boxes A, B, C, D each contain a single logic gate. **Answer the following questions by choosing the correct gate for each box.**

(a) Box A: ◯ NOT ☑ AND ◯ NAND ◯ OR ◯ NOR ◯ XOR ◯ XNOR [6]

(b) Box B: ◯ NOT ☑ AND ◯ NAND ◯ OR ◯ NOR ◯ XOR ◯ XNOR [6]

(c) Box C: ☑ NOT ◯ AND ◯ NAND ◯ OR ◯ NOR ◯ XOR ◯ XNOR [6]

(d) Box D: ◯ NOT ◯ AND ◯ NAND ☑ OR ◯ NOR ◯ XOR ◯ XNOR [6]

Arithmetic Circuits

5. The diagram below represents a **4-bit full adder** with its A, B, Carry In, Carry Out and Sum pins marked.

The following diagrams contain two 4-bit inputs (marked *IN1* and *IN2* and an output marked *OUT*.

(a) Using copies of the adder as shown above, wires, constants, and logic gates, complete the diagram below so that it represents a **4-bit subtractor** such that $OUT = IN1 - IN2$. You do not need to account for the Carry Out of the adder. Make sure that all adders have their Carry In bits connected to some input (which can be a constant). Do not attempt to make adders using logic gates - just draw adders as shown above. [10]

(b) You will be awarded **5 points of extra credit** if your submission includes **at most one adder and two logic gates**. It can still include as many wires and constants as you need. [5 EC]