universidade de aveiro

ARQUITETURAS DE ALTO DESEMPENHO
ASSIGNMENT 1 - HAMMING CODES

BIT-SERIAL ENCODER
COMBINATIONAL DECODER

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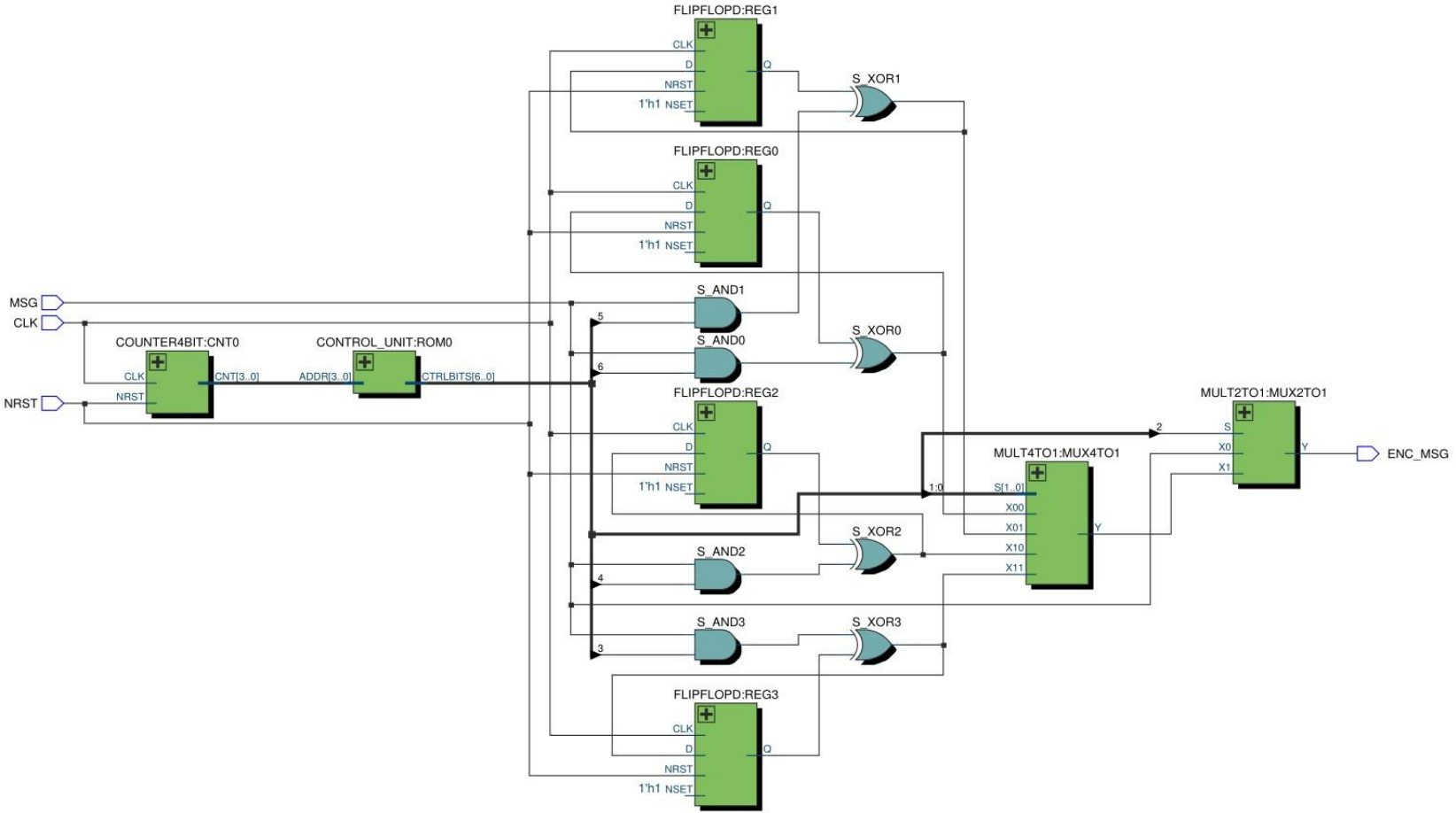
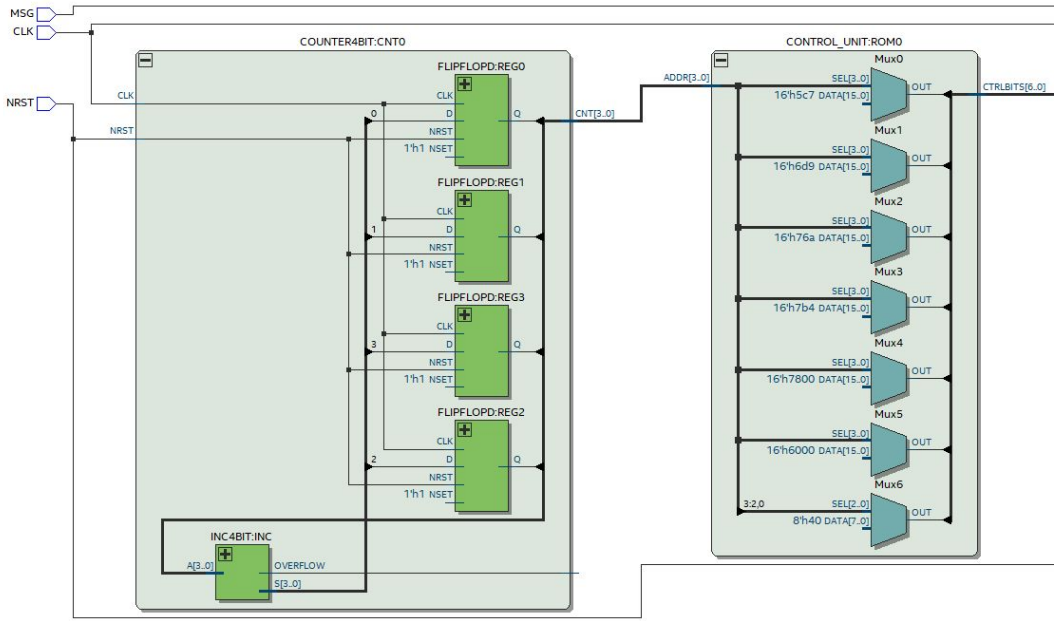
BIT-SERIAL ENCODER - DESIGN



BIT-SERIAL ENCODER - PRINCIPLES

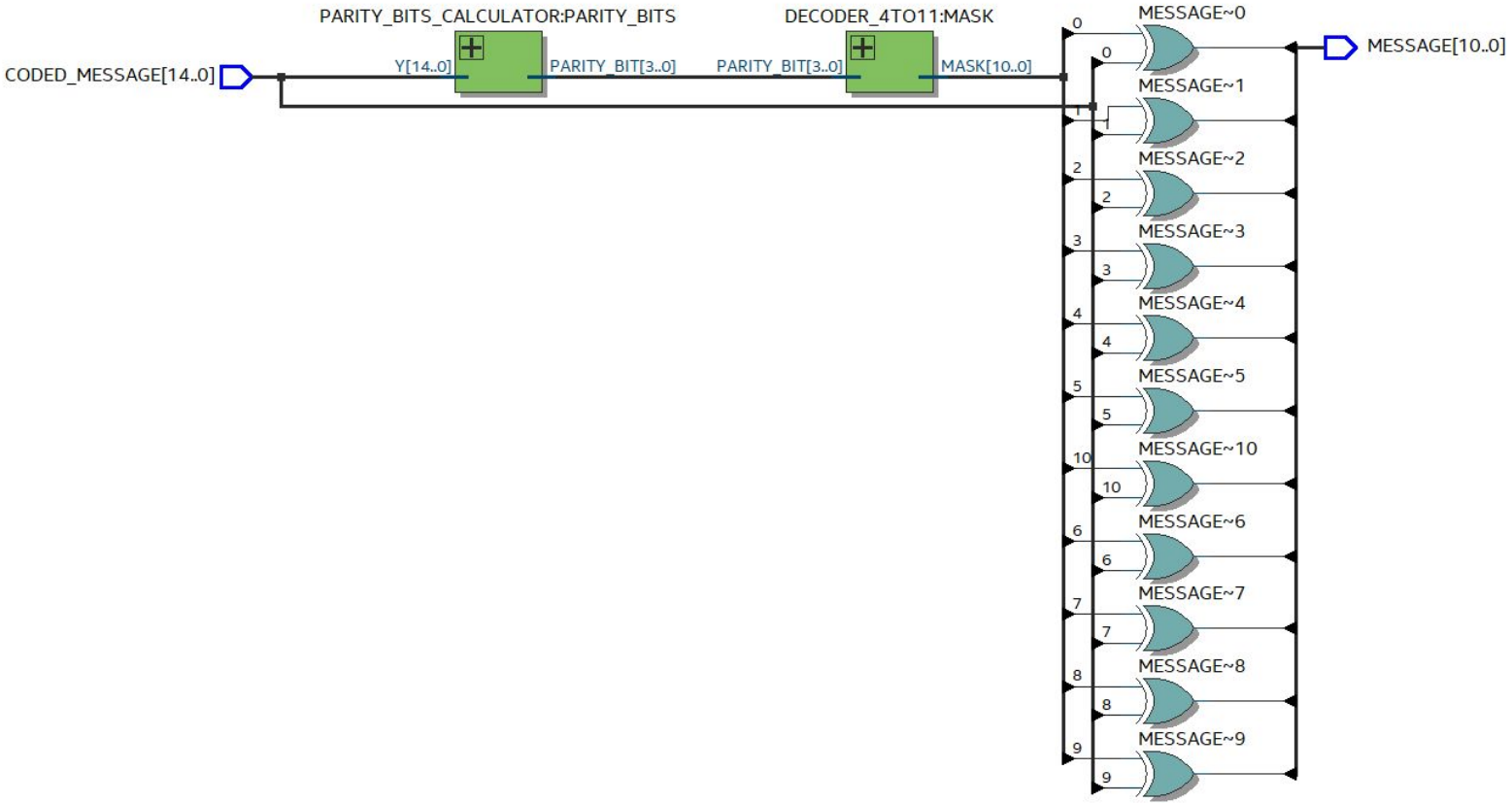


- **CONTROL UNIT**
  When the counter reaches 11, the ROM switches the Multiplexers to the parity bit outputs.

```
CONSTANT ROM_TABLE
    "1100000",
    "1010000",
    "1001000",
    "0110000",
    "0101000",
    "0011000",
    "1110000",
    "1101000",
    "1011000",
    "0111000",
    "1111000",
    "0000100",
    "0000101",
    "0000110",
    "0000111"
    );
```

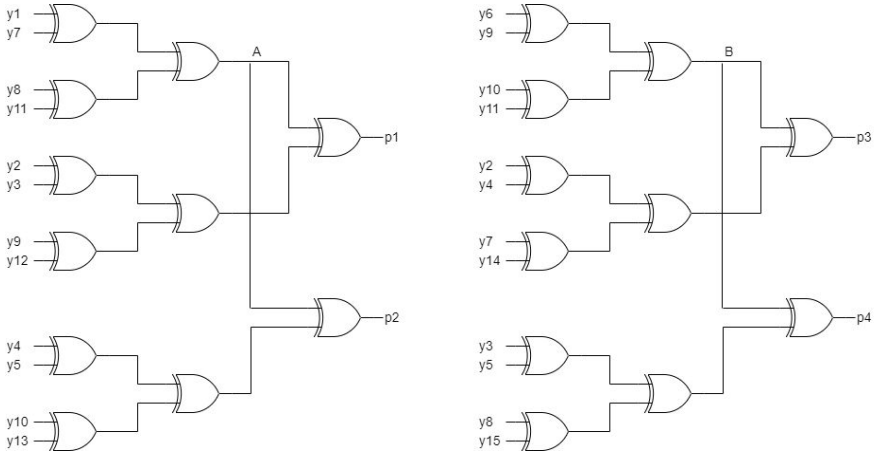
- **COUNTER 4 BIT**
  Used to increment the Control Unit.

COMBINATIONAL DECODER - DESIGN



COMBINATIONAL DECODER - PRINCIPLES

- **PARITY BITS CALCULATOR**
- **DECODER 4:11**
  From the parity-check matrix and the Parity Bits the mask (11bits) is calculated
- **IMPLEMENTATION OF THE ERROR CORRECTING PART**
  Mask ⊕ Original Message



A = m1 ⊕ m7 ⊕ m8 ⊕ m11
B = m6 ⊕ m9 ⊕ m10 ⊕ m11

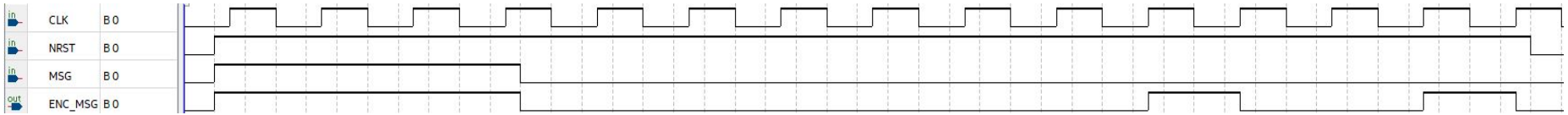
x12 = A ⊕ m2 ⊕ m3 ⊕ m9;
x13 = A ⊕ m4 ⊕ m5 ⊕ m10.
x14 = B ⊕ m2 ⊕ m4 ⊕ m7;
x15 = B ⊕ m3 ⊕ m5 ⊕ m8.

18 x-ors;
3 x-or propagation time delays in the worst case

RESULTS (VWF)

ENCODER

MESSAGE M (M1, M2, …, M11) = 11110000000
ENCODED MESSAGE X (X1, X2, …, X15) = 111100000001001



DECODER

SEVERAL EXAMPLES