



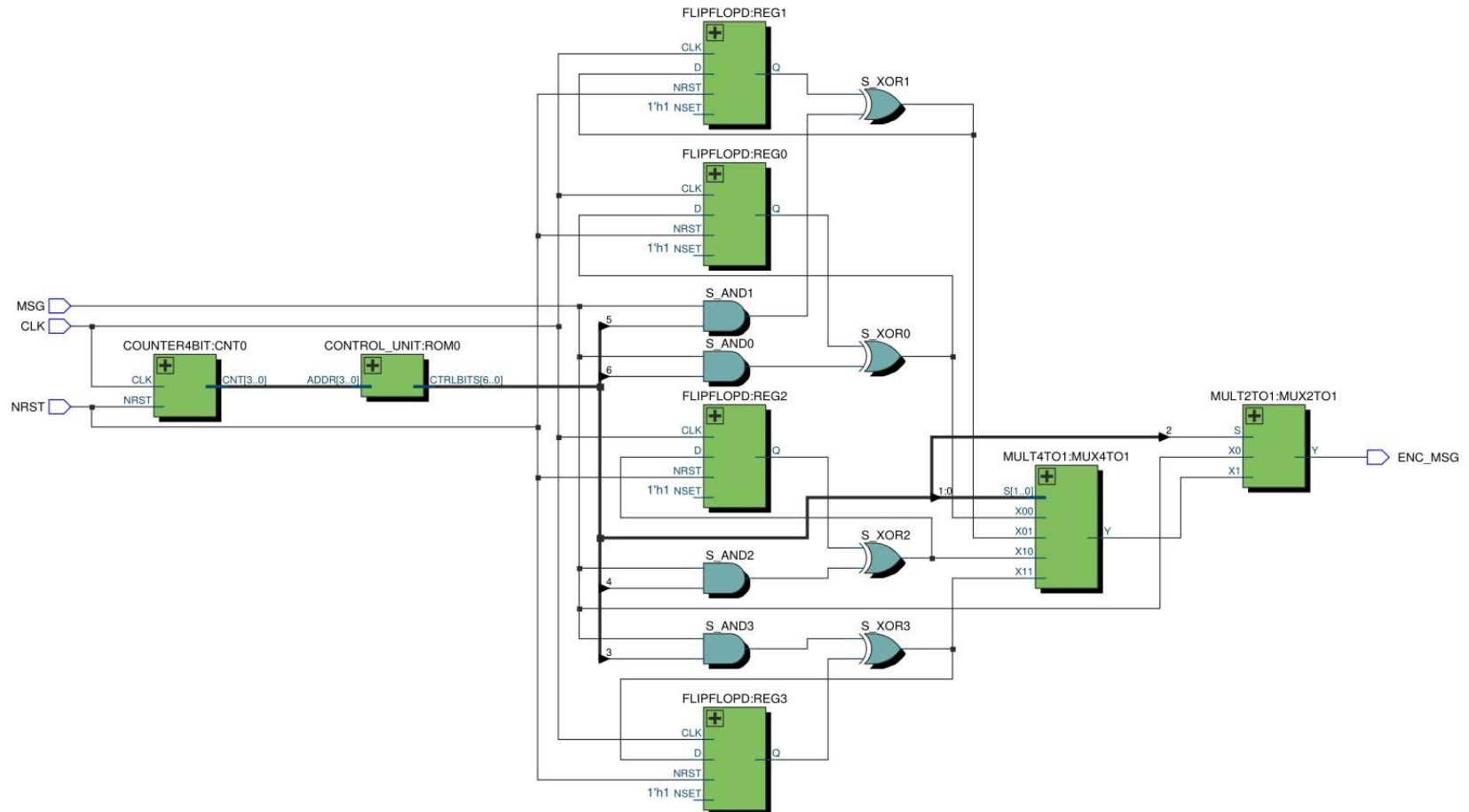
# ARQUITETURAS DE ALTO DESEMPENHO

## ASSIGNMENT 1 - HAMMING CODES

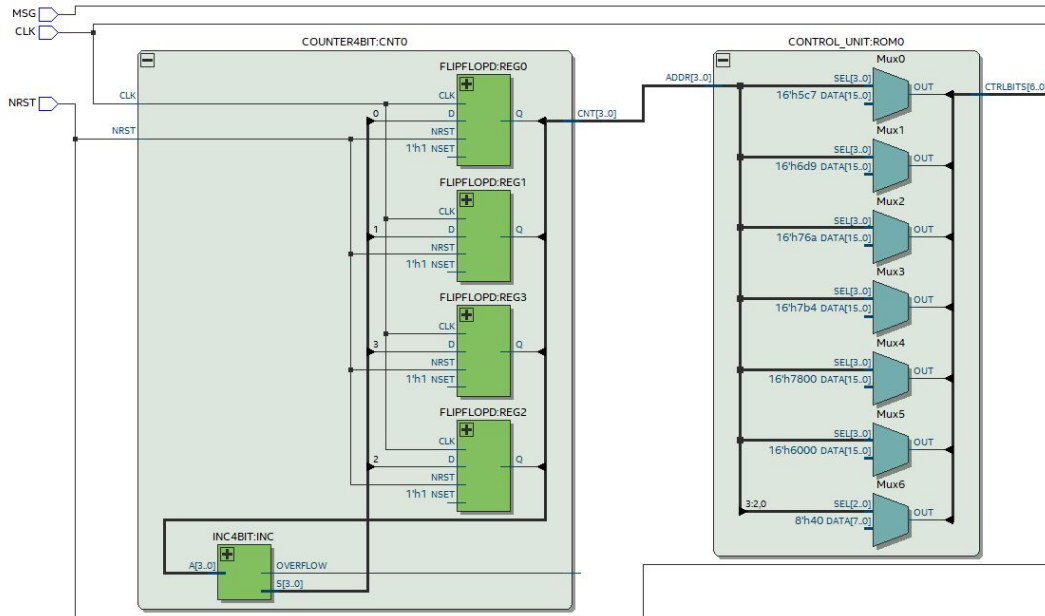
BIT-SERIAL ENCODER  
COMBINATIONAL DECODER

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# BIT-SERIAL ENCODER - DESIGN



# BIT-SERIAL ENCODER - PRINCIPLES



- CONTROL UNIT**

When the counter reaches 11, the ROM switches the Multiplexers to the parity bit outputs.

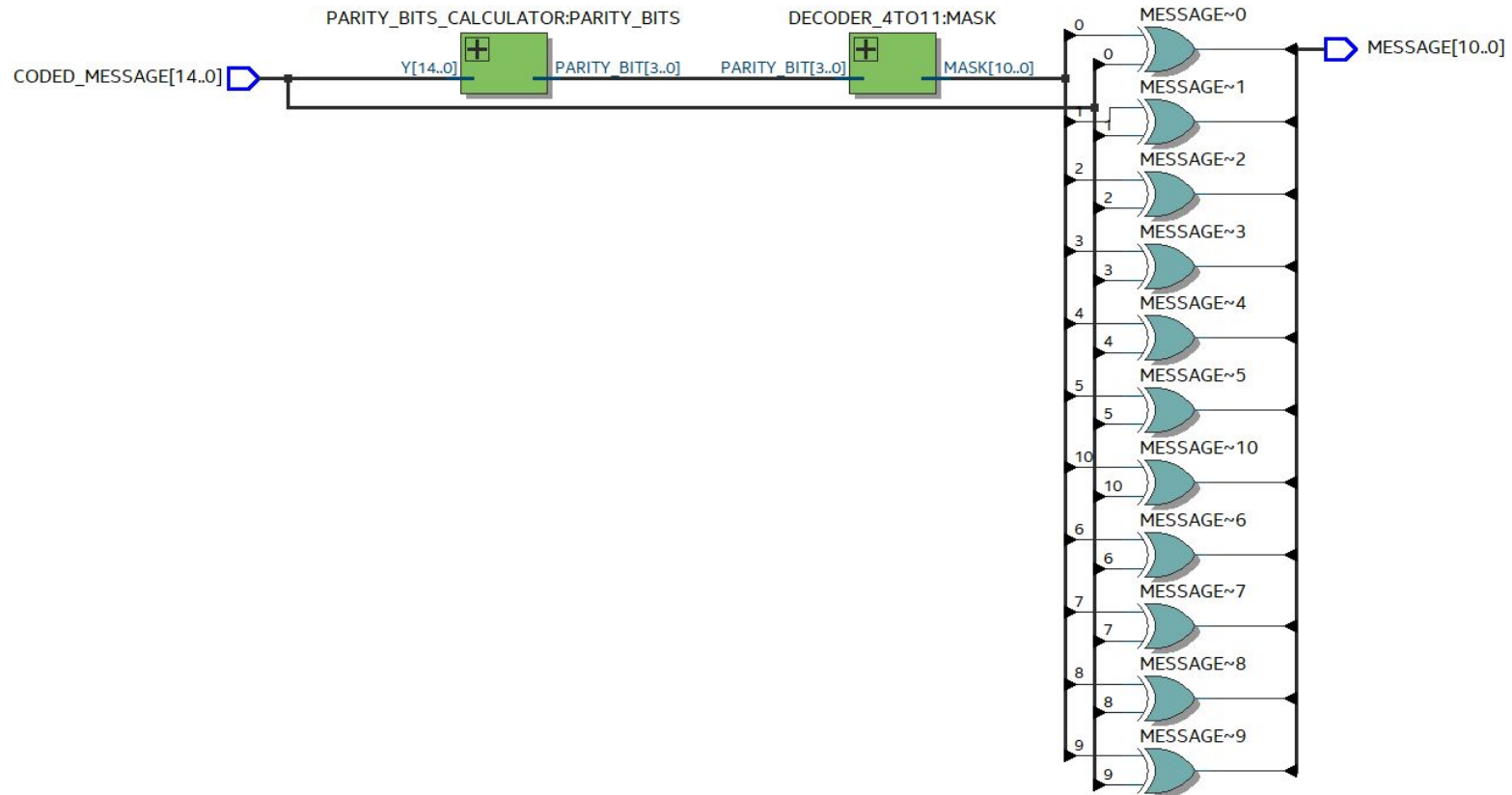
CONSTANT ROM\_TABLE

```
"1100000",
"1010000",
"1001000",
"0110000",
"0101000",
"0011000",
"1110000",
"1101000",
"1011000",
"0111000",
"1111000",
"0000100",
"0000101",
"0000110",
"0000111"
);
```

- COUNTER 4 BIT**

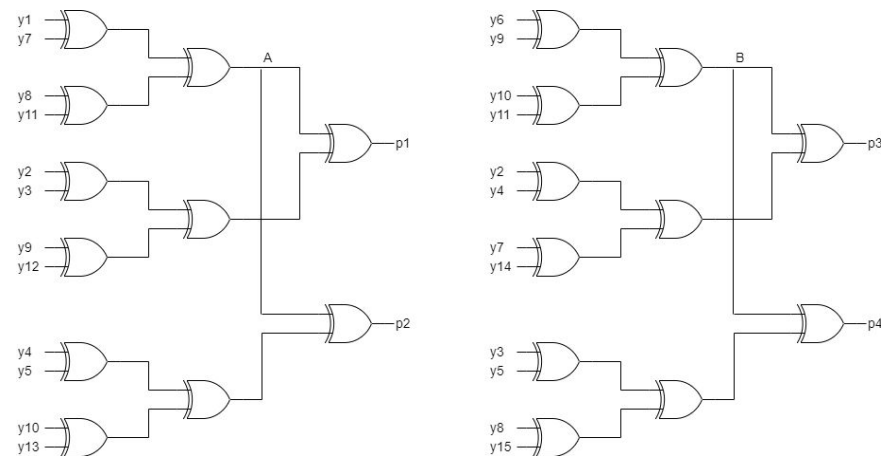
Used to increment the Control Unit.

# COMBINATIONAL DECODER - DESIGN



- **PARITY BITS CALCULATOR**
- **DECODER 4:11**  
From the parity-check matrix and the Parity Bits the mask (11bits) is calculated
- **IMPLEMENTATION OF THE ERROR CORRECTING PART**

Mask  $\oplus$  Original Message



$$\begin{aligned} A &= m1 \oplus m7 \oplus m8 \oplus m11 \\ B &= m6 \oplus m9 \oplus m10 \oplus m11 \end{aligned}$$

$$\begin{aligned} x12 &= A \oplus m2 \oplus m3 \oplus m9; \\ x13 &= A \oplus m4 \oplus m5 \oplus m10. \\ x14 &= B \oplus m2 \oplus m4 \oplus m7; \\ x15 &= B \oplus m3 \oplus m5 \oplus m8. \end{aligned}$$

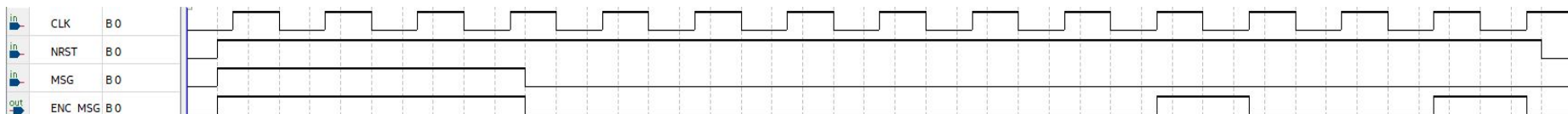
18 x-ors;  
3 x-or propagation time delays  
in the worst case

# RESULTS (VWF)

## ENCODER

MESSAGE M (M1, M2, ..., M11) = 11110000000

ENCODED MESSAGE X (X1, X2, ..., X15) = 1110000000001001



## DECODER

SEVERAL EXAMPLES

