

A CLUSTERING-BASED ML SCHEME FOR CAPACITY APPROACHING SOFT LEVEL SENSING IN 3D TLC NAND

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ABSTRACT

In a 3D TLC solid-state storage system, the LDPC decoding performance is significantly affected by the quality of soft-level sensing. Inspired by the capacity-approaching maximum mutual-information method, this work presents the data-driven approach to collect all the optimal 2-bit soft-read level pairs over the 3D TLC NAND. Due to the data transmission latency and limited configuration resources, a clustering method is proposed to extract the soft-read level pairs in the experiment data. Under the 3K Program Erase Cycles 228-hour data retention at 85°C channel condition, the proposed soft-read level pairs could provide an additional 73-error-bit tolerance in the 2K LDPC decoder.

Index Terms— Maximum Mutual Information, Clustering, 3D NAND, Machine Learning

1. INTRODUCTION

For decades, NAND flash memory has gone through a series of evolution to make the solid-state storage system applicable in consumer electronics, industrial PC, and data centers. In pursuit of higher storage capacity, NAND vendors adopt versatile methods such as process scaling, multiple layer cell techniques, and 3D NAND architecture at the cost of bit reliability over the lifetime. To overcome the degradation of NAND channels, LDPC code, featuring soft-bit iterative decoding capability, is widely utilized as a significant role to extend the lifetime of the memory device [1], [2].

In the regular read operation of the SSD, it applies a hard-read level for the one-bit decoding. If the decoding failure happens, the controller will activate the two-bit decoding mode, which requires two additional read operations for better error correction capability. If decoding failure still happens, the controller would change the read levels for the following retry reads. As a last resort, more soft-bit levels or the die-raid is applied at the cost of long transmission time

for data recovery, which is beyond the scope of discussion in this paper.

Considering transmission latency and firmware setting overhead, the number of soft-read level pairs is constrained (four in our case) and depends on the number of soft-read level register settings in the SoC. To make good use of the proprietary LDPC decoders, the SoC providers would suggest the reference soft-read offset pairs based on the additive white Gaussian noise (AWGN) model, which may not apply in degraded channel conditions.

Several publications have addressed a series of methods such as a non-uniform sensing strategy [3], progressively increasing sensing levels based on the proposed characterised channel models[4]. Considering the data retention error as the most dominant source of errors in 3D NAND flash memory [5], this work proposes a data-driven approach to construct a soft-read offset table based on a real NAND channel.

In the rest of the paper, we describe the background knowledge of 3D NAND flash and evaluate the maximum mutual information approach in section 2. Section 3 presents the sampling approach of our experiment data. The proposed data preprocessing approach and clustering optimization approach are illustrated in section 4, followed by the experiment result in section 5. The conclusion is given in section 6.

2. BACKGROUND

2.1. 3D NAND Structure and Reading Mechanism

Nowadays, most 3D NAND flash cells use a transistor with a charge trap insulator to store the electrons. Since the different amounts of electrons would change the device's I-V characteristics, this property is applied to determine the binary value in the memory cell. To achieve higher cell density of the NAND flash, the TLC technology partitions the threshold voltage into eight different cell states (ER, A - E states in our representation), which correspond to different amounts of electron programmed by the bit-pattern specific program voltage.

Figure 1 shows a simple example of the 3D TLC NAND architecture. In this example, one block (basic unit for data erase) of NAND flash memory is composed of $L = 14$ layers,

The authors thank Frankie Fu, Cloud Zeng, Frank Chen for the valuable discussion of the 3D NAND error characteristic and device structure. The work was supported by the Ministry of Science and Technology (MOST) under grants 110-2622-8-A49-007-SB and 110-2221-E-A49 -157.

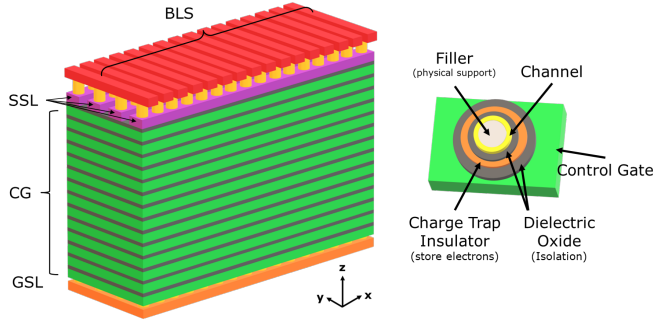


Fig. 1. 3D NAND structure and NAND flash cell

and each layer consists of $F = 4$ word lines in the y-axis. Along the word line, there are $B = 16$ bit lines (or NAND strings) placed vertically on the z-axis. Because each TLC cell can represent three different bits, a word line could be further virtually partitioned into three levels of pages (basic unit for program/read) - lower, middle, and upper pages. As a result, one TLC NAND block contains $L \times F \times 3 \times B = 2688$ bits in $L \times F \times 3 = 168$ pages.

The target word line is located by the drain-select logic (DSL) and the specific layer's control gate (CG) in the read operation. 1) The bit line select (BLS) logics are activated, and the source-select logic (SSL) is off to make sure the channels are not connected to the ground. 2) The target layer is applied by the read voltage, and the remaining layers are given the pass-through voltage (above the maximum possible V_{th}) to construct a conducted channel. 3) After the bit lines are charged with V_{dd} , the SSLs and DSLs are fully activated to allow the current flow in the above-threshold bit channel. 4) Finally, the sense amplifier [6] connected in each bit line would determine whether the bit is 1 or 0 by the given reference voltage according to the TLC page-mapping states.

2.2. Retention in 3D NAND Flash

Due to the F-N tunneling mechanism for the program and erase of NAND flash, as the number of program-erase cycles (P/E cycle) increases, the degraded oxide would trap the electrons and gradually form a leakage path. Given a high P/E cycle NAND flash, as the cell is placed a certain amount of time, the charge leakage makes the voltage distribution of NAND state left-shifted, leading to the data retention error. In addition, due to a stronger electric field induced by the higher amount of stored electrons, the higher cell states are impacted severely with a more significant voltage shift. The V_{th} distribution of the NAND flash at 3K Program Erase Cycles 372-hour data retention at 85°C (3KPE DR372Hr@T85) is shown in Fig. 2, where the distribution's valleys are misaligned with the vertical dash lines (the default hard read level provided by the NAND vendor) due to the data retention issue.

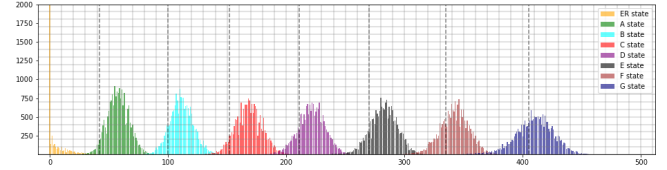


Fig. 2. V_{th} distribution of the real NAND channel. x-axis: read voltage level. y-axis: number of cells.

2.3. NAND Channel Analysis by Maximum Mutual Information Method

The location of the soft-read levels significantly affect the quality of the soft-bit information to the connected 2-Bit LDPC iterative decoder. Based on the channel capacity concept, to maximize the usage of the NAND channels, [7] propose the maximum mutual information (MMI) method to locate the optimal quantization boundary in the AWGN channel. After applying MMI in the real NAND channel as shown in Fig. 3, the MMI with higher mutual information provides a more reasonable asymmetric soft read level than the ones based on the characterized AWGN channel.

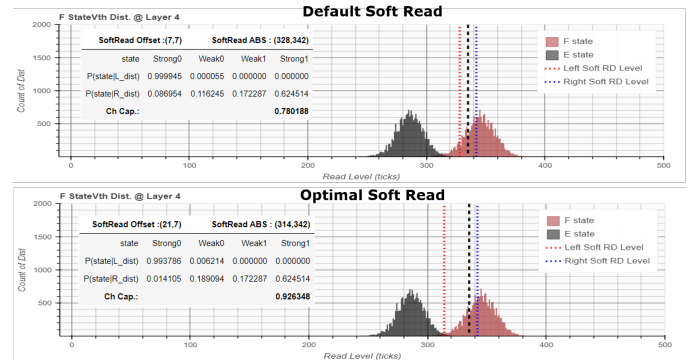


Fig. 3. MMI Soft Read v.s. Default

3. EXPERIMENT DATA

Our research group collects P/E cycle data ranging from 1K to 3K to represent a different level of degradation in TLC. In order to emulate the data retention in SSD operating at 55°C spans from months to years, we apply high temperature (e.g., 85°C) to accelerate the aging process in the experiment. Based on the Arrhenius' Law, we collect data from 83 hours to 372 hours in 85°C, which corresponds to 3 months to 1.75 years of data retention in 55°C over a 3K PE cycle. Considering a long time to collect the voltage distribution of one block, we adopt the following sampling method. Seeing that the physical structure of NAND blocks is independent in each die as observed in [5], this work sample one block of voltage distribution as the representative of the whole NAND die. To further zoom into 3D NAND structure, since the process variation in different layer make the electric characteris-

tics behave differently, we define the granularity of our raw data into layer level. Similar to the structure shown in Fig. 1, each layer consists of four word lines. Consequently, we collect the voltage distribution based on the word line selected by the same Bit-line Selectors. (e.g., WL0, WL4, WL8, ..., overall layers).

To verify the effectiveness of the channel-capacity approach in soft read level searching, the hard read level, provided by the NAND manufacturer, is adopted as the default read level among eight states. After the V_{th} distributions are collected from the die-representative block among 16 dies, we computed the mutual information on those default hard and soft read levels for our analysis. Under the same hard read level, we reach the optimal soft read level (offset from the hard-read level) by the MMI method for all 7 read condition (for 8 states) in each layer.

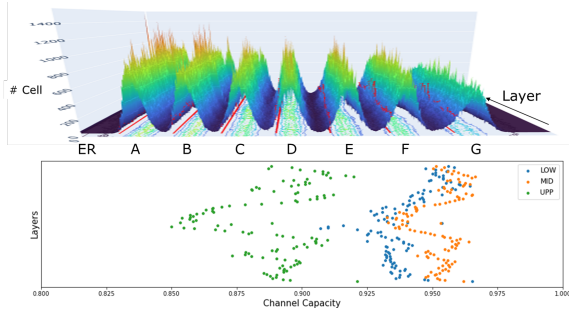


Fig. 4. Topograph of the real NAND Channel. The upper figure presents the V_{th} Topography, where red line shows the default read level of the corresponding states. The lower figure shows the channel capacity calculated in each layers.

The topograph of one sampling block is shown in the upper of Fig. 4, where each row represents the voltage distribution of one layer. (Orange indicate a large amount of bit cell, and blue as the opposite, and the red lines are the default hard read level) We could observe that the left shift of voltage distribution is significant in high cell states (states E, F, and G). In addition, this topograph also suggests that the distribution over different layers has a variant level of retention issues, which correspond to the cross-layer variation mentioned in previous publications. The average channel capacity for three pages is shown at the bottom of Fig 4; since the lower page consists of only middle states with less overlap, the lower page's channel capacity is averagely higher than the other page level. It is noted that the channel capacity distribution of the upper page also reflects on the highest data retention issue introduced in the previous section.

4. PROPOSED METHOD

4.1. Data Preprocessing

We first project all the read-level pairs over a two-dimensional plane, where the x-axis is represented as the right offset and

the y-axis as the left offset. The projection of the optimal soft read levels of 8 states in all the TLC pages is shown in Fig. 5. It addresses that the optimal soft read offset significantly tilts toward the left (y-axis) over the state F and state G, which are the dominant victims in data retention failure mode, as we expected. However, among all eight states, there are still few soft read offset tilts toward the right. Those particular points are unusual for data retention channels, which require investigation and additional data preprocessing before adopting the clustering method.

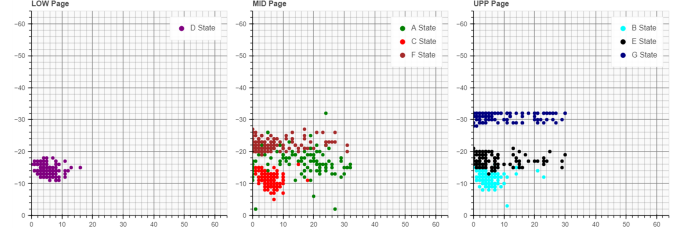


Fig. 5. Optimal Soft Read Distribution in 2-D plots. The three plots represents the distribution of the soft read levels. In each dot plots, the x-axis (y-axis) represents the right (left) offset value from the hard decision read level for the specific state in the NAND page.

As we backtrack the meta of those peculiar soft-read pairs, we have the following observation. 1) Most of the points' mutual information in default hard read is above 0.94, which is far larger than the code rate. 2) The maximum mutual information only provides negligible gain over the default soft read levels. According to the channel coding theory, if channel capacity is larger than the code rate, reliable transmission is achievable by well-designed ECC. After we decode those pages with a one-bit decoder to verify our observation, all the codewords could be successfully decoded. Consequently, we could exclude those data points that are right tilts, whose mutual information of the hard read level is beyond 0.94.

4.2. Maximal Mutual Information Based Clustering

K-mean clustering is a well-known unsupervised learning approach to distill K representatives among the data points over the data space. In our case, each optimal soft-read level pair is projected to the two-dimensional space, and it only allows four sets of soft-read level pairs in the settings. (i.e., $K=4$ is applied in the K-mean clustering method) In order to incorporate the Mutual Information in the clustering scheduling, we propose the Maximal Mutual Information Based Clustering in Alg. 1 to optimize the clustering results. We apply traditional K-means clustering with Euclidean distance metric to initialize four clusters (N_{0-3}) and the representatives (P_{0-3}). Since all the data points have already been labeled into four clusters, we first construct an extension set ($S_{ext,i}$) by the neighboring points of each cluster's members. And then, we update the representatives' data points which provide the highest total mutual information (MI) in the extension set ($S_{ext,i}$). In or-

Algorithm 1 Maximal Mutual Information Based Clustering

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1: initial  $N_{0-3}, P_{0-3} = \text{KMeans}(\text{Data}, K = 4)$ 
2: for iter= 1 to MaxIter do
3:    $Q = \emptyset$ 
4:   for each  $i \in [0, 3]$  do
5:     for each  $n \in N_i$  do
6:        $S_{ext,i} = S_{ext,i} \cup \text{Neighbors}(n)$ 
7:     end for
8:      $P_i = \max_r \sum_{dist \in S_{ext,i}} \text{MI}(dist, r), r \in S_{ext,i}$ 
9:      $N_{sort,i} = \text{Sort}(\{\text{MI}(dist, P_i), dist \in N_i\})$ 
10:     $Q = Q \cup N_{sort,i}[0 : 9]$  // Least 10 elements
11:  end for
12:  for each  $q \in Q$  do
13:     $i = \text{argmax}_j \text{MI}(q, P_j), P_j \in P_{0-3}$ 
14:     $N_i = N_i \cup q$ 
15:  end for
16: end for

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MI stands for mutual information function for NAND distribution (dist.) and soft read levels (r).

der to avoid over-fitting, we choose the 10 data points with the lowest mutual information of each cluster into the waiting list (Q). Then elements in the list would be re-assigned to the cluster by the MMI computed by the element's Vth distribution and the representatives' soft-read level. Figure 6 presents the clustering result of the proposed algorithm. Since some soft-read offset points consist of multiple data points, which could not be shown in the projected 2-dimensional plane, the representatives of four clusters are not in the center of each region.

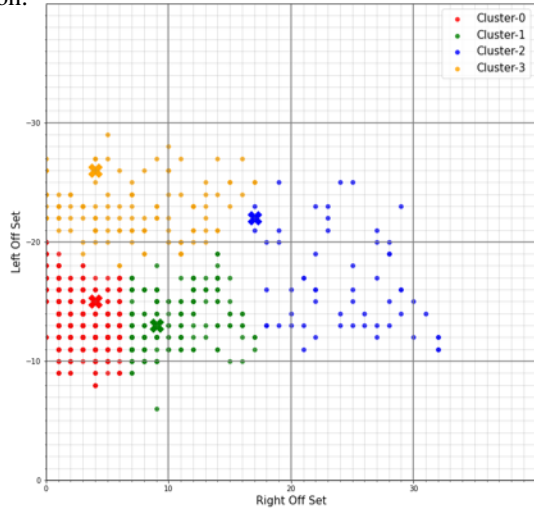


Fig. 6. Maximal Mutual Information Based Clustering Result

5. IMPLEMENTATION RESULT

In verification, this work applies one of the non-training NAND blocks over 16 dies in the same drive as the validation data set. Figure 7 shows the 2K LDPC performance

result over 3KPE DR228Hr@T85 NAND channel condition, and the proposed method provides nearly 80/80/60 Error Bit Count tolerance over Lower/Middle/Upper Page at $\text{FER}=10^{-1}$.

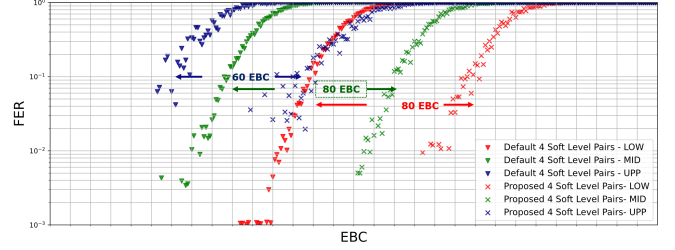


Fig. 7. Improvement of Error Bit Count

As we examine our experiment over the die variance condition, we collect the number of codeword passes in the validation block over 16 dies, as shown in the following bar chart. After applying the optimized soft-read offset settings in different data retention over the 3KPE DR228@T85 channels, the proposed method provides better correction rates overall 16 dies.

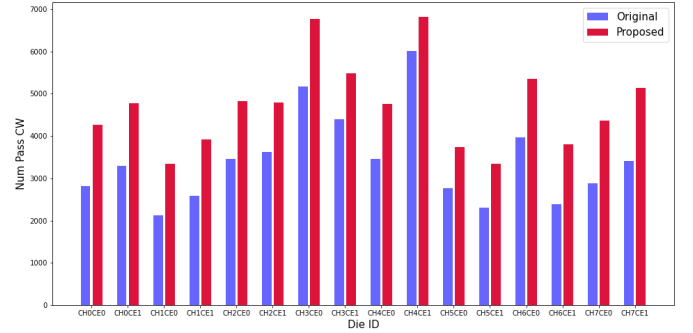


Fig. 8. Pass Codeword Count over Different Die

6. CONCLUSION

This research extends the maximum mutual information concept from the characterized AWGN channel to the real NAND channel. With the knowledge of the 3D NAND structure and data retention properties, we effectively reduce the redundant data samples in our data collection. The projected data are pre-processed and provide better performance through the detailed data visualization over the channel capacity and the corresponding word line voltage distribution. Under the constraint of the limited soft-read voltage settings, the proposed maximum mutual-information-based clustering method significantly provides in-average additional 73-error-bit tolerance from the default settings suggested by the characterized AWGN channel.

7. REFERENCES

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