CMPEN271

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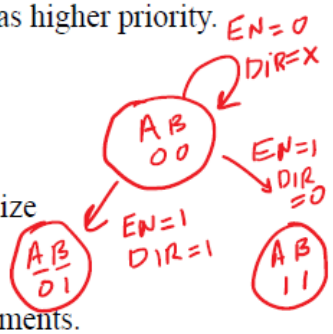
HW#9C

Finite State Machine

HW #9C – FSM Up/Down Counter

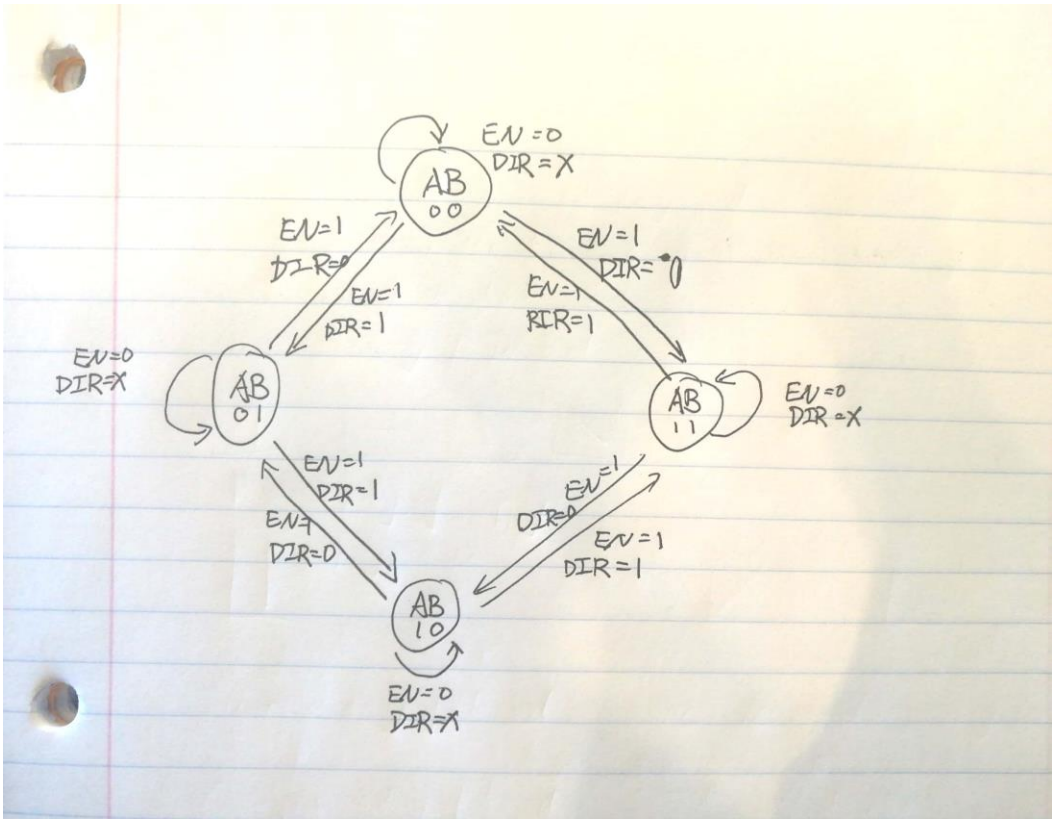
Design and simulate a 2-bit **FSM up/down counter with enable**. The counter has **two external inputs**, EN(enable) and DIR (direction). When EN = 1, the circuit count proceeds normally; when EN = 0, the counter stays in the present state. When DIR = 1 the counter counts up in the sequence 00, 01, 10, 11, repeat. When DIR = 0, the counter counts down in the sequence 11, 10, 01, 00, repeat. EN (enable) input has higher priority. Use D flip-flops.

a) construct state diagram
b) construct state table
c) add flip-flop input equations to truth table and minimize
d) draw circuit
e) simulate circuit
f) deliver circuit and timing diagram with markups/comments.



P.S.
A B EN DIR | N.S.
A B DA DB

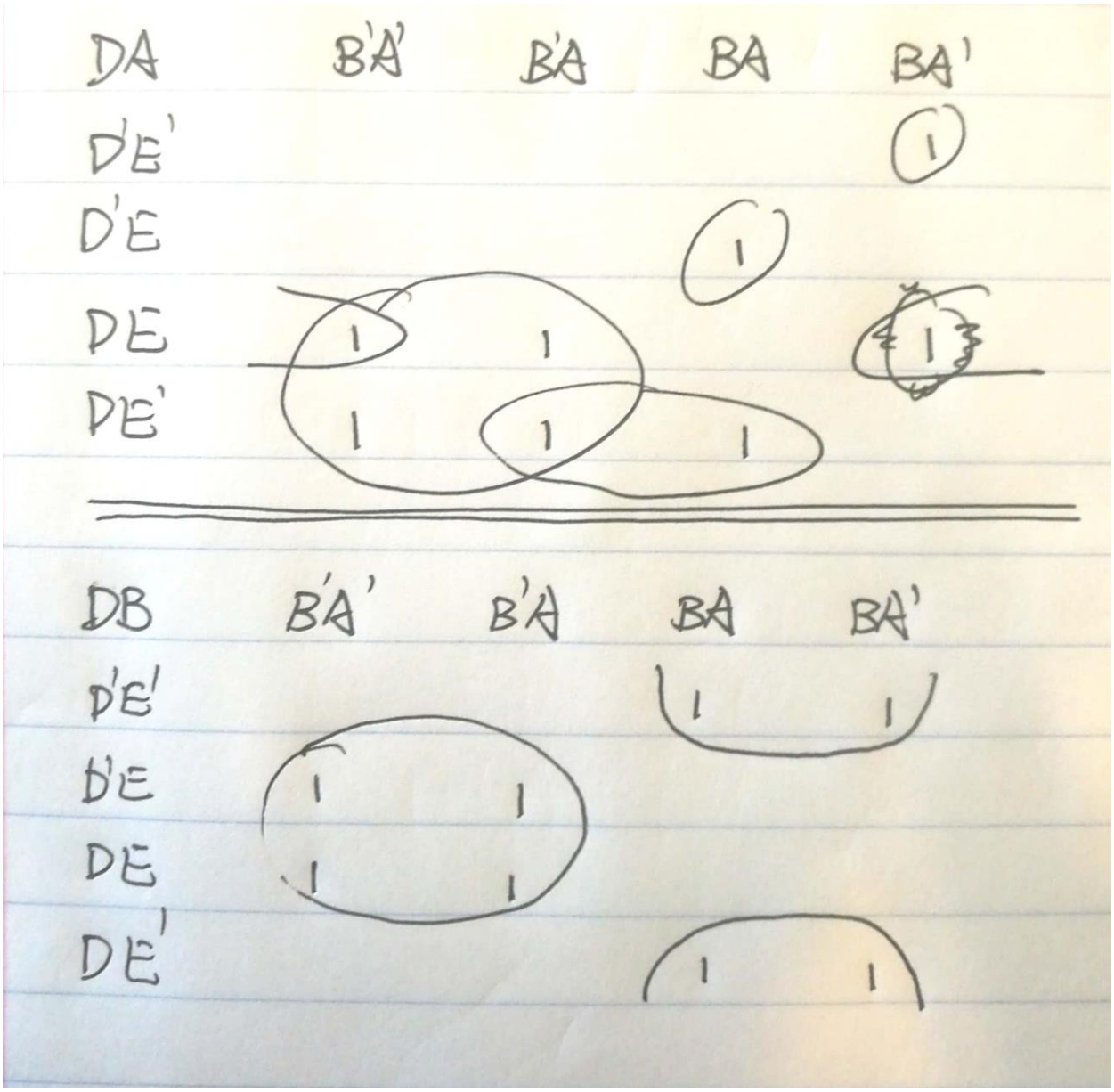
finish this!!



Present State				Next State			
A	**B**	**E**	**D**	**A**	**B**	**DA**	**DB**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	1	1	1	1
0	0	1	1	0	1	0	1
0	1	0	0	0	1	0	1
0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	0
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	0
1	0	1	0	0	1	0	1
1	0	1	1	1	1	1	1
1	1	0	0	1	1	1	1
1	1	0	1	1	1	1	1
1	1	1	0	1	0	1	0
1	1	1	1	0	0	0	0

DA = Σm(2,7,8,9,11,12,13,14)

DB = Σm(2,3,4,5,10,11,12,13,14)

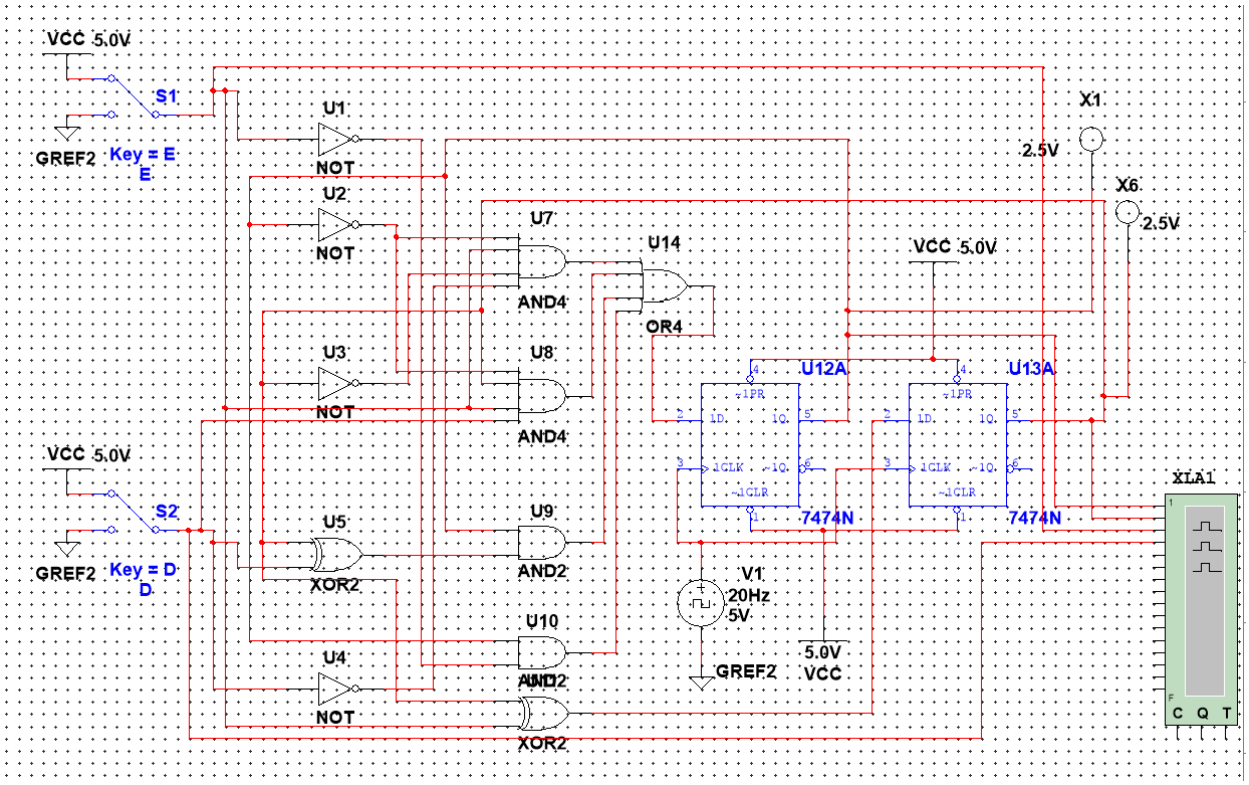


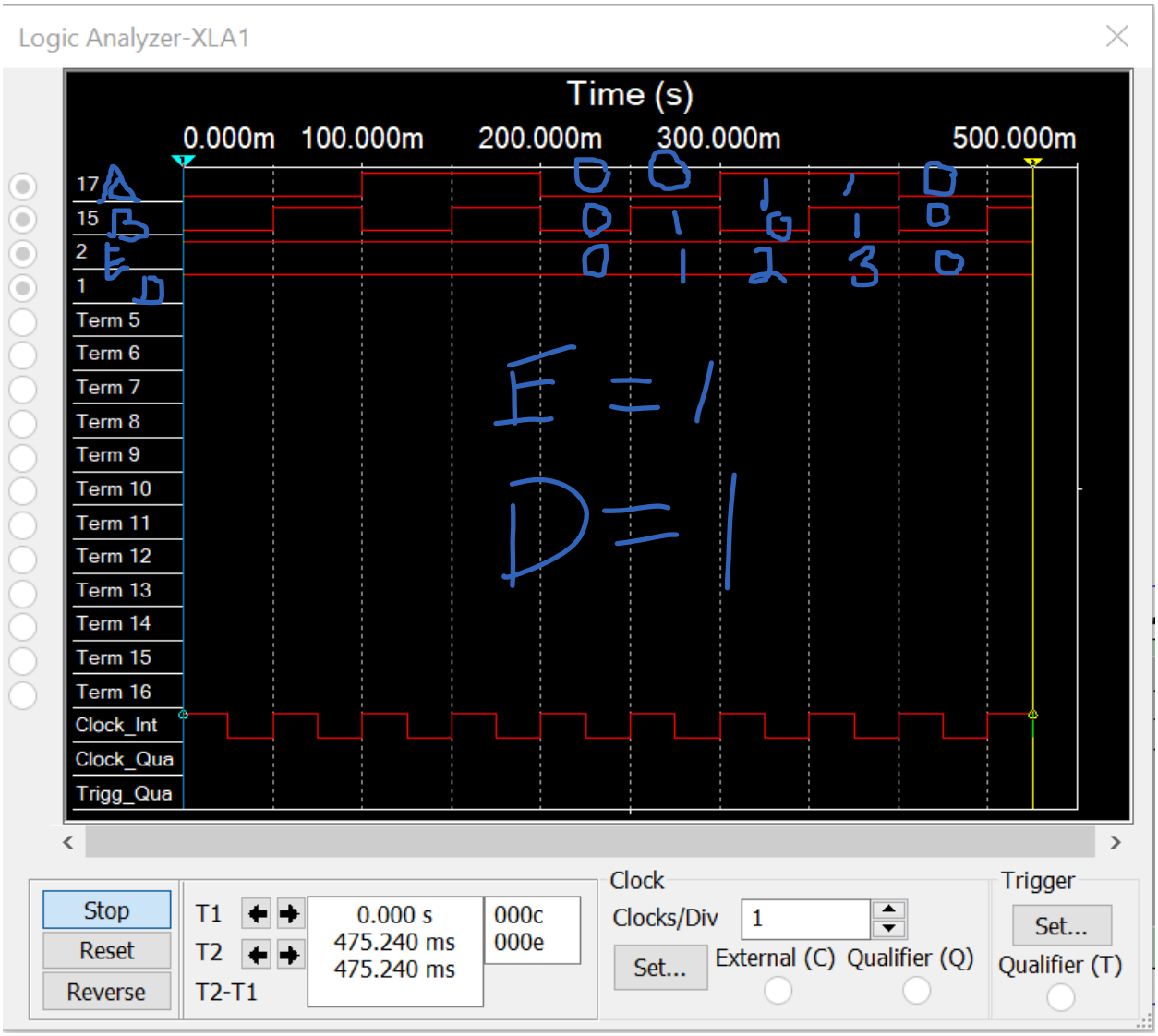
DA=A'B'ED'+A'BED+AB'E'D'+AB'E'D+AB'ED+ABE'D'+ABE'D+ABED'

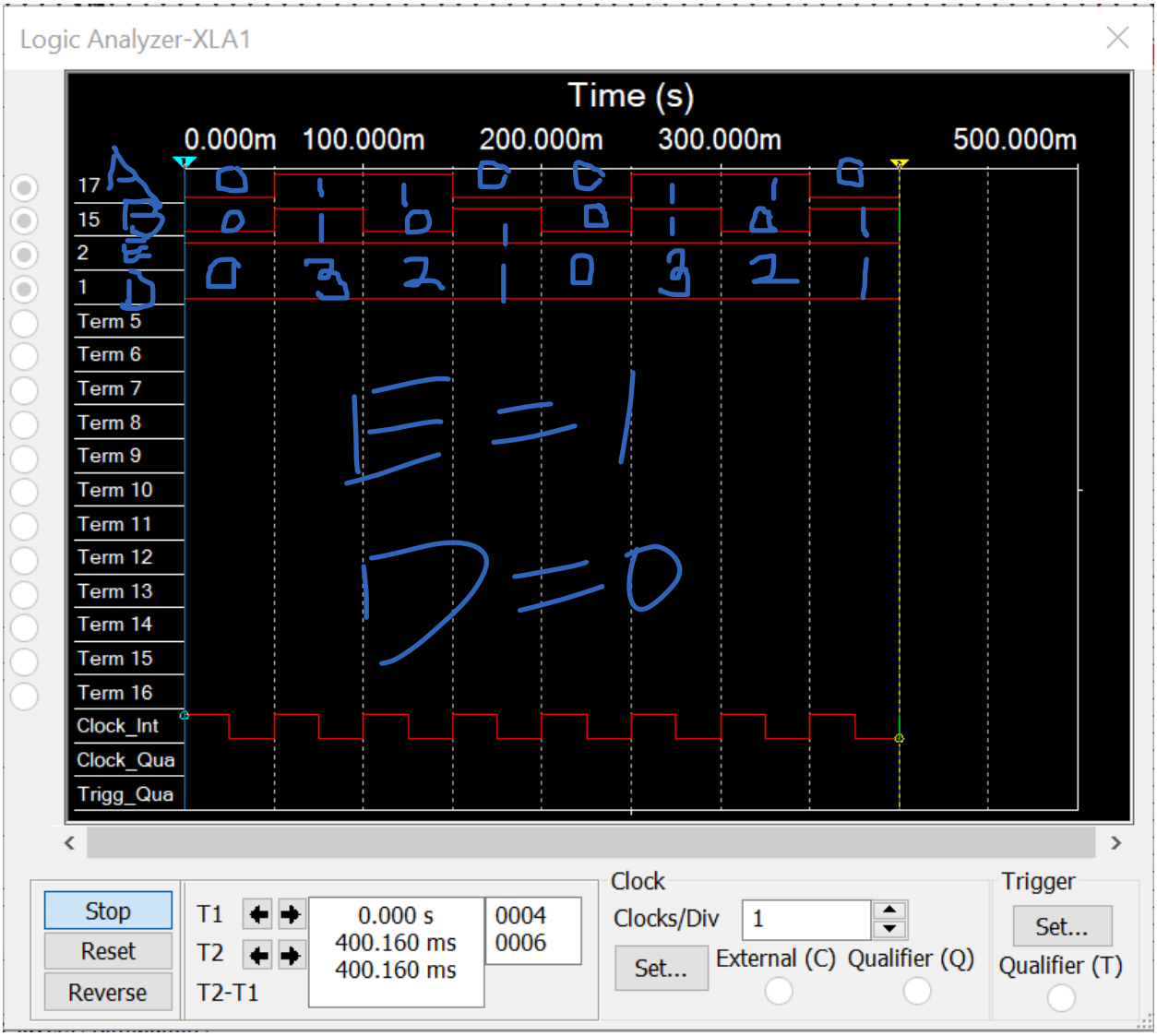
Simplify: DA=A'B'ED'+A'BED+A(B⊕D)+AE'

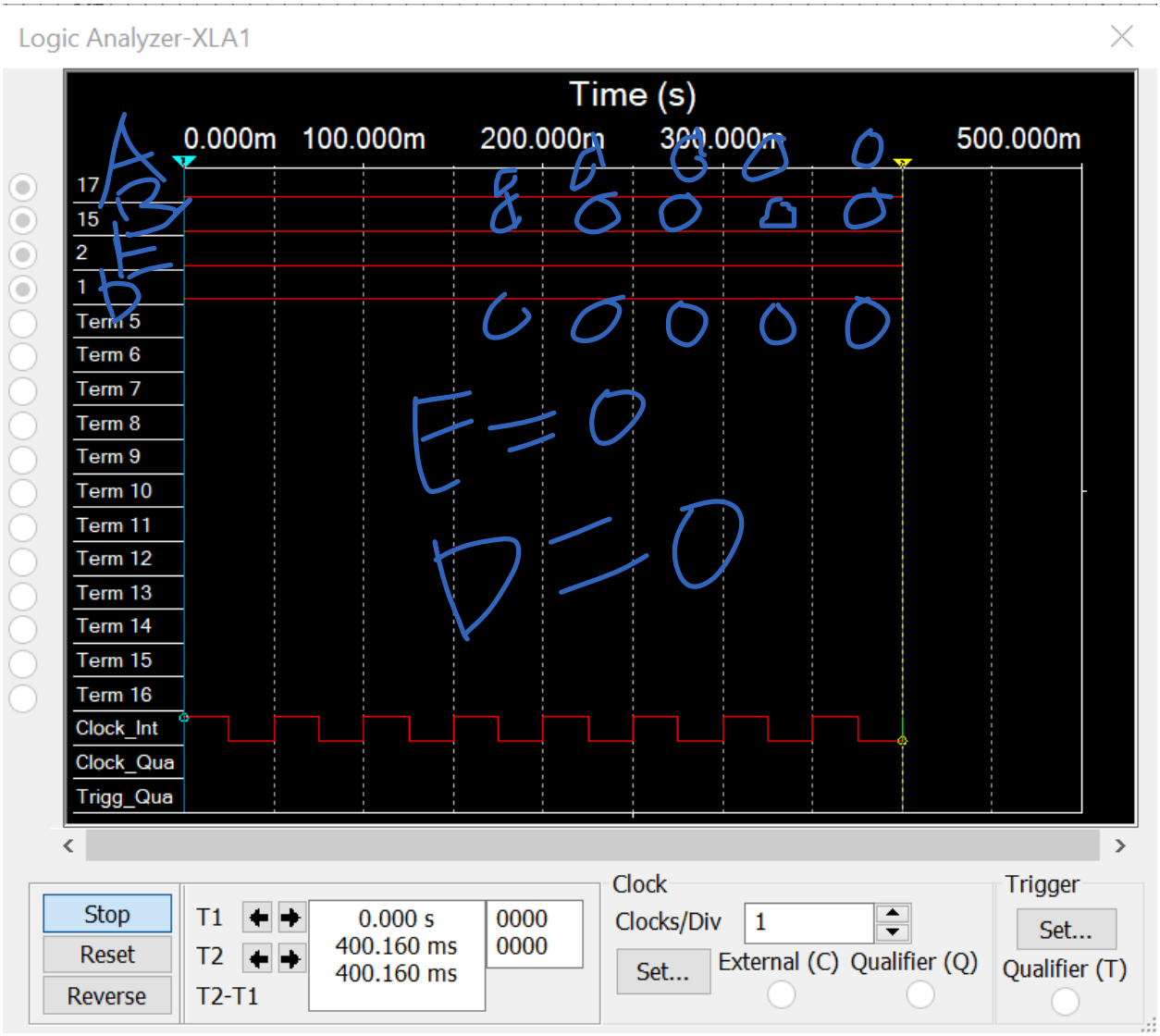
DB=A'B'ED'+A'B'ED+A'BE'D'+A'BE'D+AB'ED'+AB'ED+ABE'D'+ABE'D

Simplify: DB=B⊕E


VCC 5.0V
S1
GREF2
Key = E
E
U1
NOT
U2
NOT
U3
NOT
U4
NOT
U5
XOR2
U7
AND4
U8
AND4
U9
AND2
U10
AND2
XOR2
U14
OR4
X1
2.5V
X6
2.5V
VCC 5.0V
U12A
U13A
7474N
7474N
XLA1
C Q T
VCC 5.0V
S2
GREF2
Key = D
D
V1
20Hz
5V
GREF2
5.0V
VCC


Logic Analyzer-XLA1
Time (s)
0.000m
100.000m
200.000m
300.000m
500.000m
17
15
2
1
Term 5
Term 6
Term 7
Term 8
Term 9
Term 10
Term 11
Term 12
Term 13
Term 14
Term 15
Term 16
Clock_Int
Clock_Qua
Trigg_Qua
A
B
E
D
0 0 1 1 0
0 1 0 1 0
0 1 2 3 0
E = 1
D = 1
Stop
Reset
Reverse
T1
T2
T2-T1
0.000 s
475.240 ms
475.240 ms
000c
000e
Clock
Clocks/Div
1
Set...
External (C)
Qualifier (Q)
Trigger
Set...
Qualifier (T)


Logic Analyzer-XLA1
Time (s)
0.000m
100.000m
200.000m
300.000m
500.000m
17
15
2
1
Term 5
Term 6
Term 7
Term 8
Term 9
Term 10
Term 11
Term 12
Term 13
Term 14
Term 15
Term 16
Clock_Int
Clock_Qua
Trigg_Qua
E=1
D=0
Stop
Reset
Reverse
T1
T2
T2-T1
0.000 s
400.160 ms
400.160 ms
0004
0006
Clock
Clocks/Div
1
Set...
External (C)
Qualifier (Q)
Trigger
Set...
Qualifier (T)


Logic Analyzer-XLA1
Time (s)
0.000m
100.000m
200.000m
300.000m
500.000m
17
15
2
1
Term 5
Term 6
Term 7
Term 8
Term 9
Term 10
Term 11
Term 12
Term 13
Term 14
Term 15
Term 16
Clock_Int
Clock_Qua
Trigg_Qua
A
B
E=0
D=0
Stop
Reset
Reverse
T1
T2
T2-T1
0.000 s
400.160 ms
400.160 ms
0000
0000
Clock
Clocks/Div
1
Set...
External (C)
Qualifier (Q)
Trigger
Set...
Qualifier (T)