CMPEN271

HW# 9B

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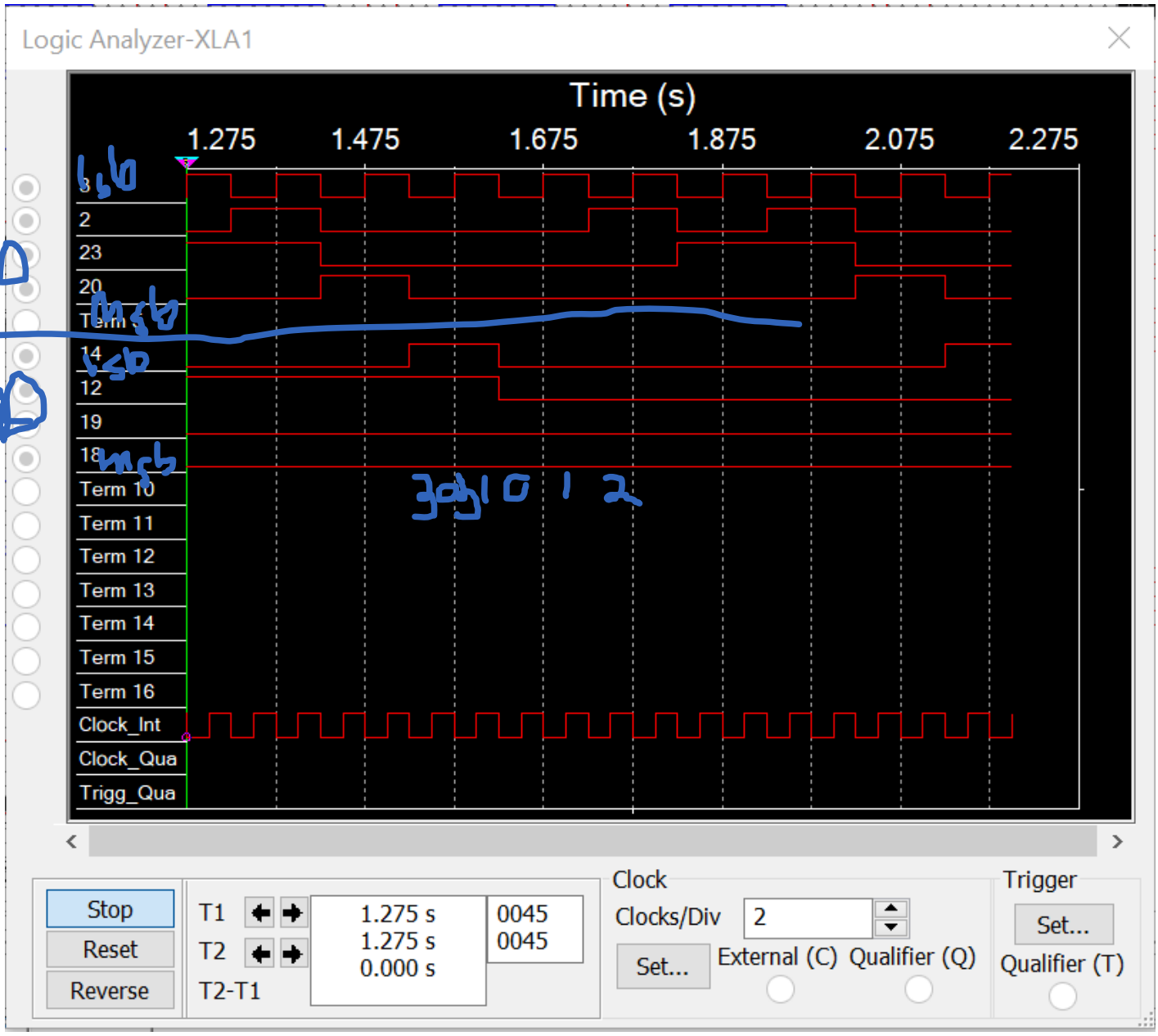
HW #9B: BCD Ripple Counter (see schedule)

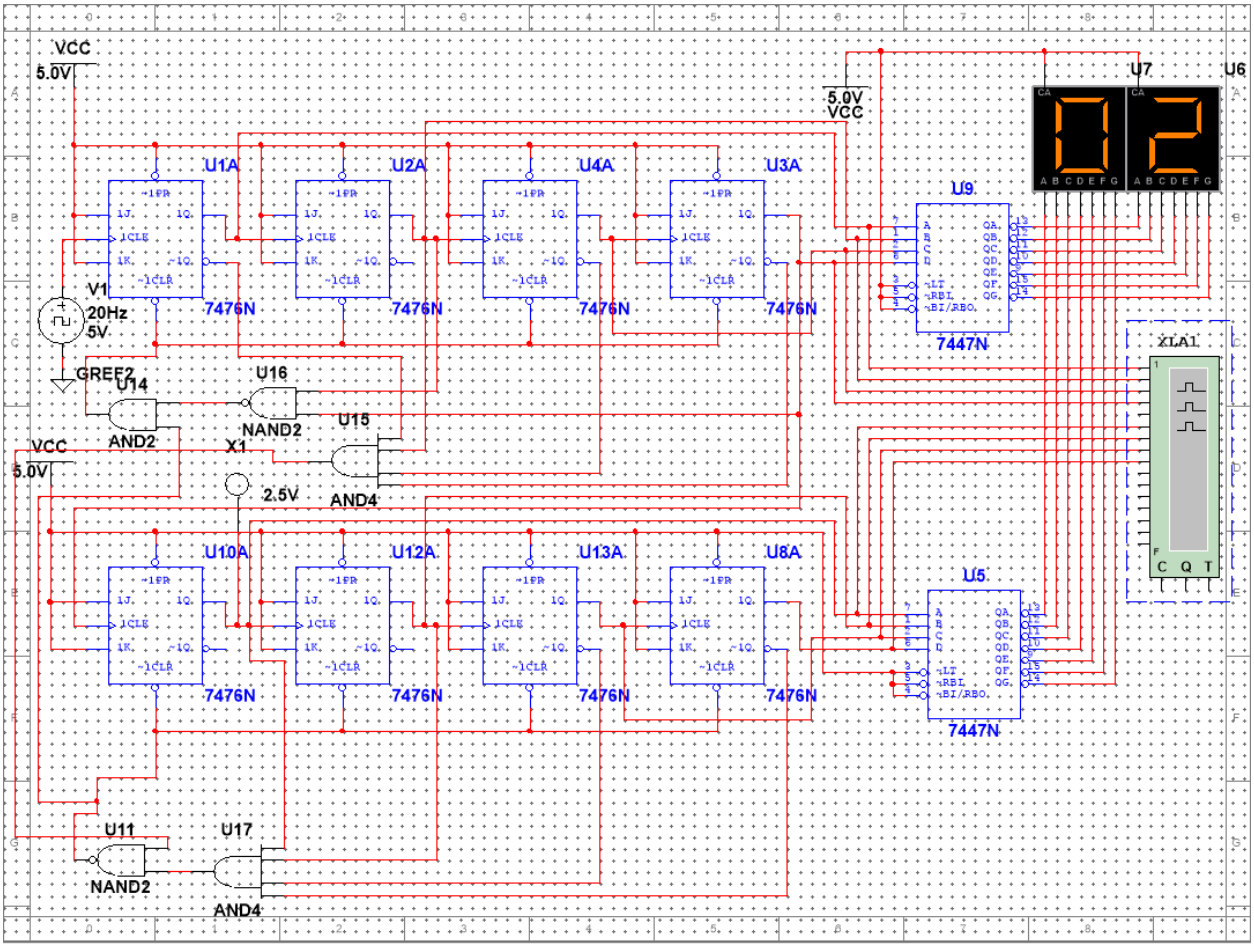
#2. Design and simulate a **BCD ripple counter** with the MOD equal to the last 2 digits, (LSDs) of your PSU email address. (If the last 2 digits of your PSU email address are less than 11 or a power of 2, then let MOD=50). See instructor for additional details.

The output to this circuit are **two, 7-segment LED displays**. Use **7447** (or equivalent) drivers. Use negative-edge triggered JK flip flops in your design and any other logic gates as needed. Include timing diagrams (with reset) with markups. Include critical portions of the timing diagrams with annotations. Include timing diagram markups for 2 counts before the reset to 0, count = 0, and 2 counts after the reset to 0. Show count values in both binary and in decimal. Label msb and lsb for each counter/digit. For example, if you have to design a MOD 50 counter (count sequence 0 to 49) then you would show binary and decimal markups on timing diagram for counts 48, 49, 0, 1, 2.
Hint: start with the 00 to 99 BCD counter discussed earlier in this lecture. Make sure the 00 to 99 BCD counter fully works with the 7-segment displays in Multisim and then modify to reset at a new count value.

MSD (most sign. digit)

LSD (least sign. digit)


Logic Analyzer-XLA1
Time (s)
1.275
1.475
1.675
1.875
2.075
2.275
3
2
23
20
14
12
19
18
Term 10
Term 11
Term 12
Term 13
Term 14
Term 15
Term 16
Clock_Int
Clock_Qua
Trigg_Qua
lsb
msb
msb
lsb
msb
3 2 1 0 1 2
Stop
Reset
Reverse
T1
T2
T2-T1
1.275 s
1.275 s
0.000 s
0045
0045
Clock
Clocks/Div
2
Set...
External (C)
Qualifier (Q)
Trigger
Set...
Qualifier (T)


VCC
5.0V
U1A
U2A
U4A
U3A
7476N
V1
20Hz
5V
GREEN
U14
AND2
U16
NAND2
U15
AND4
X1
2.5V
U10A
U12A
U13A
U8A
U11
NAND2
U17
AND4
U9
7447N
U5
7447N
U7
U6
XLA1
C Q T