Penn State Abington
CMPEN 271
Lecture Set #15
NAND/NOR Latch

R. Avanzato © 2013-2015

Topics:

- NAND Latch — **Video part 1** ←
- NOR Latch
- Timing diagrams

- Latch applications: — Video part 2
  1) debounced switch, 2) alarm

- Review Questions — Video part 3

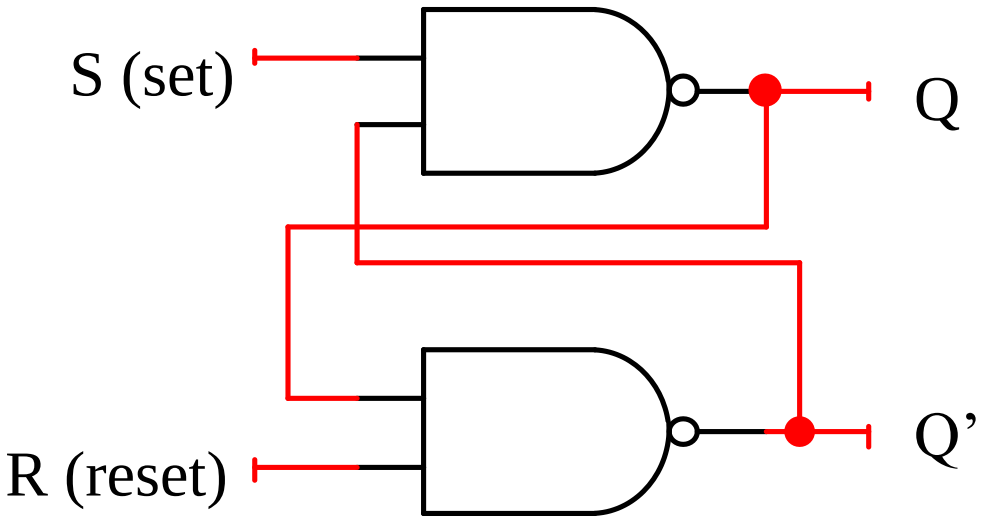
- Take Exam #2 after Lecture #15

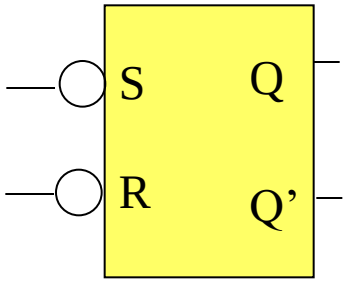
Real-world Design Problems

- How do design a circuit to **store a bit**?
- How do you design a circuit with **memory**?
- What is **switch "bounce",** and how can you correct it?
- How can you design an **alarm circuit** with a break-beam feature that **"latches"** an alarm?

NAND Latch

A latch "stores" (remembers) one bit of data





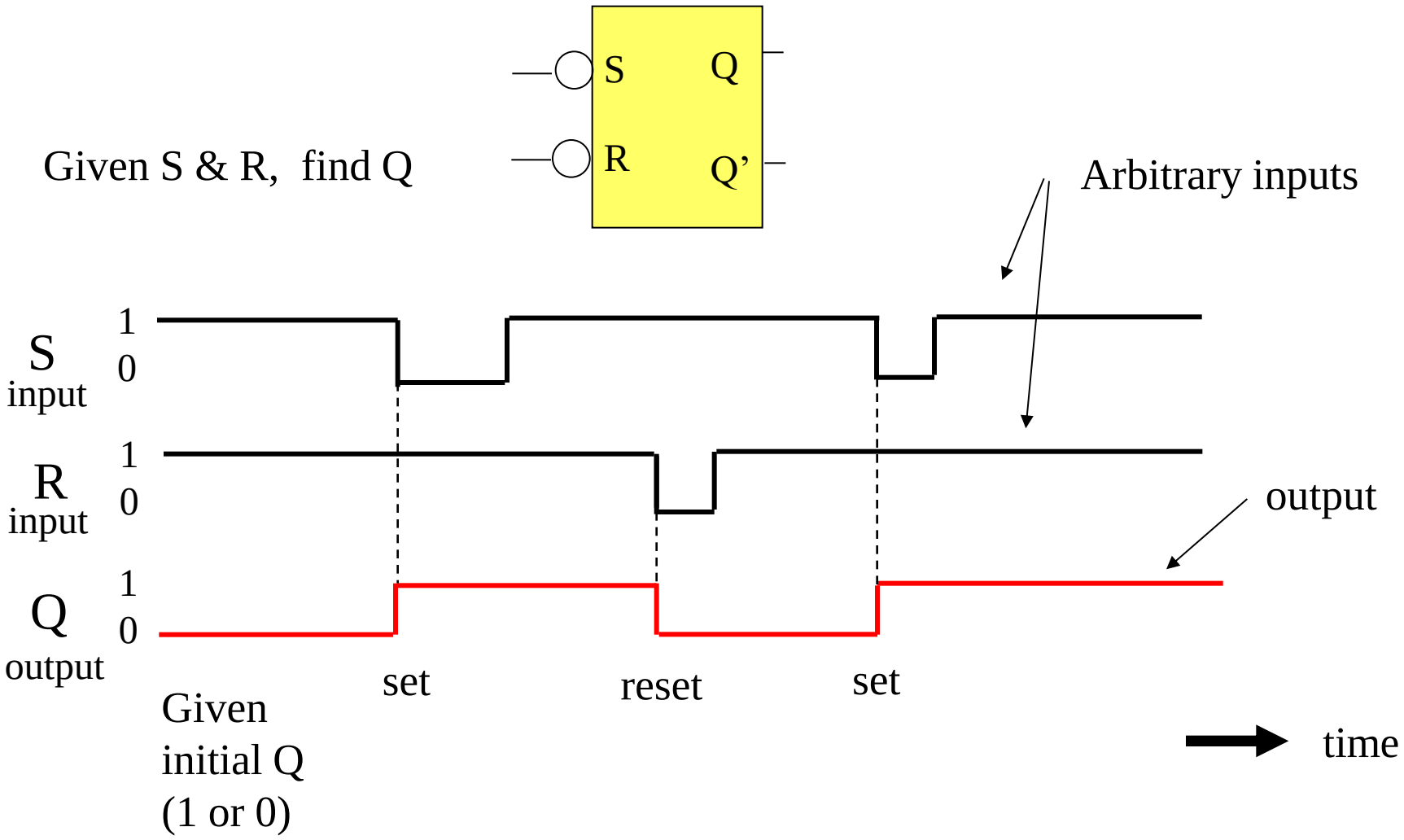
Block diagram of NAND latch

inputs		outputs		
S	R	Q	Q'	
0	1	**1**	0	**(set)**
1	1	1	0	*(resting)*
1	0	0	**1**	**(reset)**
1	1	0	1	*(resting)*
0	0	1	1	(avoid)

Notes:

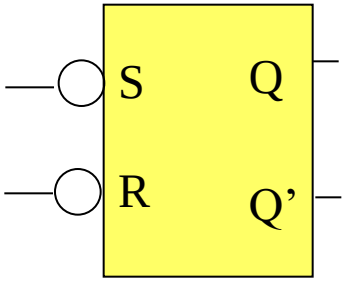
- note feedback loop (new feature)
- order of inputs is important
- different outputs for S=1, R=1, depending on history
- illegal output: Q=Q'=1 (avoid this)
- S, R are active-low inputs
- "**Set**" means set **Q=1** (and Q'=0)
- "**Reset**" means set **Q = 0** (and Q'=1)
- Feature of a NAND gate: if any input is 0, then output must be 1.
- compare to traditional truth table

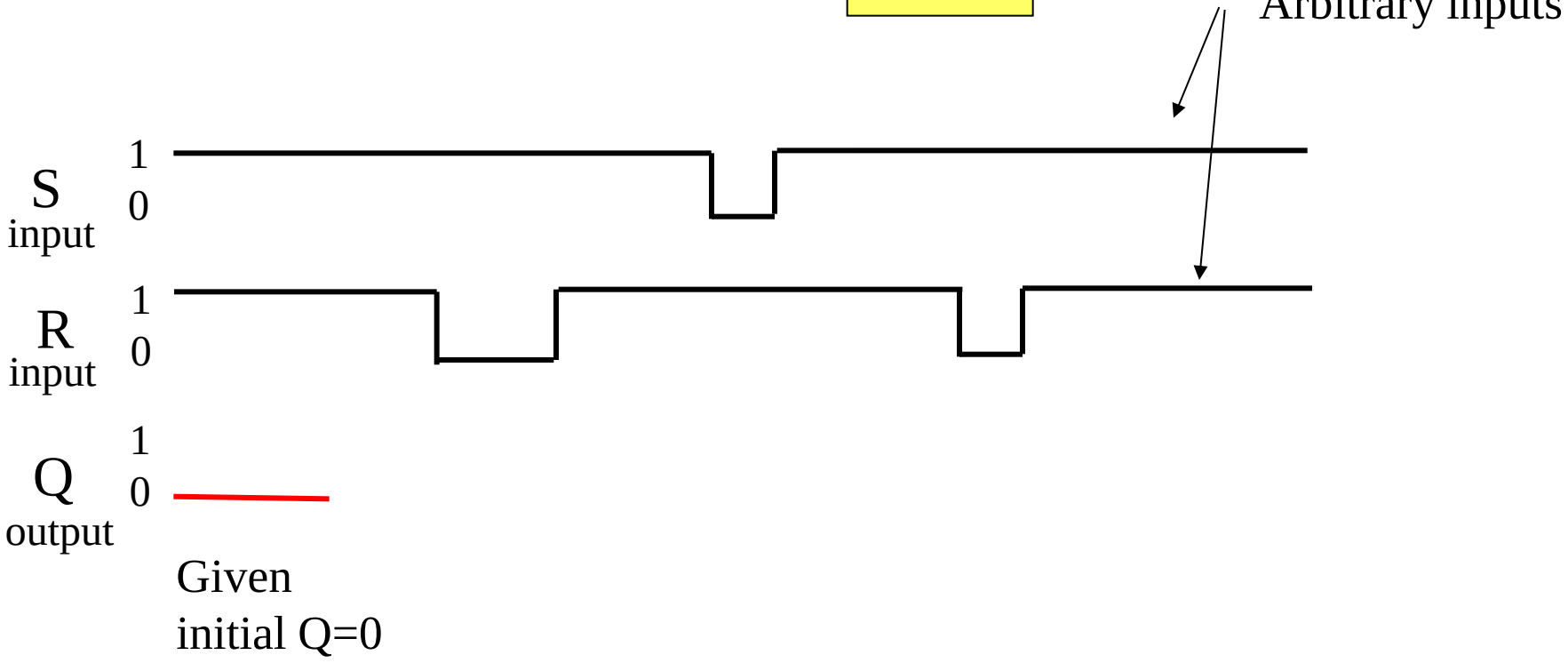
NAND Latch Timing Diagram - 1



NAND Latch Timing Diagram- 2

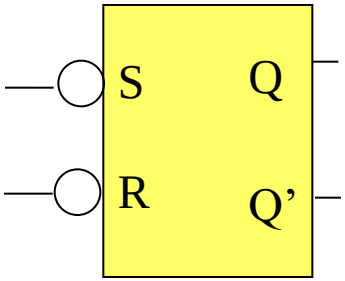
Exercise: Given S & R, find Q

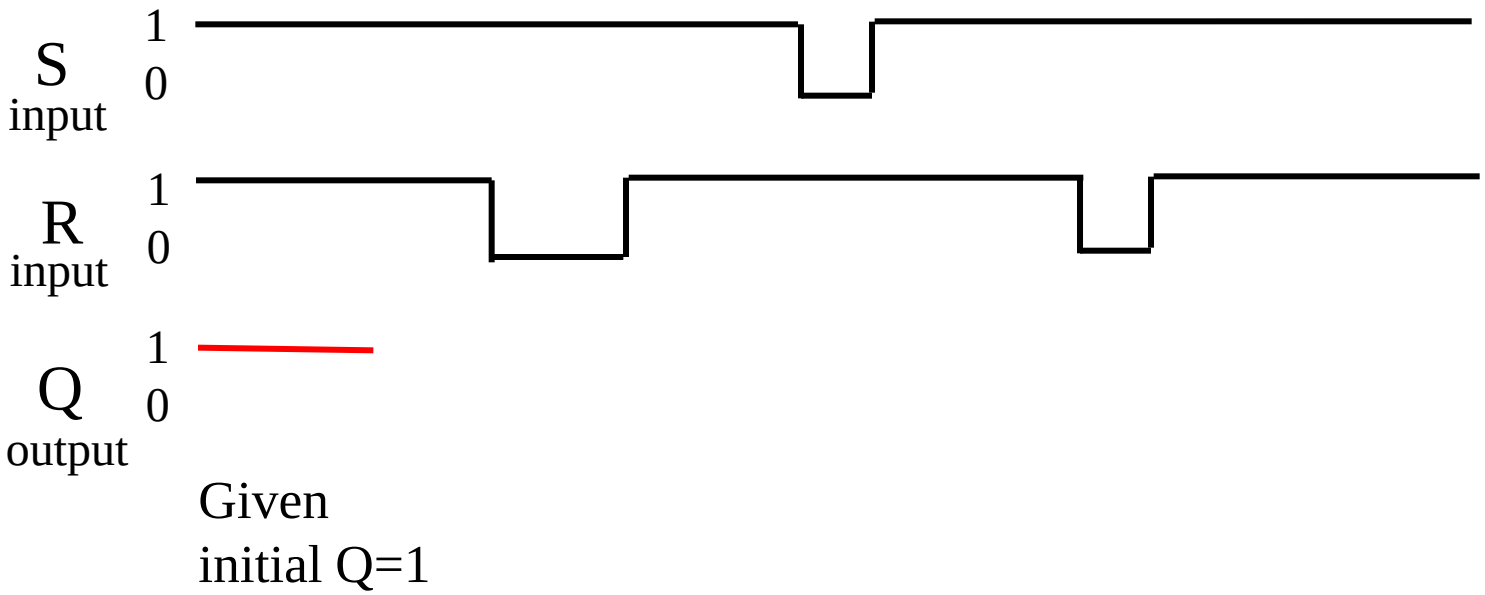




NAND Latch Timing Diagram- 3

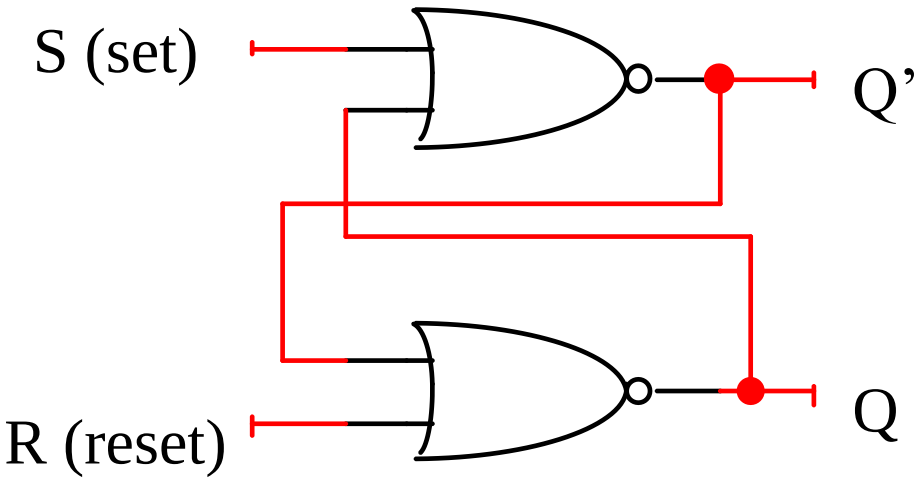
Exercise: Given S & R, find Q

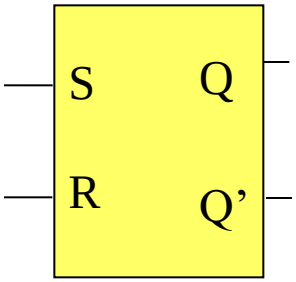




NOR Latch

A latch "stores" (remembers) one bit of data.





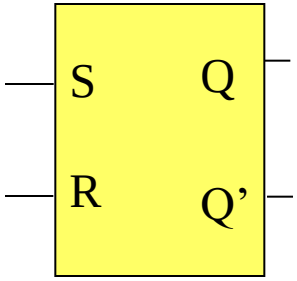
Block diagram of NOR latch

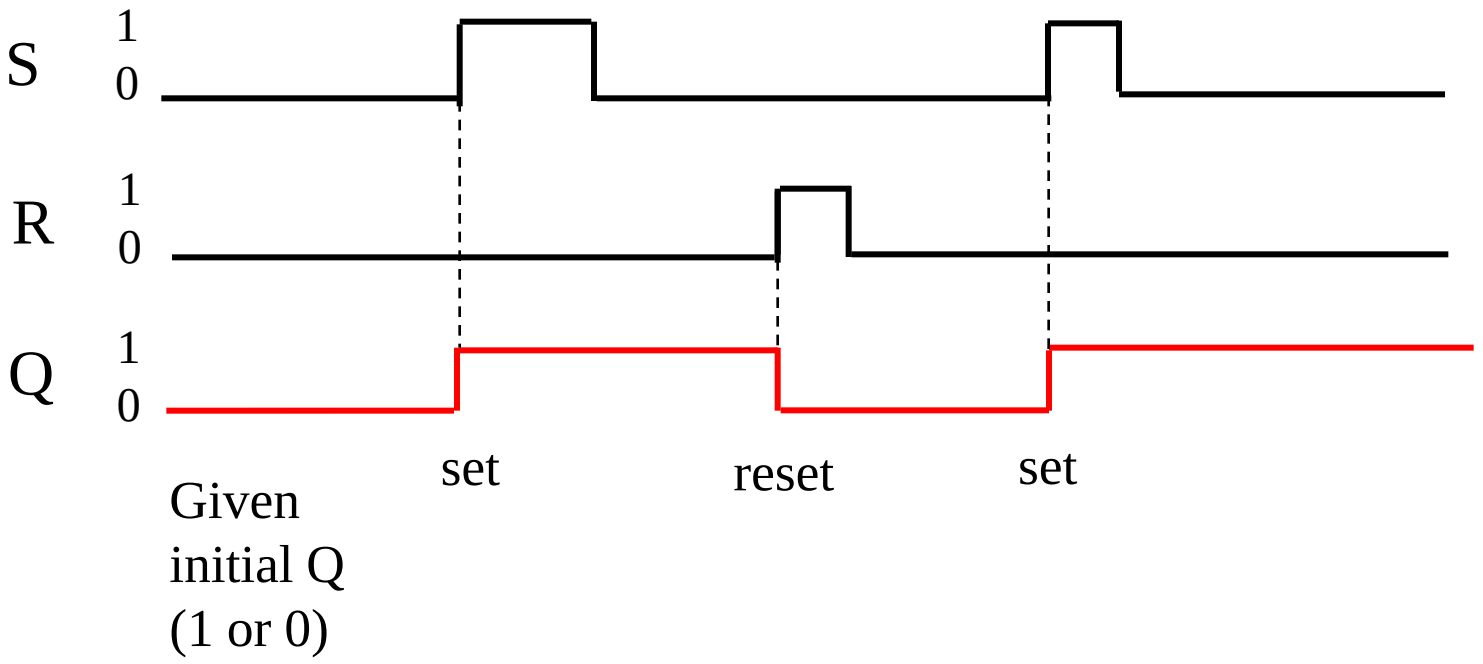
inputs		outputs		
S	R	Q	Q'	
1	0	**1**	0	**(set)**
0	0	1	0	*(resting)*
0	1	0	**1**	**(reset)**
0	0	0	1	*(resting)*
1	1	0	0	(avoid)

Notes:
- different output for S=0, R=0, depending on history
- illegal output: Q=Q'=1
- S, R are active-high inputs
- **"Set"** means set **Q=1** (and Q'=0)
- **"Reset"** means set **Q = 0** (and Q'=1)
-Feature of a NOR gate: if any input is 1, then output must be 0.
-NAND and NOR latches are equivalent in purpose.

NOR Latch Timing Diagram - 1

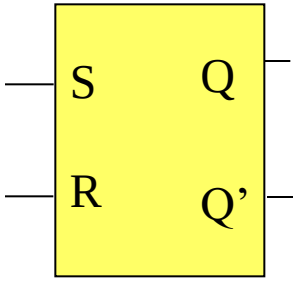
Given S & R, find Q

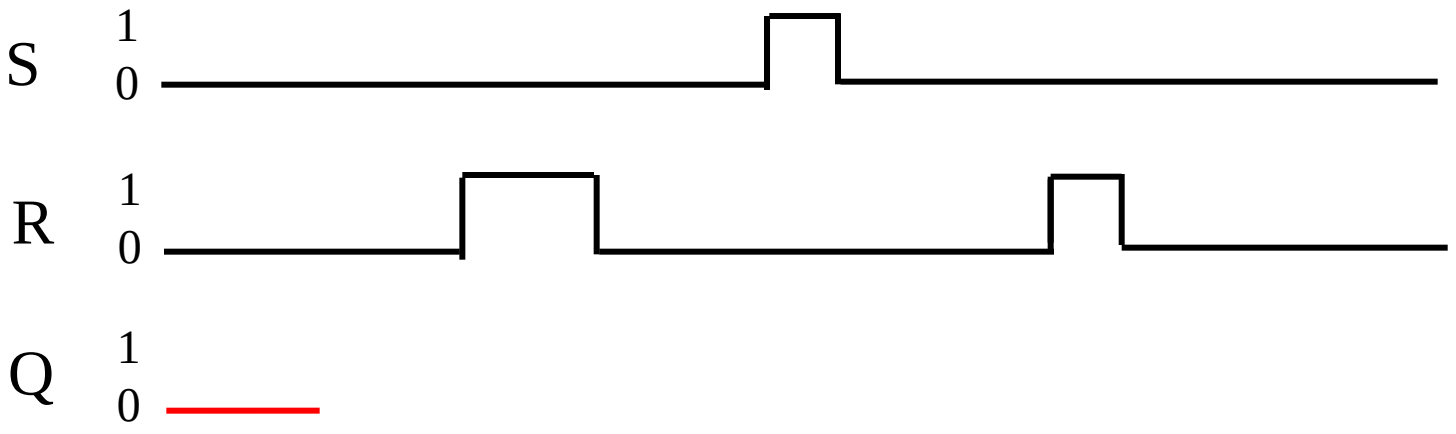




NOR Latch Timing Diagram - 2

Given S & R, find Q

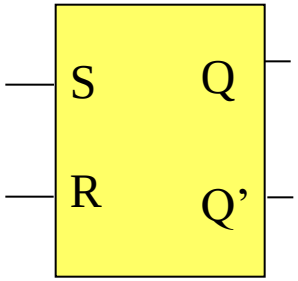


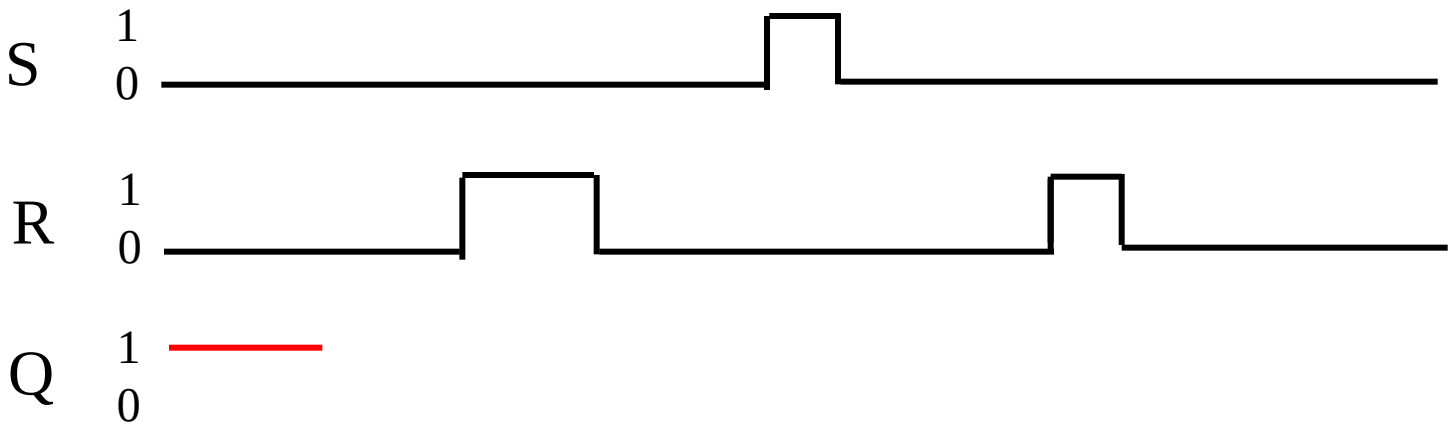


Given
initial Q=0

NOR Latch Timing Diagram - 3

Given S & R, find Q





Given
initial Q=1

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  1) debounced switch, 2) alarm

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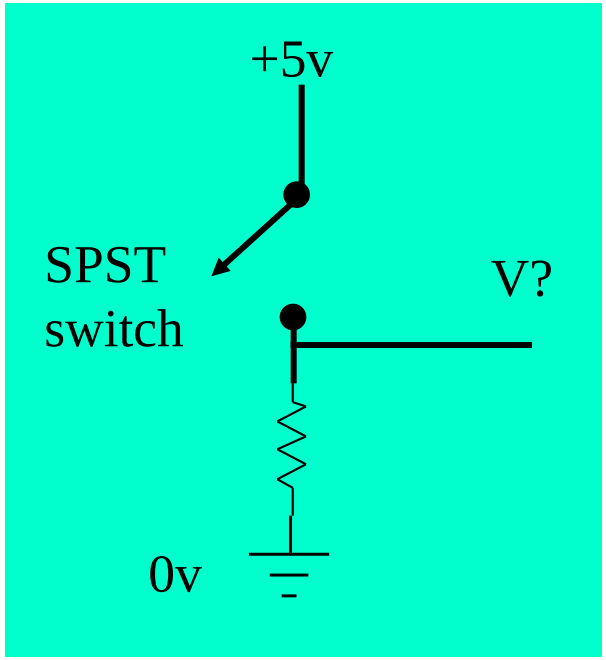
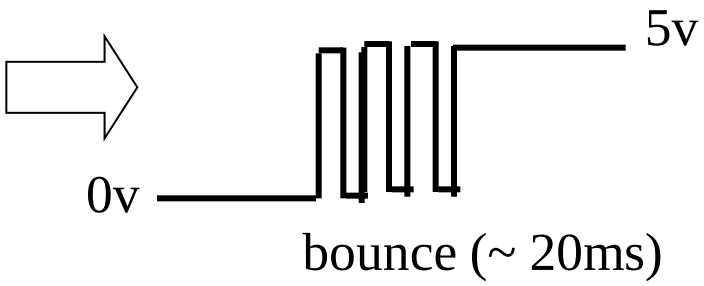
Latch Application: Debounced Switch



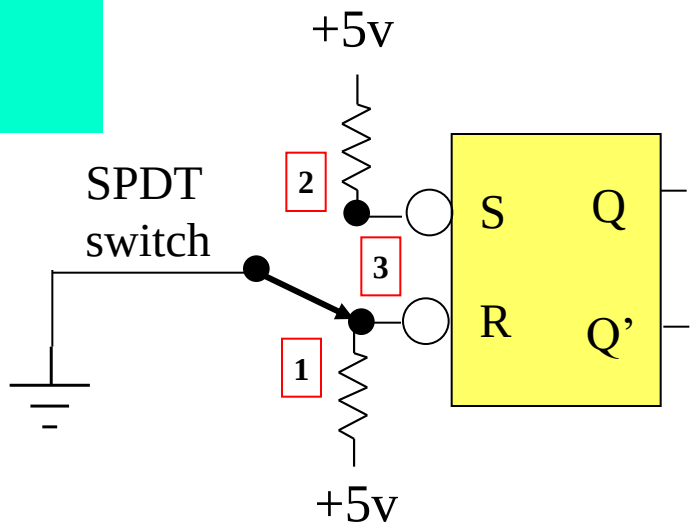


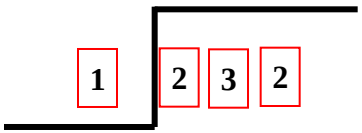
Switch bounce is undesirable for many digital applications. All mechanical switches bounce.

Solution: use latch and SPDT Switch

Assume no current flows into latch.

(Adapted from Tocci)

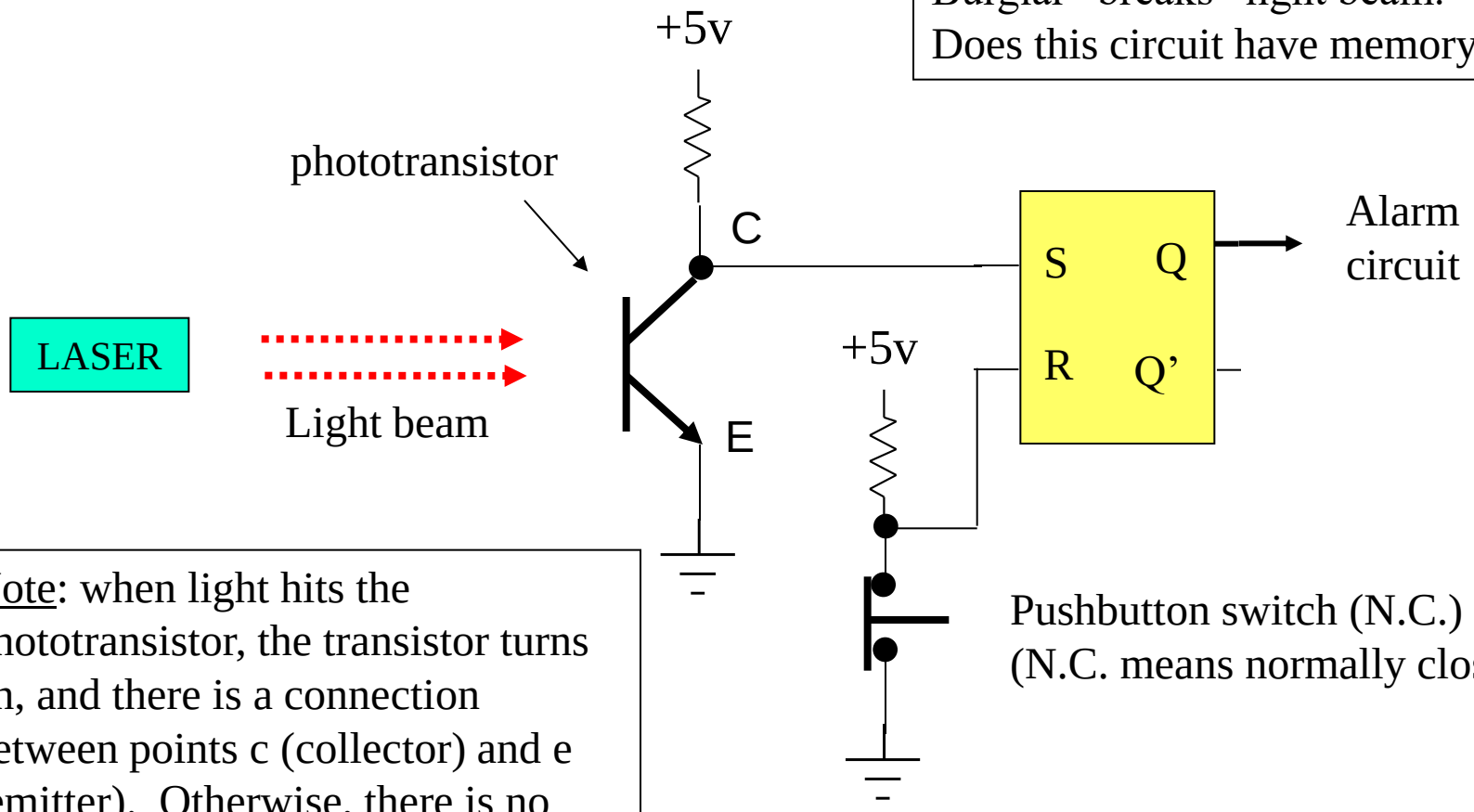




No bounce on output. (Note: mechanical SPDT switch still bounces, but output transition is clean.)

Latch Application: Burglar Alarm

Explain circuit operation.
Burglar "breaks" light beam.
Does this circuit have memory?

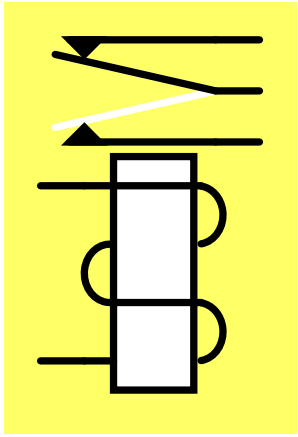


Note: when light hits the phototransistor, the transistor turns on, and there is a connection between points c (collector) and e (emitter). Otherwise, there is no electrical connection between points c and e.

(Adapted from Tocci)

Latching Relay – Extra Project

- Review operation of a standard electromechanical relay?
- What is the purpose of a relay?
- Show a simple circuit to control a 40 volt motor by way of a relay. The relay coil is operated with a 6-volts battery and a pushbutton switch
- Design a latching relay circuit to turn on the motor. One pushbutton (labeled “ON”) should turn on the motor and the motor should stay on after the pushbutton is released. Another pushbutton (labeled “OFF”) should turn off the motor when pressed, and the motor should stay off when the pushbutton is released.
- Explain the complete operation of the circuit in plain English language.
- Note: Recall how to make "AND" and "OR" gates with relays



Latching Relay – Extra Project

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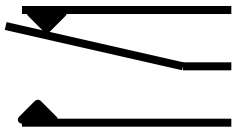

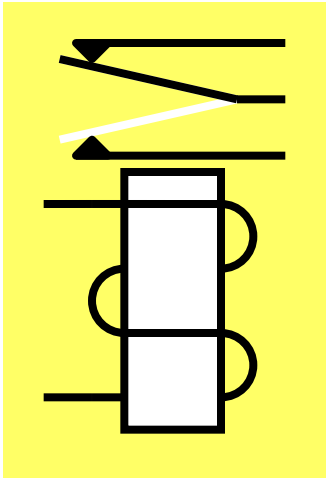

Exercises (optional)

- Redesign the debounce circuit using a NOR latch (active-high inputs) instead of a NAND latch (active-low inputs). Use any other appropriate components.

- Redesign the burglar alarm circuit using a NAND latch (active-low inputs) instead of a NOR latch (active-high inputs). Use phototransistor and any other appropriate components. (Remember, current flows in the direction of the arrow from collector and out of the emitter of the phototransistor).

(Reference: Tocci)

Summary

- **NAND and NOR latches** are specially designed logic circuits that store or **"remember" their previous state**. These latches store 1 bit of data.
- A NAND or NOR latch has **2 valid states**: either 1) Q = 1 (and Q'= 0) or 2) Q = 0 (and Q' = 1).
- The output of a NAND or NOR latch can depend on the state in the past.
- When a NAND or NOR latch is **SET**, then the Q output is equal to 1, and the Q' output is equal to 0.
- When a NAND or NOR latch is **RESET**, then the Q output is 0, and the Q' output is 1.
- The block diagram for a NAND latch has **active-low inputs** for S and R.
- The block diagram for the NOR latch has **active-high inputs** for S and R.
- A **timing diagram** is often used to show when the inputs cause a NAND or NOR latch to change states.
- The **initial condition** or initial state of a NAND or NOR (whether Q = 0 or Q = 1) latch must be provided.
- NAND and NOR latches can be used to design **switch debouncers** and **alarm** circuits. These devices are also the basis for computer memory circuits.
- NAND and NOR latches are basically **equivalent in function**, and can be used for the same applications, but the interface circuitry will be different because the NAND latch has active-low inputs and the NOR latch has active-high inputs.

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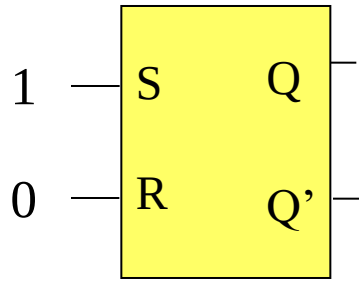
Review Questions

#1.- Given the latch circuit below, what are the outputs Q and Q`?

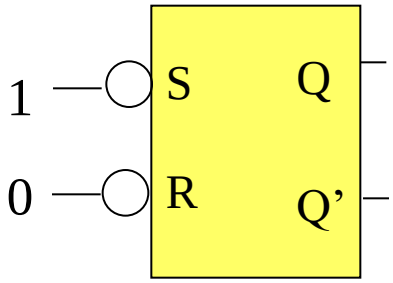


a) Q=1, Q'=1 b) Q=1, Q'=0 c) Q=0, Q'=0

d) Q=0, Q'=1 e) cannot be determined

Review Questions

#2.- Given the latch circuit below, what are the outputs Q and Q`?



a) Q=1, Q'=0 b) Q=1, Q'=1 c) Q=0, Q'=0

d) Q=0, Q'=1 e) cannot be determined

Review Questions

#3.- Given the latch circuit below and the inputs R and S, determine output Q waveform