CMPEN 271 Exam #2 Practice Problems v3
Part 2: MSI Devices; Multiplexers, Decoder, Adders, Magnitude Comparators; Addition; Multiplication; Signed Number Systems; HDL; Latches

Note: correct answer is choice "a" for every question

Contents:

Part 1. MSI Devices

A decoder is a(n)
a) MSI device b) logic gate c) flip-flop d) number system

A 3x8 decoder has how many "data" inputs?
a) 3 b) 1 c) 2 d) 8

A 3x8 decoder has how many "data" outputs?
a) 8 b) 1 c) 2 d) 3

A decoder can be used to
a) implement Boolean functions b) store information c) minimize Boolean functions d) create K-maps

A 4x16 decoder has how many data inputs?
a) 4 b) 1 c) 2 d) 16

A 4x16 decoder has how many data outputs?
a) 16 b) 4 c) 1 d) 2

Which of the following is an application of an encoder?
a) keyboard circuit b) adder c) subtractor d) demultiplexer

A 4x16 decoder can be constructed from
a) two 3x8 decoders b) two 2x4 decoders c) two 1x2 decoders d) two 4x1 multiplexers

A multiplexer is a(n)
a) MSI device b) logic gate c) flip-flop d) number system

A multiplexer can be used primarily to
a) implement Boolean functions b) store information c) reduce Boolean functions

d) act as driver to 7-segment display

A 4x1 multiplexer has how many data inputs?
a) 4 b) 3 c) 2 d) 1

A 4x1 multiplexer has how many data outputs?
a) 1 b) 2 c) 3 d) 4

A 4x1 multiplexer has how many select/control inputs?
a) 2 b) 1 c) 4 d) 8

An 8x1 multiplexer has how many data inputs?
a) 8 b) 4 c) 2 d) 1

An 8x1 multiplexer has how many data outputs?
a) 1 b) 2 c) 4 d) 8

An 8x1 multiplexer has how many select/control inputs?
a) 3 b) 1 c) 4 d) 8

A demultiplexer has the same architecture as a
a) decoder b) multiplexer c) encoder d) adder

A 1x4 demultiplexer has how many data inputs?
a) 1 b) 2 c) 3 d) 4

A 1x4 demultiplexer has how many data outputs?
a) 4 b) 3 c)2 d) 1

A 1x4 demultiplexer has how many select/control inputs?
a) 2 b) 1 c) 4 d) 8

A 4-bit adder device is also called a(n)
a) ripple adder b) multiplexed adder c) serial adder d) complex adder

A 4-bit adder chip is internally composed of
a) full-bit adders b) half-adders c) decoders d) multiplexers

The technique used to increase the speed of a 4-bit adder device is called
a) lookahead carry b) overflow c) carry bit d) integration by parts

In a digital multiplication circuit, the component used to multiply two bits together is a(n)
a) AND gate b) OR gate c) NAND gate d) XOR gate

The components of a combinational multiplication circuit primarily consist of

a) AND gates and adders b) OR gates and decoders c) XOR gates and multiplexers d) NAND gates and encoders

An ALU MSI device is a(n)
a) arithmetic logic unit b) adder logic unit c) asynchronous logic unit d) average level unit

What outputs are generated by the decoder circuit below?

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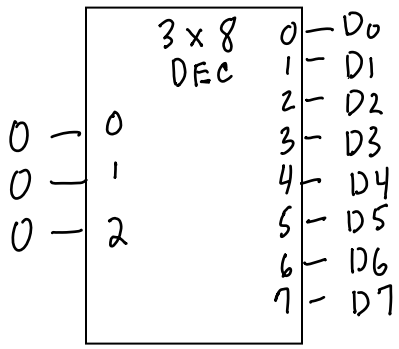

a) D0=1, D1=0, D2=0, D3=0, D4=0, D5=0, D6=0, D7=0
b) D0=0, D1=0, D2=0, D3=0, D4=0, D5=0, D6=0, D7=0
c) D0=1, D1=1, D2=1, D3=1, D4=1, D5=1, D6=1, D7=1
d) D0=0, D1=1, D2=1, D3=1, D4=1, D5=1, D6=1, D7=1

What outputs are generated by the decoder circuit below?

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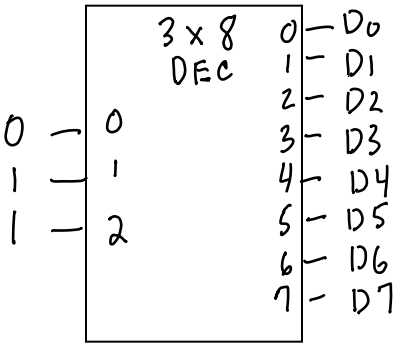

a) D0=0, D1=0, D2=0, D3=0, D4=0, D5=0, D6=1, D7=0
b) D0=0, D1=0, D2=0, D3=1, D4=0, D5=0, D6=0, D7=0
c) D0=0, D1=0, D2=1, D3=1, D4=0, D5=0, D6=0, D7=0
d) D0=1, D1=1, D2=1, D3=0, D4=1, D5=1, D6=1, D7=1
e) D0=1, D1=1, D2=1, D3=1, D4=1, D5=1, D6=0, D7=1

What outputs are generated by the decoder circuit below?

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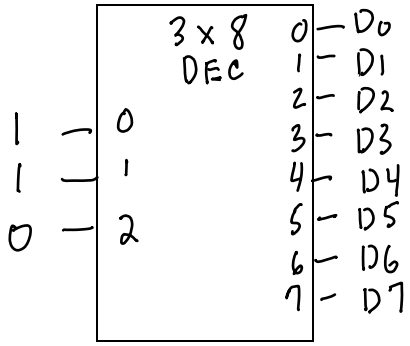

a) D0=0, D1=0, D2=0, D3=1, D4=0, D5=0, D6=0, D7=0
b) D0=0, D1=0, D2=0, D3=1, D4=0, D5=0, D6=0, D7=0
c) D0=0, D1=0, D2=0, D3=1, D4=0, D5=0, D6=1, D7=0
d) D0=1, D1=1, D2=1, D3=0, D4=1, D5=1, D6=1, D7=1
e) D0=1, D1=1, D2=1, D3=0, D4=1, D5=1, D6=1, D7=1

What outputs are generated by the decoder circuit below?

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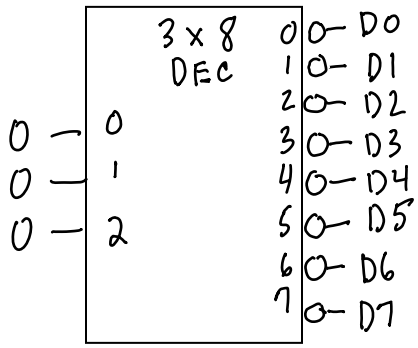

a) D0=0, D1=1, D2=1, D3=1, D4=1, D5=1, D6=1, D7=1
b) D0=0, D1=0, D2=0, D3=0, D4=0, D5=0, D6=0, D7=0
c) D0=1, D1=1, D2=1, D3=1, D4=1, D5=1, D6=1, D7=1
d) D0=1, D1=0, D2=0, D3=0, D4=0, D5=0, D6=0, D7=0

What outputs are generated by the decoder circuit below?

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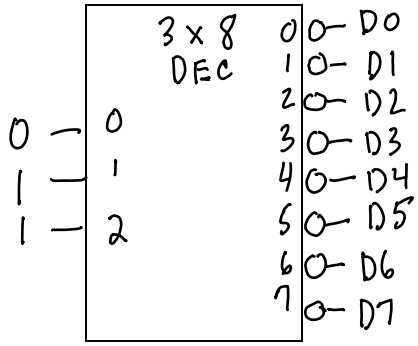

a) D0=1, D1=1, D2=1, D3=1, D4=1, D5=1, D6=0, D7=1
b) D0=1, D1=1, D2=1, D3=0, D4=1, D5=1, D6=1, D7=1
c) D0=1, D1=1, D2=1, D3=1, D4=1, D5=1, D6=1, D7=1
d) D0=0, D1=0, D2=0, D3=0, D4=0, D5=0, D6=1, D7=0

What outputs are generated by the decoder circuit below?

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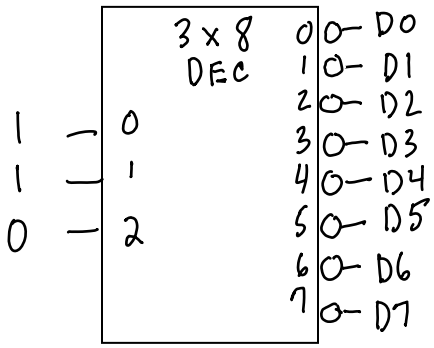
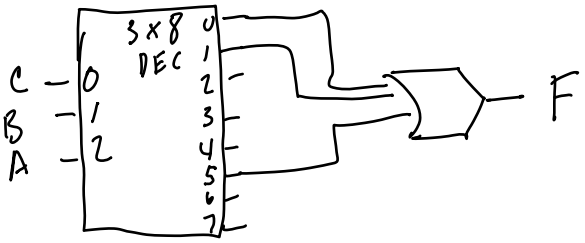


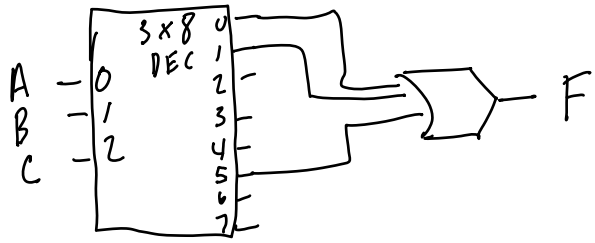
a) D0=1, D1=1, D2=1, D3=0, D4=1, D5=1, D6=1, D7=1
b) D0=1, D1=1, D2=1, D3=1, D4=1, D5=1, D6=0, D7=1
c) D0=1, D1=1, D2=1, D3=1, D4=1, D5=1, D6=1, D7=1
d) D0=0, D1=0, D2=0, D3=0, D4=0, D5=0, D6=1, D7=0

What function is implemented by the decoder circuit below?



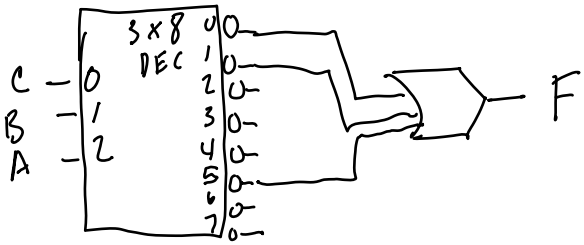
a) F(A,B,C = ∑m(0, 1, 5) b) F = 0 c) F = 1 d) F(A,B,C) = ∑m(1, 2, 6)

What function is implemented by the circuit below?



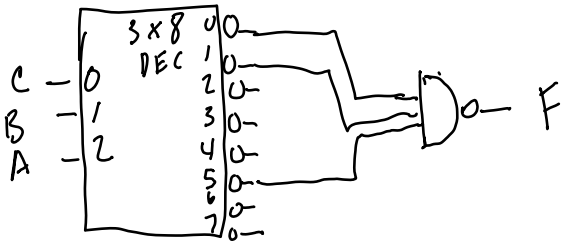
a) F(A,B,C) = ∑m(0, 4, 5) b) F = 0 c) F = 1 d) F(A,B,C) = ∑m(0, 1, 5)

What function is implemented by the circuit below?



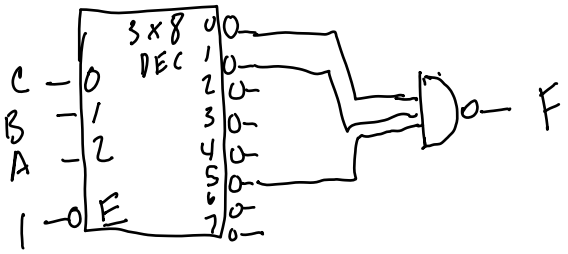
a) F = 1 b) F(A,B,C) = ∑m(0, 1, 5) c) F = 0 d) F(A,B,C) = ∑m(2,3,4,6,7)

What function is implemented by the circuit below?



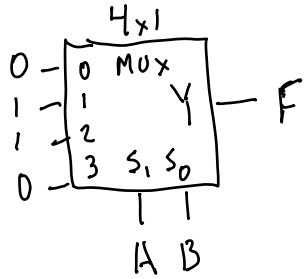
a) F(A,B,C) = ∑m(0, 1, 5) b) F = 0 c) F = 1 d) F(A,B,C) = ∑m(2,3,4,6,7)

What function is implemented by the circuit below?



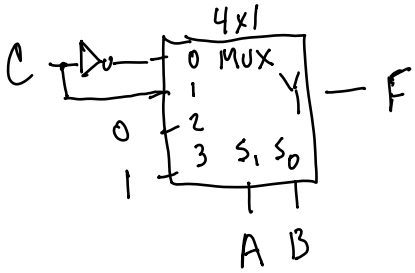
a) F = 0 b)F(A,B,C) = ∑m(0, 1, 5) c) F = 1 d) F(A,B,C) = ∑m(2,3,4,6,7)

What function is implemented by the multiplexer circuit below?



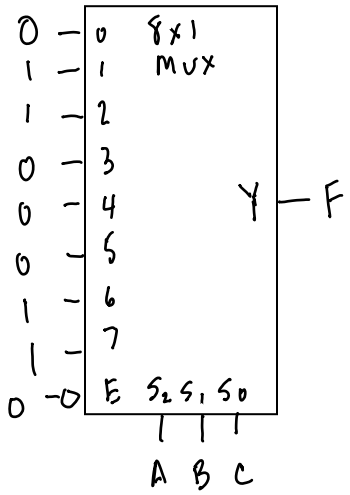
a) F(A,B) = ∑m (1, 2) b) F(A,B) = ∑m (0, 3) c) F = 0 d) F = 1

What function is implemented by the circuit below?



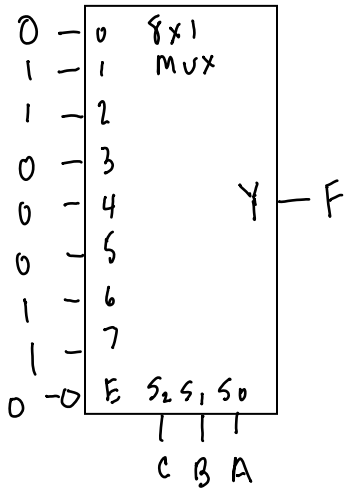
a) F(A,B,C) = ∑m (0,3,6,7) b) F(A,B,C) = ∑m (0, 1) c) F = 0 d) F = 1

What function is implemented by the circuit below?



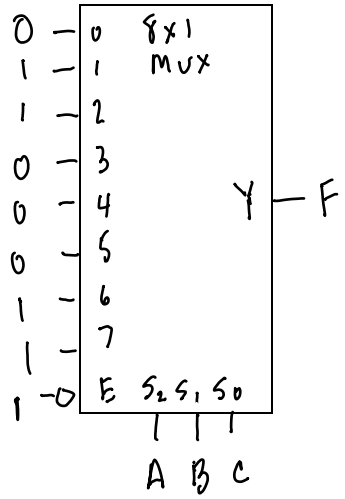
a) F(A,B,C) = ∑m (1,2,6,7) b) F(A,B,C) = ∑m (0,1,2) c) F = 0 d) F = 1

What function is implemented by the circuit below?



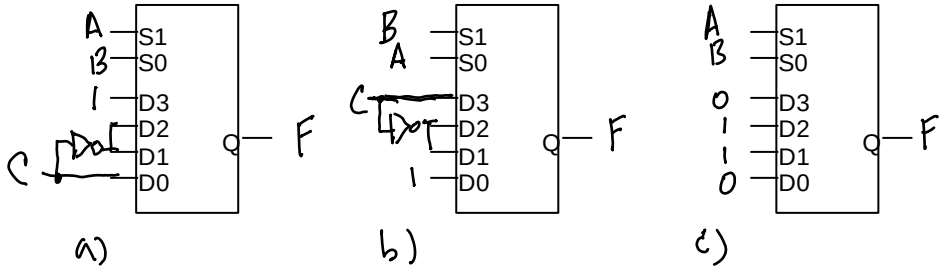
a) F(A,B,C) = ∑m (2, 3, 4, 7) b) F(A,B,C) = ∑m (1,2,6,7) c) F = 0 d)F = 1

What function is implemented by the circuit below?

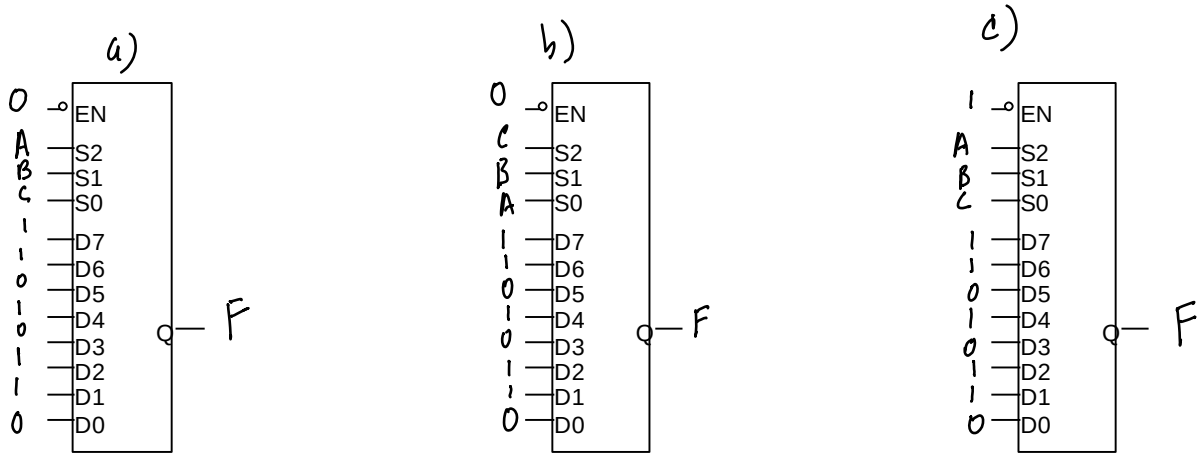


a) F= 0 b) F = ∑m (1,2,6,7) c) F = ∑m (0,1,2) d) F = 1

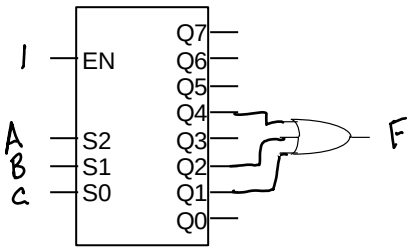
-- Implement the function F(A,B,C) = ∑m (1,2,4,6,7) on a 4x1 MUX



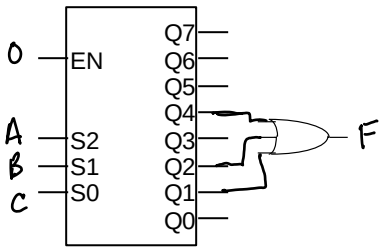
-- Implement the function F(A,B,C) = ∑m (1,2,4,6,7) on a 8x1 MUX



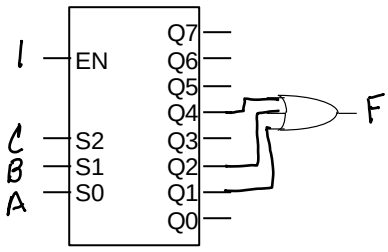
Implement the function F(A,B,C) = ∑m (1,2,4) on a 3x8 Decoder



a)

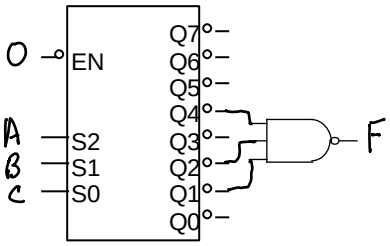


b)

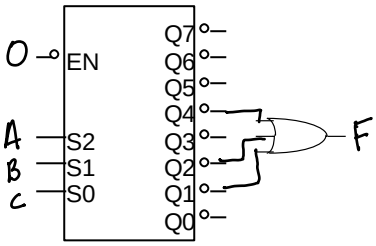


c)

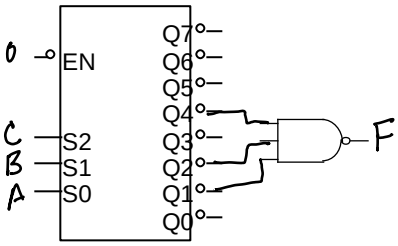
Implement the function F(A,B,C) = ∑m (1,2,4) on a 3x8 Decoder



a)

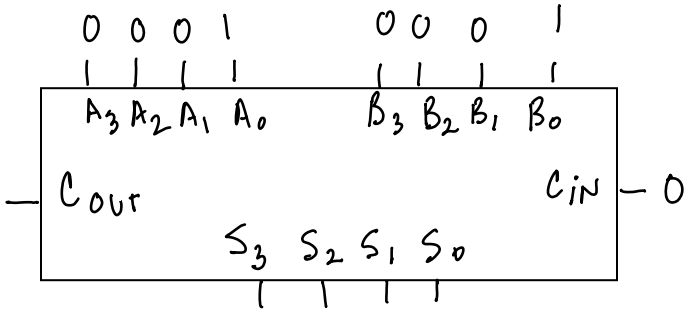


b)



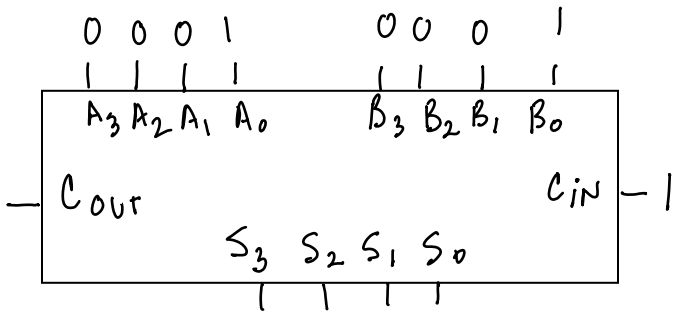
c)

What are the outputs of the following 4-bit adder circuit?



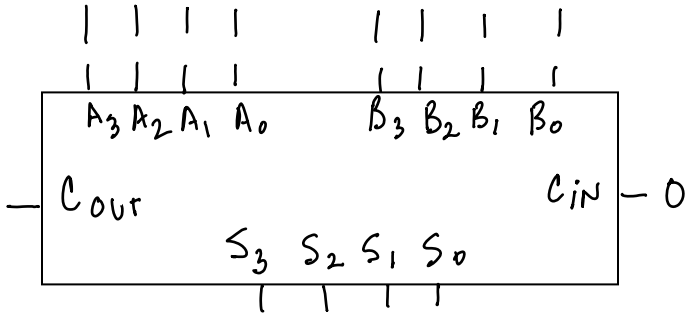
a) Cout = 0; S3=0; S2=0;S1=1; S0=0
b) Cout = 0; S3=0; S2=0;S1=1; S0=1
c) Cout = 1; S3=0; S2=0;S1=1; S0=0
d) Cout = 1; S3=0; S2=0;S1=1; S0=1

What are the outputs of the following adder circuit?



a) Cout = 0; S3=0; S2=0;S1=1; S0=1 b) Cout = 0; S3=0; S2=0;S1=1; S0=0
c) Cout = 1; S3=0; S2=0;S1=1; S0=1 d) Cout = 1; S3=0; S2=0;S1=1; S0=0

What are the outputs of the following adder circuit?



a) Cout = 1; S3=1; S2=1;S1=1; S0=0 b) Cout = 1; S3=1; S2=1;S1=1; S0=1
c) Cout = 1; S3=0; S2=0;S1=1; S0=0 d) Cout = 1; S3=0; S2=0;S1=1; S0=1

How many outputs are required for a circuit that multiplies 2, 2-bit numbers?
a) 4 b) 2 c) 3 d) 5 e) 6

How many outputs are required for a circuit that multiplies 2, 3-bit numbers?
a) 6 b) 2 c) 3 d) 4 e) 5

Part 2: Signed Number Systems

The value, -1, is represented in a 5-bit 1's complement system as
a) 11110 b) 11111 c) 00001 d) 10001

The value, -1, is represented in a 5-bit signed-magnitude system as
a) 10001 b 11111 c) 11110 d) 00001

The value, -1, is represented in a 5-bit 2's complement system as
a) 11111 b) 11110 c) 00001 d) 10001

The value, -1, is represented in a 5-bit 2's complement system in hex is
a) 1F b) 1E c) 01 d) 11

The value, +3, is represented in a 5-bit 1's complement system as
a) 00011 b) 00010 c) 10011 d) 10011

The value, +3, is represented in a 5-bit signed-magnitude system as
a) 00011 b) 00010 c) 10011 d) 10011

The value, +3, is represented in a 5-bit 2's complement system as
a) 00011 b) 00010 c) 10011 d) 10011

The value, -3, is represented in a 4-bit 1's complement system as
a) 1100 b) 1011 c) 1101 d) 1001

The value, -3, is represented in a 4-bit signed-magnitude system as
a) 1011 b) 1101 c) 1100 d) 1001

The value, -3, is represented in a 4-bit 2's complement system as
a) 1101 b) 1100 c) 1011 d) 1001

The most positive value in a 4-bit, 2's complement signed number system is
a) 7 b) 15 c) 16 d) 8

The most positive value in a 4-bit, 1's complement signed number system is
a) 7 b) 15 c) 16 d) 8

The most positive value in a 4-bit, signed-magnitude number system is
a) 7 b) 15 c) 16 d) 8

The most negative value in a 4-bit, 2's complement signed number system is
a) -8; b) -7 c) -15 d) -16

The most negative value in a 4-bit, 1's complement signed number system is
a) -7 b) -8 c) -15 d) -16

The most negative value in a 4-bit, signed-magnitude number system is
a) -7 b) -8 c) -15 d) -16

The most positive value in a 5-bit, 2's complement signed number system is
a) 15 b) 16 c) 7 d) 31

The most positive value in a 5-bit, 1's complement signed number system is
a) 15 b) 16 c) 7 d) 31

The most positive value in a 5-bit, signed-magnitude number system is
a) 15 b) 16 c) 7 d) 31

The most negative value in a 5-bit, 2's complement signed number system is
a) -16 b) -15 c) -8 d) -7

The most negative value in a 5-bit, 1's complement signed number system is
a) -15 b) -16 c) -8 d) -7

The most negative value in a 5-bit, signed-magnitude number system is
a) -15 b) -16 c) -8 d) -7

What is the binary representation of +10 in a 6-bit, 2's complement system?
a) 001010 b) 110101 c) 1010 d) 110110

What is the binary representation of +10 in a 6-bit, 1's complement system?
a) 001010 b) 110101 c) 1010 d) 110110

What is the hex representation of +10 in a 6-bit, 2's complement system?
a) 0A b) 35 c) A d) 36

What is the binary representation of -10 in a 6-bit, 2's complement system?
a) 110110 b) 110101 c) 111010 d) 101010

What is the hex representation of -10 in a 6-bit, 2's complement system?
a) 36 b) 35 c) 3A d) 2A

What is the binary representation of -10 in a 6-bit, 1's complement system?
a) 110101 b) 110110 c) 111010 d) 101010

What is the hex representation of -10 in a 6-bit, 1's complement system?
a) 35 b) 36 c) 3A d) 2A

What is the binary representation of -10 in a 6-bit, signed+magn. complement system?
a) 101010 b) 110110 c) 111010 d) 101011

What is the hex representation of -10 in a 6-bit, signed+magn. system?
a) 2A b) 36 c) 3A d) 2B

Part 3: HDL

The term "HDL" means
a) Hardware Description Language b) Hardware Description Laboratory
c) Half-adder Decoder Logic d) Hardware Decoder Language

What does the term "VHDL" mean?
a) VHSIC Hardware Description Language
b) Very High Speed Design Language
c) Very High Speed Design Laboratory
d) VHSIC Hardware Description Laboratory

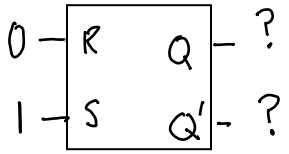
The term “ASIC” means
a) Application Specific Integrated Circuit
b) Application Speed Integrated Circuit
c) Assisted Specific Integrated Circuit
d) Auxiliary Sector Integrated

Which of the following is not a HDL?
a) MultiSim b) VHDL c) Verilog

MultiSim simulation software primarily supports
a) schematics capture b) VHDL c) ABEL d) Verilog

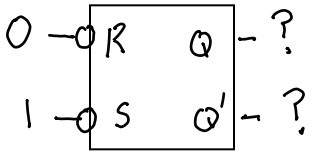
Part 4: RS (NAND and NOR) Latches

Given the latch circuit below, what are the outputs Q and Q`?



a) Q=1, Q'=0 b) Q=1, Q'=1 c) Q=0, Q'=0 d) Q=0, Q'=1 e) cannot be determined

Given the latch circuit below, what are the outputs Q and Q`?



a) Q=0, Q'=1 b) Q=0, Q'=0 c) Q=1, Q'=0 d) Q=1, Q'=1 e) cannot be determined

Given the latch circuit below and the inputs R and S, determine output Q waveform