CMPEN 271 Final Exam Practice Questions (with solutions)
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Version 1.9 (6-3-2017) Note: Be able to GENERALIZE!! Ask questions.
Note: Choice "a" is the correct answer for each question

Part 1: D FFs, shift registers and ring counters (Lecture #16)
Part 2: JK FFs; ripple counters (Lecture #17)
Part 3: Finite State Machines (FSM) with D Flip Flops (Lecture #18)
Part 4: State Machines with JK Flips flops and Applications Lecture #19)
Part 5: MSI Counters and MSI Shift Registers (Lecture #20)
Part 6: Memory Concepts (Lecture #21)

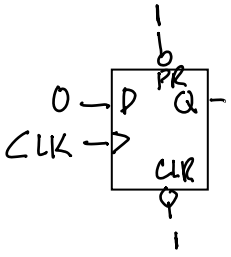
Part 1: D FFs, shift registers and ring counters

1.1.- How many bits are stored in a single D flip flop?
a) 1 b) 2 c) 3 d) 4

1.2.-When a flip-flop is "set", then the outputs of the flip-flop are
a) Q=1, Q' =0 b) Q=0, Q'=1 c) Q=0, Q'=0 d) Q=1, Q'=1

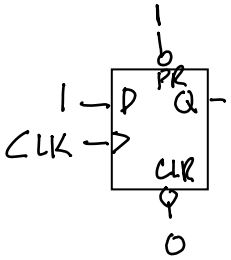
1.3.-When a flip-flop is "reset" or "cleared", then the outputs of the flip-flop are
a) Q=0, Q' =1 b) Q=1, Q'=0 c) Q=0, Q'=0 d) Q=1, Q'=1

1.4.- What is the output of this D flip-flop below after 1 clock pulse?



a) Q= 0, Q'= 1 b) Q = 0, Q' = 0 c) Q = 1, Q' = 0 d) Q = 1, Q' = 1

1.5.- What is the output of this D flip-flop below after 1 clock pulse?



a) Q= 0, Q'= 1 b) Q = 0, Q' = 0 c) Q = 1, Q' = 0 d) Q = 1, Q' = 1

1.6.- A 3-bit shift register has how many D flip-flops?

a) 3 b) 4 c) 6 d) 8

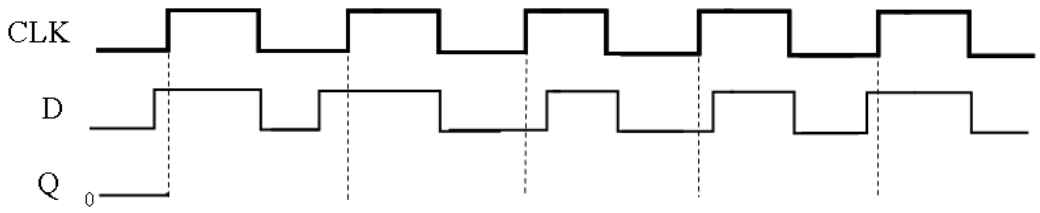
1.7.- A 3-bit ring counter has how many D flip-flops?

a) 3 b) 4 c) 6 d) 8

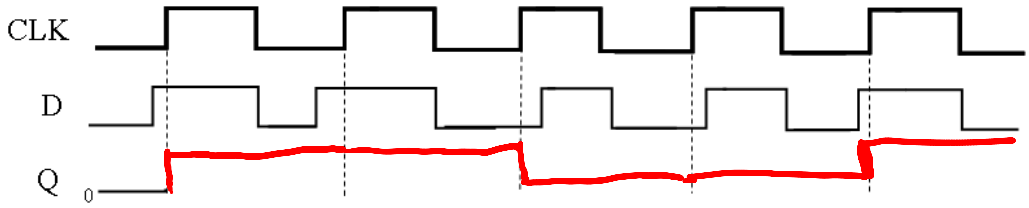
1.8.- A digital circuit which contains at least one flip-flop is called a(n)

a) sequential circuit b) combinational circuit c) analog circuit

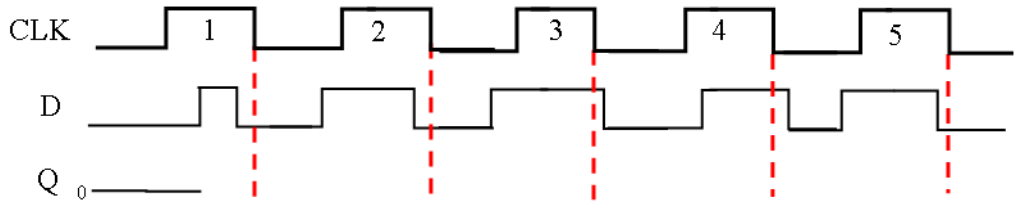
1.9.- Fill in the waveform which describes the output Q of a positive-edge triggered D flip-flop



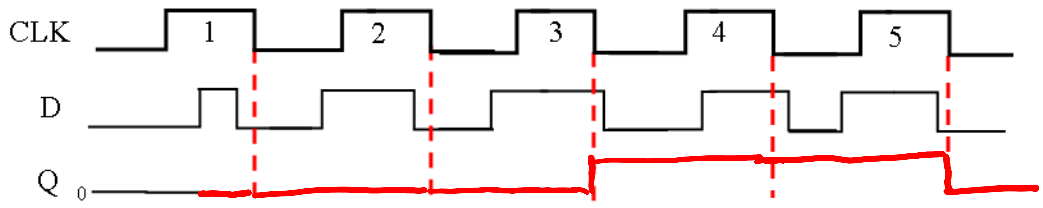
(answer)



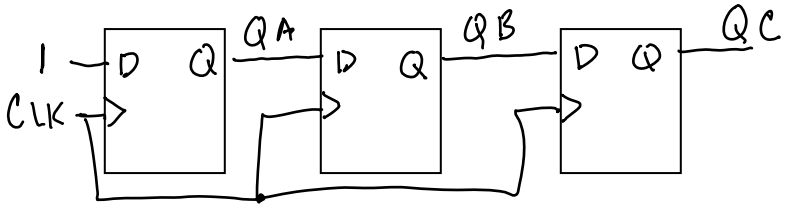
1.10.- Fill in the waveform which describes the output Q of a negative-edge triggered D flip-flop



Answer:



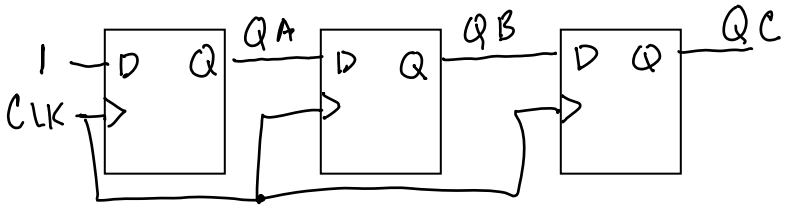
1.11.- Consider the shift register below. Assume all FFs are initially set to 0.



What are the FF outputs after 1 clock pulse?

a) QA=1, QB = 0, QC=0 b) QA=0, QB = 0, QC=0
c) QA=1, QB = 1, QC=0 d) QA=1, QB = 1, QC=1

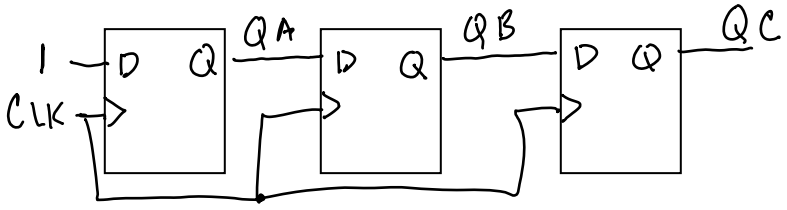
1.12.- Consider the shift register circuit below. Assume all FFs are initially set to 0.



1.13.- What are the FF outputs after 2 clock pulses?

a) QA=1, QB = 1, QC=0 b) QA=0, QB = 0, QC=0
c) QA=1, QB = 1, QC=0 d) QA=1, QB = 1, QC=1

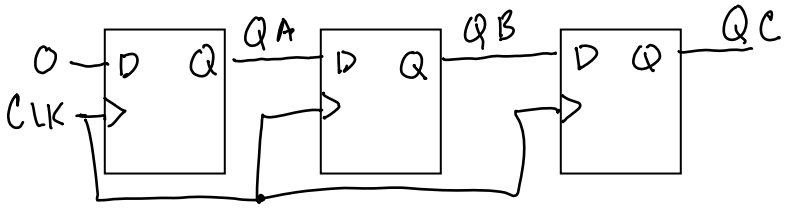
1.14.- Consider the shift register circuit below. Assume all FFs are initially set to 0.



What are the FF outputs after 10 clock pulses?

a) QA=1, QB = 1, QC=1 b) QA=0, QB = 0, QC=0
c) QA=0, QB = 1, QC=0 d) QA=0, QB = 1, QC=1

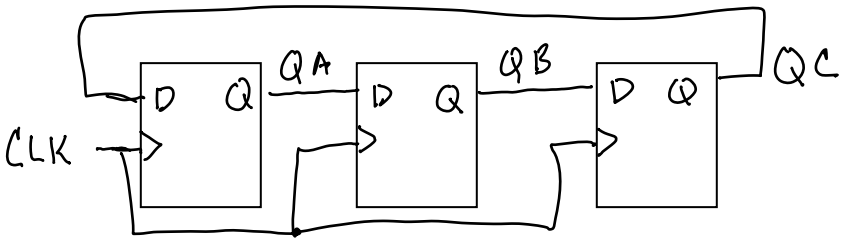
1.15.- Consider the shift register circuit below. Assume all FFs are initially set to 1.



What are the FF outputs after 2 clock pulses?

a) QA=0, QB=0, QC=1 b) QA=1, QB = 1, QC=0
c) QA=0, QB=1, QC=1 d) QA=0, QB = 1, QC=1

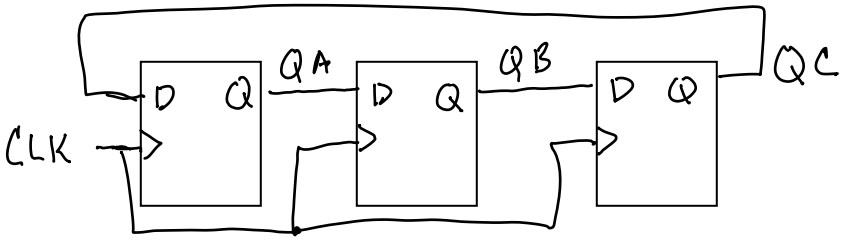
1.16.- Consider the ring counter below. Assume initially QA=1, QB=0, QC=0.



What are the FF outputs after 1 clock pulse?

a) QA=0, QB = 1, QC=0 b) QA=0, QB = 0, QC=0
c) QA=1, QB = 0, QC=0 d) QA=1, QB = 1, QC=1

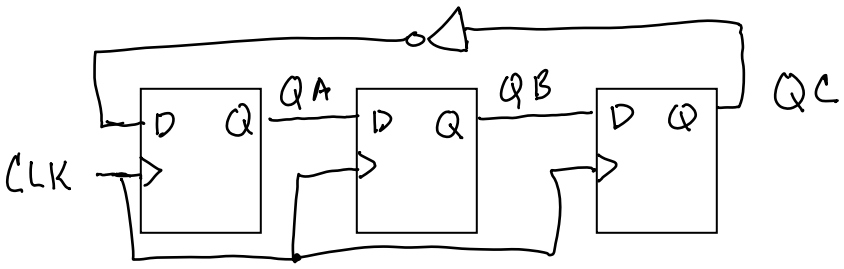
1.17.- Consider the ring counter below. Assume initially QA=1, QB=0, QC=0.



What are the FF outputs after 3 clock pulses?

a) QA=1, QB = 0, QC=0 b) QA=0, QB = 1, QC=0
c) QA=0, QB = 0, QC=1 d) QA=1, QB = 1, QC=1

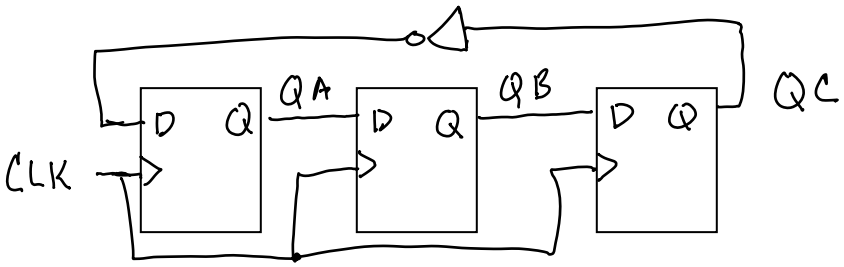
1.18.- Consider the "twisted" ring counter below. Assume initially QA=1, QB=0, QC=0.



What are the FF outputs after 1 clock pulse?

a) QA=1, QB = 1, QC=0 b) QA=0, QB = 0, QC=0
c) QA=1, QB = 0, QC=0 d) QA=1, QB = 1, QC=1

1.19.- Consider the "twisted" ring counter below. Assume initially QA=1, QB=0, QC=0.



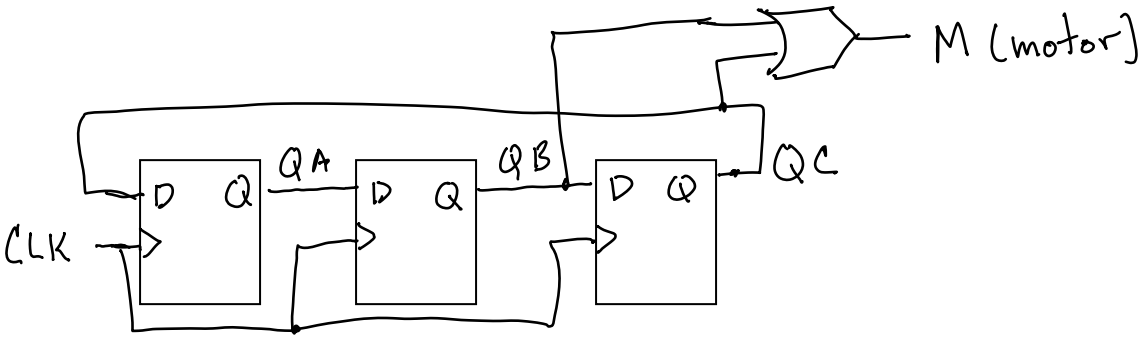
1.20.- What are the FF outputs after 2 clock pulses?

a) QA=1, QB = 1, QC=1 b) QA=0, QB = 0, QC=0
c) QA=1, QB = 1, QC=0 d) QA=1, QB = 1, QC=1

1.21.- A digital circuit which contains no flip-flop or memory elements is called a(n)

a) combinational circuit b) sequential circuit c) analog circuit

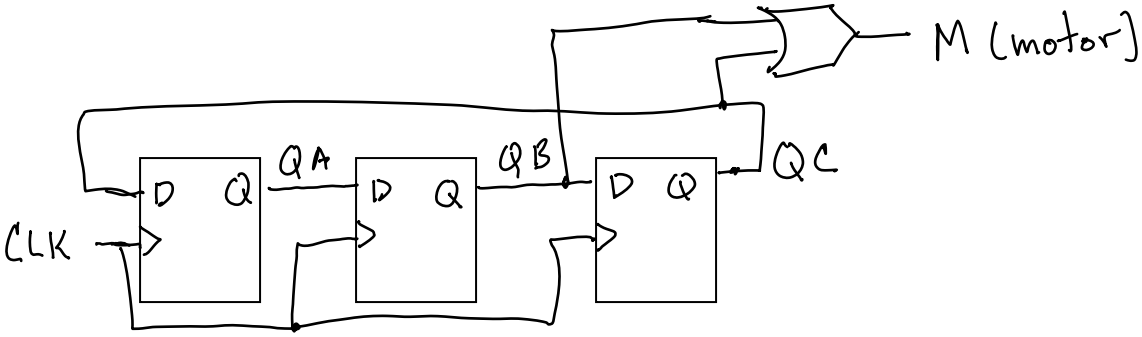
1.22.- Consider the ring counter circuit below. Assume initially QA=1, QB=0, QC=0.



How would you describe the behavior of the motor output M?

a) M is on for 2 seconds, off for 1 second, then repeat
b) M is on for 3 seconds, off for 1 second, then repeat
c) M is on for 1 second, off for 2 seconds, then repeat
d) M is always on
e) M is always off

1.23.- Consider the ring counter circuit below. Assume initially QA=1, QB=1, QC=0.



How would you describe the behavior of the motor output M? (Be careful with initial conditions)

a) M is always on
b) M is on for 2 seconds, off for 1 second, then repeat
c) M is on for 3 seconds, off for 1 second, then repeat
d) M is on for 1 second, off for 2 seconds, then repeat
e) M is always off

Part 2: JK FFs; ripple counters

2.1.- How many bits are stored in a single JK flip flop?
a) 1 b) 2 c) 3 d) 4

2.2.- To place a JK flip-flop in "toggle" mode, the data inputs should be
a) J=1, K=1 b) J=0, K=0 c) J=0, K=1 d) J=1, K=0

2.3.- To "set" a JK flip-flop, the inputs should be (assuming initial Q is unknown)
a) J=1, K=0 b) J=0, K=0 c) J=0, K=1 d) J=1, K=1

2.4.- To "reset" or "clear" a JK flip-flop, the inputs should be (assuming initial Q is unknown)
a) J=0, K=1 b) J=0, K=0 c) J=1, K=0 d) J=1, K=1

2.5.- If J=1 and K=1 for a JK flip-flop and the initial Q = 0, what are the outputs after one clock pulse?
a) Q = 1, Q' = 0 b) Q = 0, Q' = 0 c) Q = 1, Q' = 1 d) Q = 0, Q' = 1

2.6.- If J=1 and K=1 for a JK flip-flop and the initial Q = 0, what is output after two clock pulses?
a) Q = 0, Q' = 1 b) Q = 0, Q' = 0 c) Q = 1, Q' = 1 d) Q = 1, Q' = 0

2.7.- A 3-bit ripple counter uses how many JK flip-flops?
a) 3 b) 2 c) 4 d) 8

2.8.- A 3-bit ripple counter has a count sequence of
a) 0 to 7 b) 0 to 8 c) 0 to 3 d) 1 to 4

2.9.- A 3-bit ripple counter is also known as a
a) MOD-8 counter b) MOD-4 counter c) MOD-3 counter d) MOD-16 counter

2.10.- A 3-bit ripple counter is also known as a
a) divide-by-8 counter b) divide-by-4 counter c) divide-by-3 counter
d) divide-by-16 counter

2.11.- A MOD-9 ripple counter has a count sequence of
a) 0 to 8 b) 0 to 9 c) 0 to 3 d) 0 to 10

2.12.- A MOD-9 ripple counter requires how many JK flip-flops?
a) 4 b) 3 c) 2 d) 5

2.13.- When you design a MOD-9 ripple counter with JK flips-flops, at what number do you active the reset for all of the flip-flops?
a) 9 b) 8 c) 10 d) 11 e) 16

2.14.- If the clock input to a 3-bit ripple counter is 1KHz, then the frequency of the lsb of the counter is
a) 500Hz b) 1KHz c) 250Hz d) 125Hz

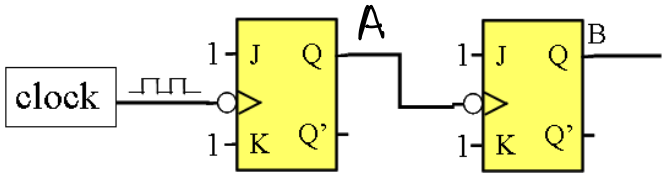
2.15.- If the clock input to a 3-bit ripple counter is 1KHz, then the frequency of the msb of the counter is
a) 125Hz b) 1KHz c) 250Hz d) 500Hz

2.16.- If the clock input to a 5-bit ripple counter is 32 KHz, then the frequency of the lsb of the counter is
a) 16Hz b) 32KHz c) 1KHz d) 500Hz

2.17.- If the clock input to a 5-bit ripple counter is 32 KHz, then the frequency of the msb of the counter is
a) 1KHz b) 8KHz c) 16KHz d) 32KHz

2.18.- A ripple counter is a(n) _____ circuit.
a) asynchronous b) synchronous c) combinational d) MSI

Consider the ripple counter circuit below



2.19.- What is the MOD of the ripple counter above?
a) MOD 4 b) MOD 2 c) MOD 3 d) MOD 8

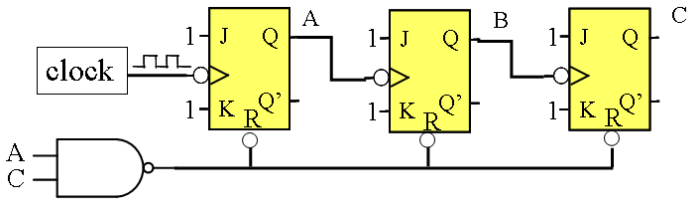
2.20.- What is the count sequence of the ripple counter above?
a) 0 to 3 b) 1 to 4 c) 1 to 3 d) 0 to 7 e) 0 to 1

2.21.- How many states does the ripple counter above contain?
a) 4 b) 2 c) 3 d) 5 e) 8

2.22.- What is the least significant bit of the ripple counter above?
a) A b) B

2.23.- What is the most significant bit of the counter above?
a) B b) A

Consider the ripple counter circuit below:



2.24.- How many FFs are contained in the circuit above?
a) 3 b) 2 c) 4 d) 8

2.25.- What is the MOD of the ripple counter above?
a) MOD 5 b) MOD 2 c) MOD 3 d) MOD 8

2.26.- What is the count sequence of the ripple counter above?
a) 0 to 4 b) 1 to 4 c) 1 to 5 d) 0 to 5 e) 0 to 1

2.27.- How many states does the ripple counter above contain?
a) 5 b) 2 c) 4 d) 6 e) 8

2.28.- What is the least significant bit of the ripple counter above?
a) A b) B c) C

2.29.-What is the most significant bit of the counter above?
a) C b) A c) B

2.30.- A MOD-50 ripple counter has a count sequence of
a) 0 to 49 b) 0 to 50 c) 1 to 49 d) 0 to 5

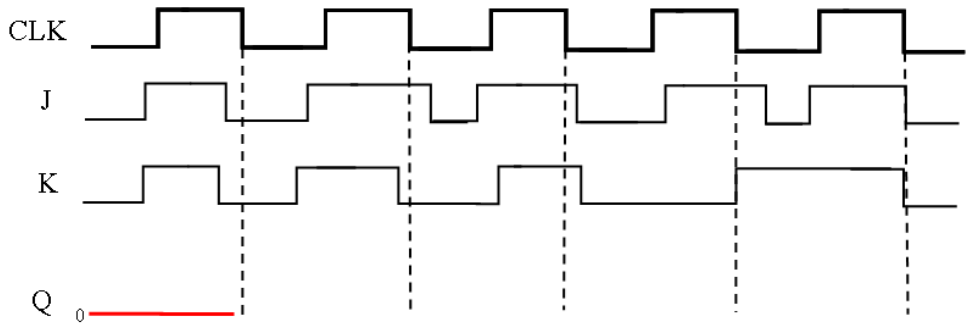
2.31.- A MOD-50 ripple counter has how many JK flip-flops?
a) 6 b) 5 c) 4 d) 7 e) 50

2.32.- If you want to design a ripple counter with a count sequence of 0 to 75, on what count would you reset all of the FFs to zero?
a) 76 b) 74 c) 75 d) 73

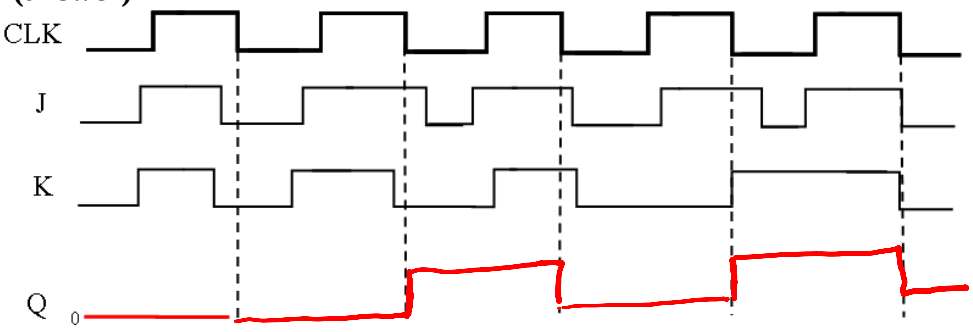
2.33.- A ripple counter with a count sequence of 0 to 75 would correspond to what MOD?
a) 76 b) 74 c) 75 d) 77

2.34.- Ripple counters are referred to as “asynchronous” circuits because…
a) not every JK flip-flop is connected directly to the master clock
b) each JK flip-flop has a reset input
c) each JK flip-flop is in toggle mode

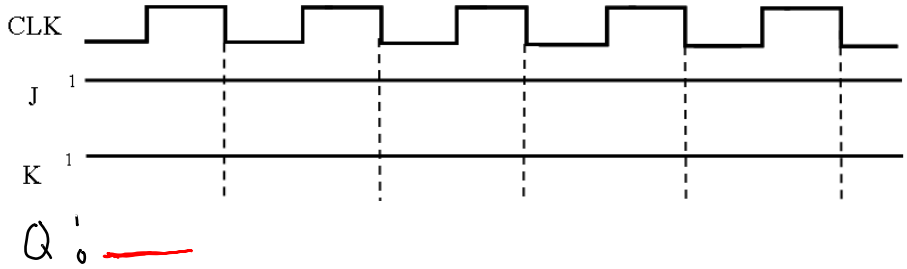
2.35.- Fill in the waveform for the output Q of a negative-edge triggered FF



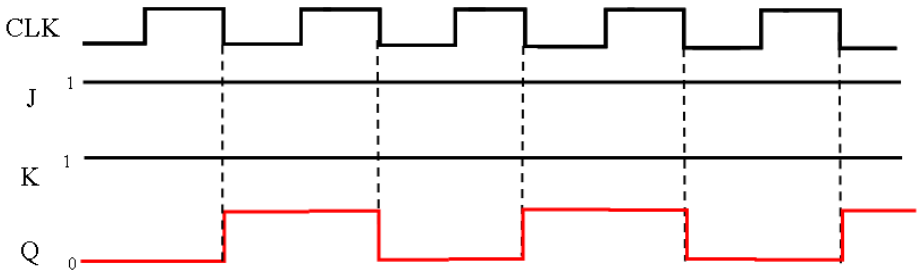
(answer)



2.36.- Fill in the waveform for the output Q of a negative-edge triggered FF



(answer)



Part 3: Finite State Machines (FSM)

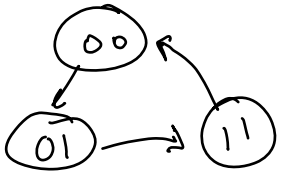
3.1 A "synchronous" circuit means that every FF in the circuit is
a) directly connected to master clock b) a D FF c) is a JK FF d) has a reset
e) is positive-edge triggered

3.2 Every sequential circuit is synchronous.
a) false b) true

3.3 Every synchronous circuit is sequential.
a) true b) false

3.4 A state machine is a(n) _____ circuit.
a) synchronous b) asynchronous c) combinational d) analog

3.5 Consider the following state diagram.



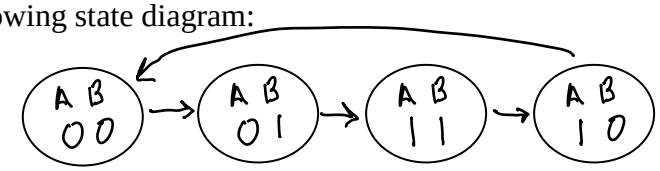
3.6 How many states are represented in the state diagram above?
a) 3 b) 1 c) 2 d) 5

3.8.How many FFs (minimum) would be required to implement the state diagram above?
a) 2 b) 1 c) 3 d) 4

3.9 How many external inputs are represented in the state diagram above?
a) 0 b) 1 c) 2 d) 3

3.10 How many unused states are represented in the state diagram above?
a) 1 b) 0 c) 2 d) 3

Consider the following state diagram:



3.11 How many states are represented in the state diagram above?
a) 4 b) 1 c) 2 d) 3 e) 5

3.12 How many FFs (min) would be required to implement the state diagram above?
a) 2 b) 1 c) 3 d) 4

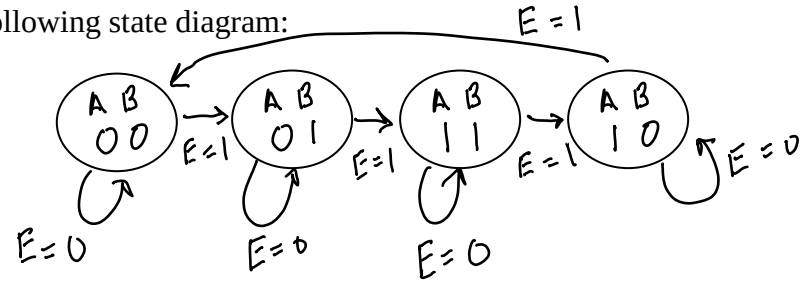
3.13 How many external inputs are represented in the state diagram above?
a) 0 b) 1 c) 2 d) 3

3.14 How many unused states are represented in the state diagram above?
a) 0 b) 1 c) 2 d) 3

3.15 What is the FF input equation DA represented in the state diagram above?
a) DA = B b) DA = A c) DA = AB d) DA = 0 e) DA = 1

3.16 What is the FF input equation DB represented in the state diagram above?
a) DB = A' b) DB = A c) DB = B d) DB = 0 e) DB = 1

Consider the following state diagram:

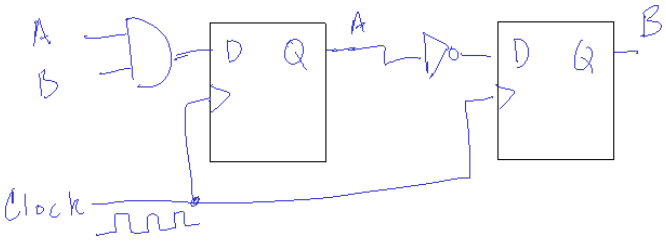


3.17 How many external inputs are represented in the state diagram above?
a) 1 b) 0 c) 2 d) 3

3.18 Assume initially A=1, B=1. What is value of A, B after 3 clock pulses? Let input E=1.
a) A=0, B=1 b) A= 0, B=0 c) A=1, B=0 d) A=1, B=1

3.19 Assume initially A=1, B=0. What is value of A, B after 3 clock pulses? Let input E=0.
a) A=1, B=0 b) A= 0, B=0 c) A=0, B=1 d) A=1, B=1

Consider the state machine below:



3.20 What is the flip-flop equation for flip-flop A?

a) DA = AB b) DA = A' c) DA = Clock d) DA = A

3.21 What is the flip-flop equation for flip-flop B?

a) DB = A' b) DA = AB c) DB = Clock d) DB = A

3.22 Draw the state table for state machine circuit above.

a)

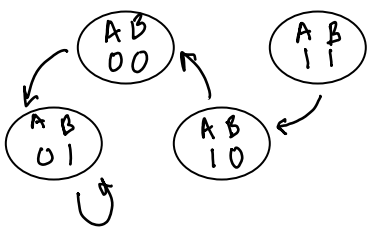
P. S.		N. S.	
A	B	A	B
0	0	0	1
0	1	0	1
1	0	0	0
1	1	1	0

b)

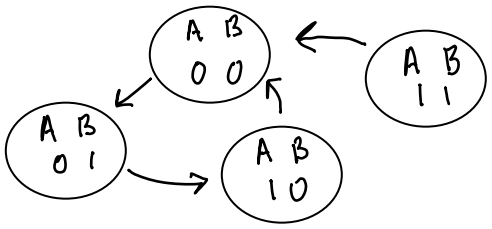
P. S.		N. S.	
A	B	A	B
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	0

3.23 Draw the state table for state machine circuit above.

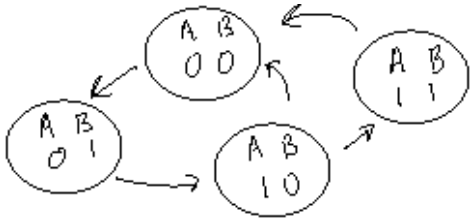
a)



b)



c)

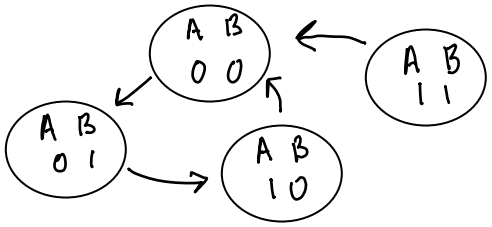


Consider the state table below

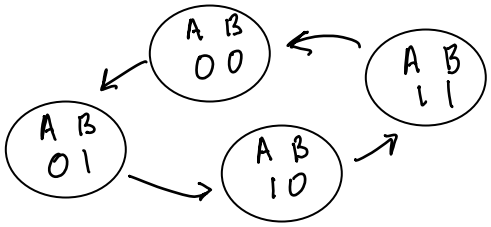
P.S.		N.S.	
A	B	A	B
0	0	0	1
0	1	1	0
1	0	0	0
1	1	0	0

3.24 Choose the state diagram which corresponds to the state table above:

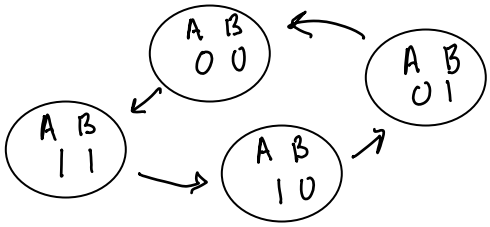
a)



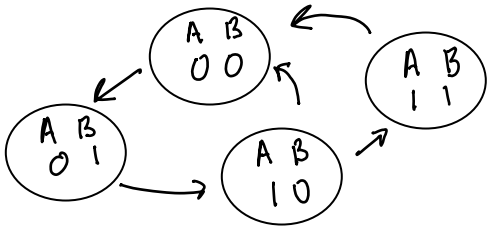
b)



c)



d)



3.25 What are the FF input equations for the state table above?

a) DA = A'B; DB = A'B'
b) DA = A'B'; DB = A'B
c) DA = AB'; DB = 0
d) DA = 0; DB = A'B

Part 4: FSM with JK Flip Flops and Applications

Consider the following state table for a FSM using JK flip-flops

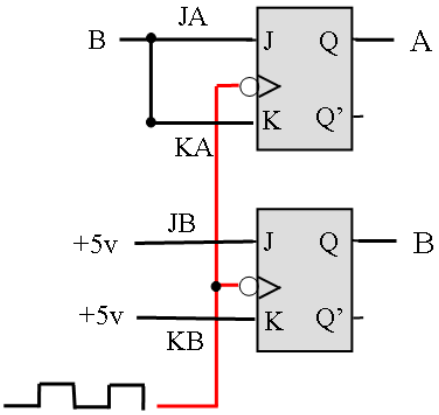
Present State		Next State		FF input eq's			
A	B	A	B	JA	KA	JB	KB
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1

3.26 How many flip-flops are represented in above state diagram?
a) 2 b) 3 c) 4 d) 5

3.27 What is the flip-flop input equation for flip-flop A?
a) JA=B, KA=B b) JA =AB, KA=B c) JA=0, KA=B d) JA=1, KA=1

3.28 What is the flip-flop input equation for flip flop B?
a) JB=1, KB=1 b) JB =A, KB=B c) JB=0, KB=B d) JB=A, KB=1

3.29 Consider the state machine below designed with JK flip-flops?

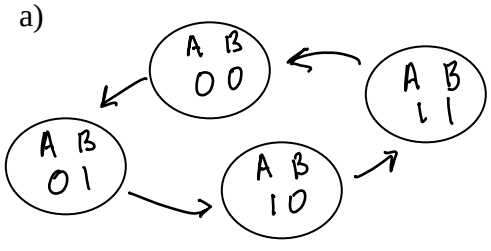


3.20 What is the flip-flop input equation for flip-flop A?
a) JA=B, KA=B b) JA =AB, KA=B c) JA=0, KA=B d) JA=1, KA=1

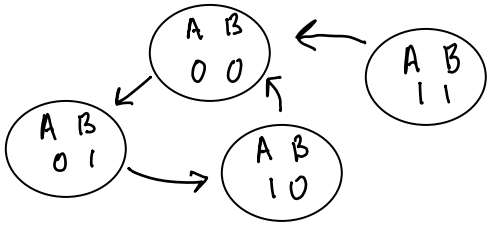
3.21 What is the flip-flop input equation for flip flop B?
a) JB=1, KB=1 b) JB =A, KB=B c) JB=0, KB=B d) JB=A, KB=1

3.22 Draw the state diagram for the circuit above

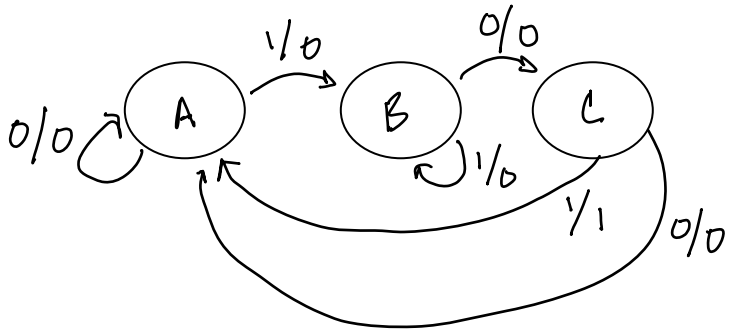
a)



b)



Consider the following state diagram for a binary sequence detector.



3.23 In the state machine form above, the notation "x/y" denotes
a) x is an input and y is an output b) x is an input and y is an input
c) x is an output and y is an output d) x is divided by y

3.24 What does the symbol "0/1" mean in a state diagram?
a) if the input = 0 then set the output = 1 and make the state transition
b) if the input = 1 then set the output = 0 and make the state transition
c) if the input = 0 then set the output = 0 and make the state transition

3.25 What does the symbol "1/0" mean in a state diagram?
a) if the input = 1 then set the output = 0 and make the state transition
b) if the input = 0 then set the output = 1 and make the state transition
c) if the input = 0 then set the output = 0 and make the state transition

3.26 What binary sequence is detected in the FSM above? That is, starting at state A, what sequence of bits will produce an output of 1?
a) 101 b) 111 c) 1011 d) 0100 e) 110

3.27 Initially the state machine is in state A. What is the output of this circuit if the input sequence = 001010 ?
a) 000010 b) 001010 c) 000011 d) 000111

3.28 Initially the state machine is in state A. What is the output of this circuit if the input sequence = 00000 ?
a) 00000 b) 00101 c) 000011 d) 000111

3.29 Initially the state machine is in state A. What is the output of this circuit if the input sequence = 11111 ?
a) 00000 b) 11111 c) 000011 d) 000111

3.20 Initially the state machine is in state A. What is the output of this circuit if the input sequence = 10110101
a) 00100100 b) 00100000 c) 11111101 d) 00000010

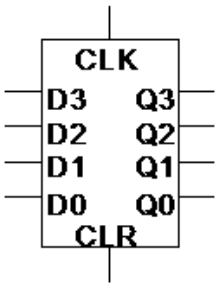
3.21 How many states does the state diagram for the sequence detector above contain?
a) 3 b) 2 c) 4 d) 5 e) 6

3.22 How many flip-flops (minimum) are necessary to implement the circuit above?

a) 2 b) 1 c) 3 d) 4 e) 8

Part 5: MSI Counters and MSI Shift Registers

Consider the following circuit (fig. 4.0)



4.1 What type of MSI device is depicted above (fig 4.0)?

a) register b) counter c) decoder d) multiplexer e) ripple counter

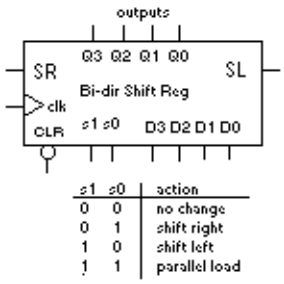
4.2 How many flip-flops are contained within the device above (fig 4.0)?

a) 4 b) 2 c) 3 d) 5 e) 8

4.3 How many bits are stored in the device above (fig 4.0)?

a) 4 b) 2 c) 3 d) 5 e) 8

Given the bi-directional shift register below (fig 4.1),



s1	s0	action
0	0	no change
0	1	shift right
1	0	shift left
1	1	parallel load

SR -> Q3 -> Q2 -> Q1 -> Q0

Q3 <- Q2 <- Q1 <- Q0 <- SL

4.3 How many flip-flops are contained in the device above (fig 4.1)?

a) 4 b) 3 c) 5 d) 6 e) 8

4.5 In Fig. 4.1, assume initially Q3= Q2 = Q1 = Q0 = 0, S1=0 and S0=1, and SR = 1, then what are the outputs after one clock pulse?

a) Q3=1, Q2=0, Q1=0, Q0=0 b) Q3=1, Q2=1, Q1=0, Q0=0

c) Q3=0, Q2=0, Q1=0, Q0=0 d) Q3=1, Q2=1, Q1=1, Q0=1

4.6 In Fig. 4.1, assume initially Q3= Q2 = Q1 = Q0 = 0, S1=0 and S0=1, and SR = 1, then what are the outputs after two clock pulses?

a) Q3=1, Q2=1, Q1=0, Q0= 0 b) Q3=1, Q2=0, Q1=0, Q0= 0
c) Q3=0, Q2=0, Q1=0, Q0= 0 d) Q3=1, Q2=1, Q1=1, Q0= 1

4.7 In Fig. 4.1, assume initially Q3= Q2 = Q1 = Q0 = 0, S1=0 and S0=0, and SR = 1, then what are the outputs after two clock pulses (fig. 1)?

a) Q3=0, Q2=0, Q1=0, Q0= 0 b) Q3=1, Q2=0, Q1=0, Q0= 0
c) Q3=1, Q2=1, Q1=0, Q0= 0 d) Q3=1, Q2=1, Q1=1, Q0= 1

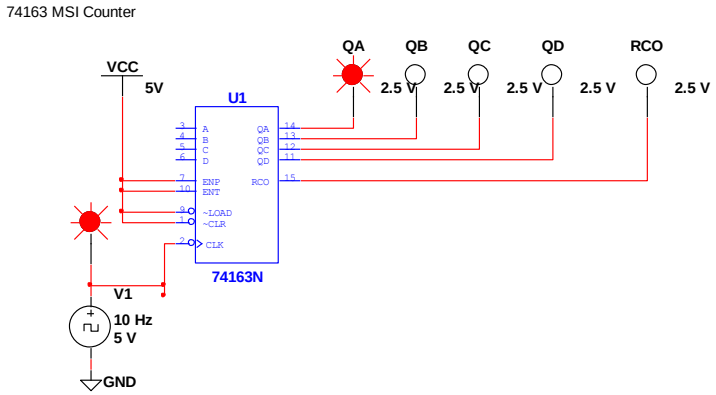
4.8 In Fig. 4.1, assume initially Q3=Q2=Q1= Q0 = 0, S1=1 and S0=0, and SL = SR = 1, then what are the outputs after two clock pulses (fig. 1)?

a) Q3=0, Q2=0, Q1=1, Q0= 1 b) Q3=1, Q2=0, Q1=0, Q0= 0
c) Q3=1, Q2=1, Q1=0, Q0= 0 d) Q3=1, Q2=1, Q1=1, Q0= 1

4.9 In Fig. 4.1, assume initially Q3= Q2 =Q1=Q0 = 1, S1=0 and S0=1, and SL = SR =0, then what are the outputs after two clock pulses (fig. 1)?

a) Q3=0, Q2=0, Q1=1, Q0= 1 b) Q3=1, Q2=0, Q1=0, Q0= 0
c) Q3=1, Q2=1, Q1=0, Q0= 0 d) Q3=1, Q2=1, Q1=1, Q0= 1

Consider the MSI 74163 counter below (fig 4.2)



4.10 How many flip-flops are contained within the MSI counter above?

a) 4 b) 2 c) 3 d) 5

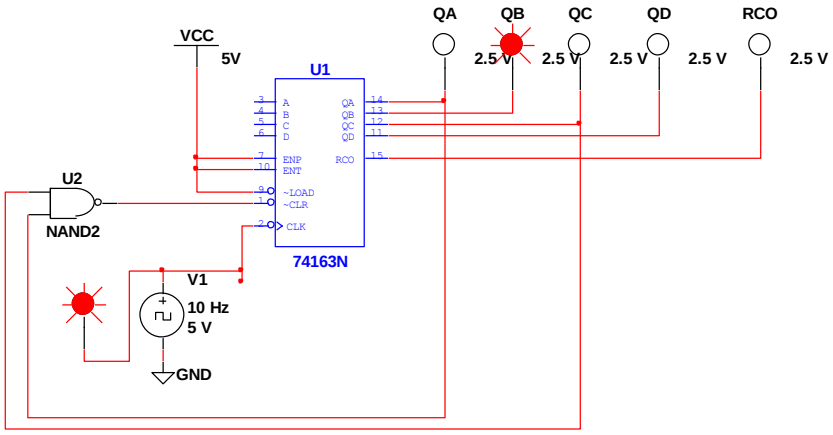
4.11 What is the count sequence of the circuit above (fig. 4.2)?

a) 0 to 15 b) 0 to 4 c) 0 to 16 d) 1 to 15 e) 0 to 31

4.12 What is the MOD of the counter above (fig. 4.2)?

a) MOD 16 b) MOD 15 c) MOD 4 d) MOD 8

Consider the MSI 74163 counter circuit diagram below (fig. 4.3)



4.13 How many flip-flops are contained within the MSI counter above (fig. 4.3)?

a) 4 b) 2 c) 3 d) 5

4.14 What is the count sequence of the circuit above (fig. 4.3)?

a) 0 to 5 b) 0 to 4 c) 0 to 6 d) 1 to 15 e) 0 to 7

4.15What is the MOD of the counter above (fig. 4.3)?

a) MOD 6 b) MOD 4 c) MOD 5 d) MOD 8

4.16 If you want to design a MOD-10 counter with a 74163 counter, at what count value do you activate the flip flop clear?

a) 9 b) 8 c) 10 d) 11 e) 16

4.17 In general, a 16-bit register has how many flip-flops?

a) 16 b) 8 c) 4 d) 2

4.18 In general, a 16-bit register can store how many bits?

a) 16 b) 8 c) 4 d) 2

Part 6: Memory Concepts

5.1 The term "RAM" means
a) random access memory b) radix arithmetic memory
c) random average memory d) raster access machine

5.2 The term "ROM" means
a) read-only memory b) random-only memory
c) read-often memory d) reset-only memory

5.3 The term "DRAM" means
a) dynamic RAM b) differential RAM c) D flip-flop RAM d) digital RAM

5.4 The term "SRAM" means
a) static RAM b) sonic RAM c) standard RAM d) synchronous RAM

5.5 The term "EPROM" means
a) erasable ROM b) electric ROM c) energy ROM d) entropy ROM

5.6 Flash memory is a type of
a) EEPROM b) SRAM c) DRAM d) EPROM

5.7 RAM memory is
a) volatile b) non-volatile

5.8 ROM memory is
a) non-volatile b) volatile

5.9 EEPROM memory is
a) non-volatile b) volatile

5.10 Flash memory is
a) non-volatile b) volatile

5.11 EPROM memory is
a) non-volatile b) volatile

5.12 SRAM memory is
a) volatile b) non-volatile

5.13 DRAM memory is
a) volatile b) non-volatile

5.14 Cache memory is generally of what type?
a) SRAM b) DRAM c) ROM d) PROM

5.15 The storage unit of SRAM consists of a(n)
a) flip-flop b) capacitor c) inductor d) electron

5.16 The storage unit of DRAM consists of a(n)
a) capacitor b) flip-flop c) inductor d) electron

5.17 Which memory technology uses UV light to erase its contents?
a) EPROM b) EEPROM c) Flash d) RAM

5.18 How many address lines are required for a 1Kx8 memory module?
a) 10 b) 8 c) 9 d) 1024

5.19 How many data lines are required for a 1Kx8 memory module?
a) 8 b) 9 c) 10 d) 16

5.20 How many address lines are required for a 64x16 memory module?
a) 6 b) 8 c) 9 d) 1

5.21 How many data lines are required for a 64x16 memory module?
a) 16 b) 6 c) 10 d) 8

5.22 How many address lines are required for a 16Kx8 memory module?
a) 14 b) 8 c) 16 d) 10

5.23 How many data lines are required for a 16Kx8 memory module?
a) 8 b) 9 c) 10 d) 16

5.24 A tri-state (or 3-state) output means
a) the output is either logic 0, logic 1, or high impedance (Z)
b) the output is a voltage between 0v and 5 v
c) there are 3 outputs

5.25 Tri-state logic supports
a) communication on a common bus
b) driving high current devices
c) high frequency counters