

Penn State Abington

CMPEN 271

Lecture Set #11

Decoders, Encoders

Video

Topics:

- Discuss HW

Video part 1 of 5 ←

- Decoder
- Circuit Simulation Demonstration
- Decoder Applications
- Decoder IC Specs

Video part 2 of 5

- Sample Decoder Exercises

Video part 3 of 5

- Encoder
- Encoder Applications

Video part 4 of 5

- Summary

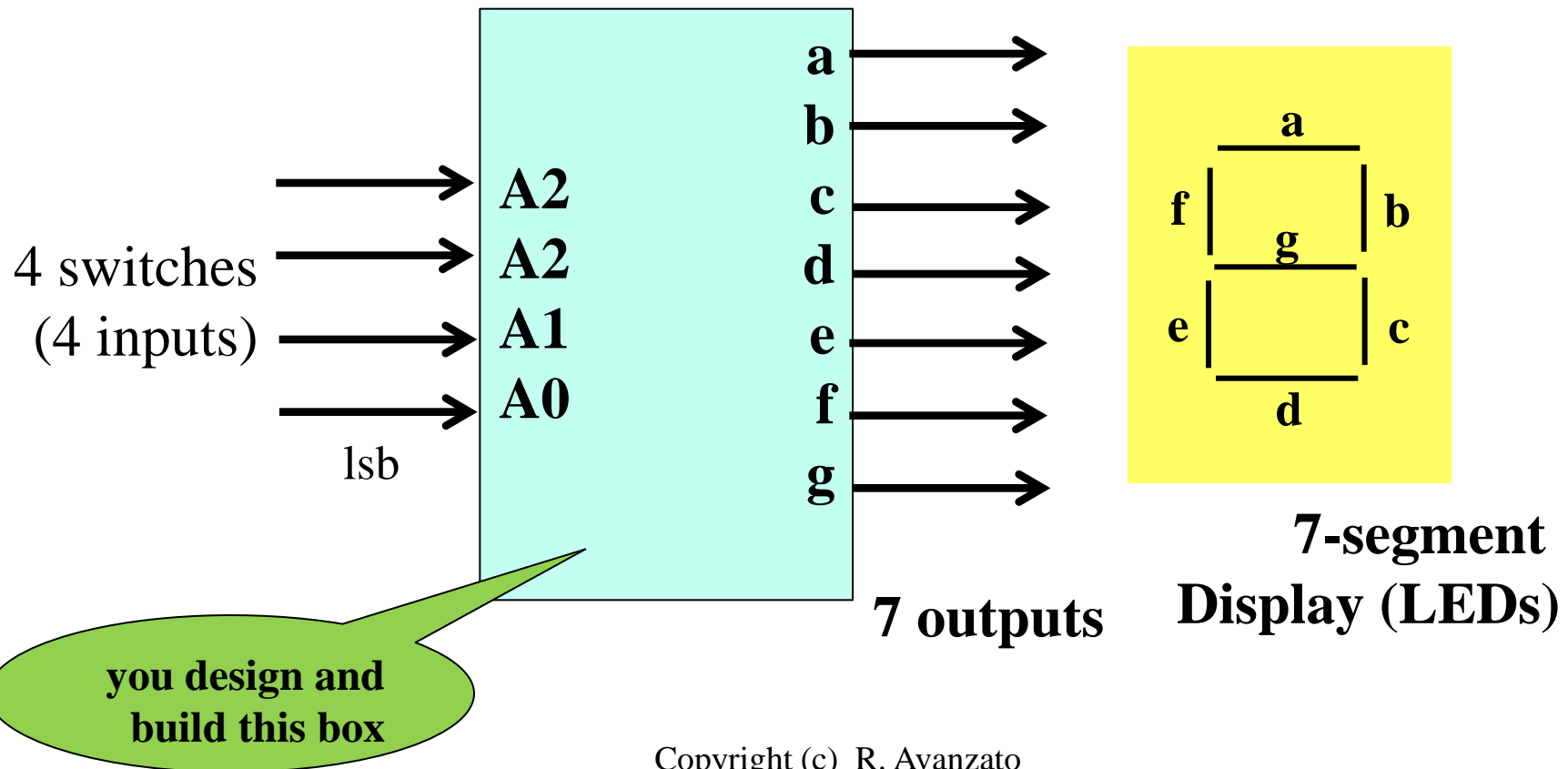
Video part 5 of 5

Discussion

- **Homework #5 (see due date)**; **BCD to 7-segment display** requires lots of thought for testing; MultiSIM;
- **Question**: How to you document and **fully test** the functional BCD to 7-segment circuit in Multisim?
 - How many test cases are needed for your solution?
 - Important HW (20 pts), Must be well organized and professional.
- Show all **K-maps and functions** clearly. Use proper labels (don't redefine/relabel inputs; use proper variables).
- Include **full truth table** Are you using don't cares?
- Include copy of **original problem** (copy and paste from PPT notes); do not include instructions on formatting.
- Include **all test cases**; clearly label each.
- **Label all input wires and output wires on MultiSim** (use text tool; Place text)

HW#5 – Block Diagram

- Block diagrams clearly show the inputs and outputs, but hide the internal details. Block diagrams give the “big picture”.
- Block diagrams are very useful when planning and designing circuits.



Discussion Forum

- Instructor has setup a general **student discussion forum** on Angel course page. Counts for 10% of final grade in CMPEN 271
- You need to make **15 posts** and **15 replies** by end of semester (distributed)
- **Students can “post” questions/comments about any topic:**
 - Lecture notes, labs
 - Homework help and clarifications (but do not post HW solutions)
 - Multisim problems, questions or tips
 - Interesting articles or news stories, videos related to computer technology, robotics, engineering, careers in engineering, coops, etc.
 - **Students should also post answers (replies) to questions and news**
 - Examples: robotic videos, articles from IEEE Spectrum, Wired.com, etc.
 - Posts are typically 3 to 5 sentences with a link. Pick appropriate subject.
- Go into **“communicate”** in Angel and **“subscribe” to discussion forum**
 - Posts will automatically be forwarded to your email
 - You need to log into Angel to post to forum

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Real World Design Problem (MSI)

- Designing circuits with AND, OR, NOT, NAND, XOR, XNOR gates is somewhat **inefficient** as number of variables increases...why?
- As circuits get sophisticated, we need **to reduce IC chip counts** using module circuits that can be adapted to many applications
- Answer: **MSI chips** (take a modular approach)
- **We will cover some basic MSI chips in the upcoming lectures:** Decoders, Encoders, Multiplexers, De-multiplexers, Magnitude comparators, Adders

What is a Decoder?

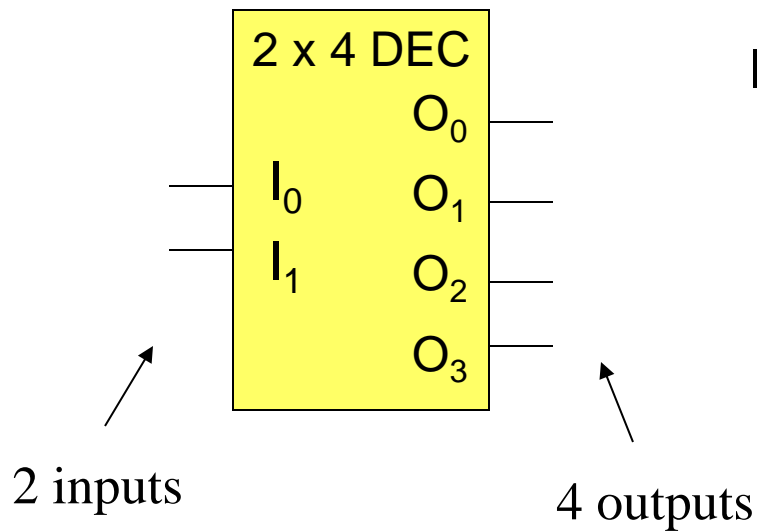
- A **decoder** is an **MSI** (medium-scale integrated circuit) device
- The input of a decoder is an **n-bit binary number**
- A decoder has **one output** for each n-bit binary input code
- Only **one output** of a decoder is active at any given time.
- A decoder has **n** inputs and **2ⁿ** outputs.
- Decoders exist in a variety of **sizes**: 2x4, 3x8, 4x16, 5x32, etc
- A **2x4 decoder** has 2 inputs and 4 outputs.
- A **3x8 decoder** has 3 inputs and 8 outputs.
- Decoders are represented by **block diagrams** (block diagrams hide the inside details)

What is a Decoder?

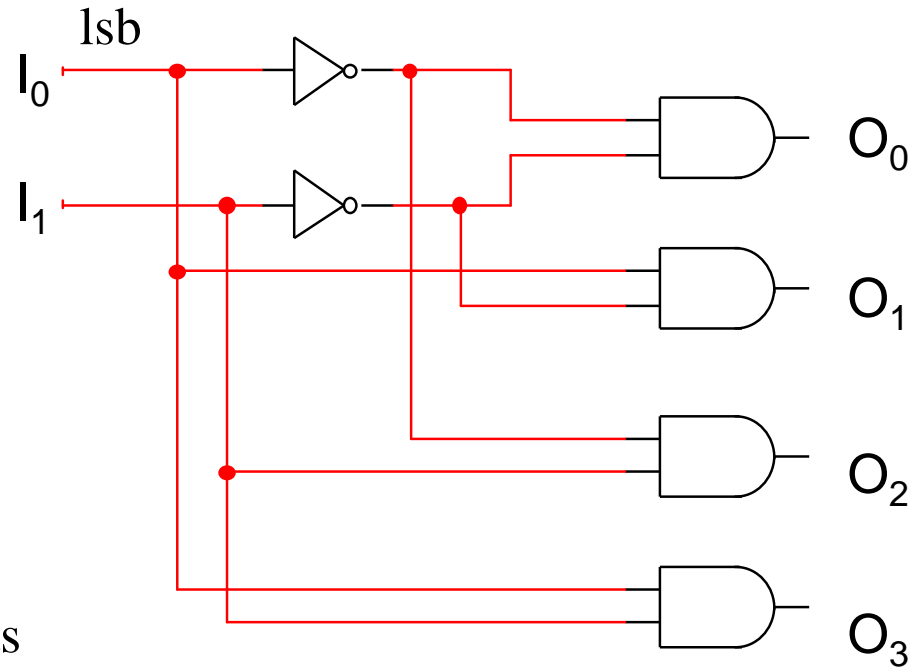
- Decoders can have active-high or active-low outputs
- Decoders can optionally have an “enable” input.
- Enable inputs can be either active-high or active-low
- Decoders can be used to implement arbitrary Boolean functions (also need external OR gates)
- Decoders can be used to reduce the number of IC's in a design
- Decoders are used in memory circuits to select memory modules (more later).
- Decoders can be used to control external devices (turn on & off)
- Decoders are commonly used as “building blocks” in digital design.
- It is often advantageous to design and build a complex circuit using a few MSI “building blocks” rather than using hundreds of individual logic gates.

2 x 4 Decoder

only 1 output is high (active)



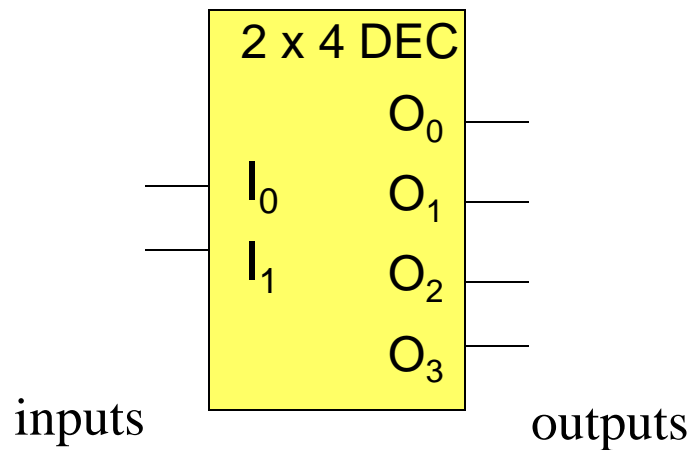
Block Diagram
(hides internal details)



Circuit (explain operation)

2 x 4 Decoder (truth table)

only 1 output is high (active)



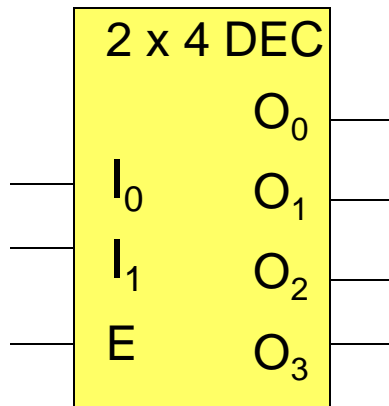
inputs		outputs			
I_1	I_0	O_3	O_2	O_1	O_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Truth table

Block Diagram

Note: only one output is “active” at a time

2 x 4 Decoder (with enable)



Block Diagram with
active-high enable

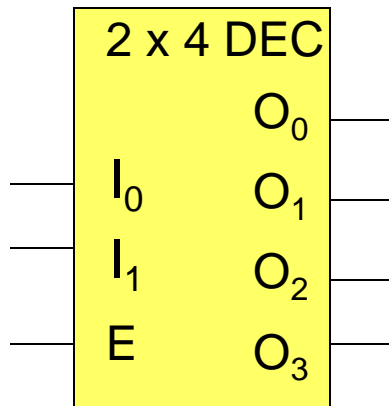
inputs			outputs			
E	I_1	I_0	O_3	O_2	O_1	O_0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0
0	X	X	0	0	0	0

when E is 0, it doesn't matter what I_1 and I_0 are
Truth table (explain X's)

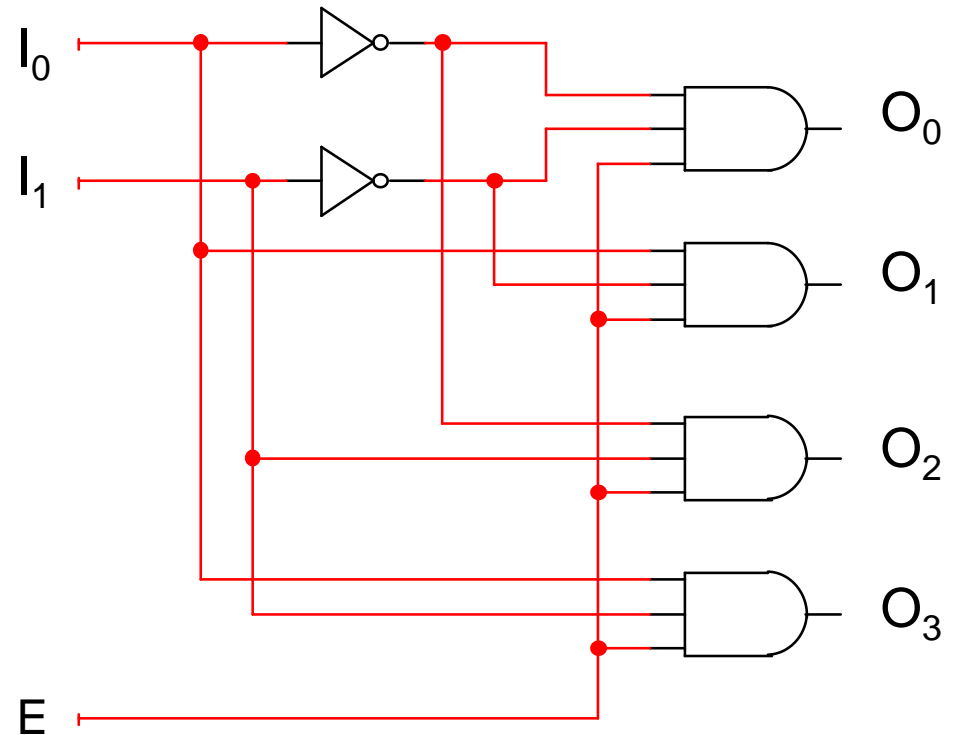
set $E = 1$ (or 5volts) to enable;

set $E = 0$ (ground or neg. side of battery) to disable (make all outputs = 0)

2 x 4 Decoder (with enable)



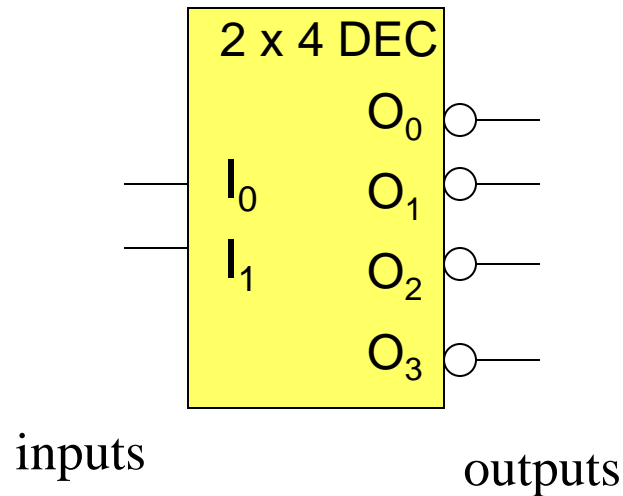
Block Diagram with
active-high enable



Circuit (explain operation)

2 x 4 Decoder (with active-low outputs)

only 1 output is low or "0" (active)

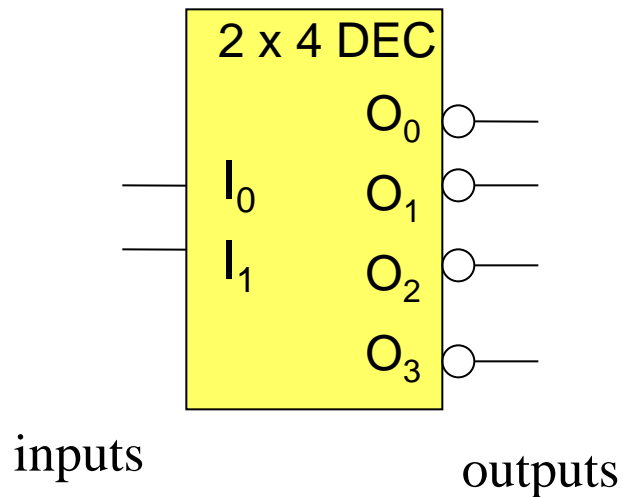


inputs		outputs			
I_1	I_0	O_3	O_2	O_1	O_0
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

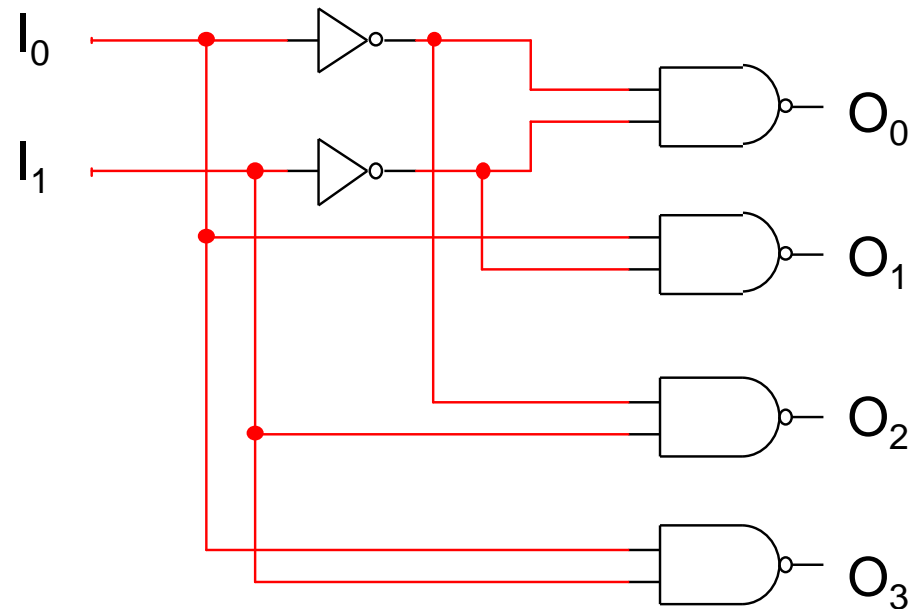
Truth table

Block Diagram with
active-low outputs

2 x 4 Decoder (with active-low outputs)



Block Diagram with
active-low outputs

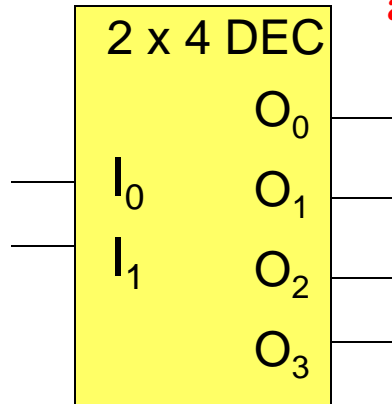


Circuit (explain operation)

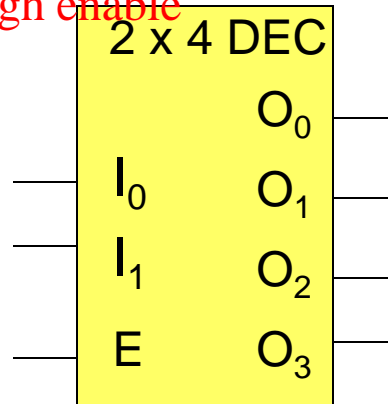
2 x 4 Decoder (summary)

(describe inputs and outputs)

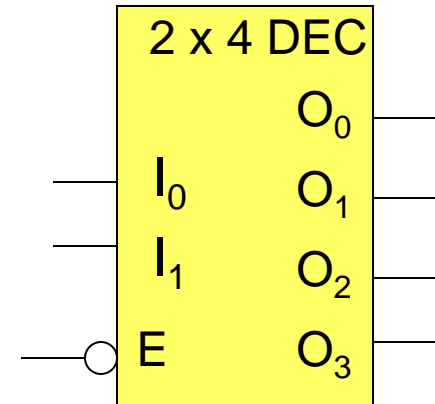
active-high inputs
active-high outputs



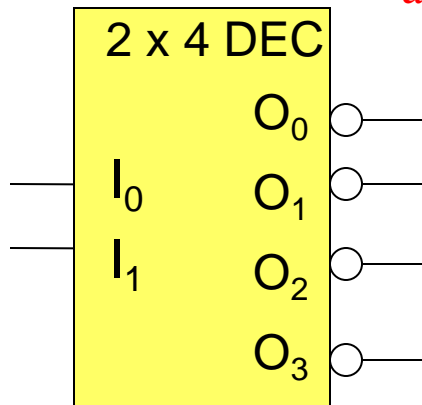
active-high inputs
active-high outputs
active-high enable



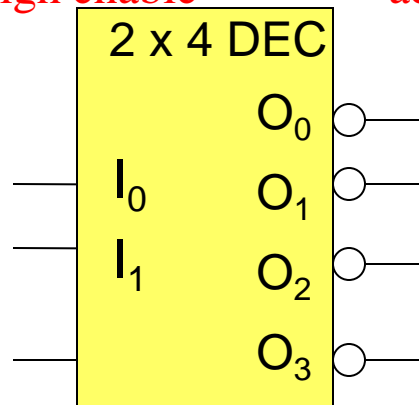
active-high inputs
active-high outputs
active-low enable



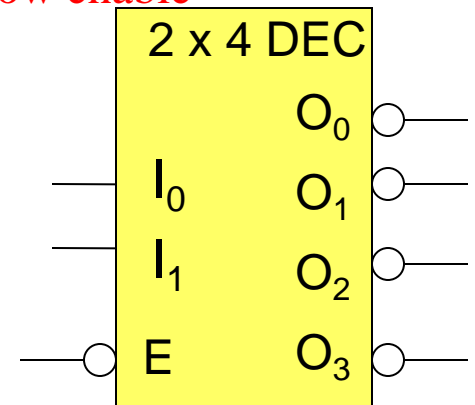
active-high inputs
active-low outputs



active-high inputs
active-low outputs
active-high enable



active-high inputs
active-low outputs
active-low enable

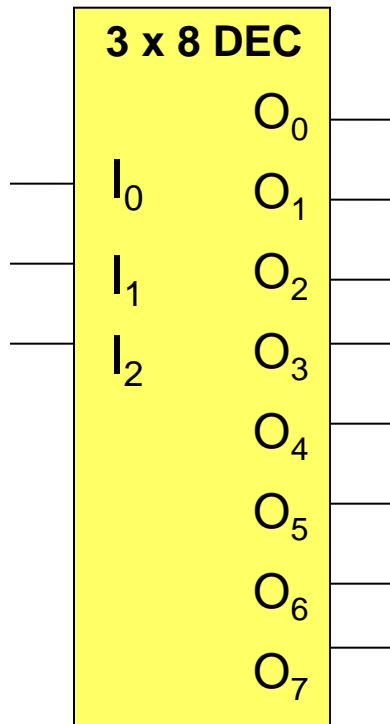


3 x 8 Decoder

only 1 output is high (active) based on inputs

inputs

outputs



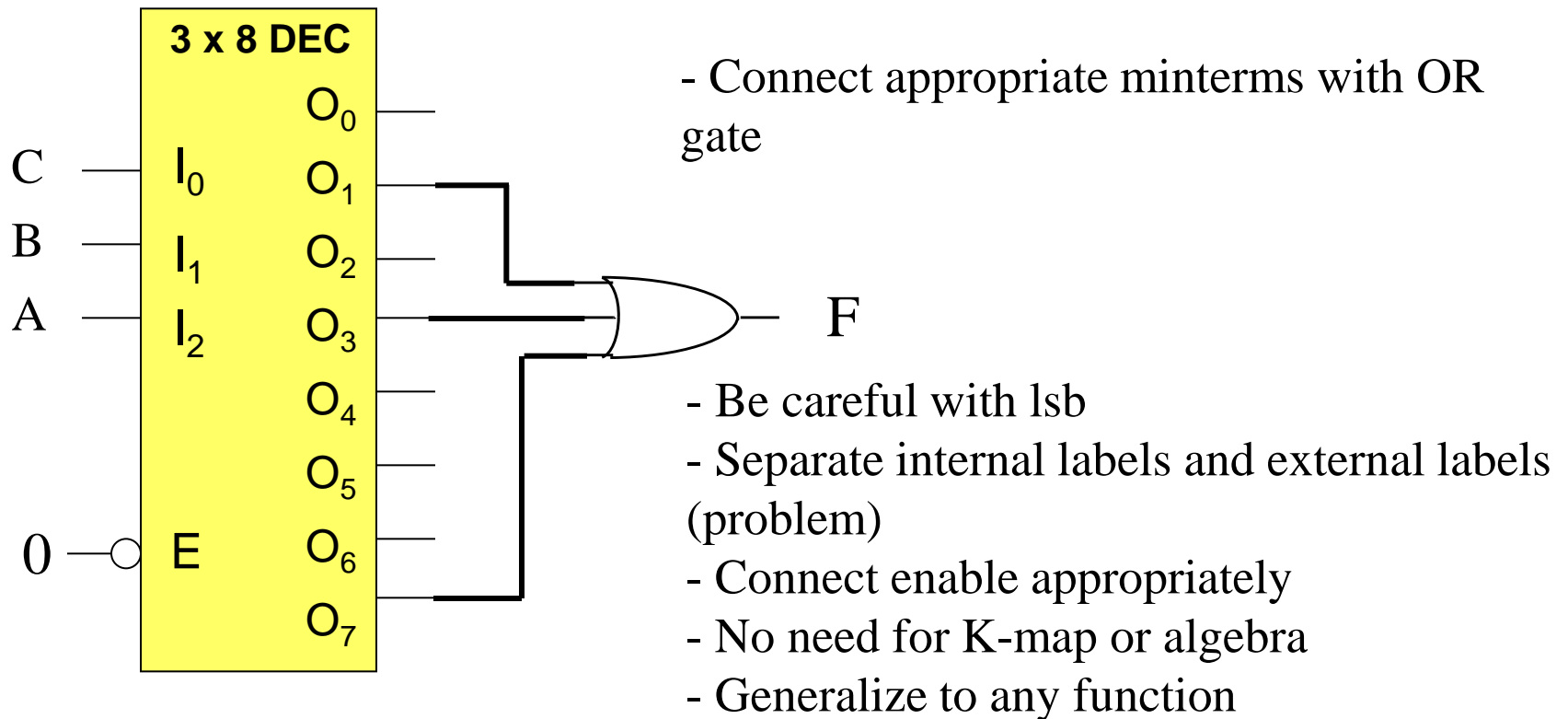
Block Diagram

lsb										
I_2	I_1	I_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Decoders may optionally possess active-low outputs and may possess an active-high or an active low enable.

Implementing a Boolean Function with a Decoder - 1

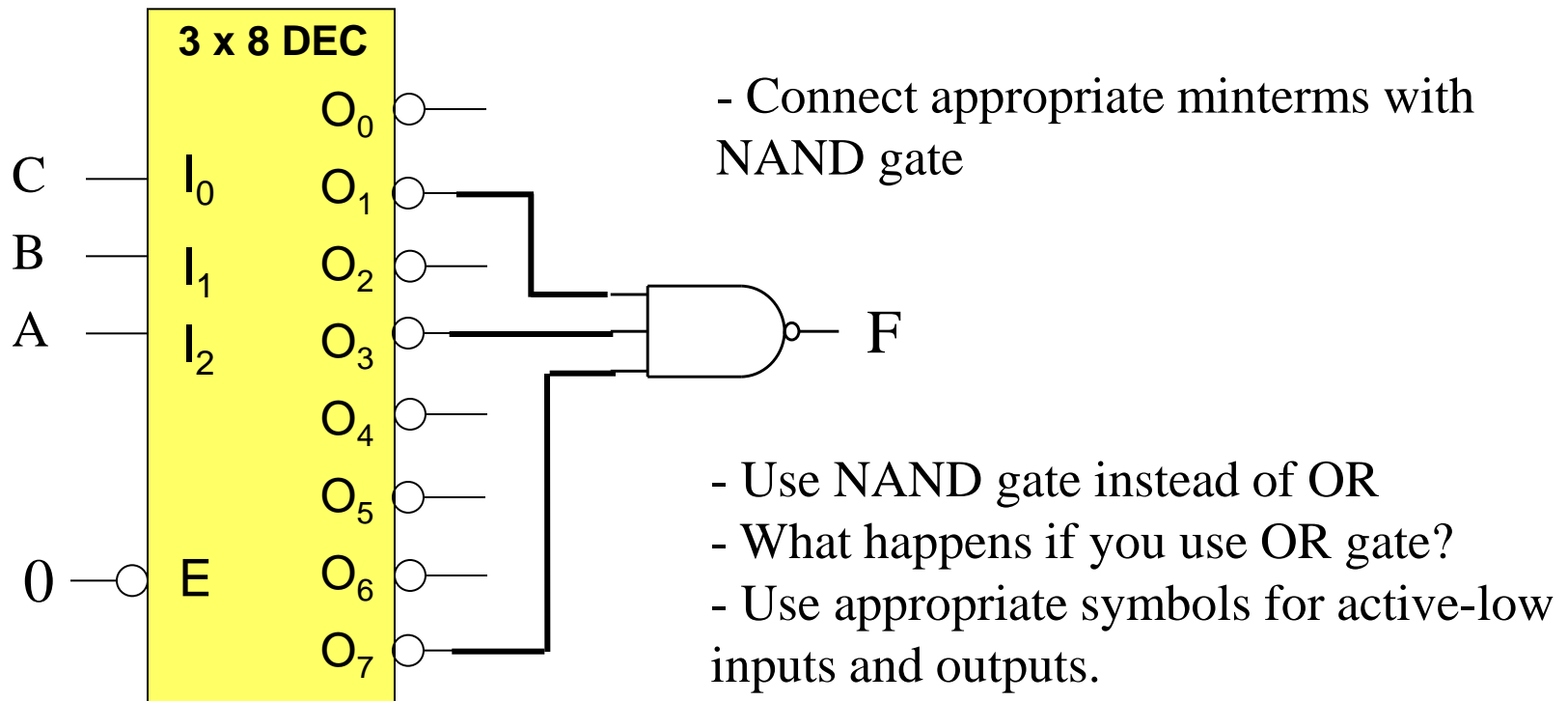
Example: Implement $F(A,B,C) = \sum m(1,3,7)$ on a 3x8 decoder with active-high outputs (default) and an active-low enable



Implementing a Boolean Function with a Decoder - 2

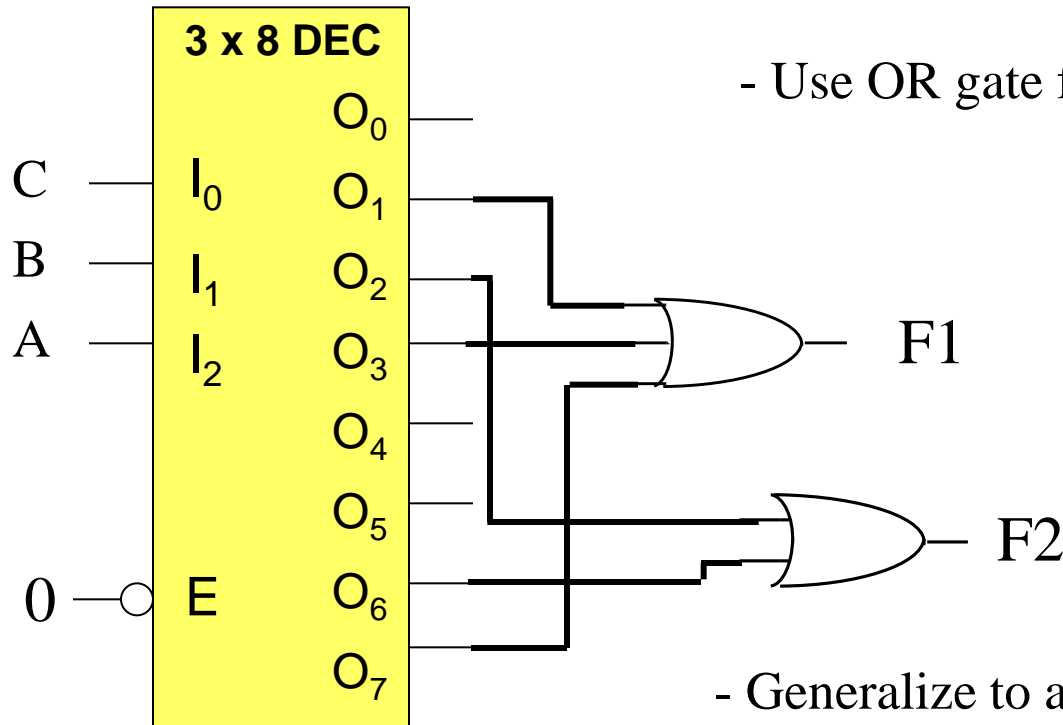
Example: Implement $F(A,B,C) = \Sigma m(1,3,7)$ on a 3x8 decoder with active-low outputs (default) and an active-low enable

only 1 output is low or “0” (active)



Implementing a Boolean Function with a Decoder - 3

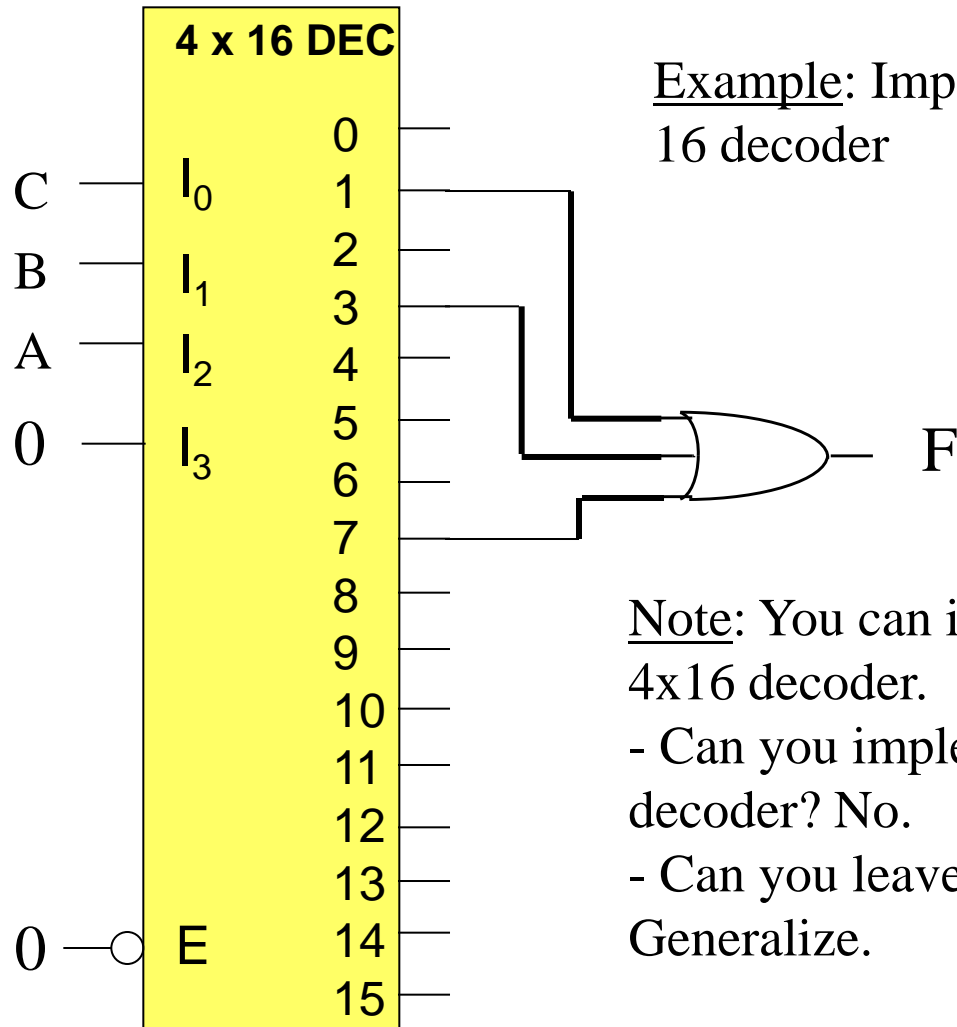
Example: Implement 2 functions: $F1(A,B,C) = \Sigma m(1,3,7)$ and $F2(A,B,C) = \Sigma m(2,6)$ on a 3x8 decoder with active-high outputs (default) and an active-low enable



- Use OR gate for each function.

- Generalize to any set of functions.
- How many IC's are required?

Implementing a Boolean Function with a Decoder - 4

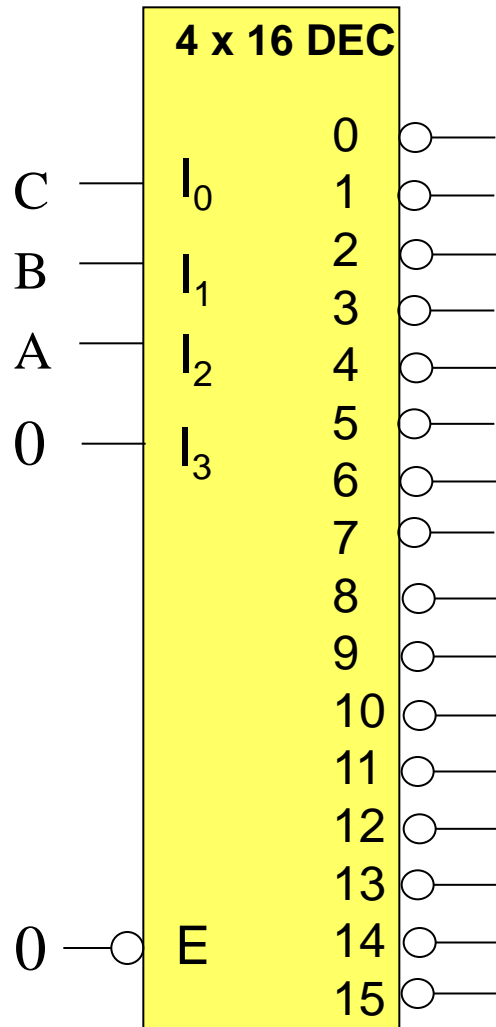


Note: You can implement a 3-variable function on a 4x16 decoder.

- Can you implement a 4-variable function on a 3x8 decoder? No.

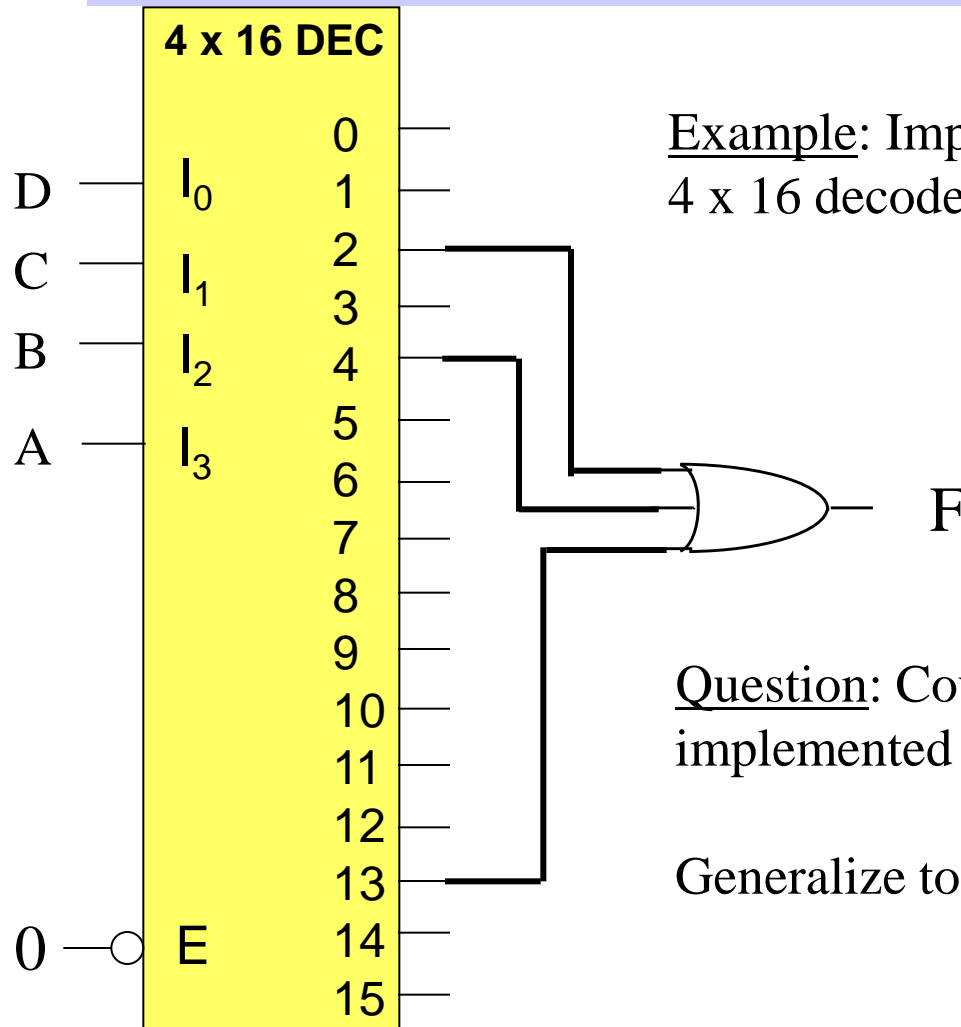
- Can you leave I_3 unconnected (floating)? - Generalize.

Implementing a Boolean Function with a Decoder – 4.5



Example: Implement $F(A,B,C) = \sum m(1,3,7)$ on a 4 x 16 decoder

Implementing a Boolean Function with a Decoder - 5

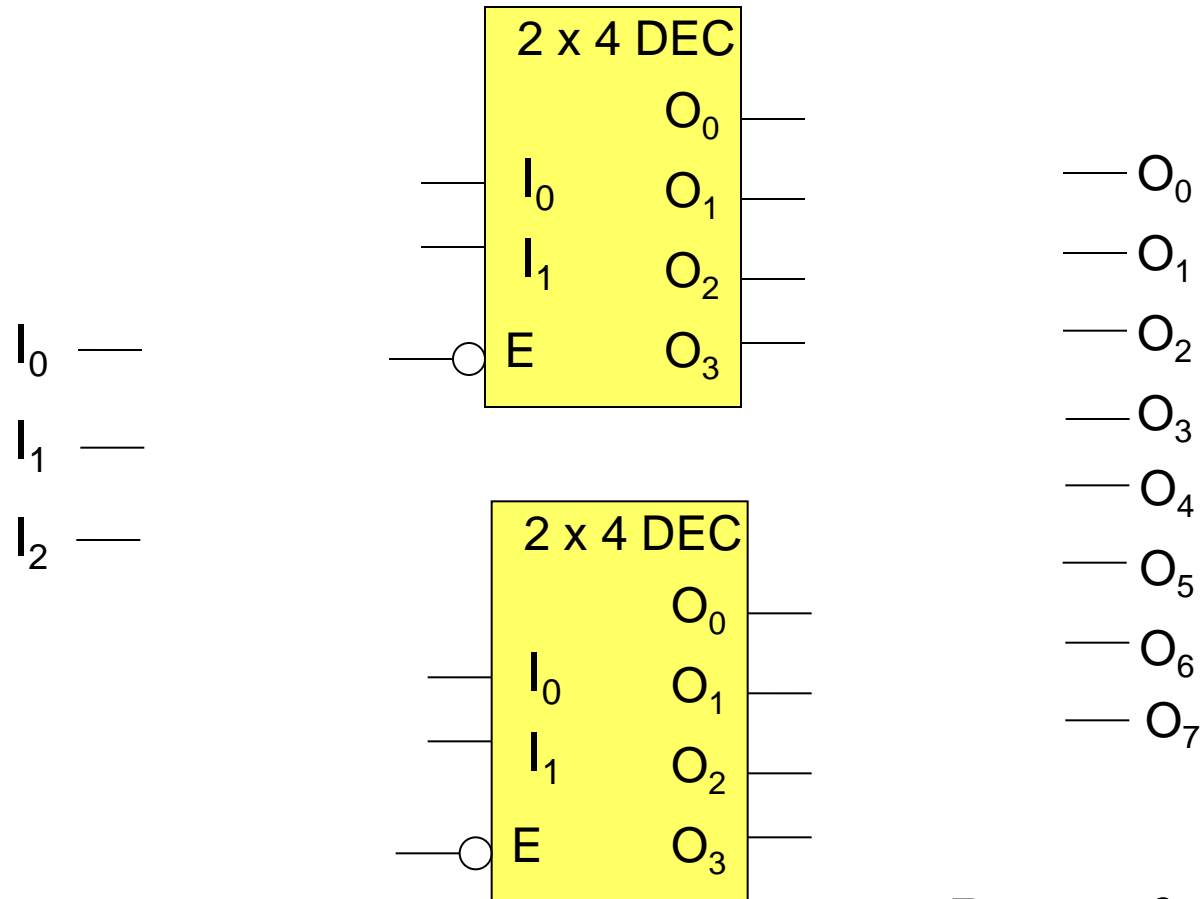


Question: Could this 4-variable function be implemented on a 5x32 decoder? Explain.

Generalize to any 4-variable function.

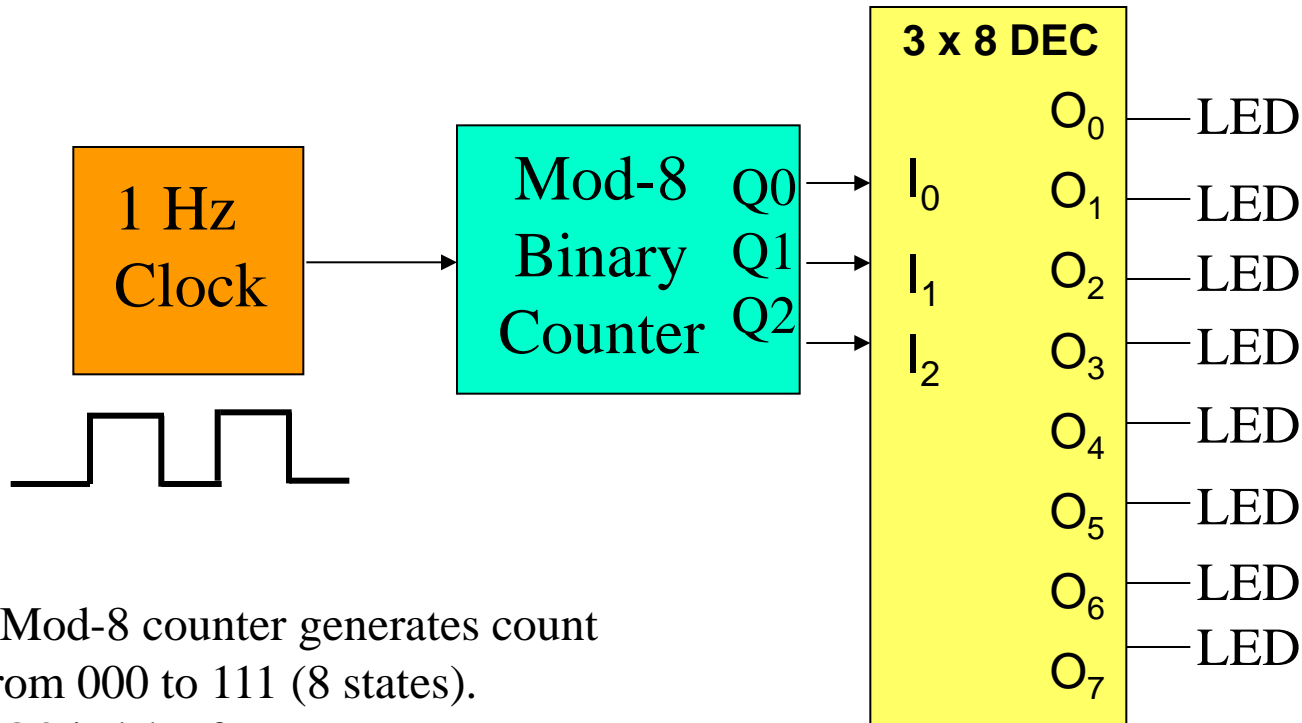
Designing a Decoder

Design problem: Design a 3x8 decoder from 2, 2x4 decoders.



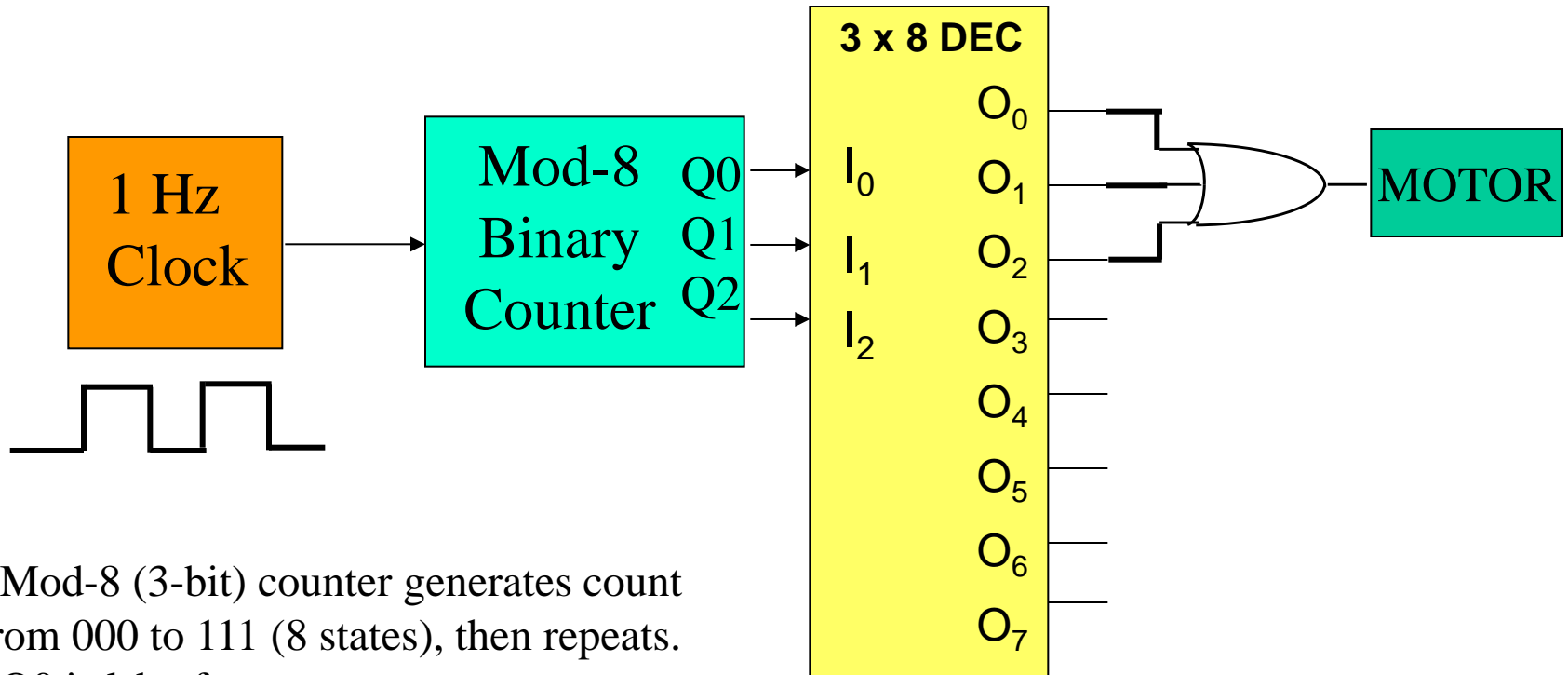
Be careful with labels

Counter and a Decoder - 1



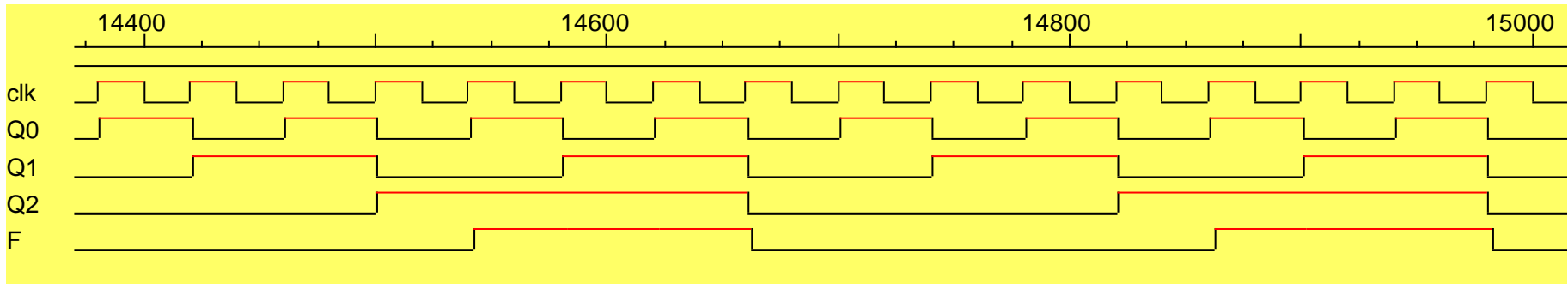
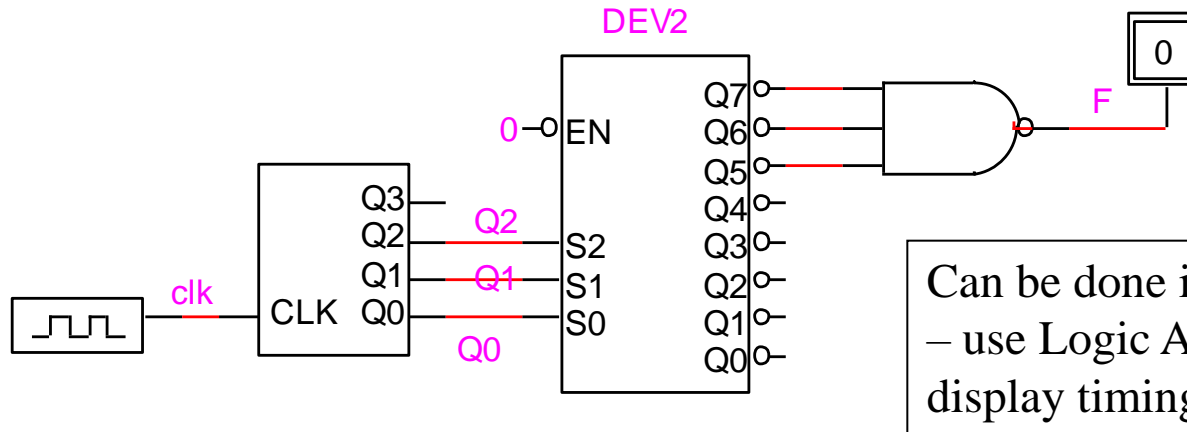
- Mod-8 counter generates count from 000 to 111 (8 states).
- Q0 is lsb of counter.
- LED is a light-emitting diode.
- Explain behavior. What would be behavior if using a decoder with active-low outputs?

Counter and a Decoder - 2



- Mod-8 (3-bit) counter generates count from 000 to 111 (8 states), then repeats.
- Q0 is lsb of counter.
- Explain behavior.
- What other control sequences are possible with a 3x8 decoder, a mod-8 counter, and a 1Hz clock?

LogicWorks Simulation



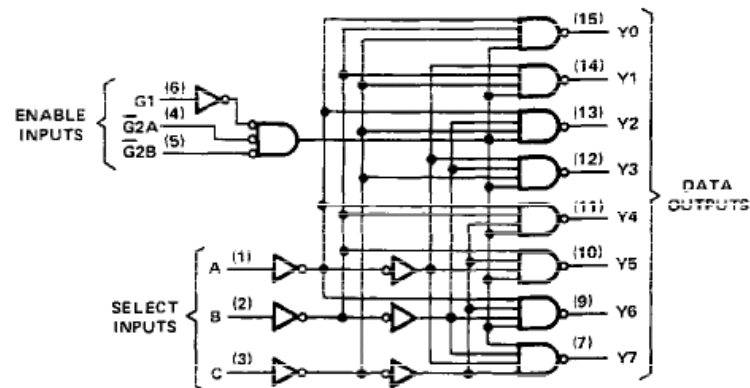
- Interpret circuit and timing diagram -- what is going on?
- Try this in LogicWorks -- use "clear unknowns" to initialize counter.
- Label all wires and they will appear on timing window.
- Drag wire names in timing window to reorder.

Decoder IC Datasheet (www.ti.com)

SN54LS138, SN54S138, SN74LS138, SN74S138A 3-LINE-TO 8-LINE DECODERS/DEMULTIPLEXERS

logic diagram and function table

'LS138, SN54S138, SN74S138A



Pin numbers shown are for D, J, N, and W packages.

'LS138, SN54S138, SN74S138A

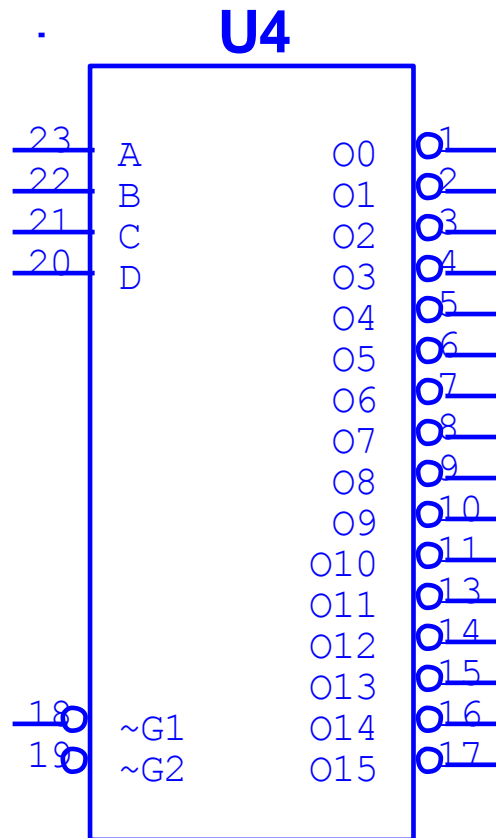
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	L	H	H	H	H	H
H	L	L	L	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	L	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H
H	L	L	L	L	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	L	H
H	L	L	L	L	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

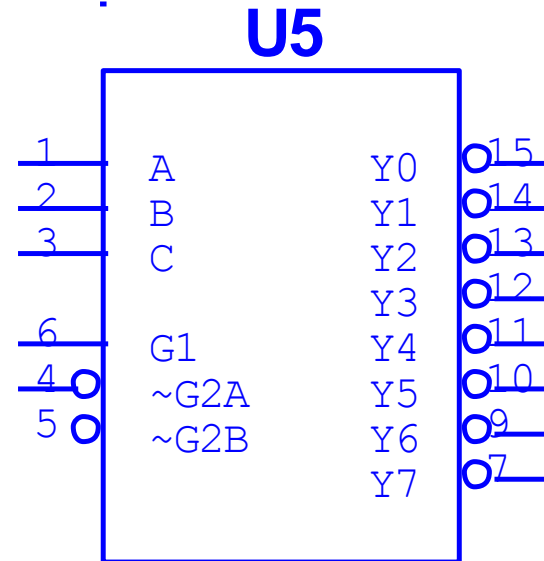
H = high level, L = low level, X = irrelevant

Decoder (MultiSim)



74154N

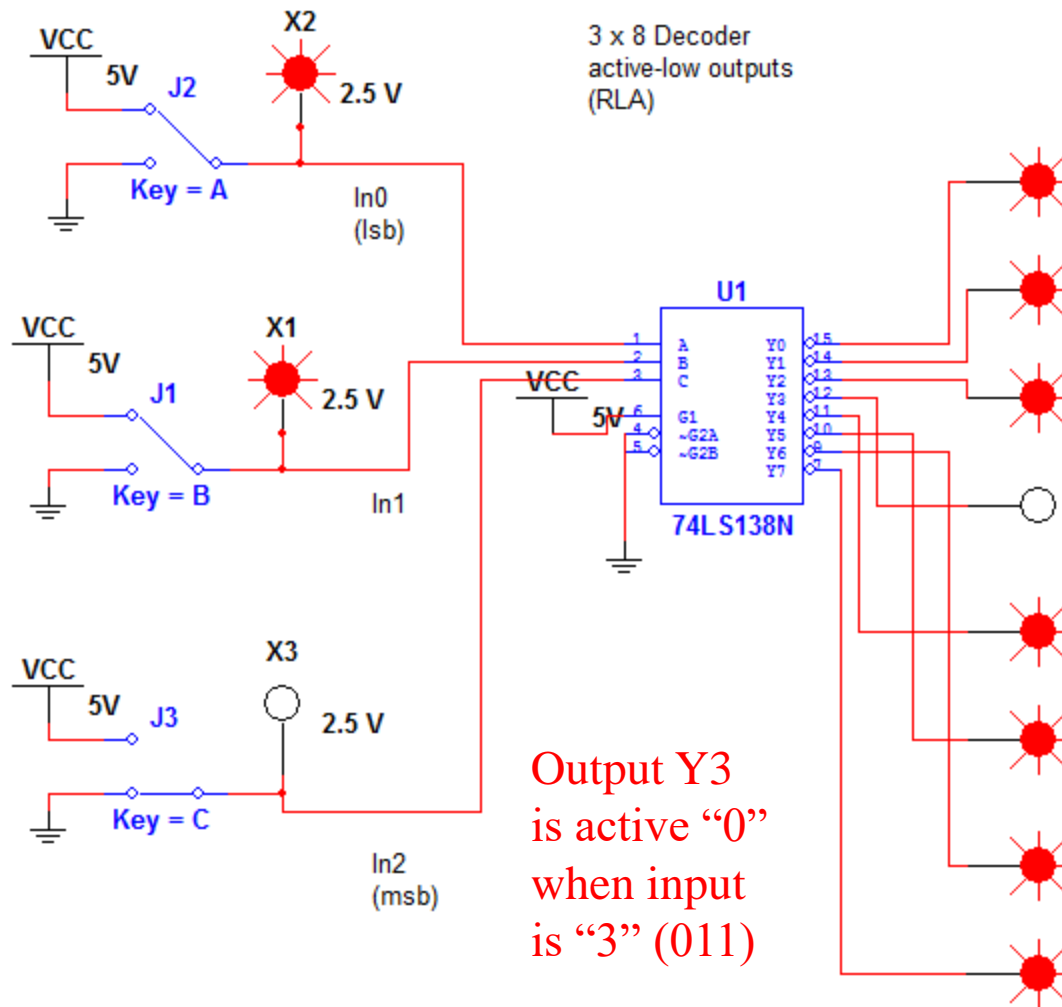
4x16 Decoder (active-low outputs)
~G1, ~G2 → active-low enables



74LS138N

3x8 Decoder (active-low outputs)
G1 → active-high enable
~G2A, ~G2B → active-low enables
Look in 74LS library

Decoder (MultiSim)



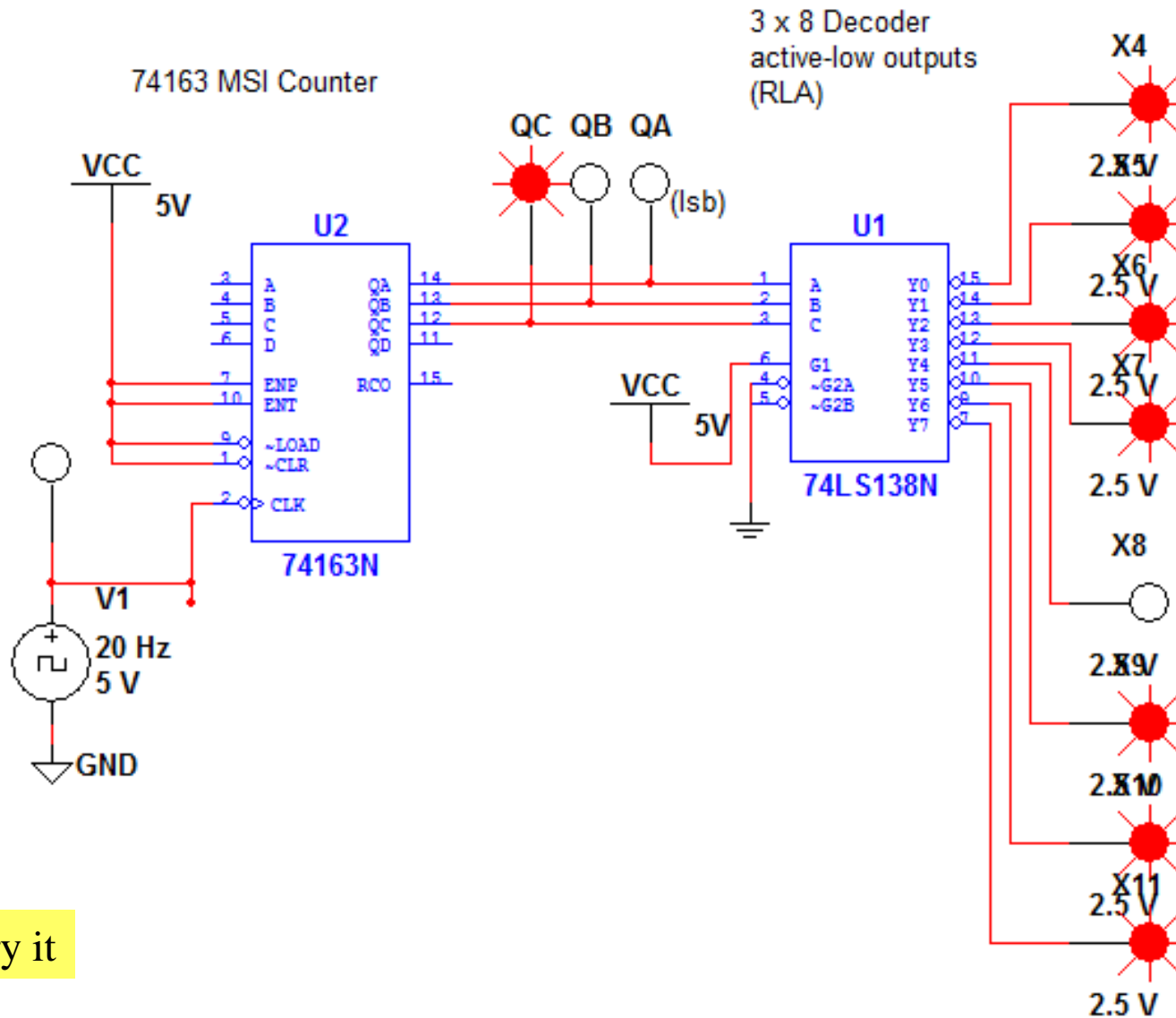
Try it

How would you modify this circuit to implement a function?

Example:
 $F = \sum m(1,3,5)$

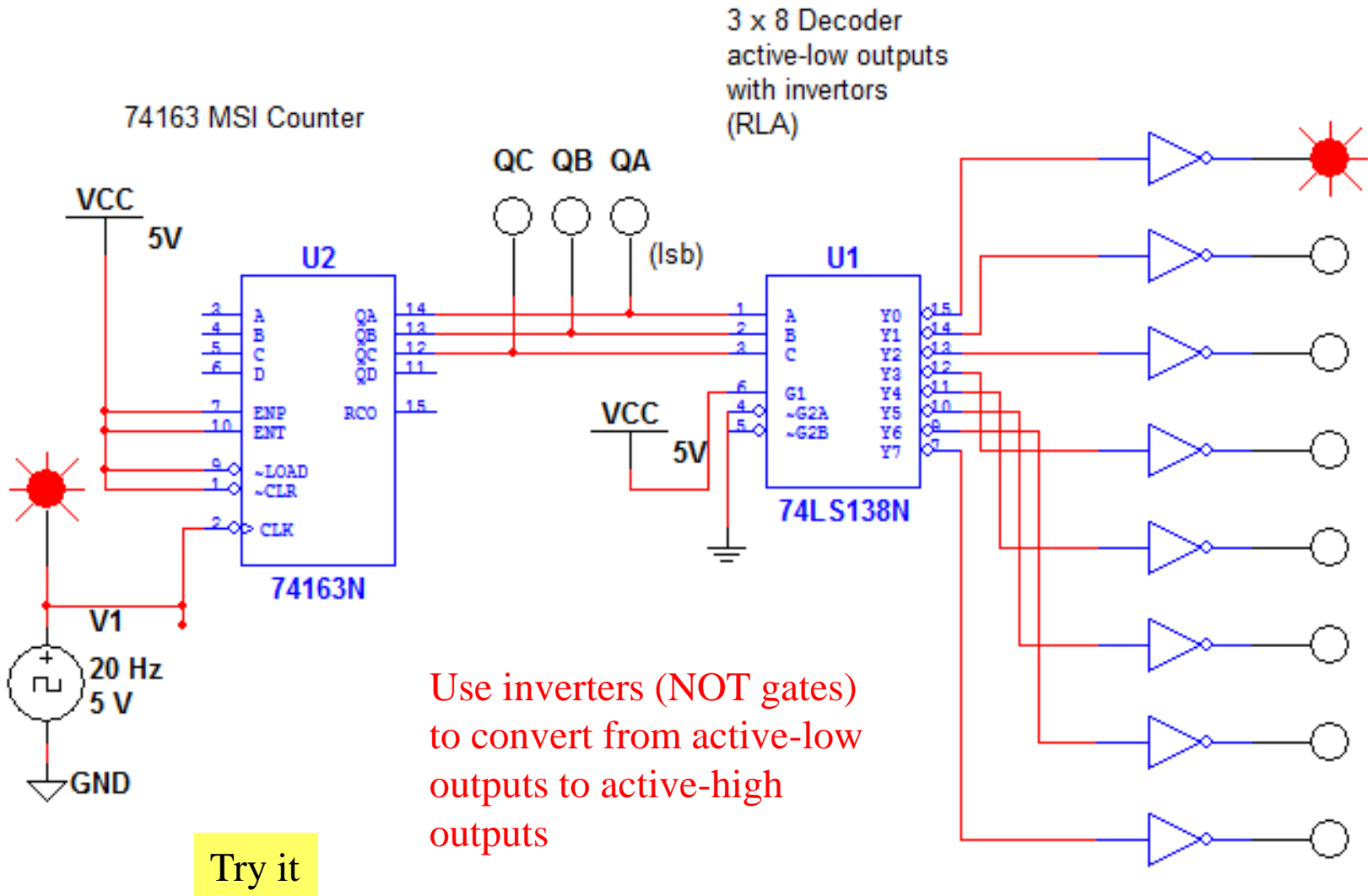
Observation: if at least one of the inputs to a NAND gate is 0, then you now the output of the NAND gate is 1.

Decoder (MultiSim)



Try it

Decoder (MultiSim)



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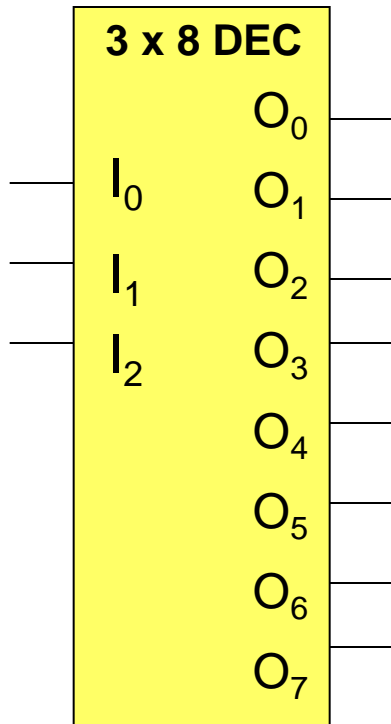
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Sample Exercises (Decoders)

1. Implement the function $F(A,B,C) = AB + BC$ on a 3x8 decoder with active-high outputs and an active-low enable. Simulate.
2. Implement the function $F(A,B,C) = ABC'$ on a 3x8 decoder with active-high outputs and an active-low enable. Simulate.
3. Implement $F(A,B,C) = \Sigma m(0, 1, 5)$ on a 3x8 decoder with active-high outputs and an active-low enable. Simulate.
4. Redo #1 above with a 3x8 decoder with active-low outputs. Simulate.
5. Redo #1 above with a 4x16 decoder with active-high outputs. Simulate.
6. Implement $F(A,B,C,D) = \Sigma m(1, 2, 14, 15)$ on a 4x16 decoder with active-high outputs and an active-low enable. Simulate.
7. Redo #4 above with a 4x16 decoder with active-low outputs. Simulate.
8. a) Design a 4x16 decoder using two, 3x8 decoders, both with active-high outputs and active-low enables. b) Use this circuit to implement $F(A,B,C,D) = \Sigma m(1, 2, 14, 15)$. Simulate.

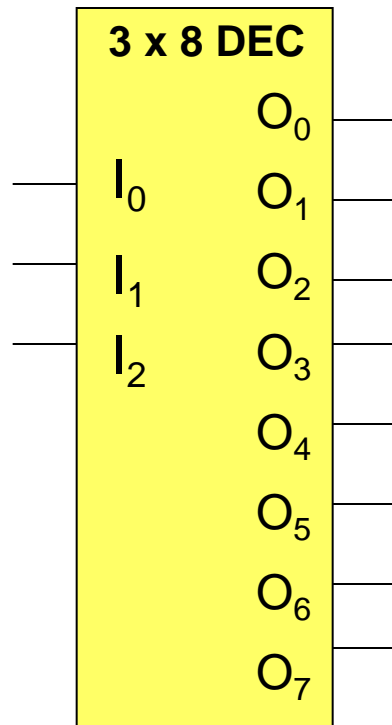
Sample Exercises (Decoders)

1. Implement the function $F(A,B,C) = AB + BC$ on a 3x8 decoder with active-high outputs and an active-low enable. Simulate.



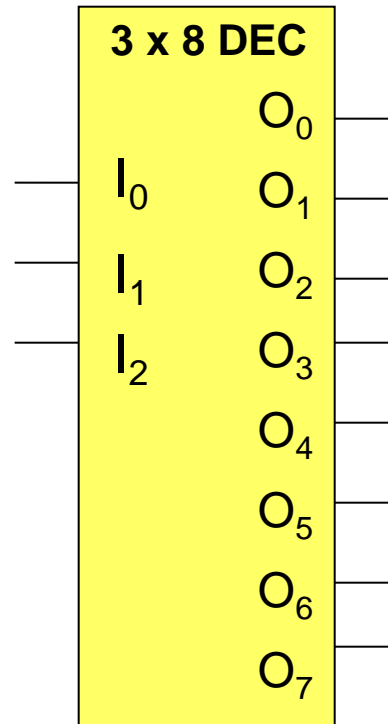
Sample Exercises (Decoders)

2. Implement the function $F(A,B,C) = ABC'$ on a 3x8 decoder with active-high outputs and an active-low enable. Simulate.



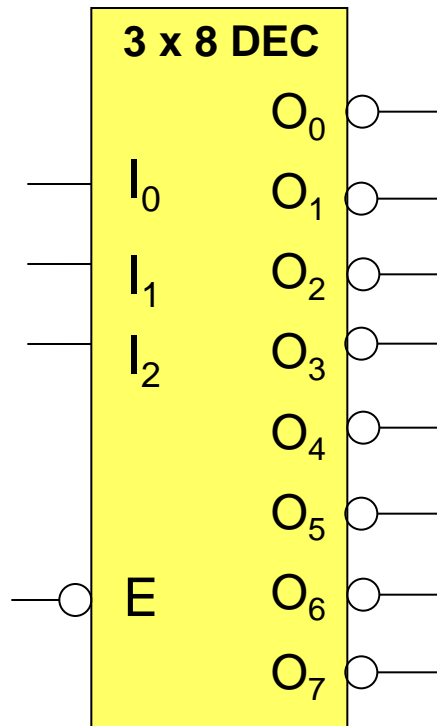
Sample Exercises (Decoders)

3. Implement $F(A,B,C) = \sum m(0, 1, 5)$ on a 3x8 decoder with active-high outputs and an active-low enable. Simulate.



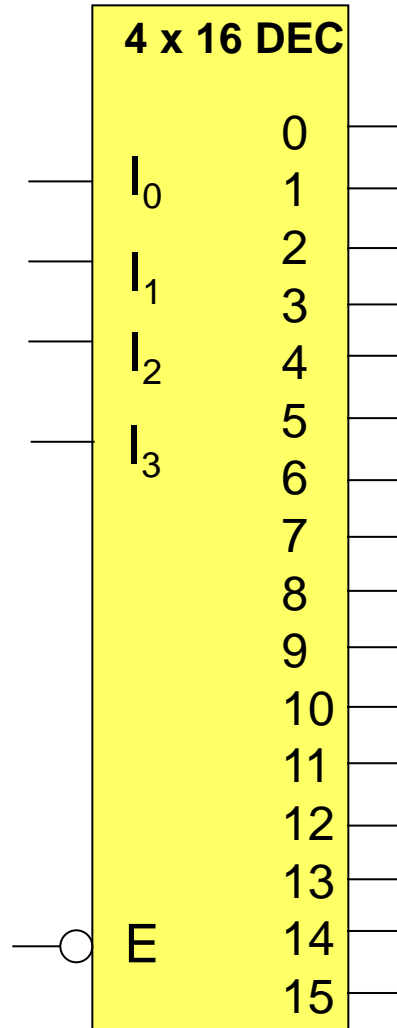
Sample Exercises (Decoders)

4. Redo $F(A,B,C) = \sum m(0, 1, 5)$ with a 3x8 decoder with active-low outputs.



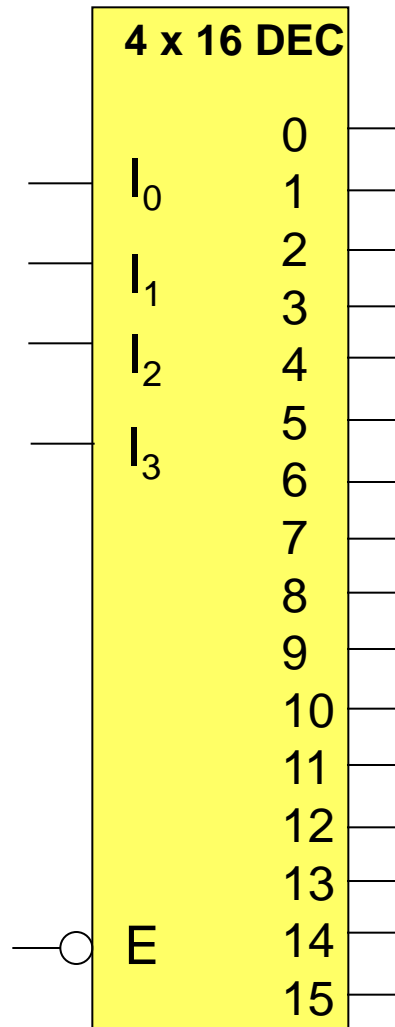
Sample Exercises (Decoders)

5. Redo $F(A,B,C) = \sum m(0, 1, 5)$ above with a 4x16 decoder with active-high outputs.



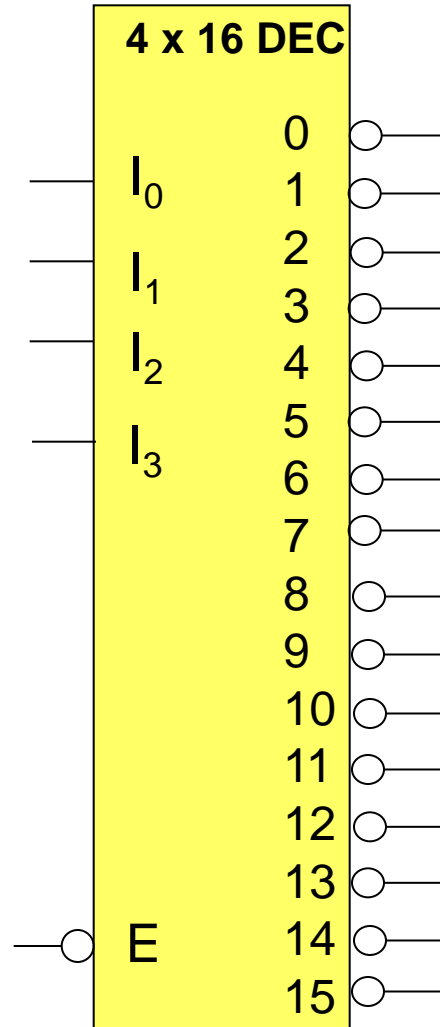
Sample Exercises (Decoders)

6. Implement $F(A,B,C,D) = \sum m(1, 2, 14, 15)$ on a 4x16 decoder with active-high outputs and an active-low enable. Simulate.



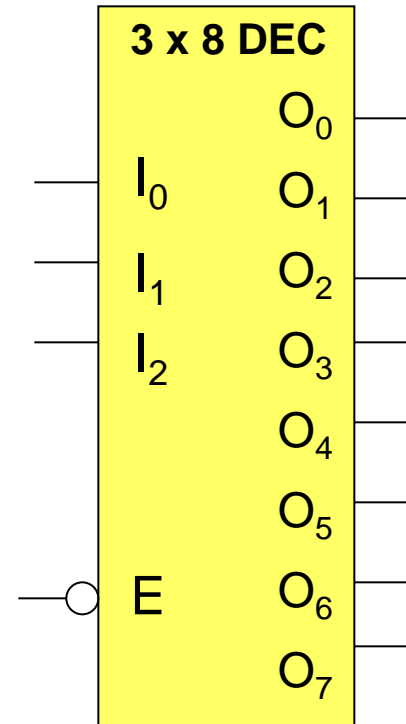
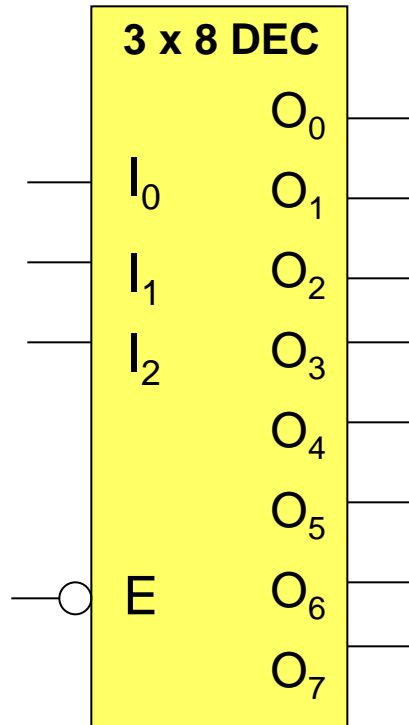
Sample Exercises (Decoders)

7. Redo $F(A,B,C,D) = \Sigma m(1, 2, 14, 15)$ above with a 4x16 decoder with active-low outputs.



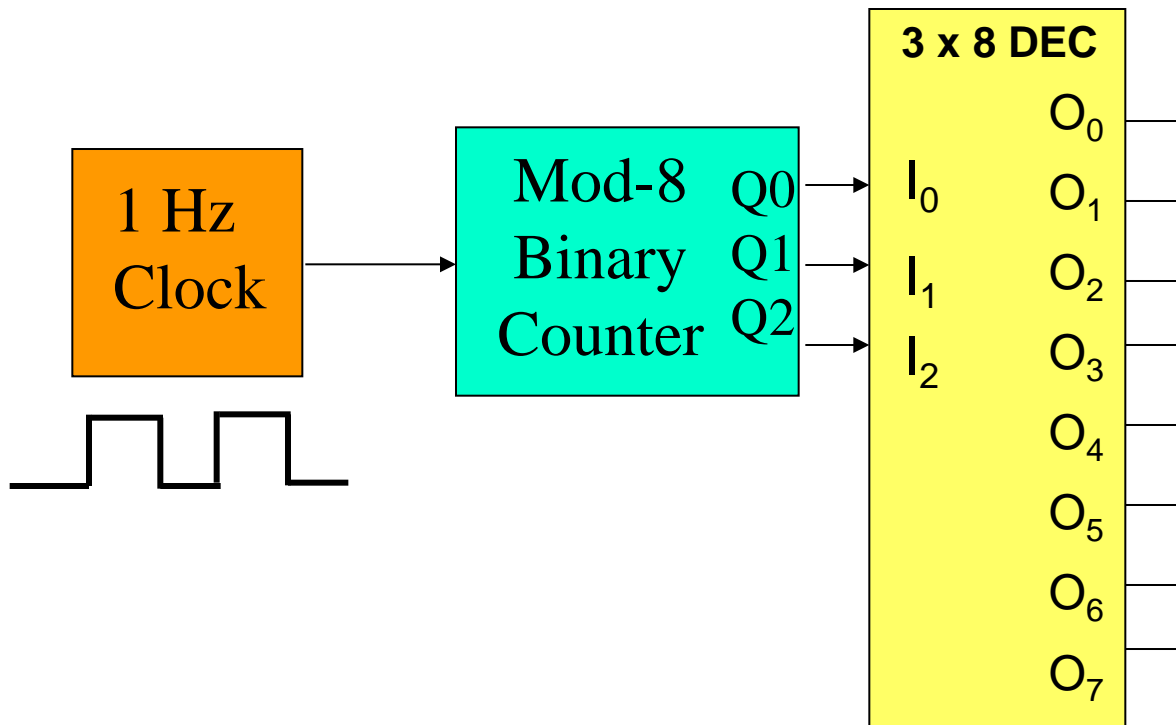
Sample Exercises (Decoders)

#8 a) Design a 4x16 decoder using two, 3x8 decoders, both with active-high outputs and active-low enables. b) Use this circuit to implement $F(A,B,C,D) = \sum m(1, 2, 14, 15)$. Simulate.



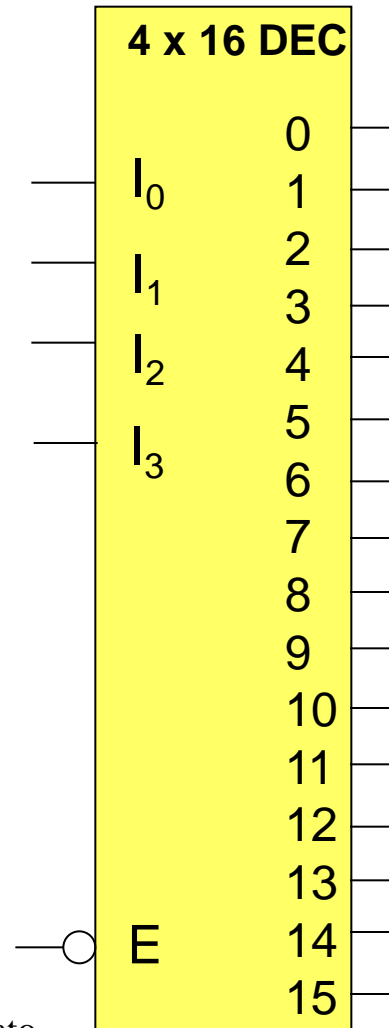
Sample Exercises (Decoders with Counter)

1. Design a control circuit which turns a motor “on” for 2 seconds, then “off” for 6 seconds, then repeats. Assume a 1Hz clock and mod-8 counter are available. Simulate in MultiSim or LogicWorks. Include circuit and timing diagram with comments.



Sample Exercises (Decoders with Counter)

2. Design a control circuit which turns a motor “on” for 6 seconds, then “off” for 10 seconds, then repeats. Assume a 1Hz clock and mod-16 counter are available. Simulate in MultiSim or LogicWorks. Include circuit and timing diagram with comments.



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In real world, the output of a logic gate cannot “drive” a motor directly; some type of transistor circuit is needed.⁴³

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Lecture Set #11

Decoders, Encoders

Video

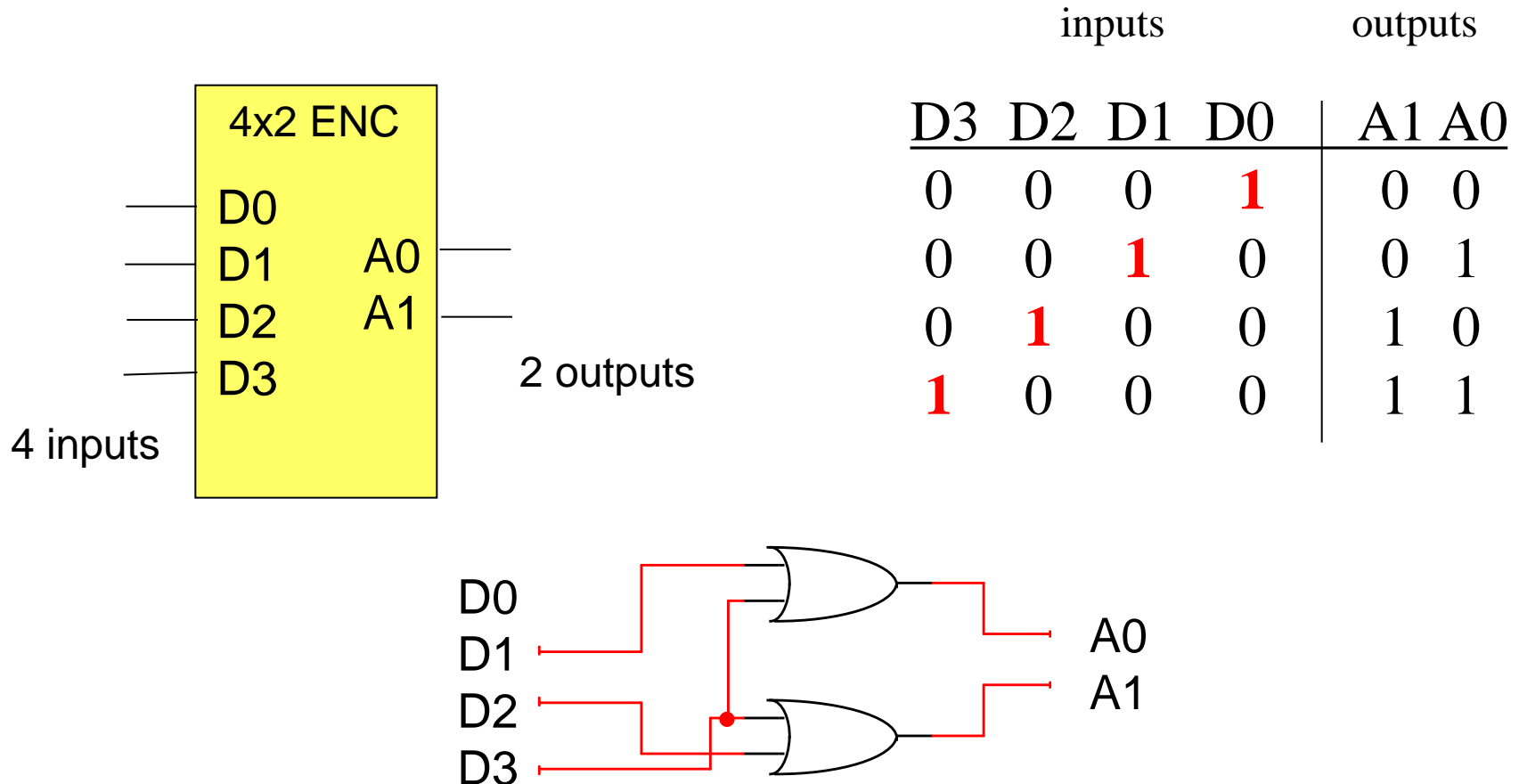
Topics:

- Discuss HW **Video part 1 of 5**
- Decoder **Video part 2 of 5**
- Circuit Simulation Demonstration
- Decoder Applications
- Decoder IC Specs
- Sample Decoder Exercises **Video part 3 of 5**
- Encoder **Video part 4 of 5 ←**
- Encoder Applications
- Summary **Video part 5 of 5**

Encoders

- **Encoders** are **MSI devices** that perform the “**inverse**” operation of decoders.
- An encoder has a number of inputs of which **only one input is active** at any one time.
- For each active input, there is a **n-bit binary value** output produced.
- Only one input should be active; however, **more than one output** can be active for a given input condition
- An encoder can be of **size** 4 x 2, 8 x 3, 16 x 4, Decimal-to BCD etc.
- A **4 x 2 encoder** has 4 inputs and 2 outputs.
- An **8 x 3 encoder** has 8 inputs and 3 outputs.
- Encoders can **have active-high or active-low inputs and outputs**
- A common **application** of an encoder is a simple **keyboard**.

4 x2 Encoder



Explain operation of circuit. What if no inputs are active?
 What if more than one input is active?

4 x2 Priority Encoder

What happens if more than one input is high at same time with an encoder?

Priority code “responds” to highest priority input if more than one is high.

Also, output “V” is high when output is valid

4x2 ENC						
D0	D1	D2	D3	A1	A0	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

- Explain operation of circuit.
- What is “V” output? (valid indicator = 1 if at least one input valid)
- What if no inputs are active?
- What if more than one input is active?
- What does “priority” mean?
- What do X’s on input side of truth table mean?
- Design circuit above. Use K-maps and don’t care.

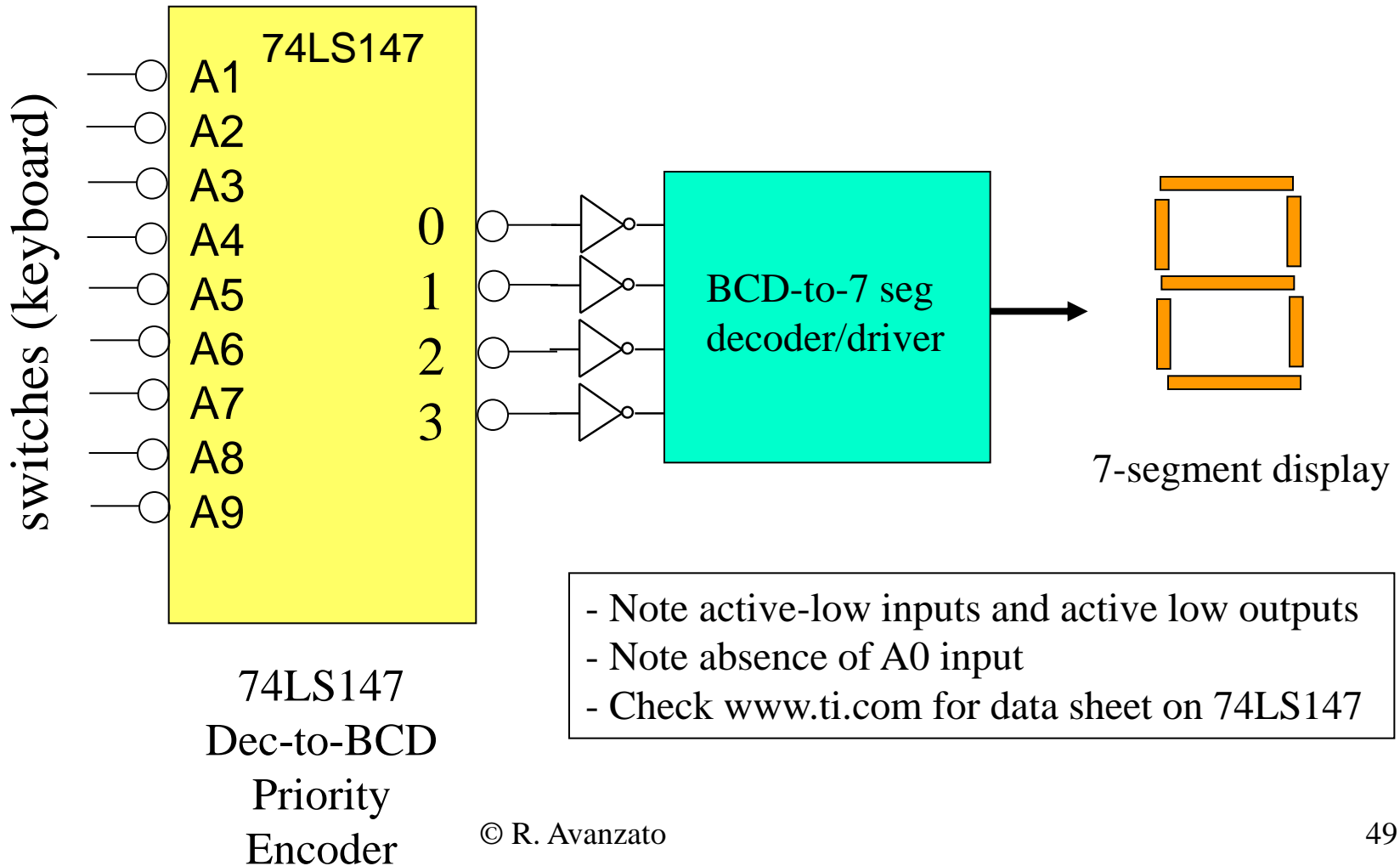
D3 has highest priority; D0 has lowest priority. Not all encoders have priority logic.

8 x 3 Encoders

			inputs								outputs		
8x3 ENC			D7	D6	D5	D4	D3	D2	D1	D0	A2	A1	A0
D0			0	0	0	0	0	0	0	1	0	0	0
D1			0	0	0	0	0	0	1	0	0	0	1
D2	A0		0	0	0	0	0	1	0	0	0	1	0
D3	A1		0	0	0	0	0	1	0	0	0	1	1
D4	A2		0	0	0	0	1	0	0	0	1	0	0
D5			0	0	0	1	0	0	0	0	1	0	1
D6			0	0	1	0	0	0	0	0	1	1	0
D7			0	1	0	0	0	0	0	0	1	1	1
			1	0	0	0	0	0	0	0	1	1	1

- Explain circuit operation. Is this a priority encoder?
- Design circuit for operation described above (by inspection).

Decimal-to-BCD Encoder



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Lecture Set #11

Decoders, Encoders

Video

Topics:

- Discuss HW

Video part 1 of 5

- Decoder
- Circuit Simulation Demonstration
- Decoder Applications
- Decoder IC Specs

Video part 2 of 5

- Sample Decoder Exercises

Video part 3 of 5

- Encoder
- Encoder Applications

Video part 4 of 5

- Summary

Video part 5 of 5 ←

What you should know...

- Be able to **construct block diagrams** of decoders with appropriate internal labels and with active low and active high inputs and outputs.
- Be able to construct logic gate diagram of **internal circuitry** of a simple decoder.
- Be able to implement an arbitrary **Boolean function** on a variety of decoders. Use block diagrams with appropriate internal and external labels. Label and define all input and output. Use enable inputs if appropriate.
- Be able to construct a **decoder with smaller decoders**. Use enable inputs if appropriate. Build decoder of arbitrary size.
- Be able to connect a counter and **clock** to a decoder to provide a sequenced output. Example: turn on a motor for 3 seconds, off for 5 seconds.
- Know the **basic operation and applications** of an encoder.
- Be able to interpret the **block diagram** of an encoder.
- Understand the operation and **advantage of a priority encoder**.
- Know how to use **software simulation** tool to simulate and analyze decoder circuits.
- In this course, we are going to focus **more on decoders** than on encoders

Summary

- MSI devices, such as decoders and encoders are used as **"building blocks"** to design more complex digital circuits. This simplifies the design process and reduces the number of ICs. Engineers do not modify the internal circuitry of decoders and other MSI devices.
- A **decoder** is an MSI device that **has n inputs and 2^n outputs**. Depending on the input pattern, one and only one of the outputs will be high. If decoder has active-low outputs, then one and only one output will be low for each unique input.
- **Commonly used decoders** are 2 x 4, 3 x 8, 4 x 16. (Note: 2 x 4 means 2 inputs and 4 outputs)
- Decoders can have **active-high outputs** or **active-low outputs**.
- Decoders may optionally have an **active-high enable or an active-low enable input**. The decoder must be enabled in order for it to operate. If the decoder is not enabled then the decoder will ignore the data inputs, and the outputs will remain inactive.
- Decoders can be used to **implement Boolean functions**. When implementing functions, there will be the need to add one or more OR gates or one or more NAND gates to the outputs of the decoder.
- Decoders can be used to **selectively activate devices** or circuits that are connected to the outputs of the decoder. For example, in computer circuits, decoders are used to select (enable) different memory modules.

Summary

- Decoders are represented by **block diagrams** showing internal labels for all input variables, any enables, and either active-low or active-high outputs.
- Decoders can be **combined to form larger decoders**. For example, two 2 x 4 decoders can be combined to form a single 3 x 8 decoder.
- **Encoders are MSI devices** with 2^n inputs and n outputs. For example, an encoder could have 8 inputs and 3 outputs, Only one input to an encoder is ever activated, then a resultant bit pattern is generated on the output wires.
- A common example of an **encoder is a decimal-to-BCD encoder** used for a calculator keyboard.
- Encoders are represented by **block diagrams** showing internal labels for all input variables, any enables, and either active-low or active-high outputs.

Further Reading

- Mano, Kime, Logic and Computer Design Fundamentals, 2nd edition, Prentice Hall, 2001 (Chapter 3).
- Tocci, R., Digital Systems, Prentice Hall, (Chapter 9, MSI Logic).