Penn State Abington
CMPEN 271
Lecture Set #16
D FFs, Shift Registers, Ring Counters

with solutions

Topics:

- Design Problem — **Video part 1 of 4** ←
- Clocked Flip-flops (FFs)
- D flip-flop
- Sample Questions

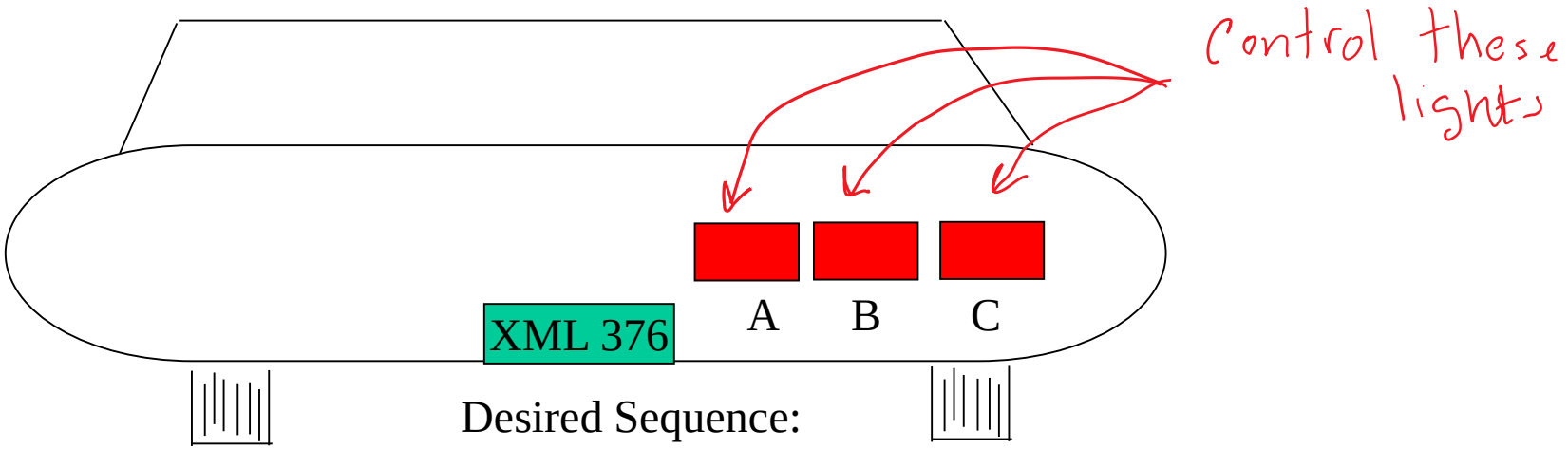
- D FF applications - shift register — **Video part 2 of 4**
- Setup and hold times
- Sample Questions

- Ring counter with applications — **Video part 3 of 4**
- Timing Diagrams
- Simulation software issues
- Sample Questions

- HW #8 Car Taillights Circuit — **Video part 4 of 4**

Design Problem – Turn Signal

Design Problem: Design and simulate a circuit to control the taillights (turn signal) of a 1965 classic Thunderbird car. (This has been reintroduced on some modern cars.) The sequence of lights is described below.



Desired Sequence:

	A	B	C	A B C	
t = 0s				0 0 0	(all lights off)
t = 1s				1 0 0	
t = 2s				1 1 0	
t = 3s				1 1 1	(all lights on)
t = 4s				0 0 0	
t = 5s				1 0 0	...repeats

Assume that the sequence time interval is 1 second, and a 1 Hz (1pps) clock generator circuit is available.

(adapted from Wakerly)

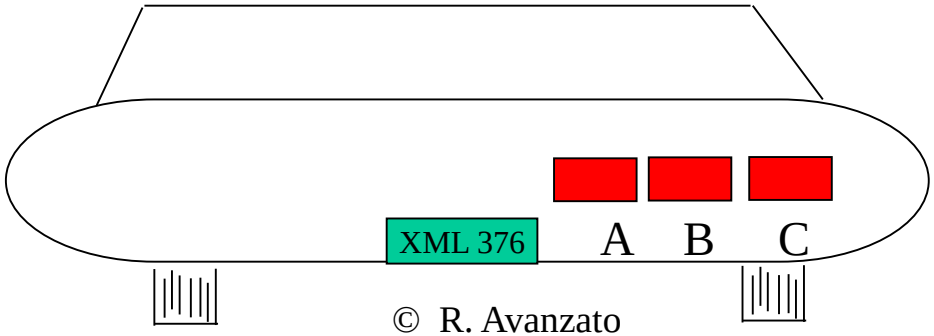
Design Problem – Turn Signal

- The turn signal circuit requires **memory elements (latches)** and a **clock** (1 pulse per second). We cannot solve the turn signal problem with just a truth table (combinational logic).

- We can try to use NAND and NOR latches for memory, but NAND and NOR latches do not have clock inputs and **do not respond to a clock signal.**

- We need to introduce **new memory elements (D latches, flip-flops) that respond and are synchronized to a clock signal**.

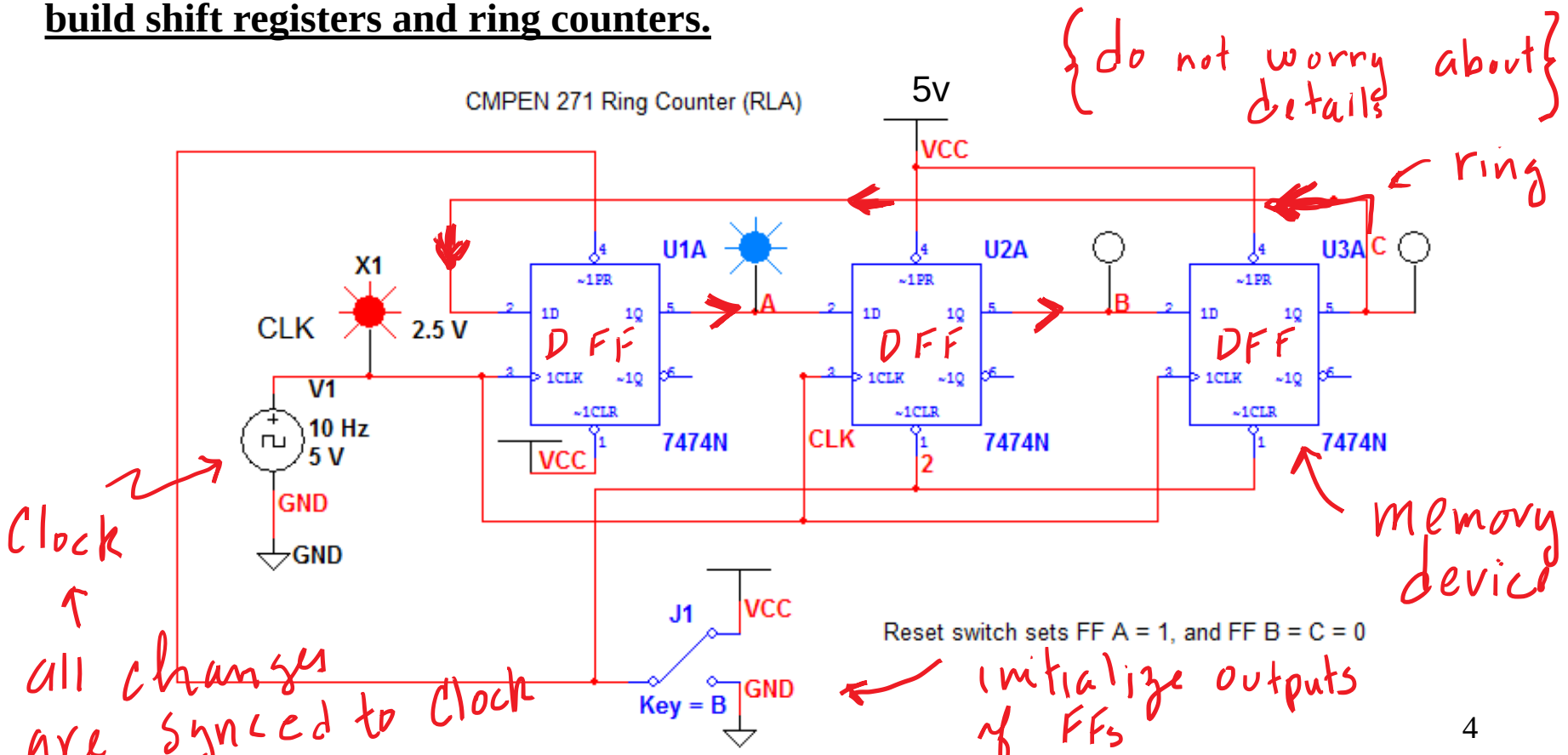
- Note: A **clock signal** is a simple square wave (0 volts, 5 volts) operating at a specified frequency such as 1Hz (1 pulse per sec) in our example. The clock signal in a modern computer might be 1GHz.



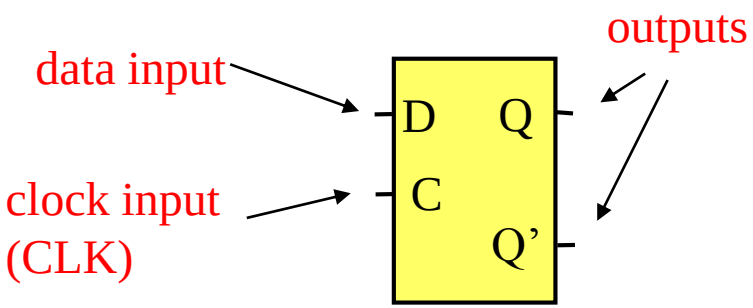
(adapted from Wakerly)

Example: Ring Counter in Multisim

The **ring counter (based on a shift register)** is the type of circuit we need to build to solve this car tail light design problem. Notice there is a **clock** and **3 D flip flops** (memory elements) and the high output is shifted to the right with each clock pulse. When the high output reaches the last flip flop then the high output starts at the first flip flop on the left (this is due to the "ring" connection). **We will now introduce the D flip flops and technology to build shift registers and ring counters.**



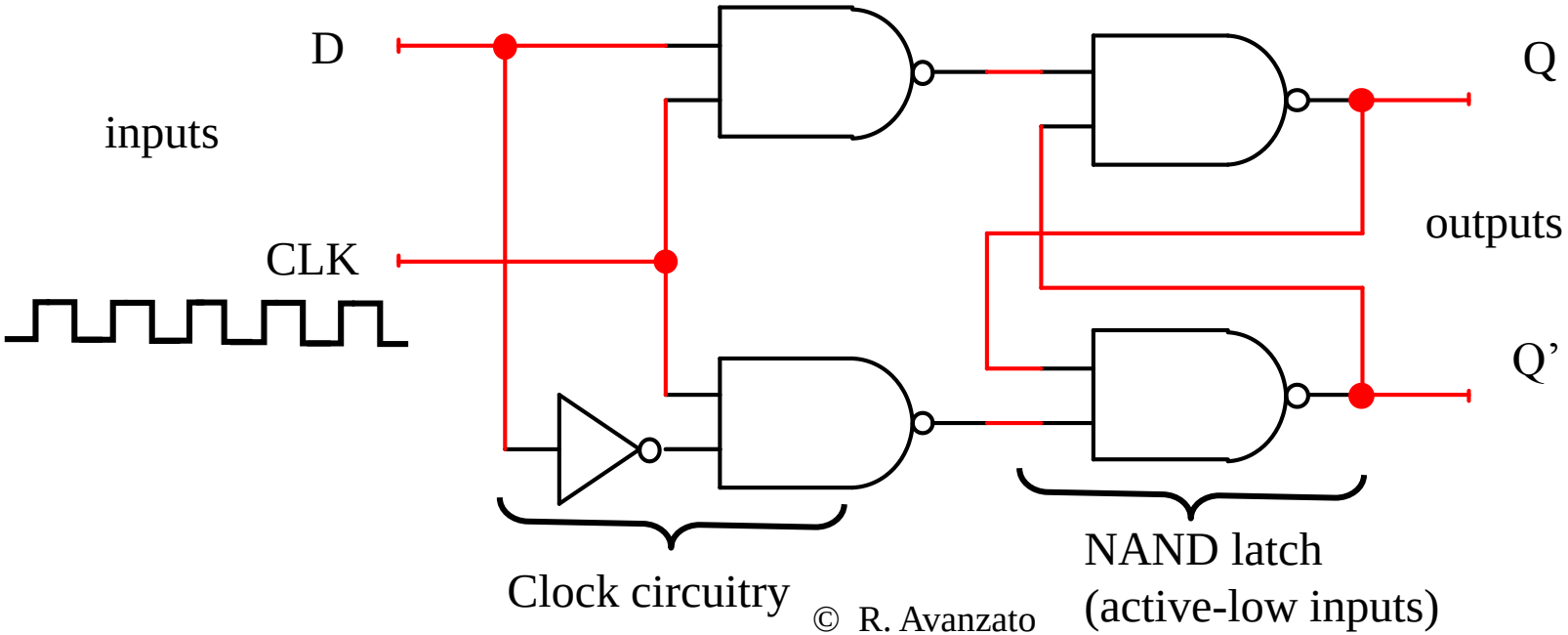
D Latch - 1



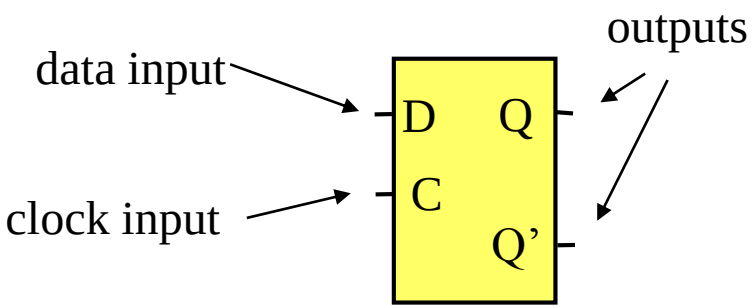
inputs		outputs	
D	**CLK**	**Q**	**Q'**
1	1	1	0 (set)
0	1	0	1 (reset)
X	0	Qold	Q'old

does not matter what D is here

A D latch will respond during the entire time the clock is high (pulse/level triggered). When the clock is low (0), the D latch will remain in the last state (memory).

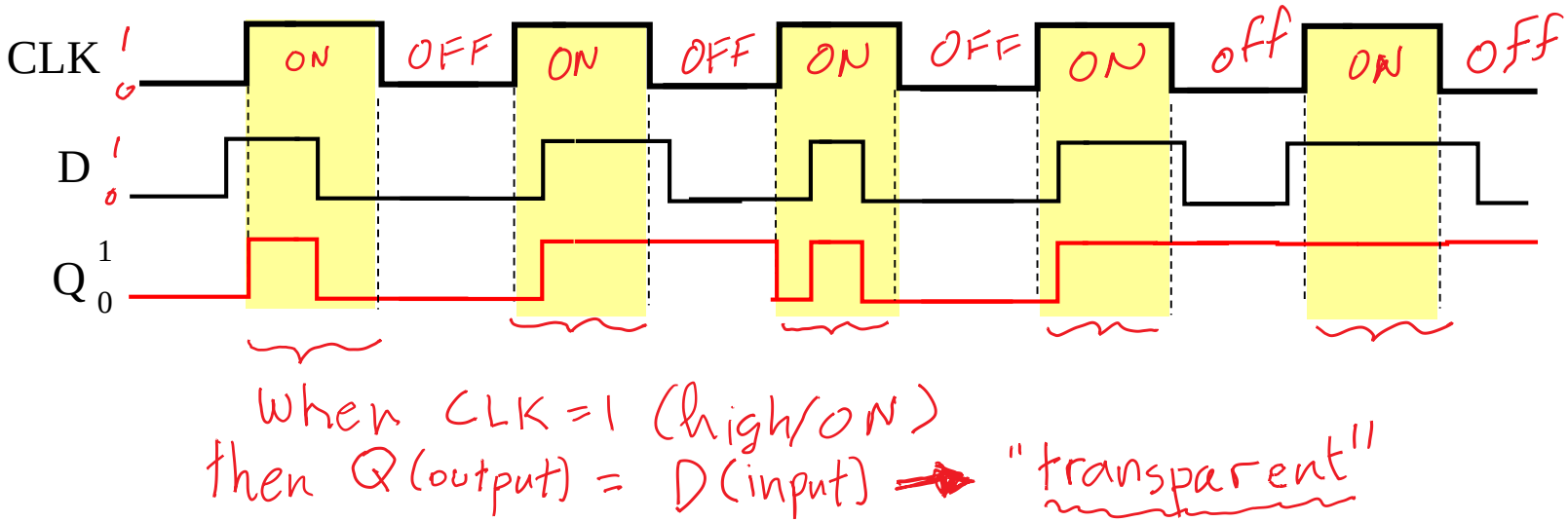


D Latch - 2

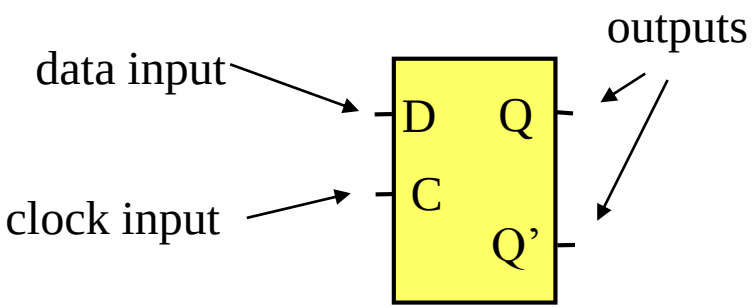


inputs		outputs	
D	**CLK**	**Q**	**Q'**
1	1	1	0 (set)
0	1	0	1 (reset)
X	0	Qold	Q'old

A D latch will respond during the entire time the clock is high. When the clock is low, the D latch will remain in the last state.



D Latch - 3

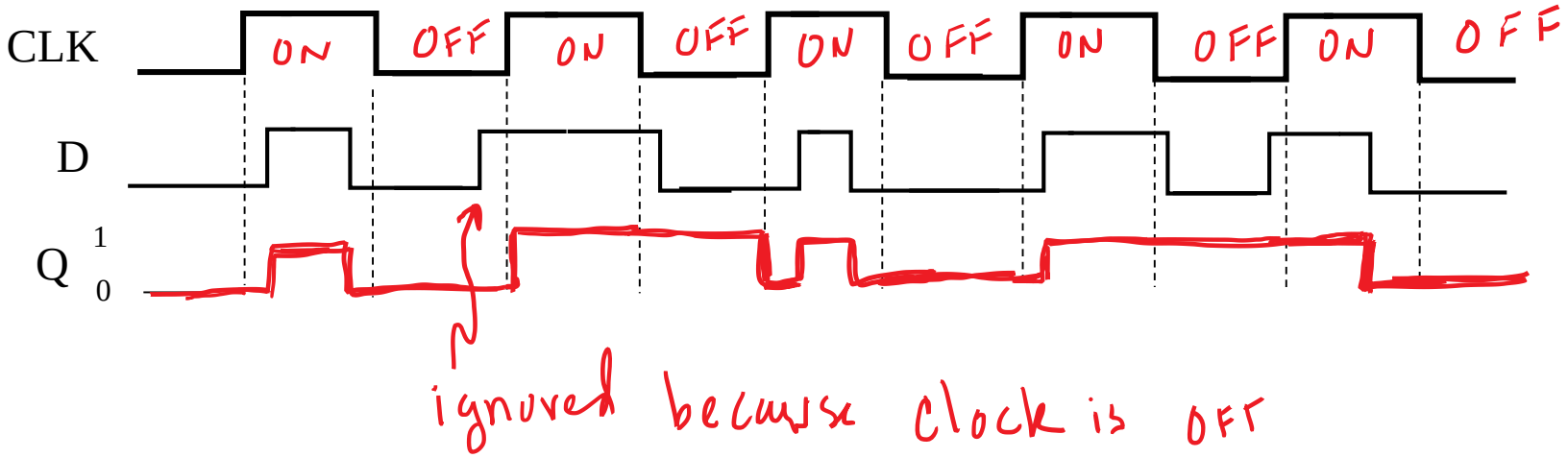


inputs		outputs	
D	**CLK**	**Q**	**Q'**
0	1	0	1
1	1	1	0
X	0	Qold	Q'old

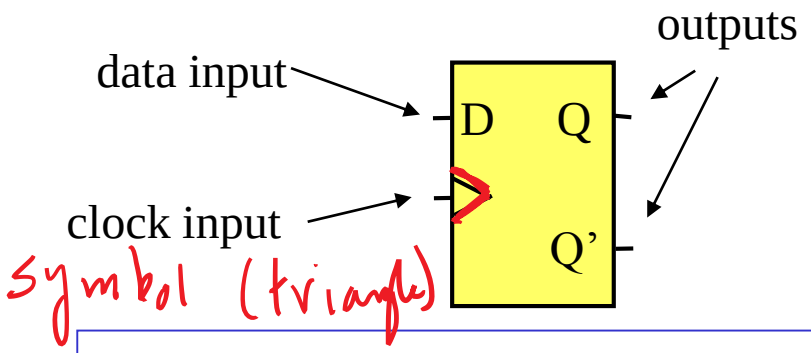
ignore input when CLK=0

when CLK is 0 (off) stay in old state

Exercise: Complete the timing diagram for Q



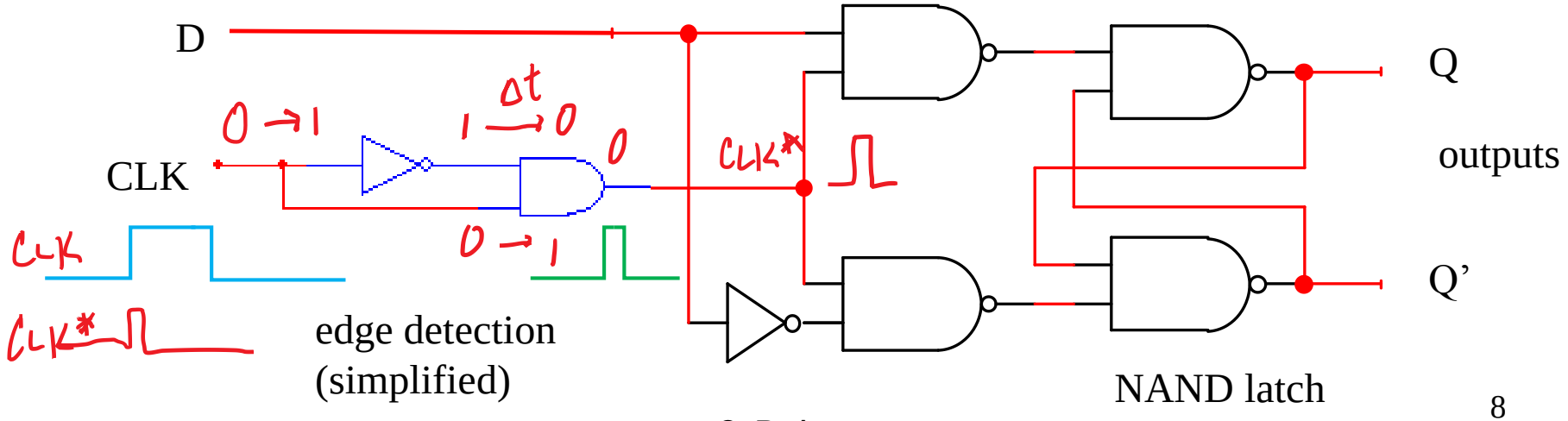
D Flip-flop - 1



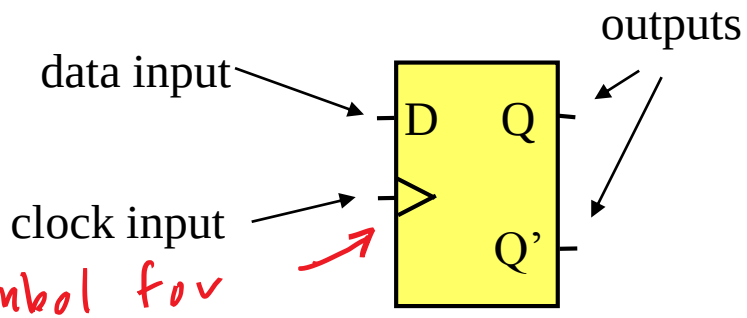
inputs		outputs	
D	**CLK**	**Q**	**Q'**
0	↑	0	1
1	↑	1	0
X	X	Qold	Q'old

symbol for pos. edge of clock

Positive-edge triggered D flip-flop. This FF only responds to input only during positive edge (0 →1) of the clock. FF output can only change during positive edge of clock. Use edge detector on clock, or master/slave (2 NAND latches) configuration. Edge detector circuit shown relies on propagation delay of inverter.



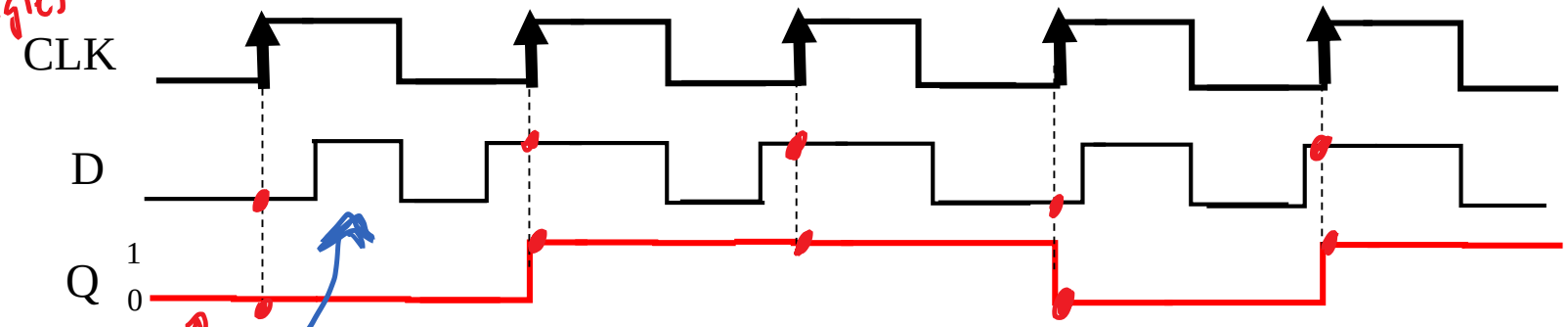
D Flip-flop - 1



Symbol for pos. edge triggered (triangle)

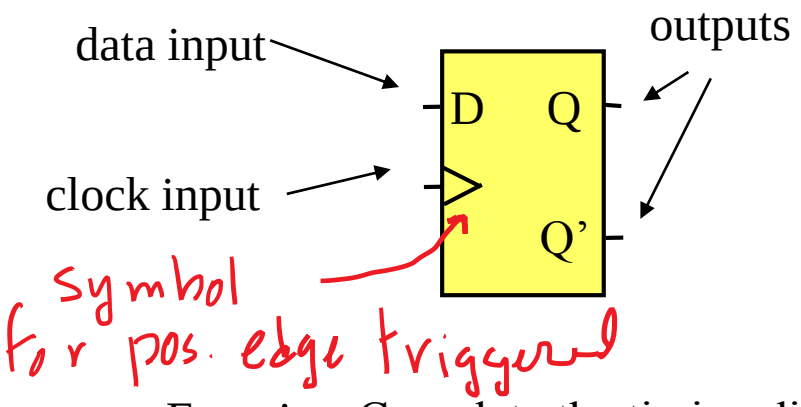
inputs		outputs	
D	**CLK**	**Q**	**Q'**
0	↑	0	1
1	↑	1	0
X	X	Qold	Q'old

Positive-edge triggered D flip-flop. This FF only responds to input only during positive edge (0 →1) of the clock. FF output can only change during positive edge of clock. Neglect propagation delay for now.



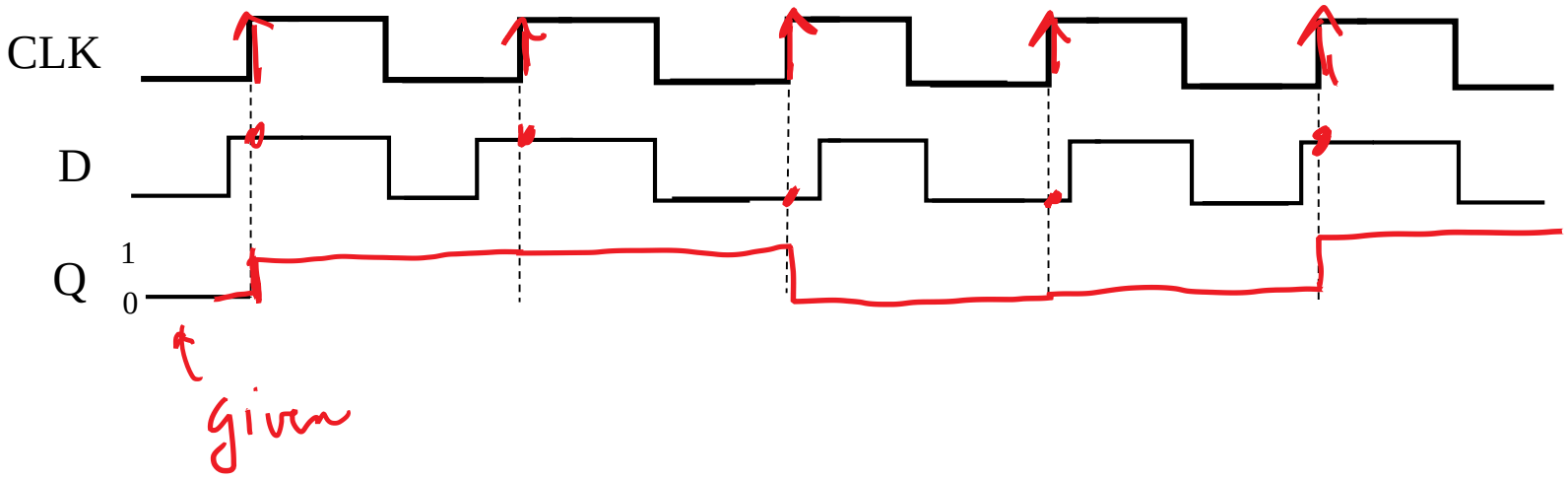
FF can only change during pos. edge ↑ of clock pulse

D Flip-flop - 2

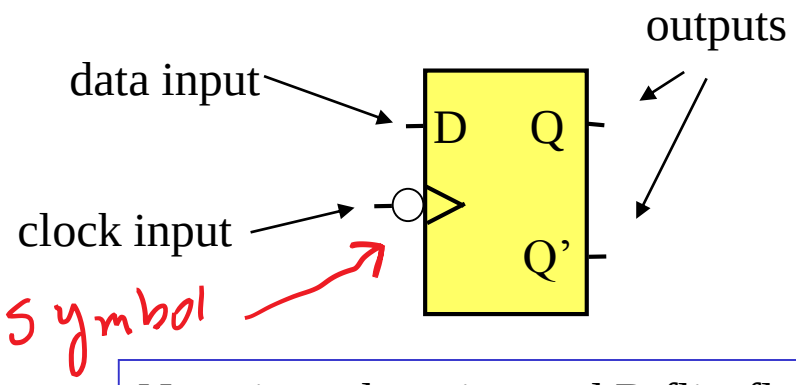


inputs		outputs	
D	**CLK**	**Q**	**Q'**
0	↑	0	1
1	↑	1	0
X	X	Qold	Q'old

Exercise: Complete the timing diagram for Q and Q'.



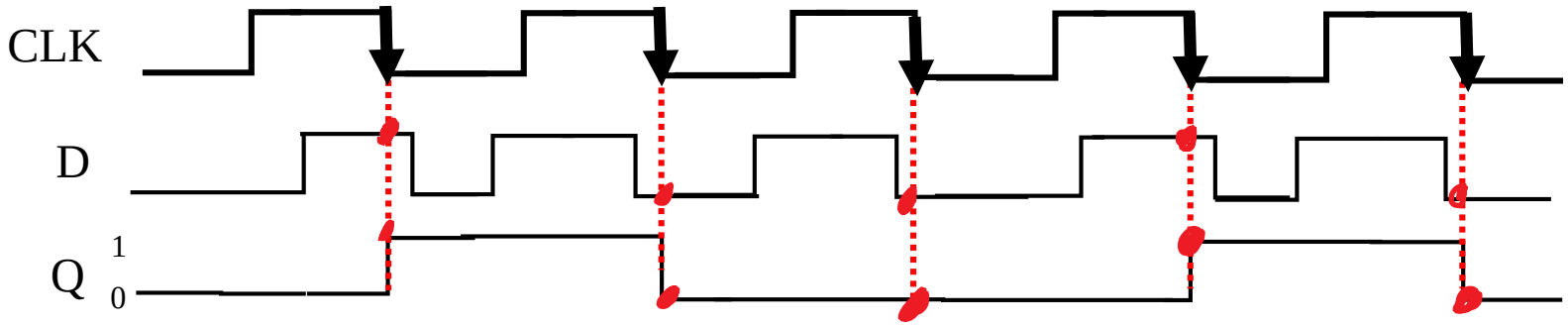
D Flip-flop - 3



inputs		outputs	
D	**CLK**	**Q**	**Q'**
0	↓	0	1
1	↓	1	0
X	X	Qold	Q'old

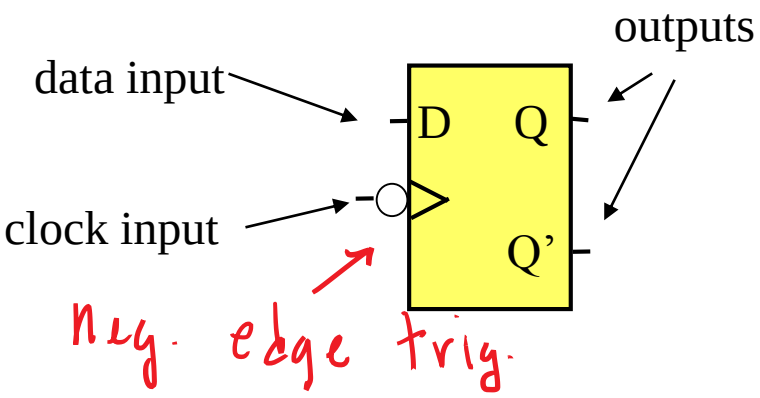
symbol for neg. edge of clock

Negative-edge triggered D flip-flop. This FF only responds to input during negative edge of clock (1 → 0). FF output can only change during negative edge of clock. Neglect propagation delay for now.



Can only change output at neg. edge of clock (↓)

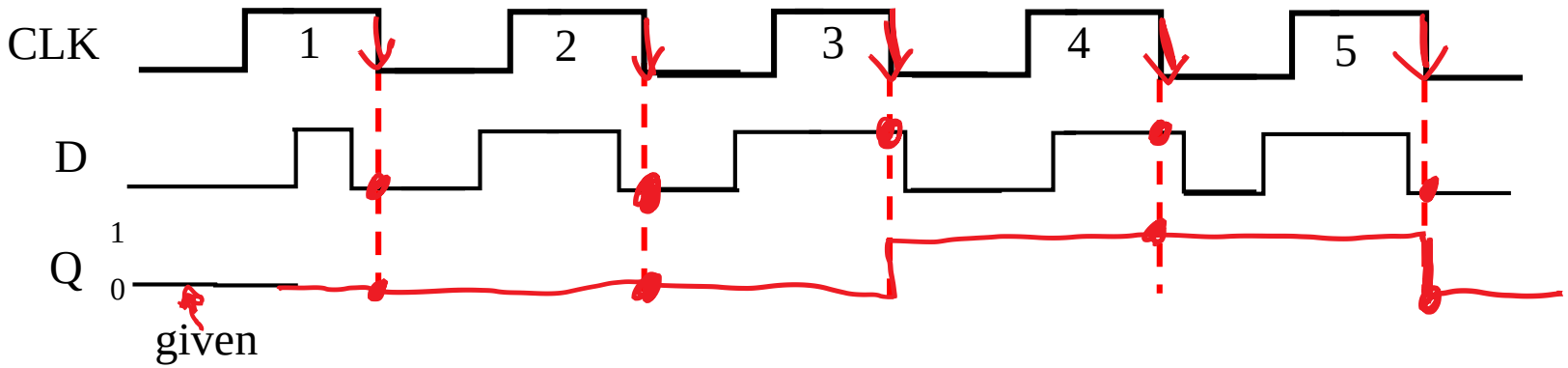
D Flip-flop - 4



inputs		outputs	
D	**CLK**	**Q**	**Q'**
0	↓	0	1
1	↓	1	0
X	X	Qold	Q'old

See Multisim Demo of D FF

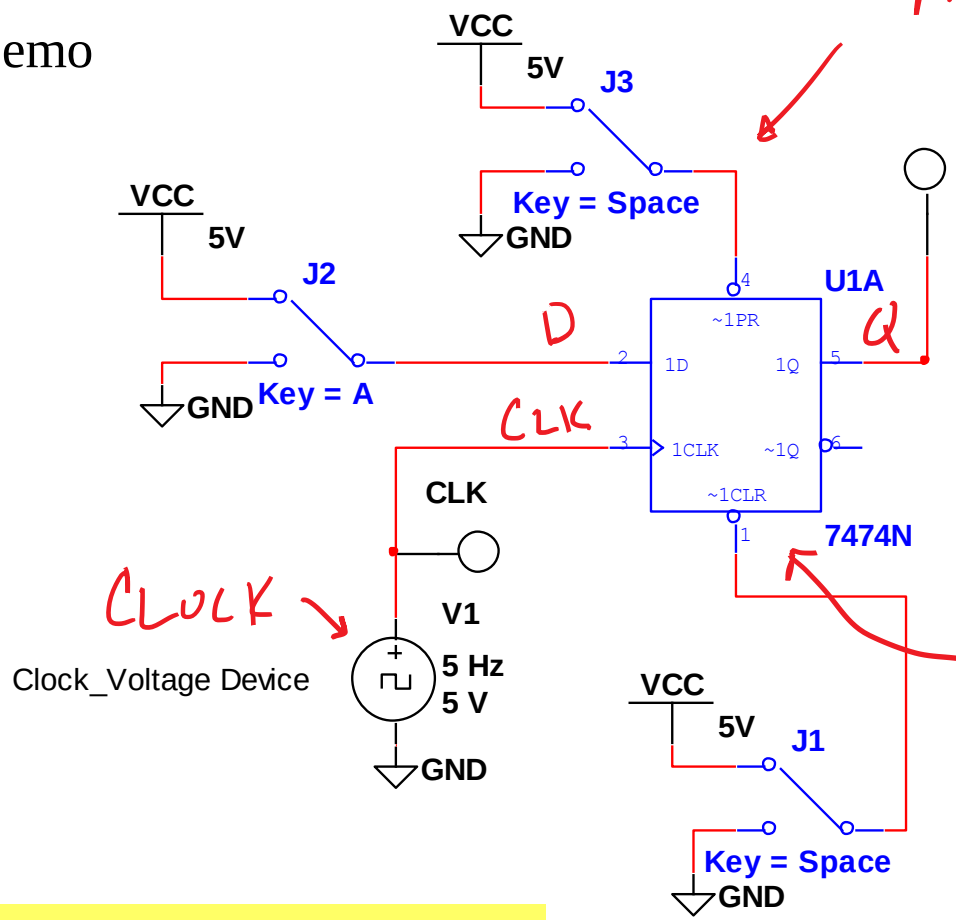
Exercise: complete the timing diagram for Q



D FF Simulation (MultiSim)

any time

D Flip Flop Demo



Asynchronous input
Active-low
PRE → force Q = 1
high priority

Asynchronous input
Active-low
CLR → make Q = 0

Try it!!!
(file can be downloaded from Canvas)

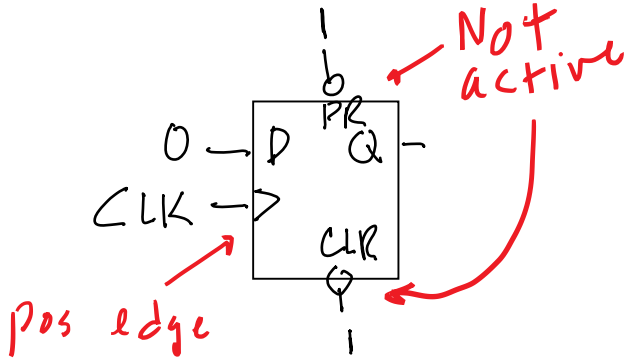
Sample Questions

#1. When a flip-flop is "set", then the outputs of the flip-flop are

a) Q=1, Q' =0 b) Q=0, Q'=1 c) Q=0, Q'=0 d) Q=1, Q'=1

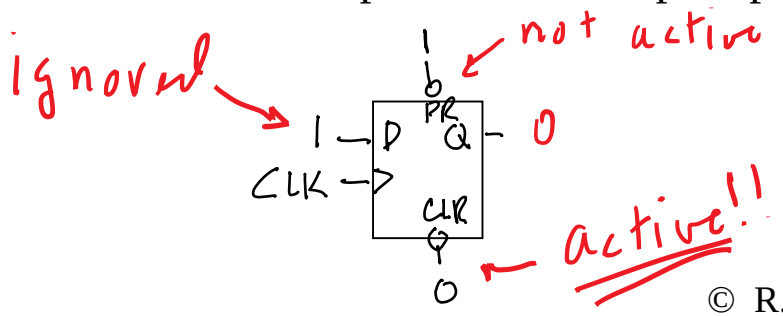
Set Reset or clear Q is never equal to Q'

#2. What is the output of this D flip-flop below after 1 clock pulse?



a) Q= 1, Q'= 0
b) Q = 0, Q' = 0
c) Q = 0, Q' = 1
d) Q = 1, Q' = 1

#3. What is the output of this D flip-flop below after 1 clock pulse?



a) Q = 0, Q' = 1
b) Q = 0, Q' = 0
c) Q = 1, Q' = 0
d) Q = 1, Q' = 1

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D FFs, Shift Registers, Ring Counters

Topics:

- Design Problem — **Video part 1 of 4**
- Clocked Flip-flops (FFs)
- D flip-flop
- Sample Questions

- D FF applications - shift register — **Video part 2 of 4** ←
- Setup and hold times
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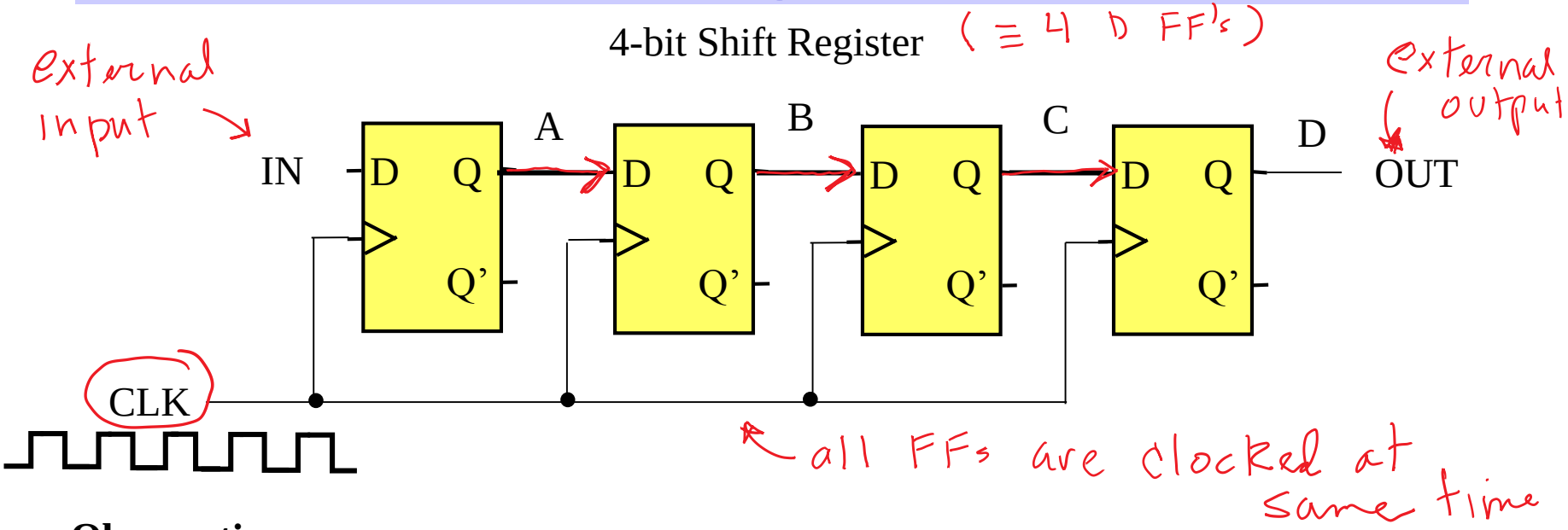
- HW #8 Car Taillights Circuit — **Video part 4 of 4**

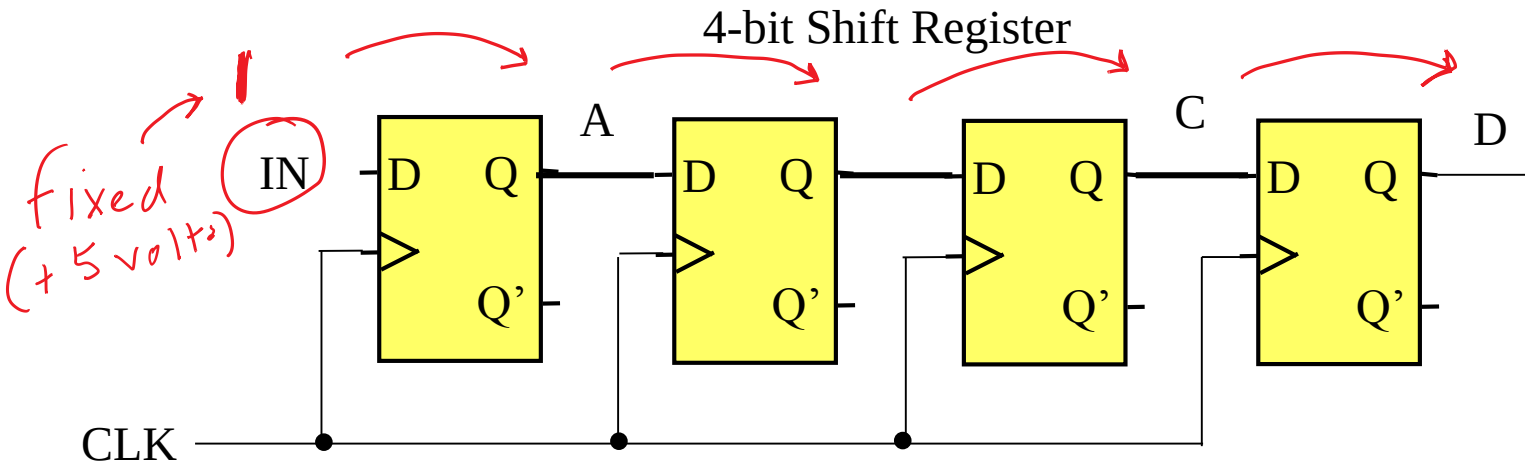
Shift Register - 1



Observations:

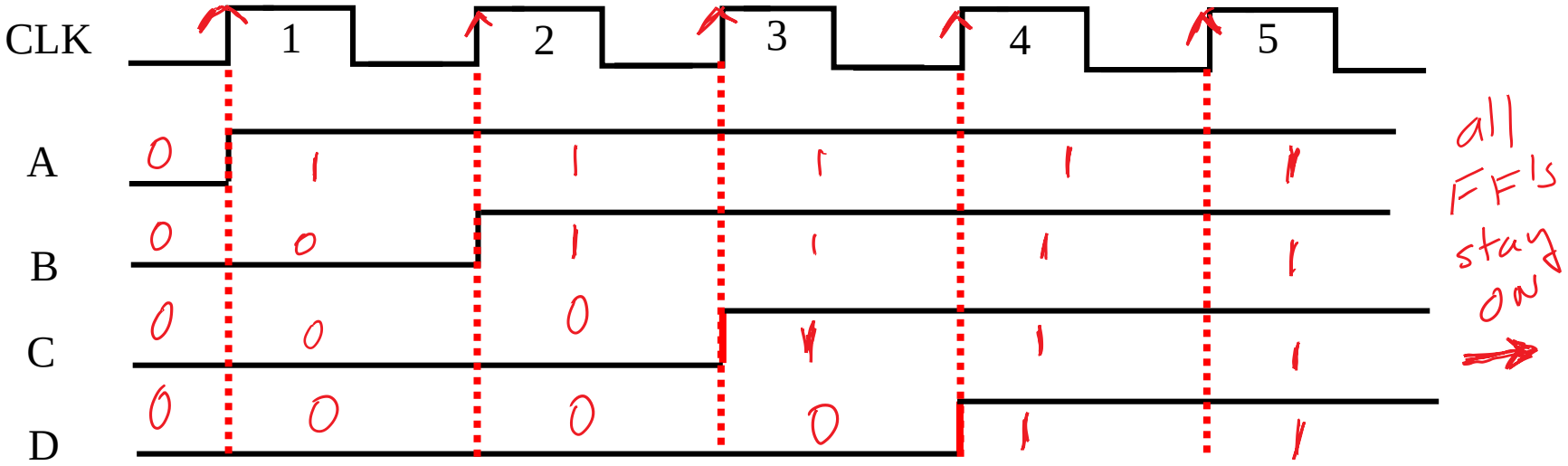
- A 4-bit shift register uses 4 D FFs. A shift register can be n bits.
- Each FF is connected directly to the clock.
- The output of one FF is connected to the input of the next FF.
- Information (bits) shift to the right at each clock pulse (positive edge).
- One clock pulse results in a shift of exactly one FF to the right.
- A, B, C, D are the outputs of the FFs.
- FF must be initialized (set or reset) before operation.
- Shift registers can be constructed from negative-edge triggered FFs, but are most commonly constructed from positive-edge triggered D FFs. D Latches cannot be used.

Shift Register - 2



See Multisim Demo of Shift Reg.

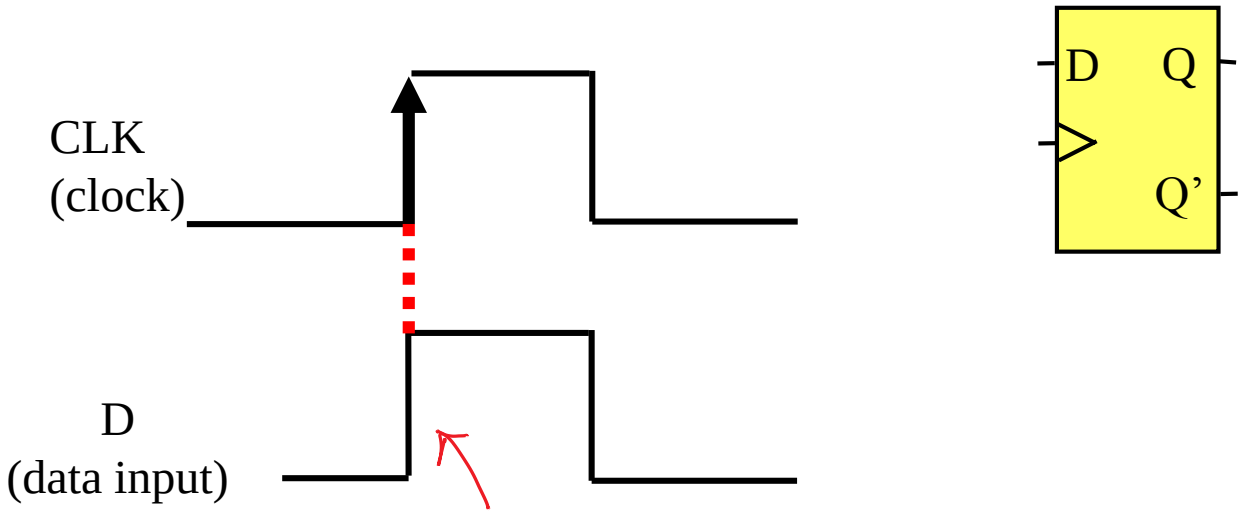
***Assume initially that A=B=C=D= 0 (all FFs are reset). Set IN to 1.



Generalize to "n" bits

FF Setup and Hold Times - 0

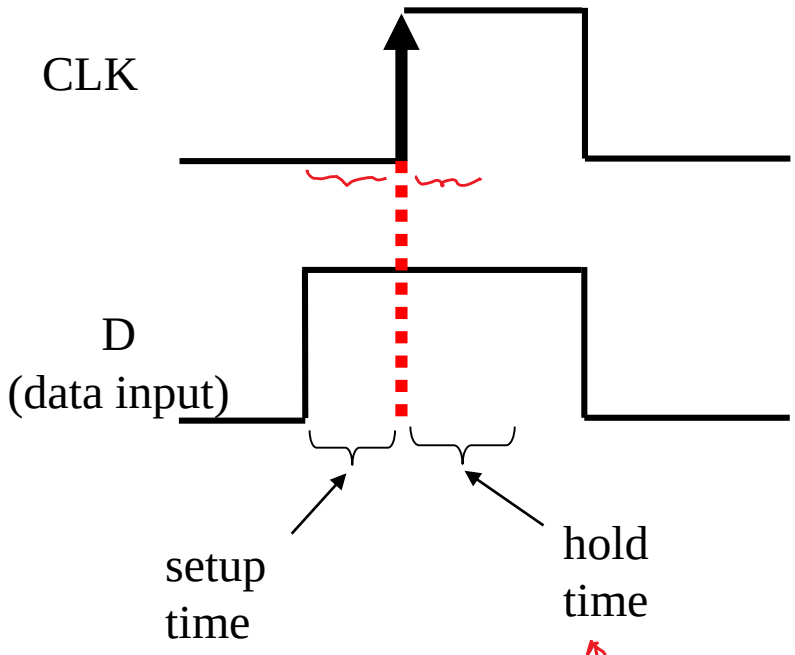
Problem: What happens if a data input (for a positive edge triggered D FF) is changing state (0 to 1) the exact same time that the clock is changing state (0 to 1)? What is FF output Q?



data is changing same time as pos. edge of clock

FF Setup and Hold Times - 1

What happens if a data input (for a positive-edge triggered D FF) is changing state (e.g. 0 to 1) the same time that the clock is changing state (e.g. 0 to 1)?

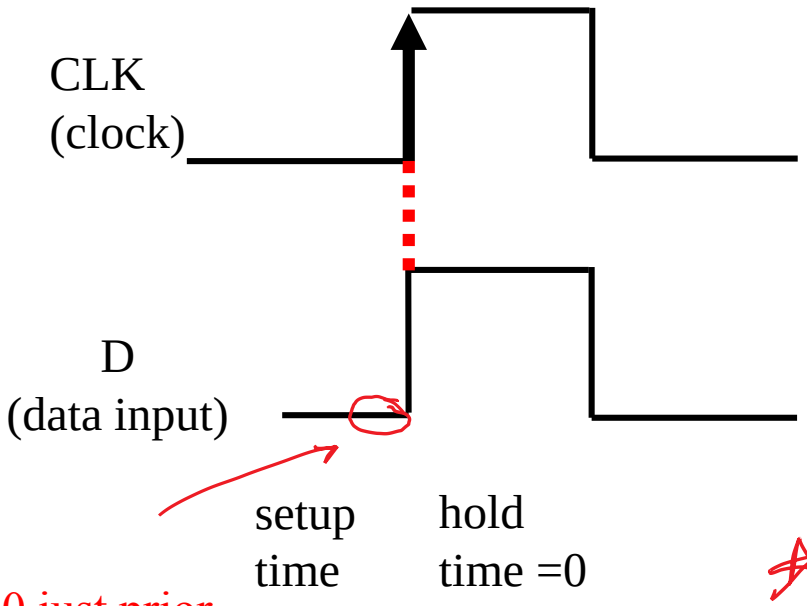


Generally, for a FF to properly "see" the data input, D, at a clock edge, the data input D should be present (not changing) at least the specified "setup time" before the edge, and the same data input should be present (not changing) after clock edge specified by the "hold time". We can assume all of our edge-triggered flip-flops have a hold time of 0.

↖ assume = 0 for modern FF

FF Setup and Hold Times - 2

What happens if a data input (for a D FF) is changing state (1 to 0, or 0 to 1) the same time that the clock is changing state (1 to 0, or 0 to 1)?



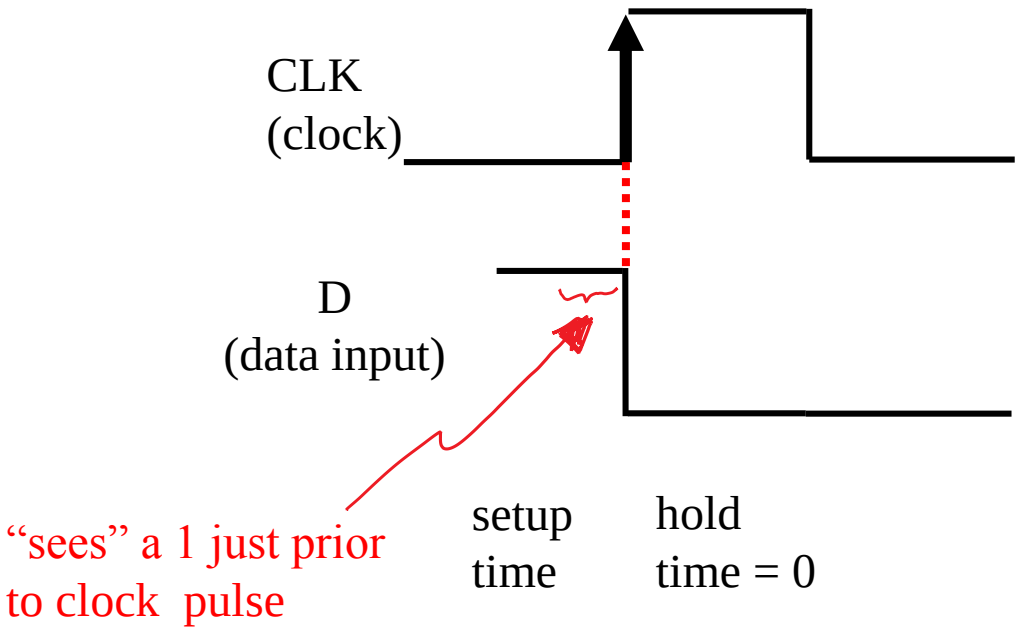
What value of data input D does a positive-edge triggered D FF "see" at the positive clock edge (a 1 or a 0)?

Input D is changing at the same time as the clock.

Assume hold time = 0

Answer: D FF will "see" a D of 0 (that is value of data input D just before clock transition.)

FF Setup and Hold Times - 3



What value of data input D does a positive-edge triggered D FF "see" at the positive clock edge (a 1 or a 0)?

Input D is changing at the same time as the clock.

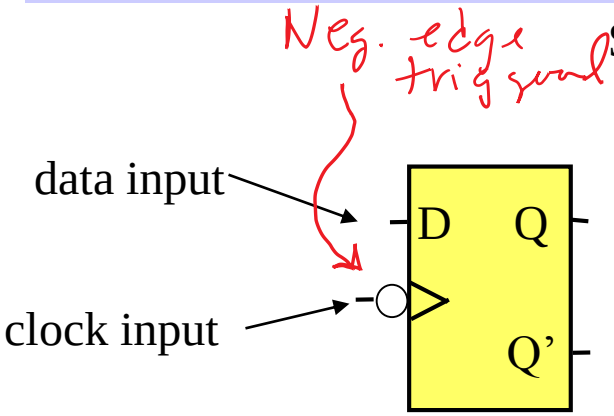
Assume hold time = 0

Answer: D FF will "see" a D of 1 (that is value of data input D just before clock transition.)

Similar operation is true for negative-edge triggered FFs.

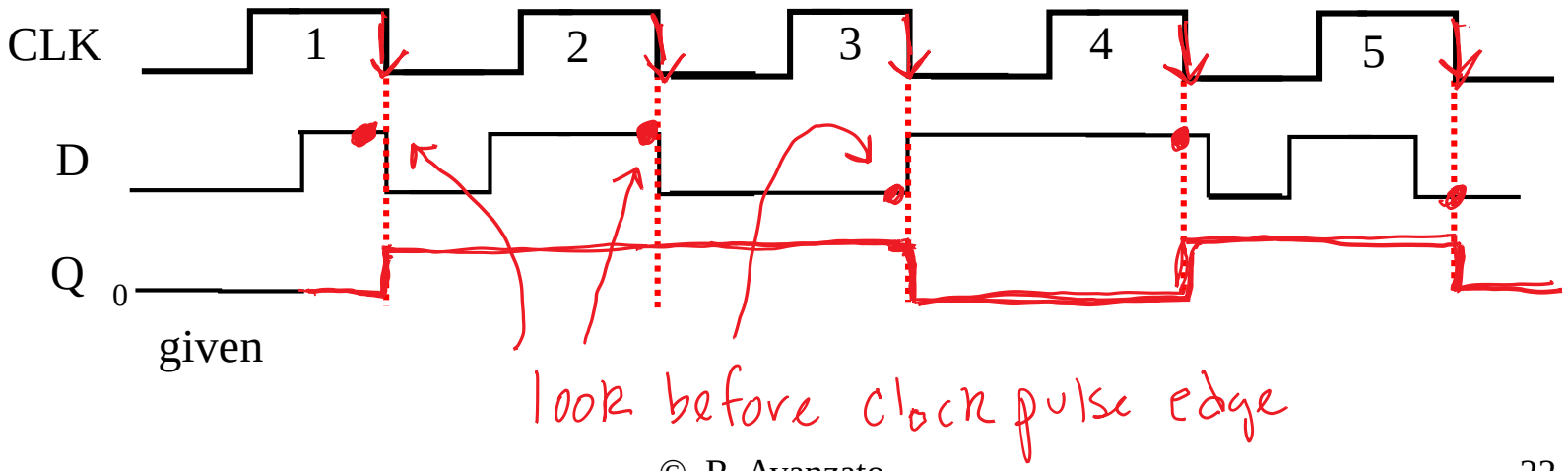
FF Setup and Hold Times - 4

Sample Question



D	CLK	Q	Q'
0	↓	0	1
1	↓	1	0
X	X	Qold	Q'old

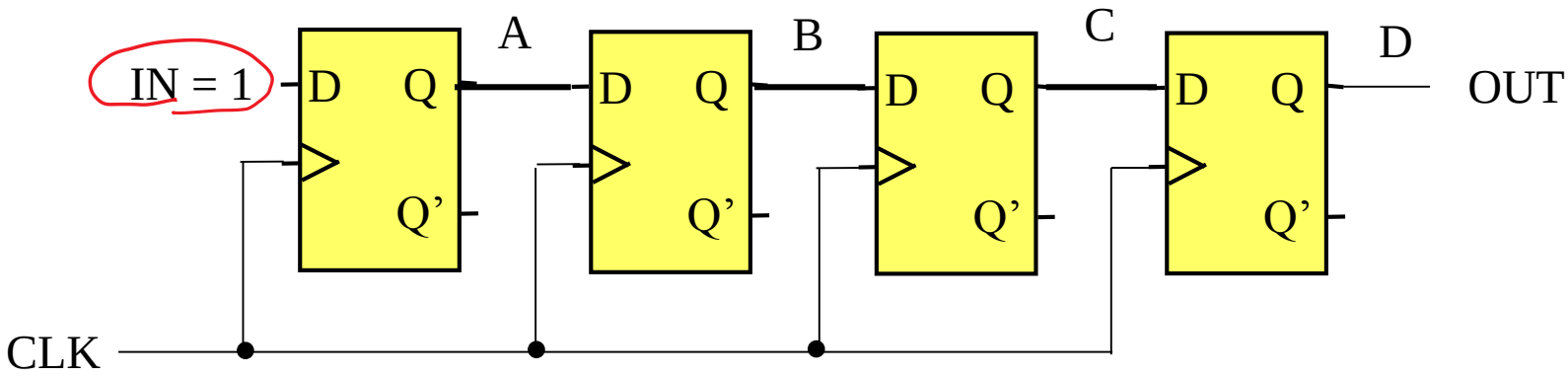
Exercise: complete the timing diagram for Q. Notice that D input changes at the same time as the clock changes. Assume hold time = 0.



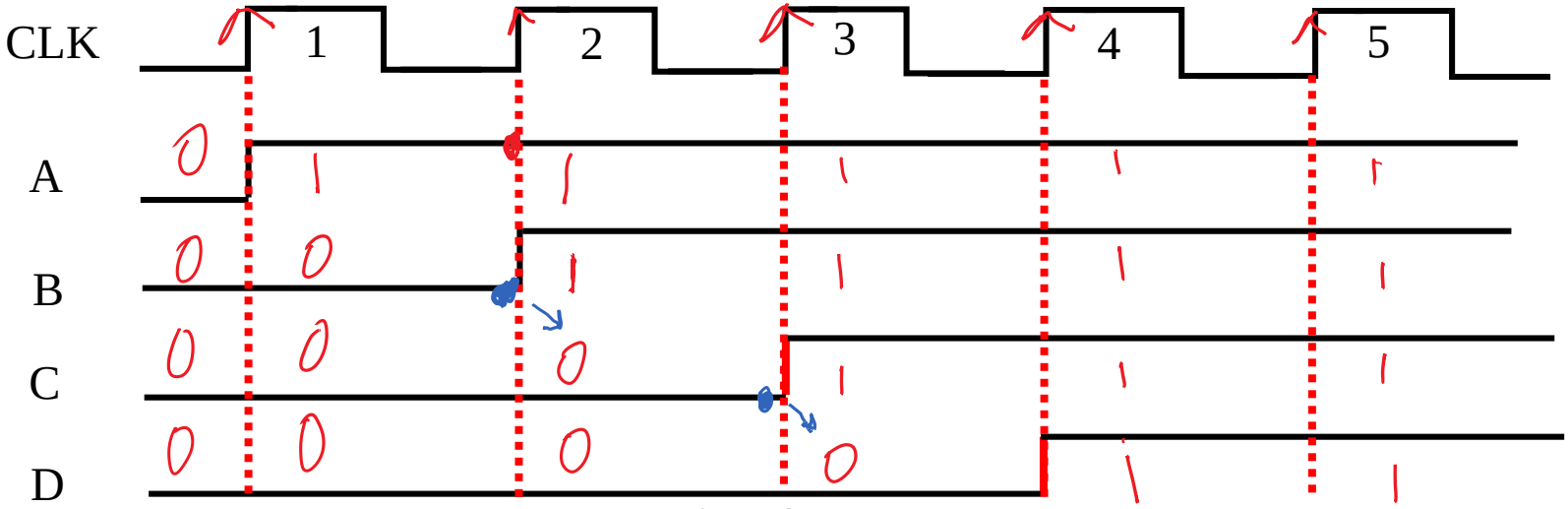
Shift Register – setup & hold

pos. edge triggered

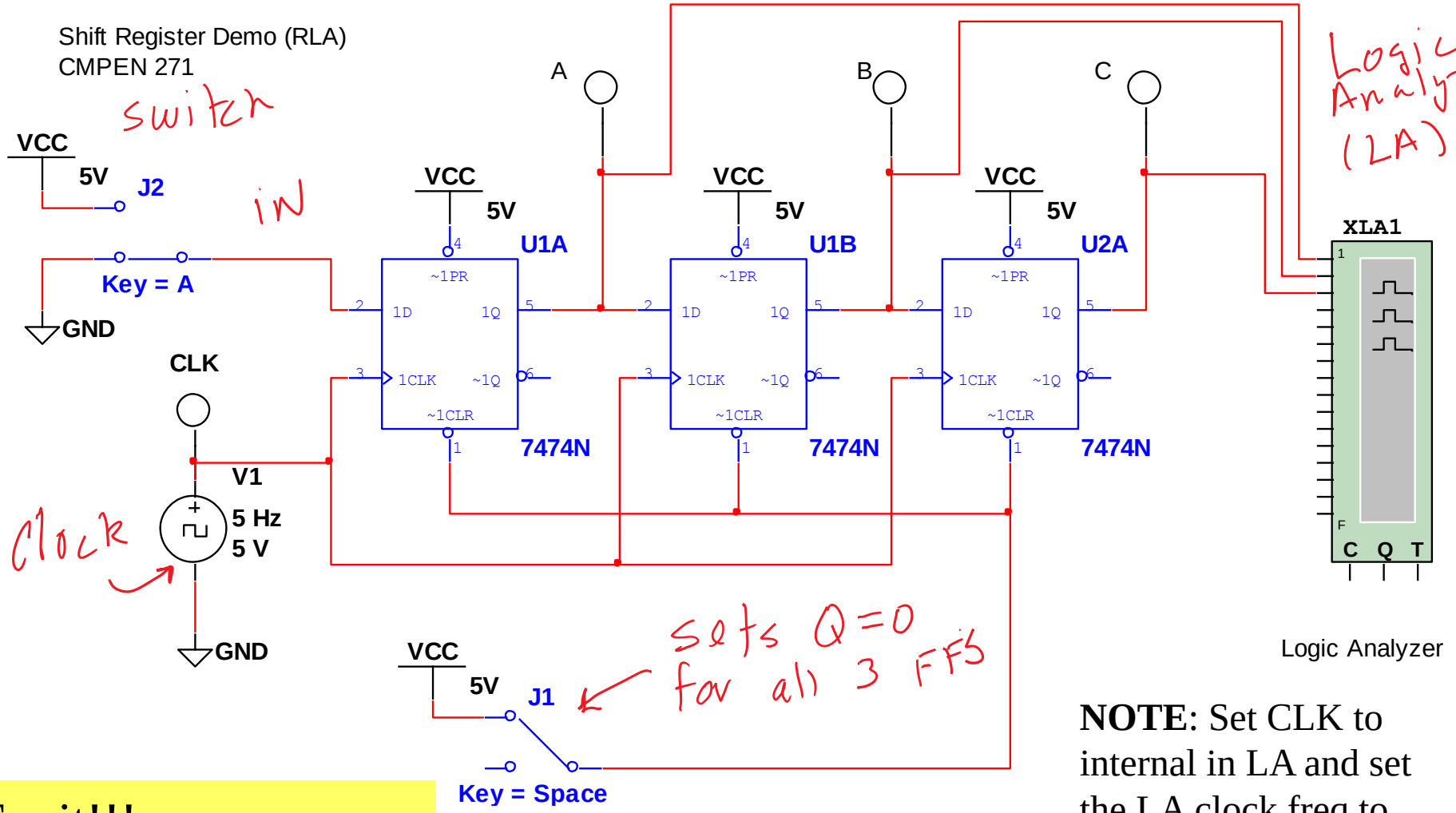
4-bit Shift Register



***Assume initially that A=B=C=D= 0 (all FFs are reset). Set IN to 1.



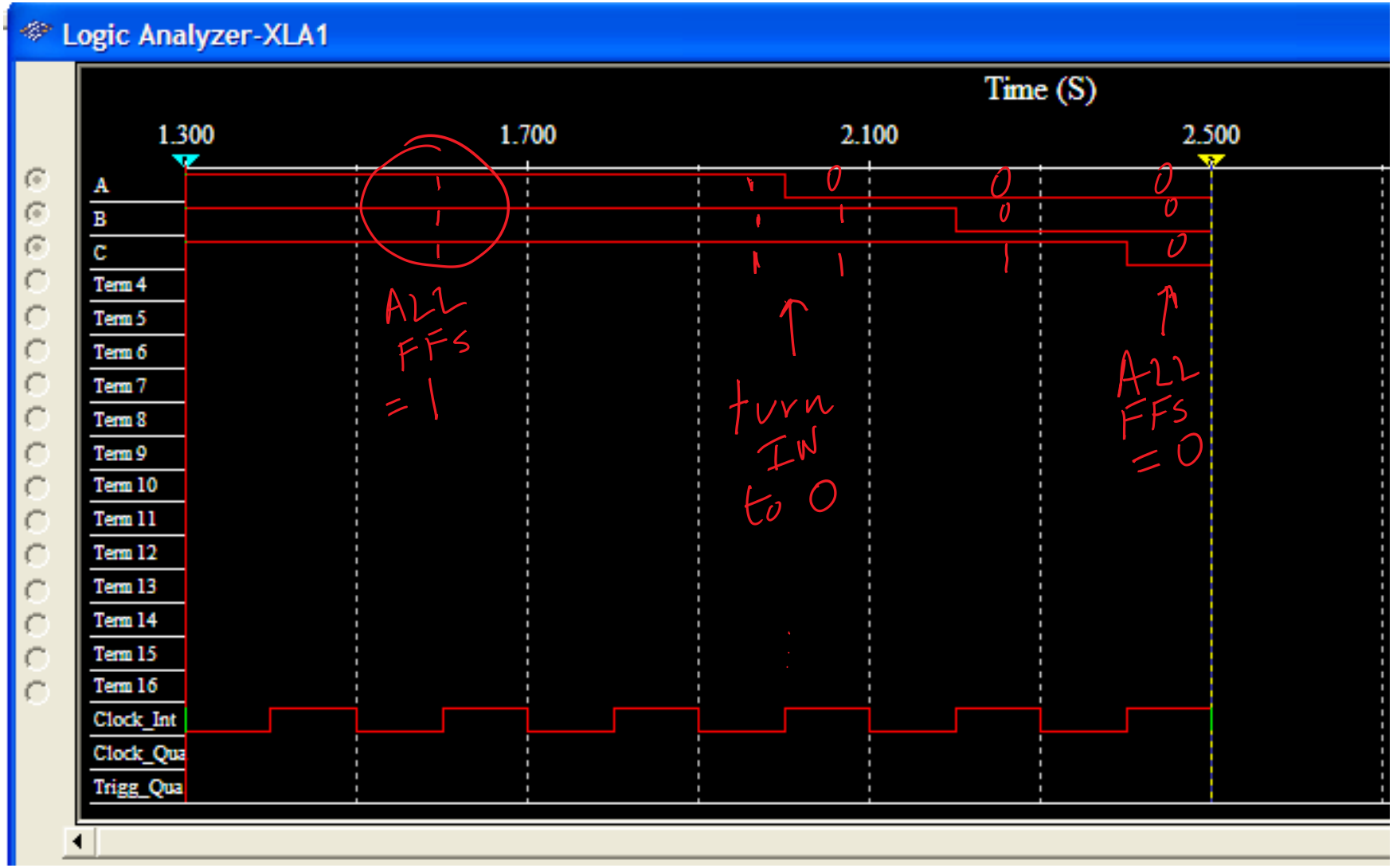
Shift Register Simulation (MultiSim)



NOTE: Set CLK to internal in LA and set the LA clock freq to same as clock frequency for circuit.

Try it!!!
(file can be downloaded from Canvas)

Shift Register Simulation (MultiSim)



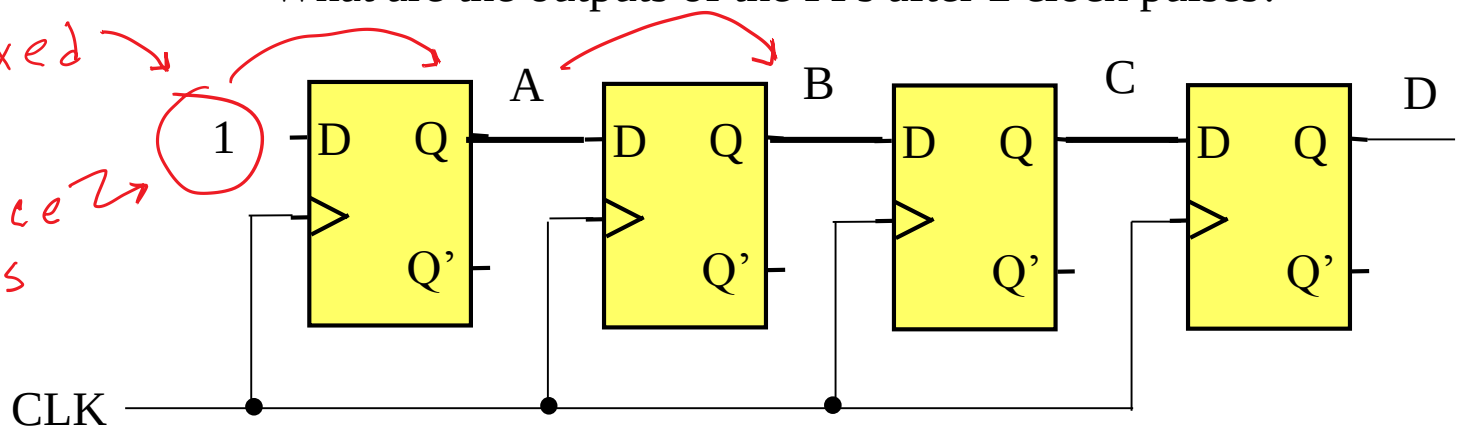
Hint → MultiSIM → Tools → Capture Screen Area

Sample Questions

#1. A 3-bit shift register has how many D flip-flops?

a) 3 b) 4 c) 6 d) 8

#2. Given the 4-bit shift register below. If initially A = B = C = D = 0. What are the outputs of the FFs after 2 clock pulses?



a) A = 0, B = 0, C = 0, D = 0
b) A = 0, B = 0, C = 1, D = 1
c) A = 1, B = 1, C = 0, D = 0
d) A = 1, B = 1, C = 1, D = 1

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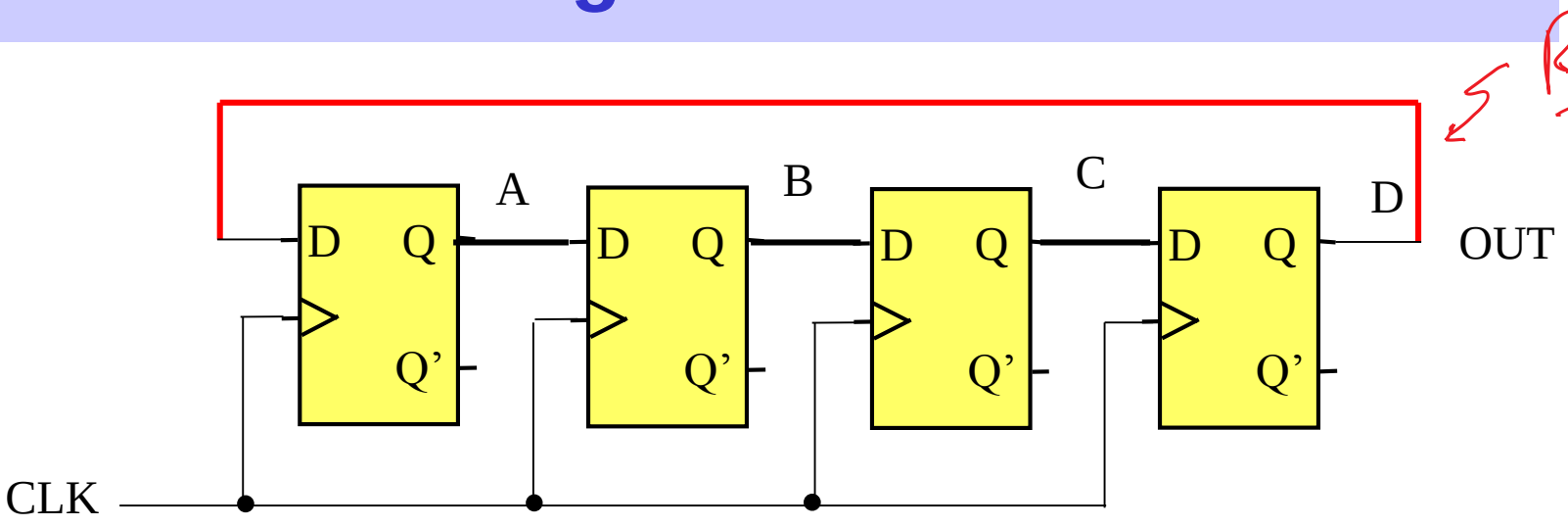
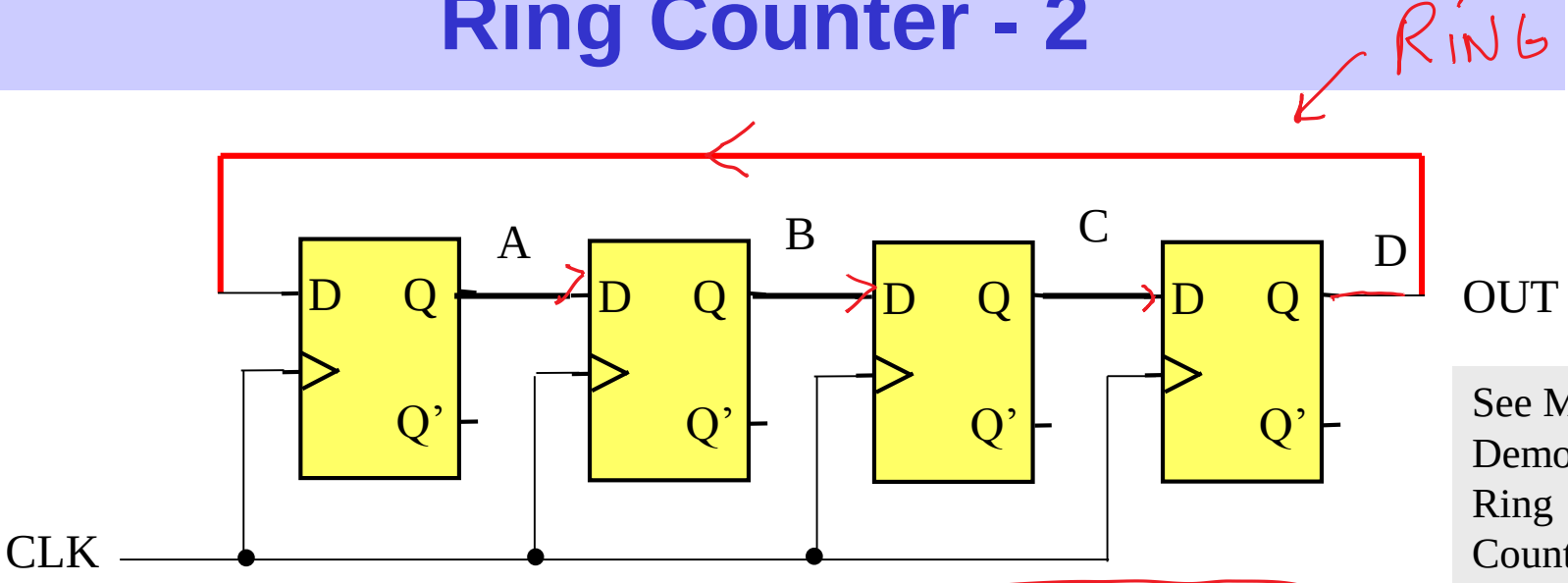
Ring Counter - 1



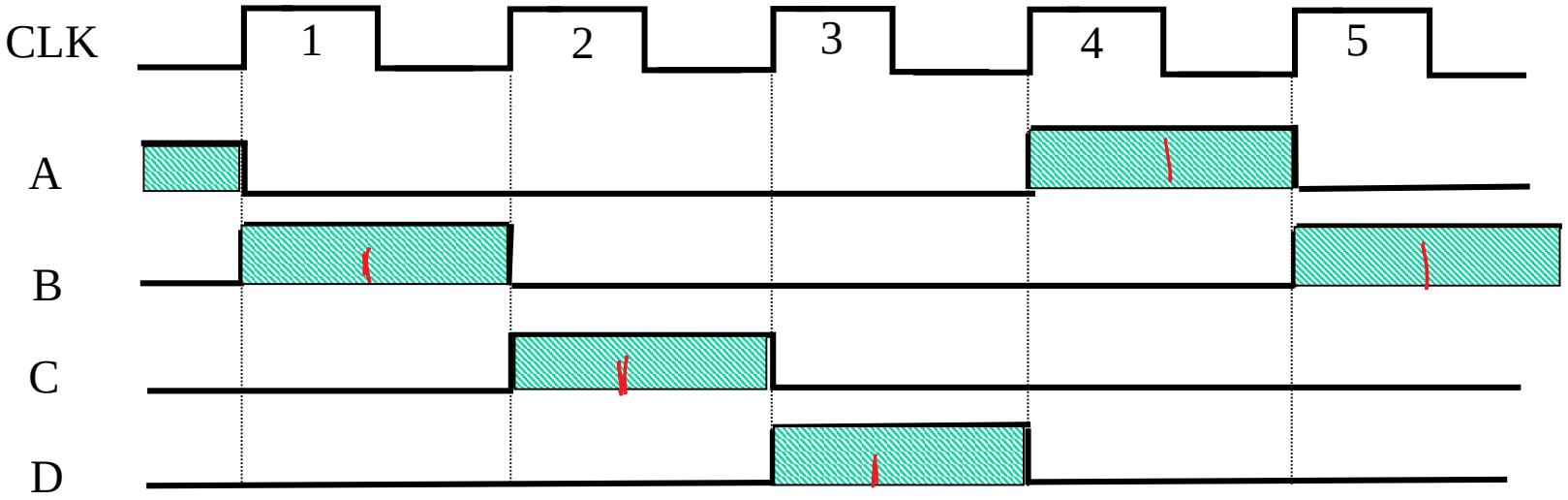
- A **ring counter** is a modified shift register. A 4-bit ring counter uses 4 D FFs.
- In a ring counter, the output of the rightmost FF is connected to the input of the leftmost FF (this forms a "loop" or a "ring".)
- Generally, ring counters are constructed with **positive-edge triggered D flip-flops**.
- A ring counter can be of **any arbitrary size** (that is, any number of FFs).
- The FF in a ring counter **must be initialized** carefully. Most commonly, all FF are set to zero, except one FF which is set to 1. Other patterns are possible, but then the analysis becomes more difficult.
- For our purposes, **set one (any one) FF output to 1**, and set the others to 0.
- Ring counters can be use to **control (turn on and off) devices** in a desired sequence.

Ring Counter - 2



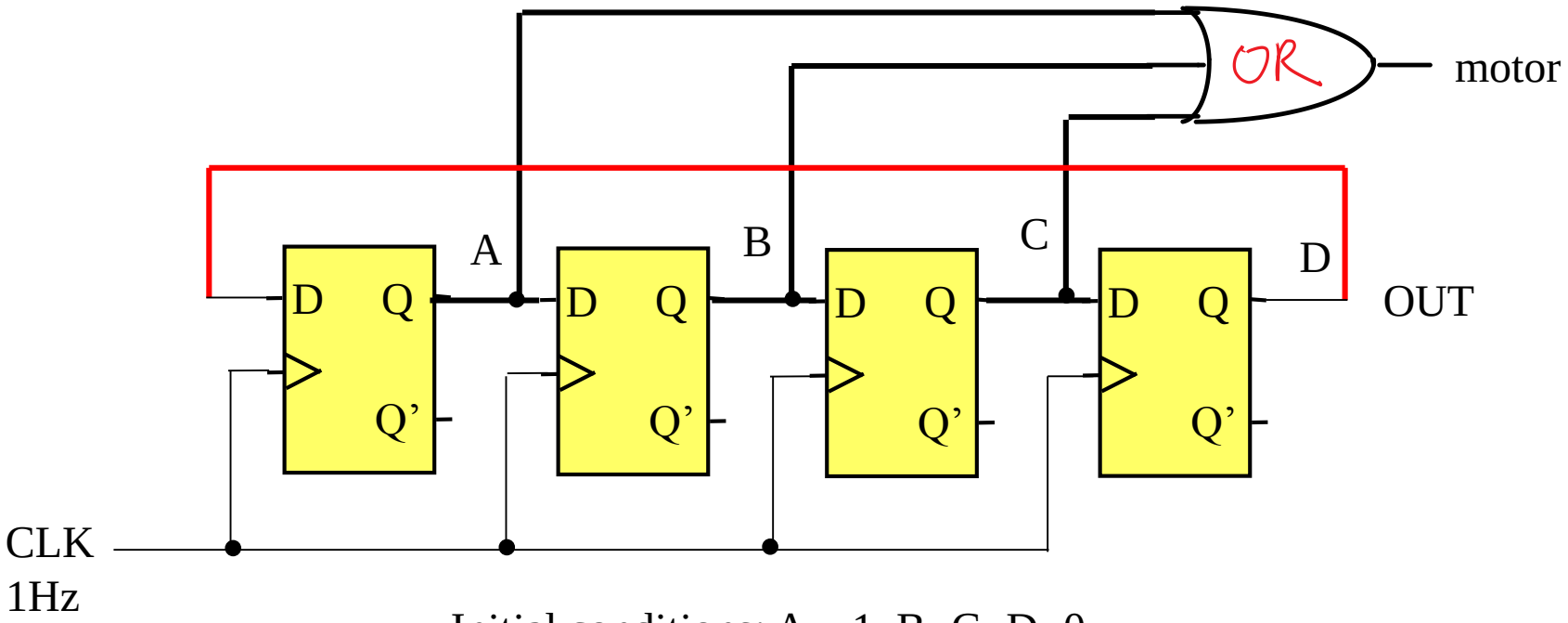
See Multisim Demo of Ring Counter

***Assume initially that A=1, B=C=D= 0; One FF must be set to 1, others to 0.



Ring Counter - 3

Example: Design a sequential control circuit that turns on a motor for 3 seconds, then off for 1 second, then repeat. Assume a 1Hz clock is available. Include FF initialization.



Initial conditions: A = 1, B=C=D=0

- Can you design above with only one inverter instead of 3-input OR gate? YES

Remove OR gate; Connect output to inverter

Ring Counter - 4

Practice Design Exercise: Design a sequential control circuit that **turns on a motor for 2 seconds, then turns off motor for 3 seconds**, then repeats. Assume a 1Hz clock is available. Include FF initialization.

total # of states = 5
so, need 5 FFs in Ring counter

What size ring counter is necessary? 5-bit

How many FF are needed? 5

Show circuit. see later slide

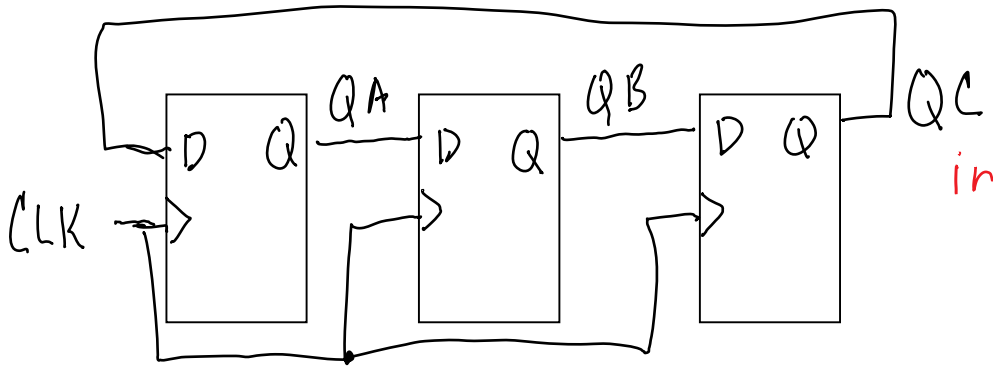
Question: Can a Decoder, counter, and clock be used to solve this problem? No

Alternative design: Try solving above motor control problem by using 1 external FF instead of OR gates. The output of this external FF (Q) is connected directly to the motor. The outputs of the FFs in the ring counter are selectively connected to the asynchronous set and rest of the external FF. What are pros and cons of this desing?

see later slide

Review Questions

#1. Consider the 3-bit ring counter below. Assume initially **QA=1, QB=0, QC=0**.



	QA	QB	QC
initial	1	0	0
①	0	1	0
②	0	0	1
③	1	0	0

What are the FF outputs after 3 clock pulses?

a) QA=1, QB = 1, QC=1

b) QA=0, QB = 1, QC=0

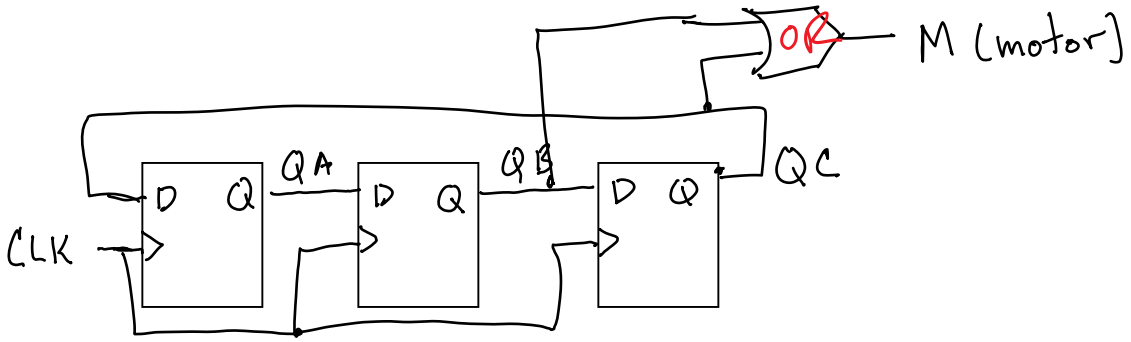
c) QA=0, QB = 0, QC=1

d) QA=1, QB = 0, QC=0

ANSWER

Review Questions

#2. Consider the ring counter circuit below. Assume initially **QA=1, QB=0, QC=0**.



QA	QB	QC	M
1	0	0	0
0	1	0	1
0	0	1	1
1	0	0	

repeats

How would you describe the behavior of the motor output M?

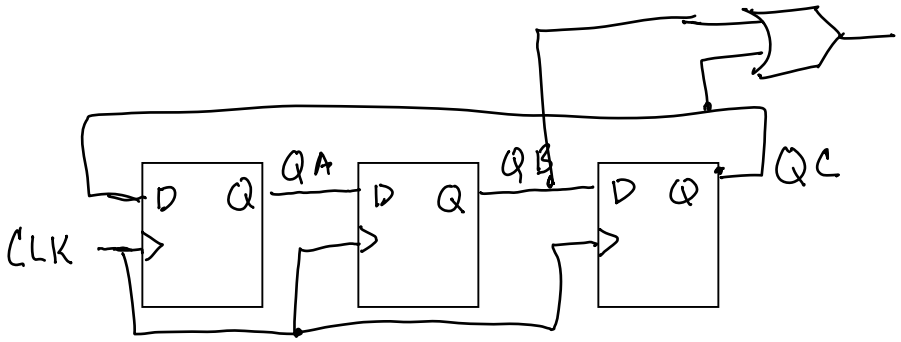
a) M is on for 1 second, off for 2 seconds, then repeat
b) M is on for 3 seconds, off for 1 second, then repeat
c) M is on for 2 seconds, off for 1 second, then repeat
d) M is always on
e) M is always off

Answer

Review Questions

Not recommended

#3. Consider the ring counter circuit below. Assume initially **QA=1, QB=1, QC=0**.



	QA	QB	QC	M
initial	1	1	0	1
1	0	1	1	1
2	1	0	1	1
3	1	1	0	1

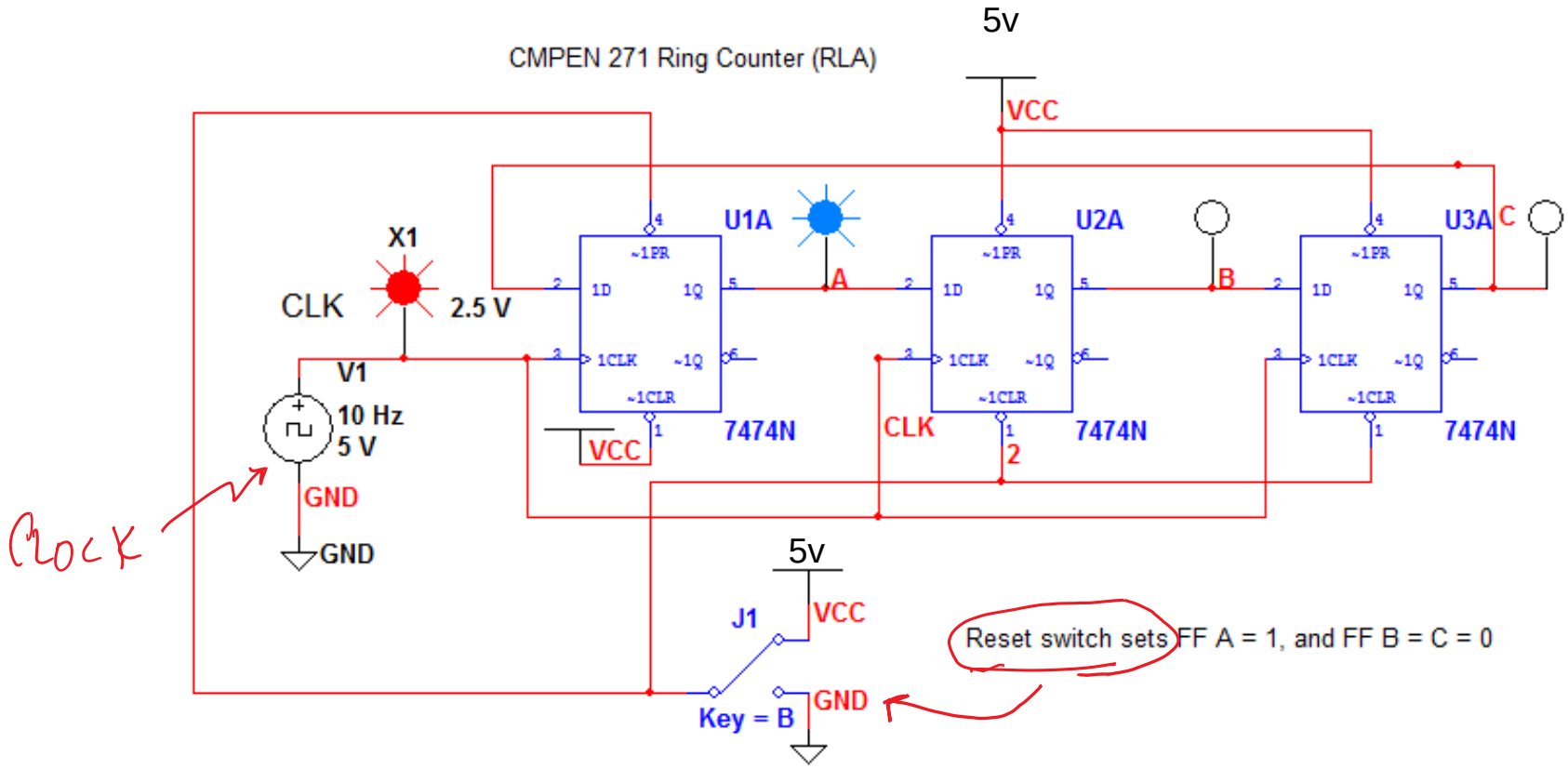
repeat

How would you describe the behavior of the motor output M?

a) M is on for 1 second, off for 2 seconds, then repeat
b) M is on for 3 seconds, off for 1 second, then repeat
c) M is on for 2 seconds, off for 1 second, then repeat
d) M is always on
e) M is always off

ANSWER → d)

Ring Counter in Multisim



- Multisim clock is not "real time". Pick a frequency for proper viewing.
- Use switch logic to set one FF output to 1 and the other FF outputs to 0
- Use "asynchonous" inputs (active-low) of D FF to do this.
- Asynchronous inputs can be activated at any time (not synced to clock) and have highest priority.

Practice Projects

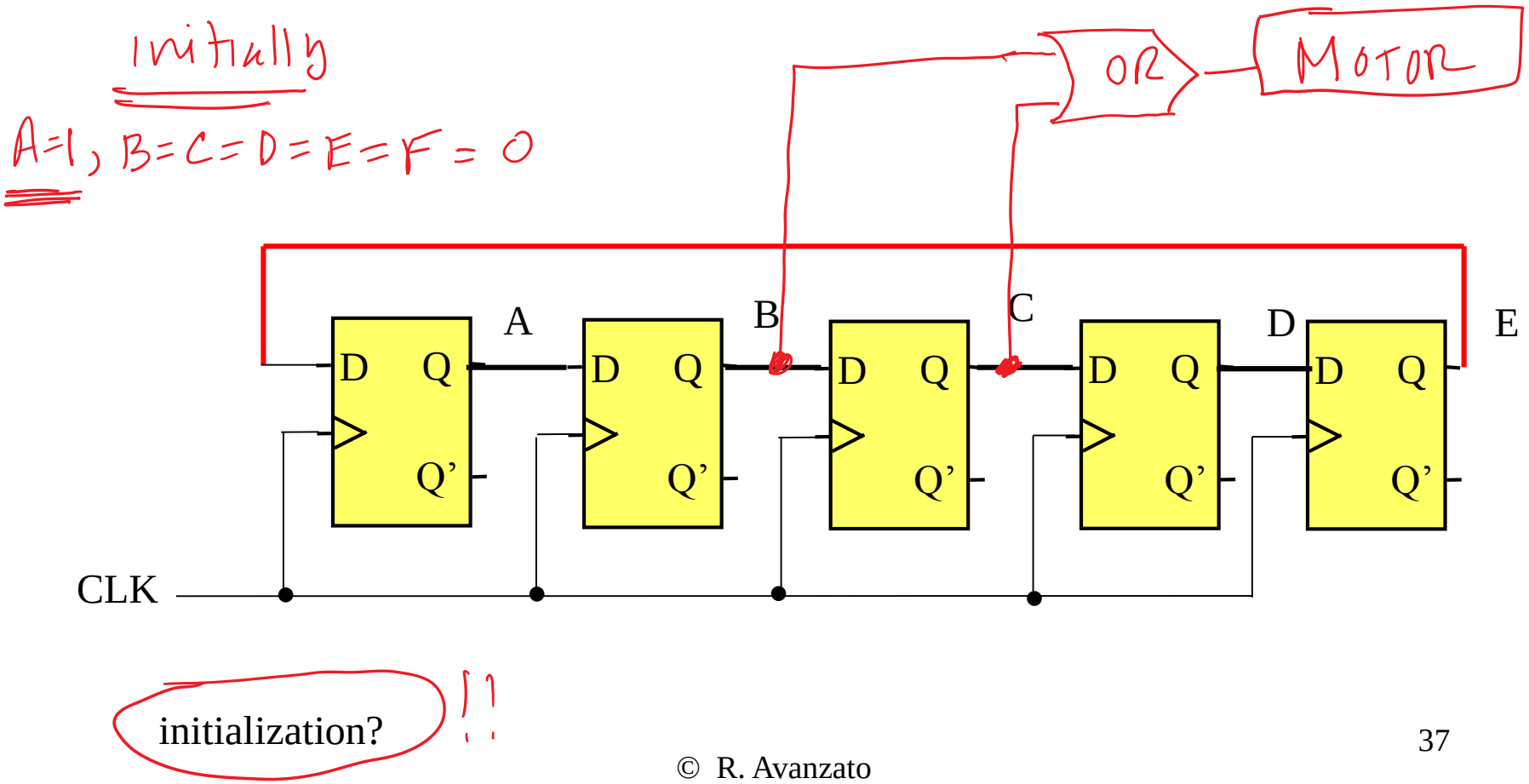
- Demonstrate Clock in MultiSIM
- Demonstrate Logic Analyzer in MultiSIM
- Simulate a simple circuit for a shift/ring counter in MultiSIM

- **Design a circuit that turns on a motor** (modeled by a LED/indicator) "on" for 2 seconds and then "off" for 3 seconds. **Use a ring counter and OR gate(s).** Design with Multisim and demonstrate operation. Use a Logic Analyzer in Multisim. Label all wires with meaningful names. Annotate the waveforms. Assume a 1 Hz clock is available. Be specific about initialization.

- **Solve the same motor control problem as above, but this time using a ring counter and an extra D FF** (with a preset and clear) instead of an OR gate. The motor (LED) will be connected directly to the output (Q) of the extra D FF. The extra D FF will not be connected to the clock, and the ring counter will turn on and off this extra D FF using the asynchronous set (preset) and clear. Simulate in MultiSim and show input and output waveforms. Use a Logic Analyzer in Multisim. Label all wires with meaningful names. Annotate the waveforms.

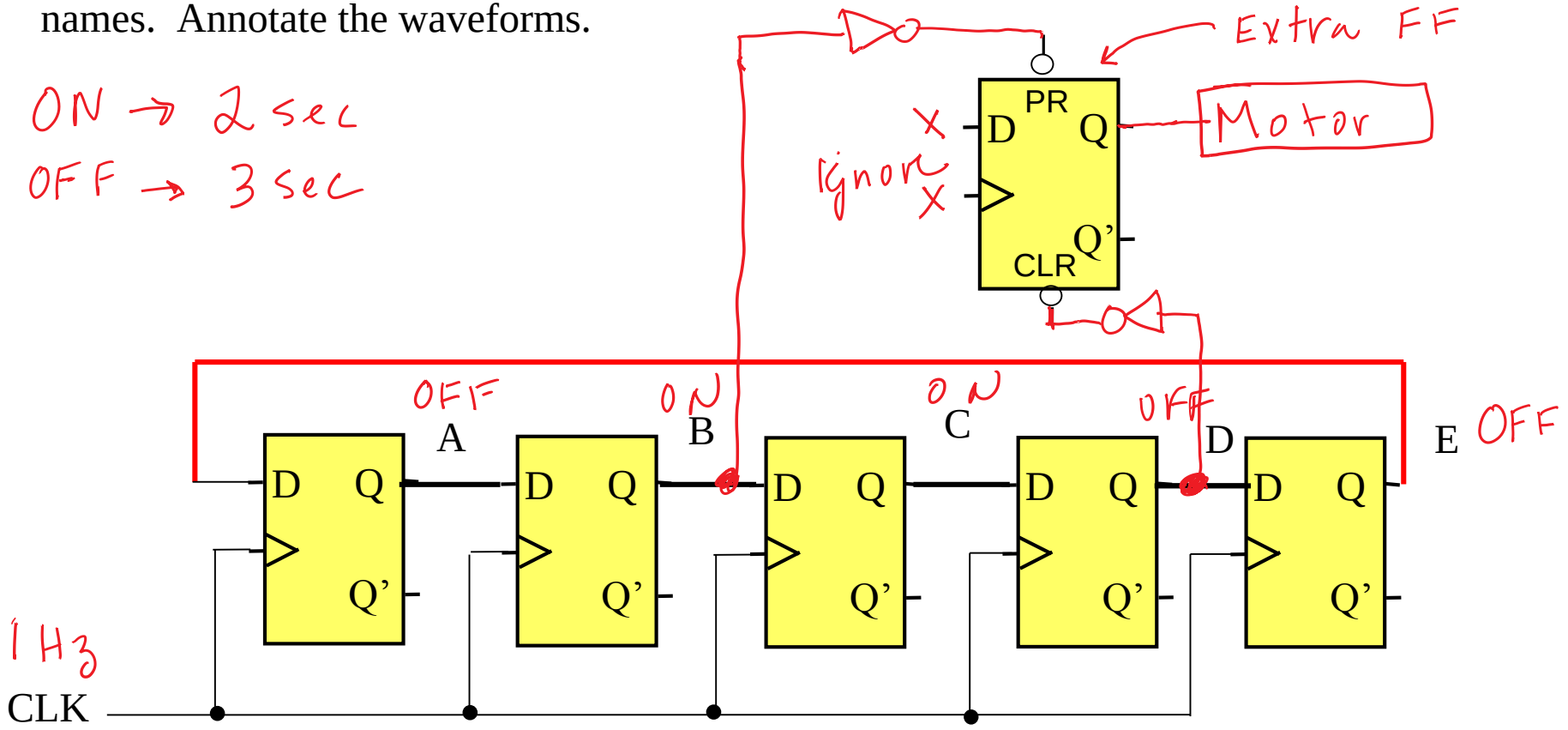
Practice Projects -1

- **#1. Design a circuit that turns on a motor** (modeled by a LED/indicator) "on" for 2 seconds and then "off" for 3 seconds. **Use a ring counter and OR gate(s).** Design with Multisim and demonstrate operation. Use a Logic Analyzer in Multisim. Label all wires with meaningful names. Annotate the waveforms. Assume a 1 Hz clock is available. Be specific about initialization.



Practice Projects - 2

- **#2. Solve the same motor control problem as above, but this time using a ring counter and an extra D FF** (with a preset and clear) instead of an OR gate. The motor (LED) will be connected directly to the output (Q) of the extra D FF. The extra D FF will not be connected to the clock, and the ring counter will turn on and off this extra D FF using the asynchronous set (preset) and clear. Simulate in MultiSim and show input and output waveforms. Use a Logic Analyzer in Multisim. Label all wires with meaningful names. Annotate the waveforms.



initialization?

Penn State Abington
CMPEN 271
Lecture Set #16
D FFs, Shift Registers, Ring Counters

Topics:

- Design Problem — **Video part 1 of 4**
- Clocked Flip-flops (FFs)
- D flip-flop
- Sample Questions

- D FF applications - shift register — **Video part 2 of 4**
- Setup and hold times
- Sample Questions

- Ring counter with applications — **Video part 3 of 4**
- Timing Diagrams
- Simulation software issues
- Sample Questions

- HW #8 Car Taillights Circuit — **Video part 4 of 4** ←

HW #8 Ring Counter (see due date)

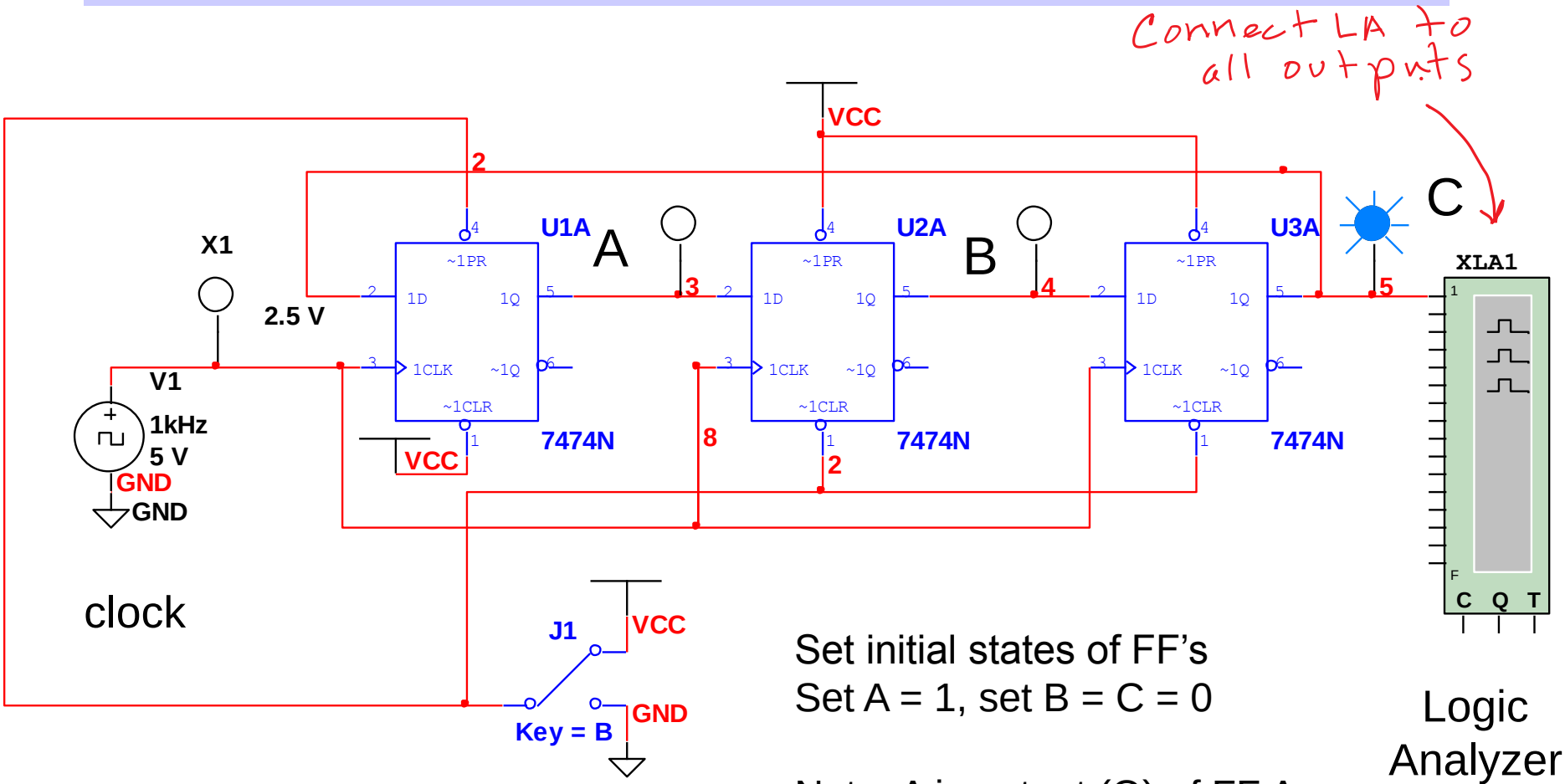
Design Problem: **Design and simulate solutions to Thunderbird taillight turn signal.** Include problem statement. Label all input and output.

Use standard "ring" counter with OR gates. Initialize a single FF to 1 and reset the other FFs (set to zero) prior to operation. Test this first, then add circuitry (OR gates, etc) to control the 3 lights (A, B, C). Use Multisim probe indicators to represent the lights. Show **circuit** and **timing diagram with markups**. (Set Multisim LA to display vertical clock-based reference lines in the timing diagram. Set CLK to internal in LA and set the LA clock freq to same as clock frequency for circuit.)

Include all results (header, problem description, circuit diagram, timing diagram with annotations, etc) in a **single Word document**.

Review Powerpoint slides. If you have questions, ask instructor.

HW #8 Hint – MultiSIM – Ring Counter

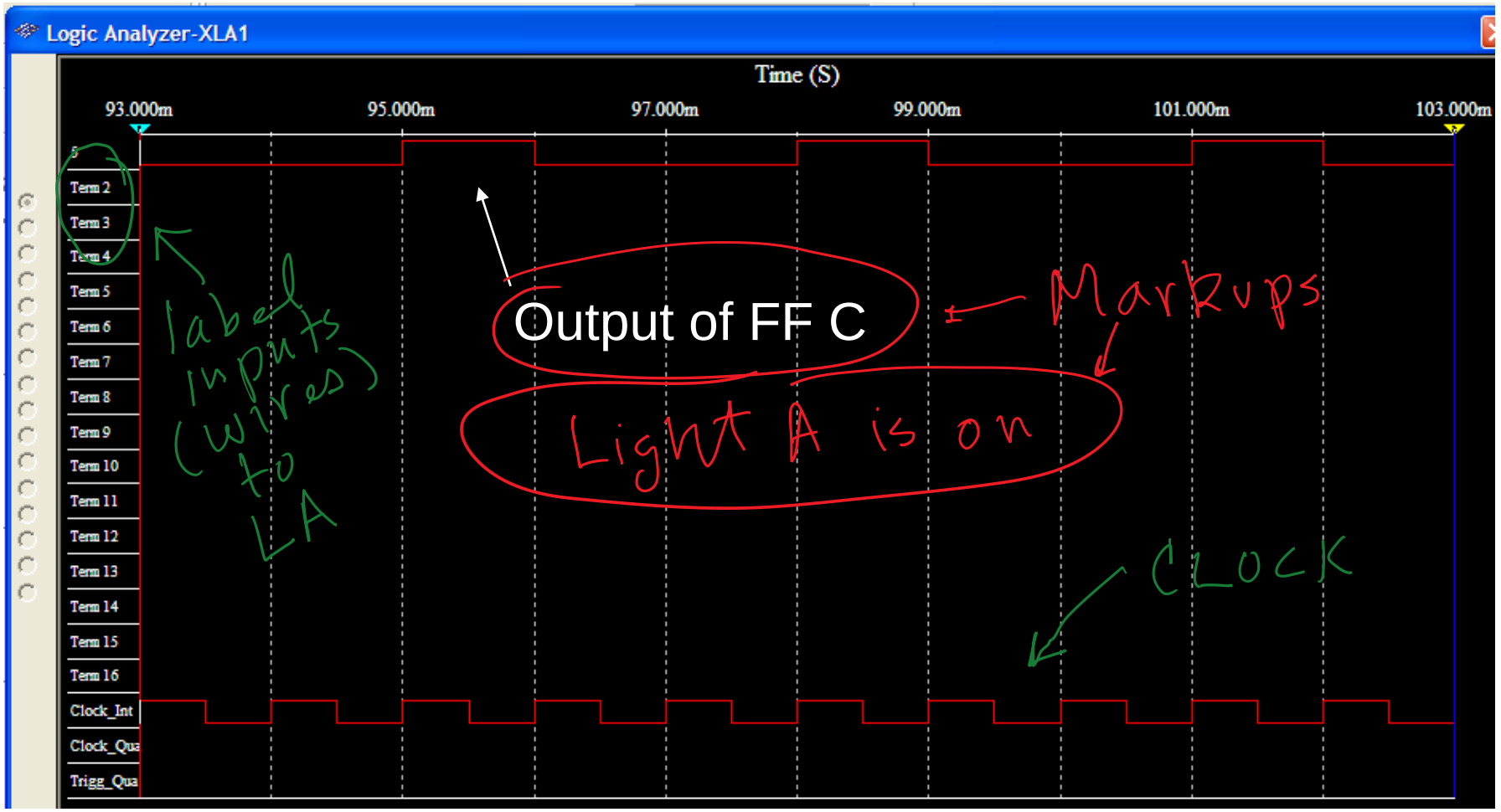


Set initial states of FF's
Set A = 1, set B = C = 0

Note: A is output (Q) of FF A;
B is output (Q) of FF B;
C is output (Q) of FF C

Logic Analyzer

HW #8 Hint – MultiSIM – Ring Counter



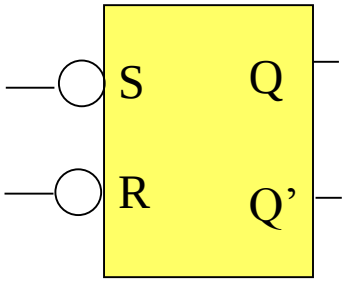
Logic Analyzer – set “internal” clock – same freq as ext clock (ex 1KHz)

Summary

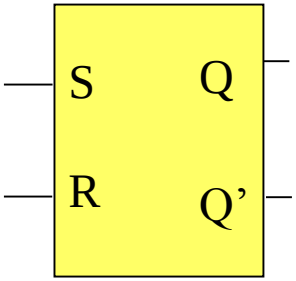
- **D latch** and D flip-flop design are based on NAND latches.
- A D latch or D flip-flop is a memory device **that stores 1 bit.**
- The **advantage** of D latches and D flip-flops is that there are clock inputs. This helps the digital designer build more predictable designs that are synchronized to a clock.
- A D latch is **level triggered** (or pulse triggered) which means that the latch will respond to input during the entire time the clock is high. This has disadvantages.
- A **clock signal is a square wave** which alternates between 0 (0volts) and 1 (5 volts). A clock signal has a period (measured in time) and a frequency (measured in Hertz)
- A **positive-edge triggered** D flip-flop responds to input only during the positive edge transition of the clock 0 → 1 (which is a very short time). This has advantages over the latch in digital design.
- D flip-flops can **be positive-edge triggered or negative-edge triggered**. Positive-edge triggered D flip-flops are more common.
- Modern D flip-flops have **a hold time = 0**. This means that if the D data input is changing state (0→1 or 1→0) during the clock edge, then the flip-flop responds to the value of the D data input **just before** the clock transition.
- **Shift registes** can be constructed from positive-edge D flip-flops.
- Shift registers can be used in **serial to parallel conversion circuits**, multiplication and division in microprocessors, linear feedback shift registers (communications).
- A **ring counter** is a modified shift register.
- Ring counters can be used to control the **on/off sequence** of one or more external devices.
- Ring counters must be **carefully initialized** in order to operate properly. Usually, one of the FFs is preset to 1, and the other FFs are reset (cleared) to zero before operation.
- Flip-flops often possess **asynchronous inputs**, such as preset (set) and reset, that allow the designer to initialize the FFs into desired states.

Summary of Latches & Flip-flops

NAND

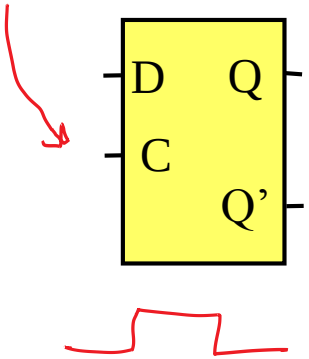


Nor



Latches
(no clock input)

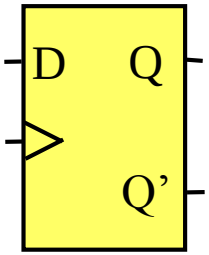
"Pulse" triggered is same thing as "level" triggered. It means the latch responds entire time clock is high.



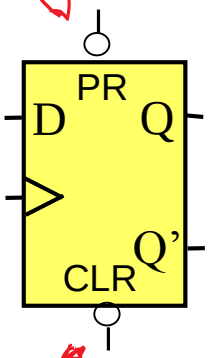
D Latch
Pulse (level) triggered;
transparent when clock is high

"transparent" means the output is same as (or follows) the input while clock is high. That is not good for shift registers and ring counters.

Pos edge trig

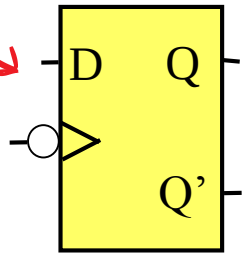


preset Q=1



make Q=0

Neg edge



or

Edge-triggered
(basis for shift registers and ring counters)