# Assignment 2

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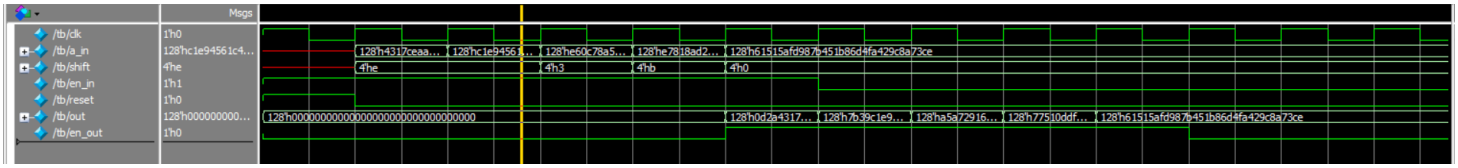
Link:

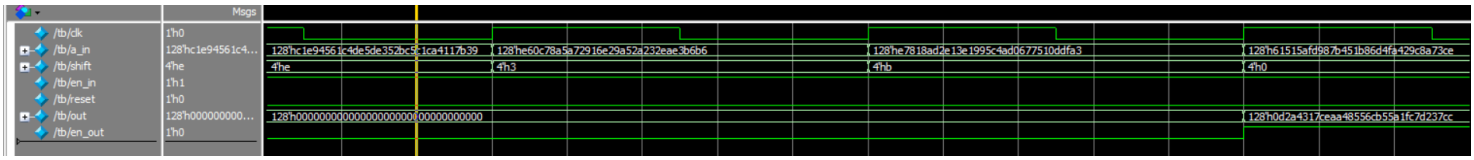
https://github.com/ruizhiz/-EE-599_Ruizhi_Zhang_8230108665.git

# Barrel Shifter

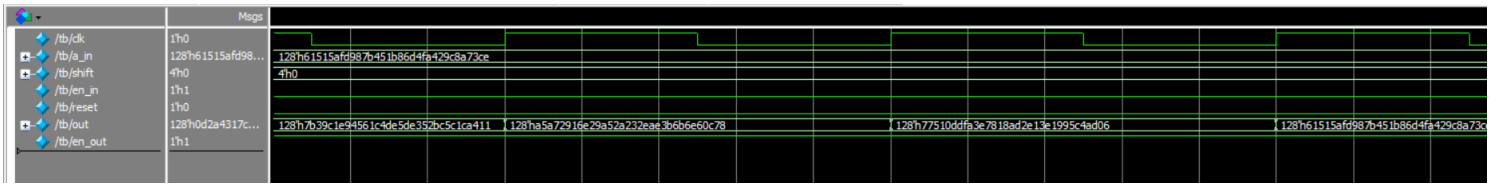
The attached files include: tb.v, top.v, barrel_shifter.v, stage.v, shift.v. tb.v is used to do simulation test. barrel_shifter.v is our IP core. However, it has too many input and output pins, and cannot be implemented on FPGA directly. So, top.v is used to help to do implementation. So, only in implementation part, top.v is included in our schematics.




*Picture 1: the overview of whole waveform*




*Picture 2: the first part of waveform*




*Picture 3: the second part of waveform*

In our testbench, both input element a_in and shifter are generated by $urandom.

As we can see from the waveform, the input elements a_in are:

4317_ceaa_4855_6cb5_5a1f_c7d2_37cc_0d2a, c1e9_4561_c4de_5de3_52bc_5c1c_a411_7b39, e60c_78a5_a729_16e2_9a52_a232_eae3_b6b6, e781_8ad2_e13e_1995_c4ad_0677_510d_dfa3, 6151_5afd_987b_451b_86d4_fa42_9c8a_73ce.

and the corresponding shifter are: e, e, 3, b, 0.

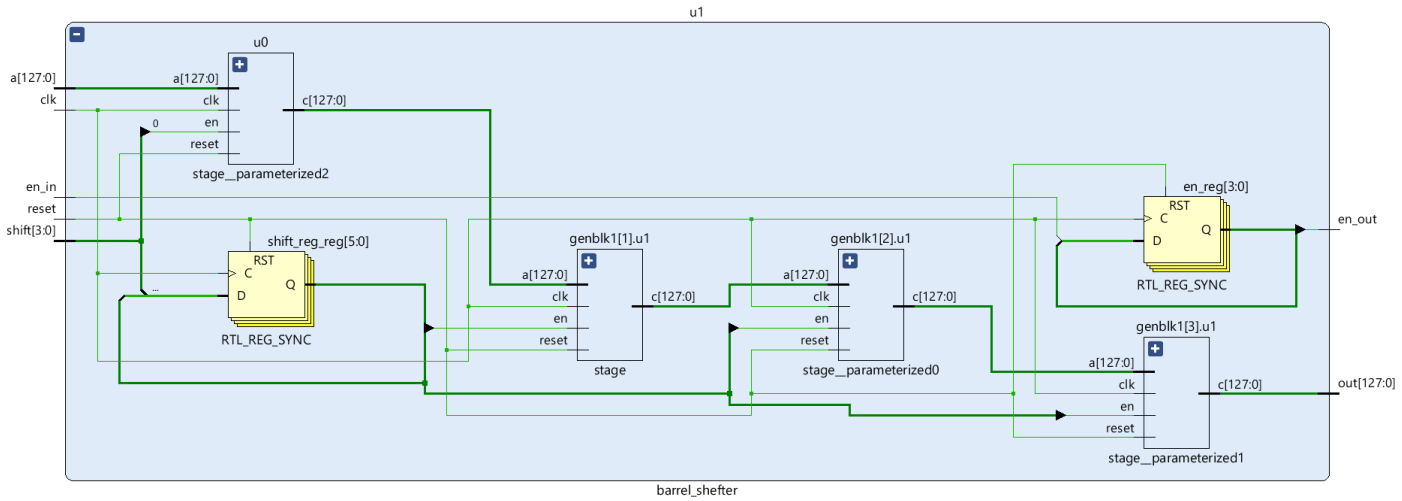
The outputs are:

0d2a_4317_ceaa_4855_6cb5_5a1f_c7d2_37cc, 7b39_ c1e9_4561_c4de_5de3_52bc_5c1c_a411, a5a7_2916_e29a_52a2_32ea_e3b6_b6e6_0c78, 7751_0ddf_a3e7_818a_d2e1_3e19_95c4_ad06, 6151_5afd_987b_451b_86d4_fa42_9c8a_73ce.

That is what we expected. So, the result is right.

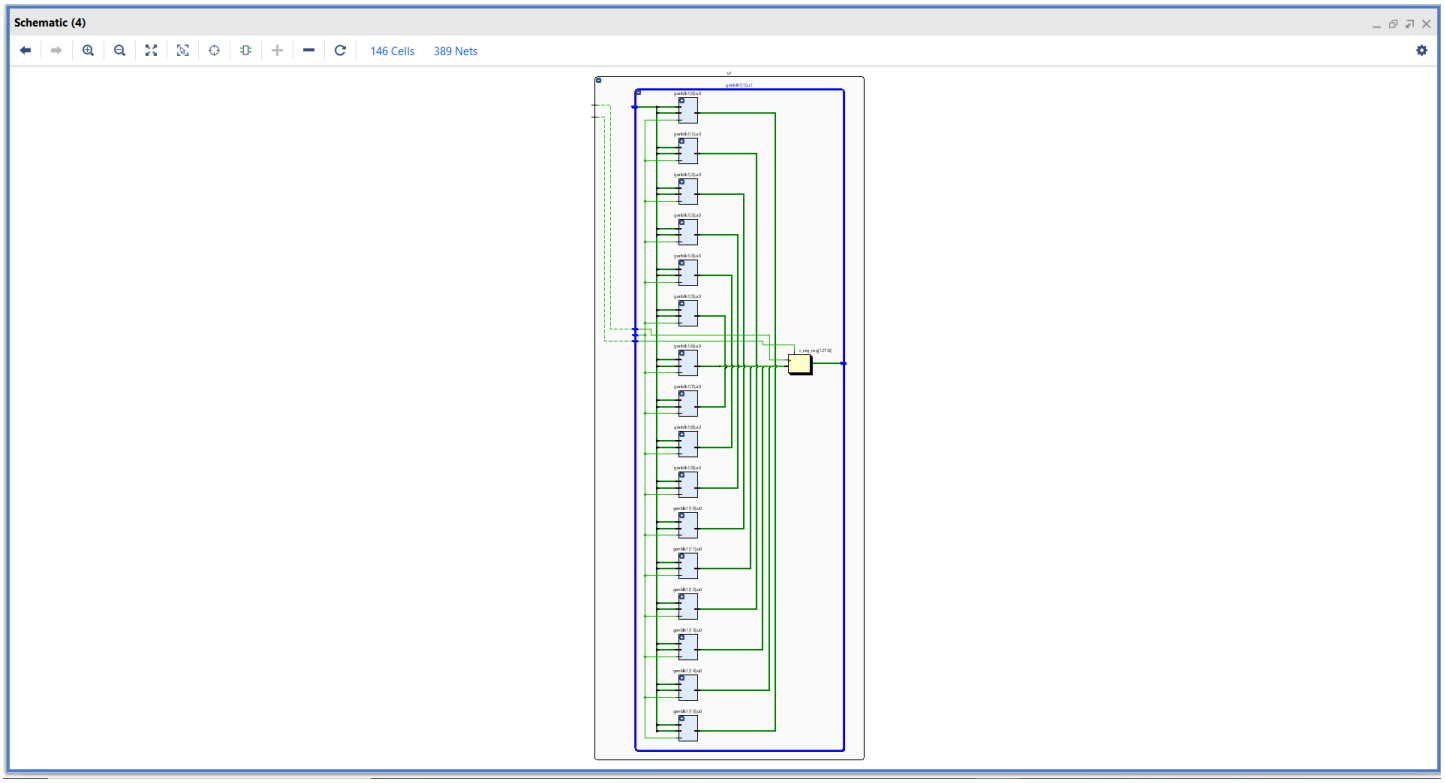
# Part 1: 16 elements

1. Elaborated design



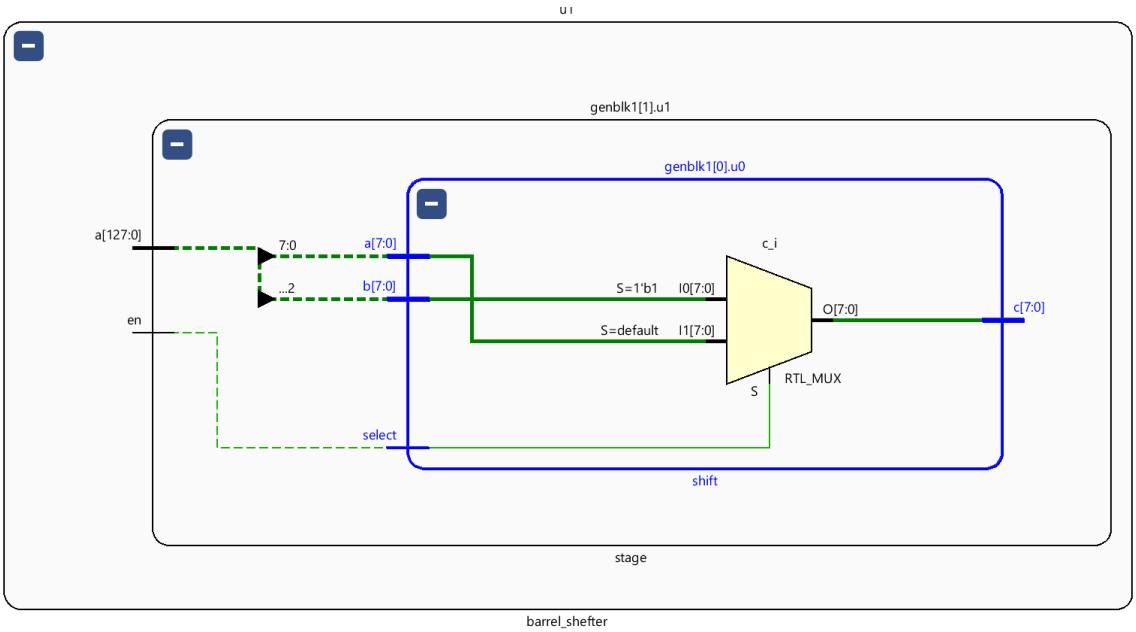

*Picture 1: 16-element 8-bit barrel shifter*

Barrel shifter includes 4 stage.



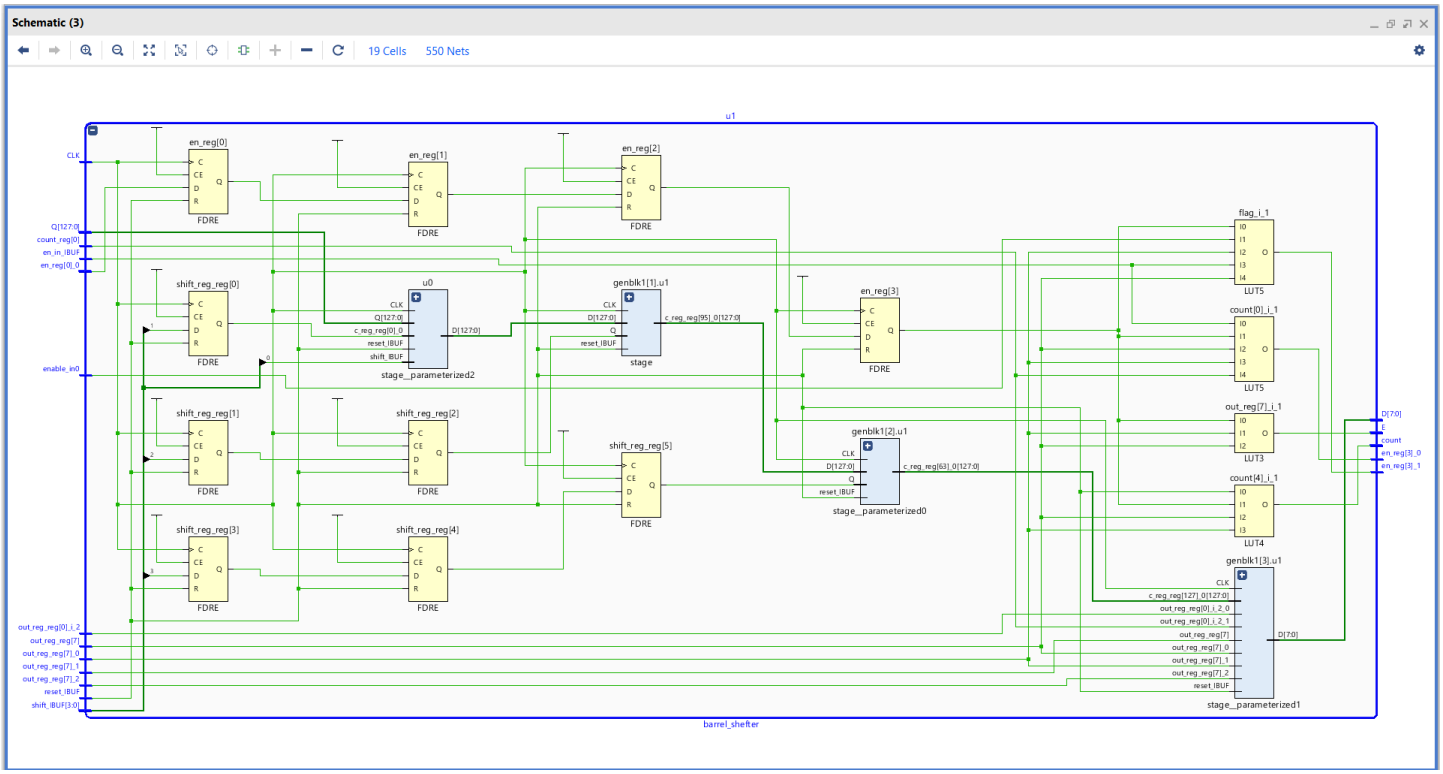

*Picture 2: stage*

1 stage include 16shifter and one 128-bit FF.

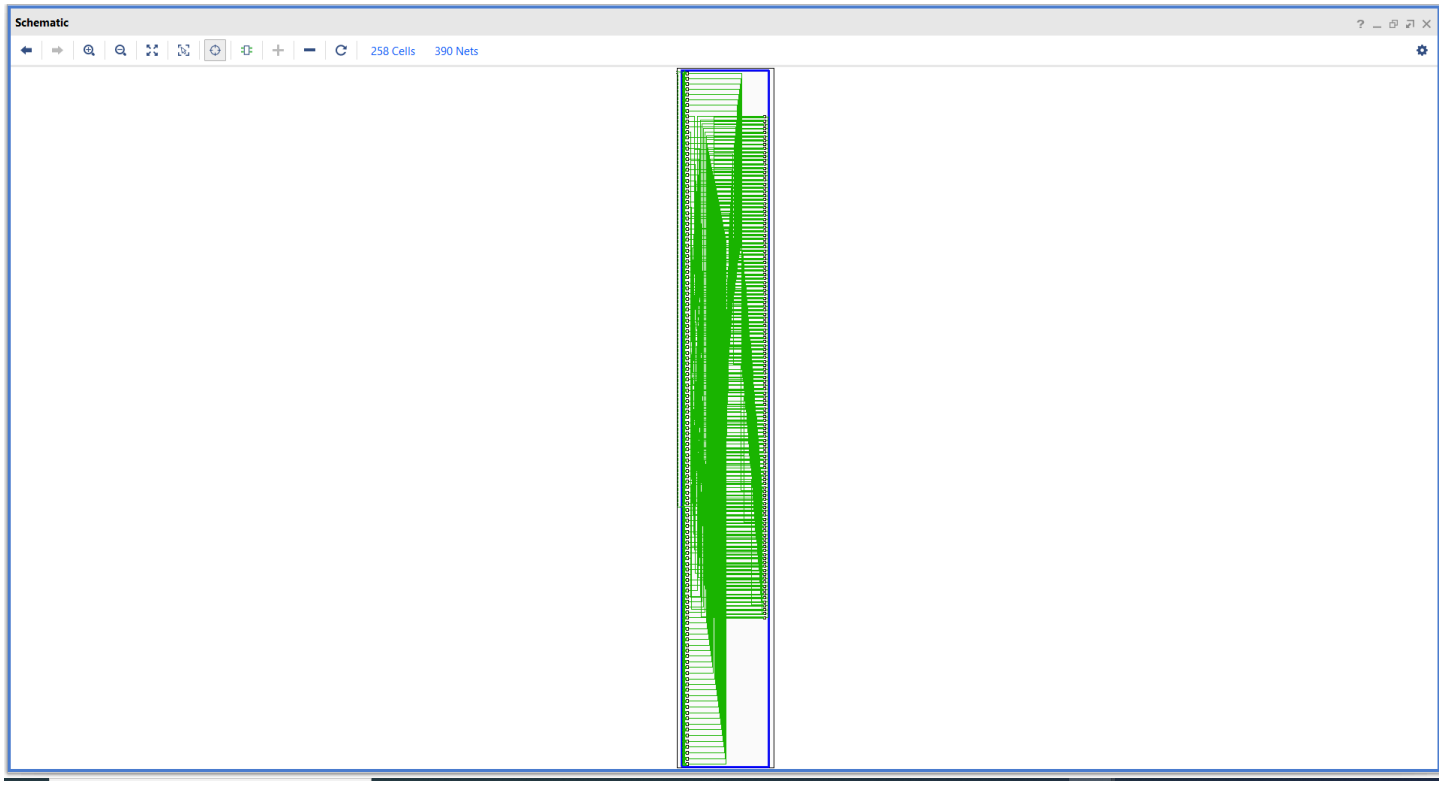



*Picture 3: shifter unit*

## 2. Synthesis and estimation




*Picture 1: the synthesis schematic*




*Picture 2: the schematics of single stage*

**Utilization** Post-Synthesis | **Post-Implementation**

Graph | **Table**

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 319 | 14400 | 2.22 |
| FF | 666 | 28800 | 2.31 |
| IO | 24 | 54 | 44.44 |
| BUFG | 1 | 32 | 3.13 |

*Picture 3: resource estimation*

**Design Timing Summary**

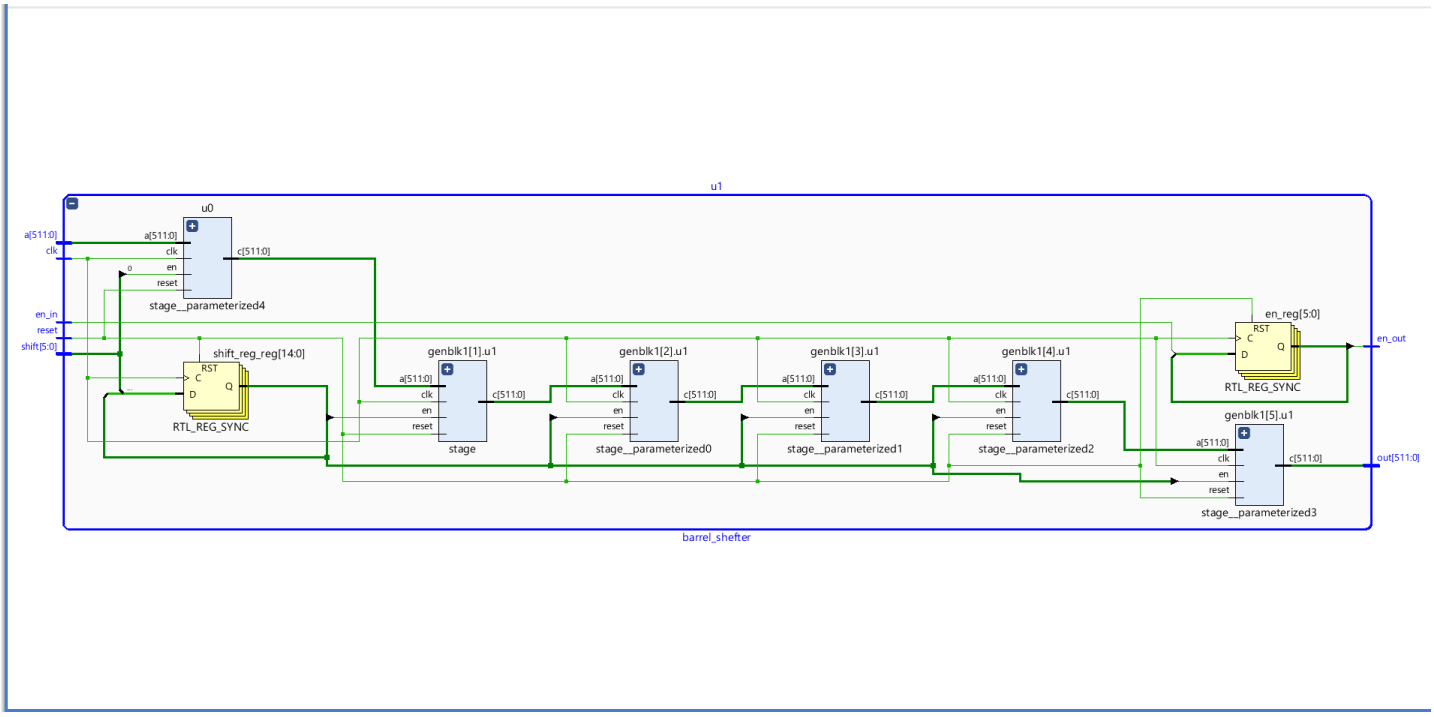
| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | 5.607 ns | Worst Hold Slack (WHS): | 0.156 ns | Worst Pulse Width Slack (WPWS): | 4.500 ns |
| Total Negative Slack (TNS): | 0.000 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 679 | Total Number of Endpoints: | 679 | Total Number of Endpoints: | 667 |

**All user specified timing constraints are met.**

*Picture 4: timing estimation*

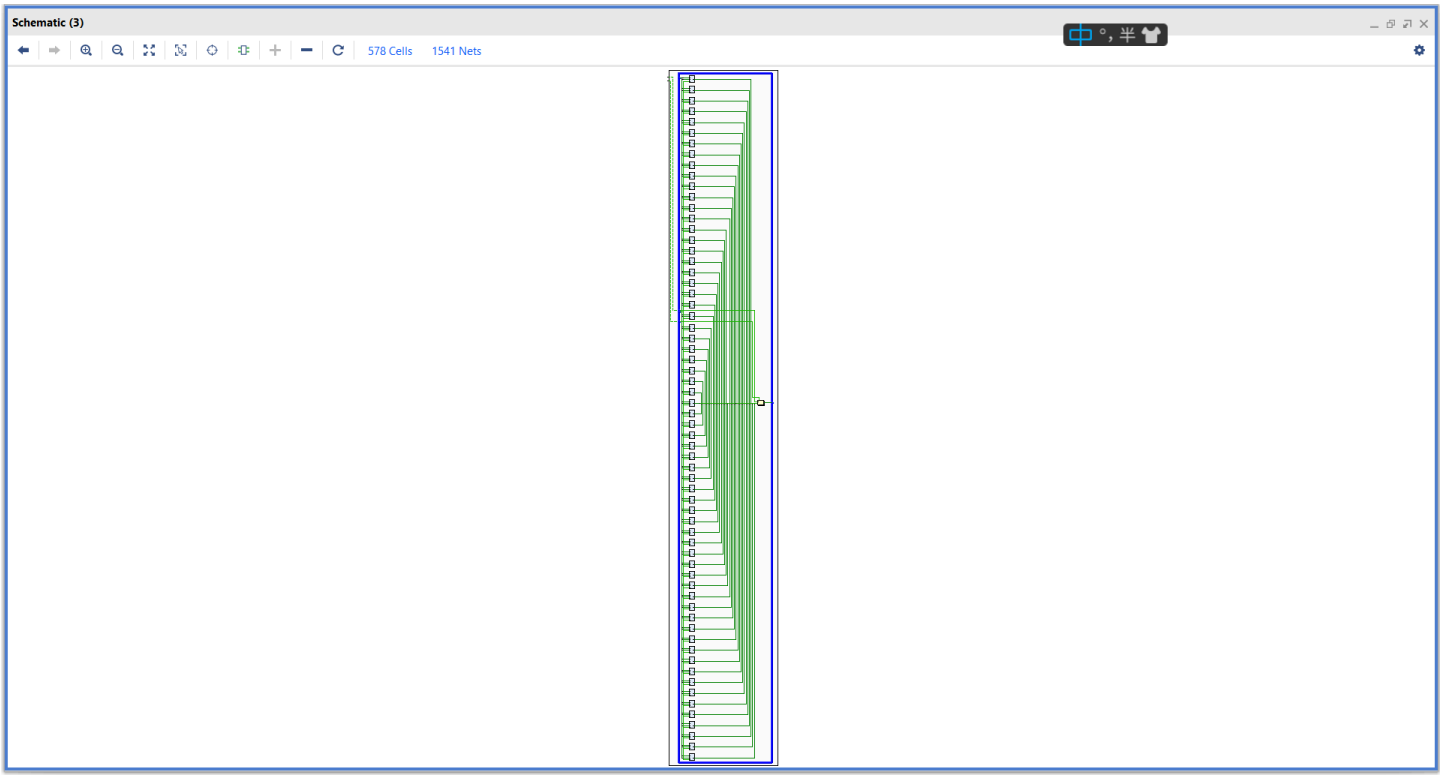
# Part 2: 64 element barrel shifter

1. Elaborated design



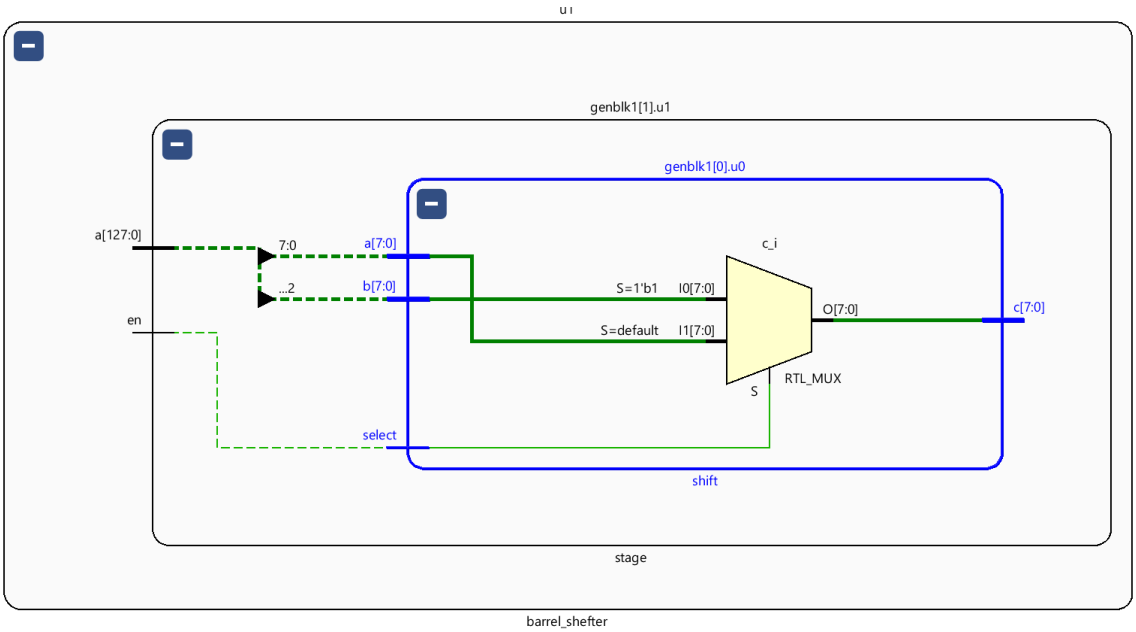

*Picture 1: 64-element 8-bit barrel shifter*

Barrel shifter includes 6 stage.



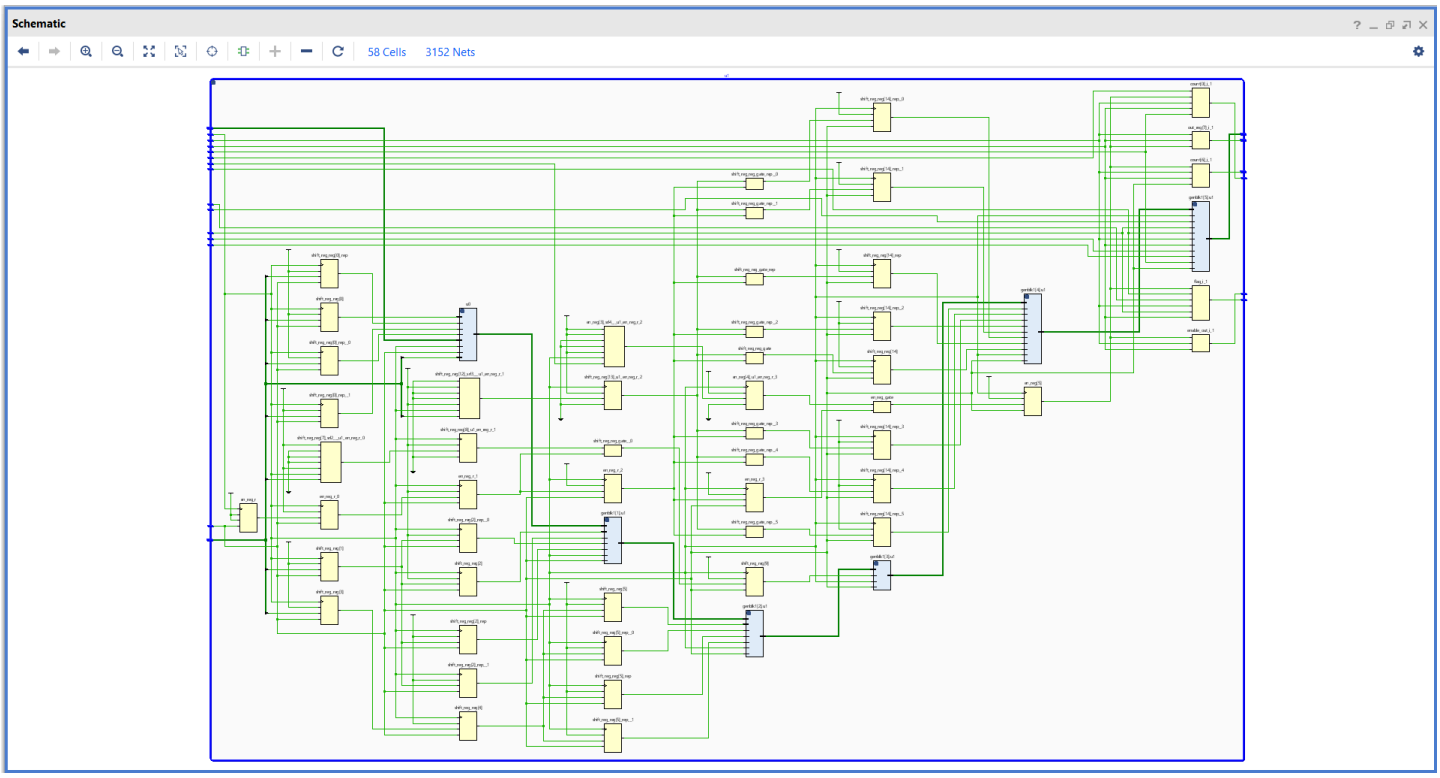

*Picture 2: stage*

1 stage include 64 shifters and one 512-bit FF.




*Picture 3: shifter unit*

## 2. Synthesis and estimation




*Picture 1: the synthesis schematic*

**Utilization** Post-Synthesis | **Post-Implementation**

Graph | **Table**

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 2023 | 14400 | 14.05 |
| LUTRAM | 3 | 6000 | 0.05 |
| FF | 3635 | 28800 | 12.62 |
| IO | 26 | 54 | 48.15 |
| BUFG | 1 | 32 | 3.13 |

*Picture 2: resource estimation*

**Design Timing Summary**

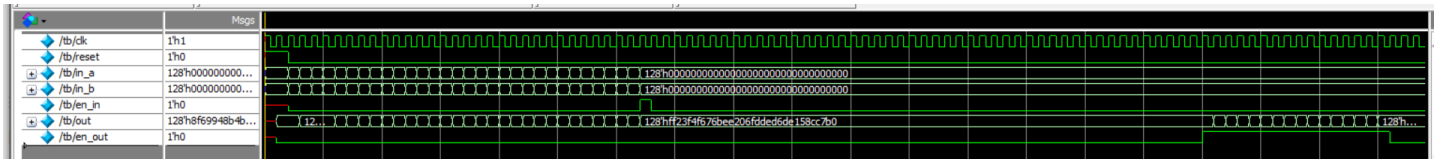
| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | 3.976 ns | Worst Hold Slack (WHS): | 0.043 ns | Worst Pulse Width Slack (WPWS): | 4.146 ns |
| Total Negative Slack (TNS): | 0.000 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 3649 | Total Number of Endpoints: | 3649 | Total Number of Endpoints: | 3639 |

**All user specified timing constraints are met.**

*Picture 3: timing estimation*

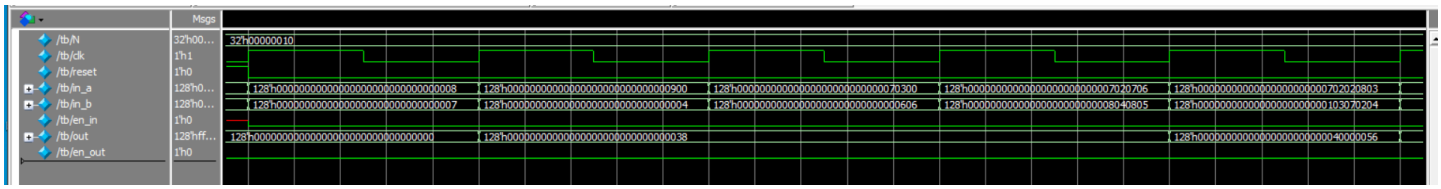
# systolic array

the attached file include: adder.v, multi.v, tb.v, top.v, unit.v. tb.v is used to do simulation test for 16 * 16 matrices. Top.v is systolic array. Unit.v is processing elements.

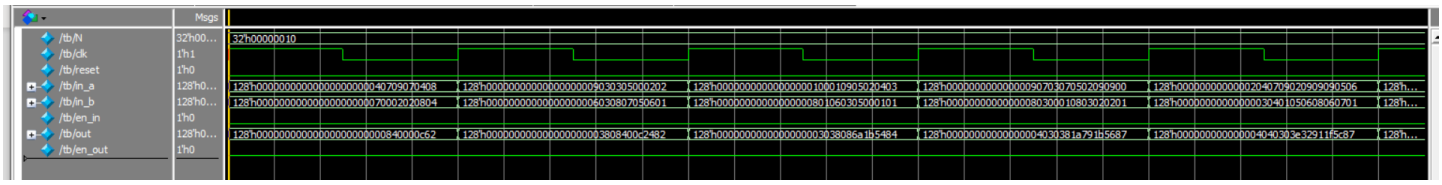



*Picture 1: the overview of whole waveform*

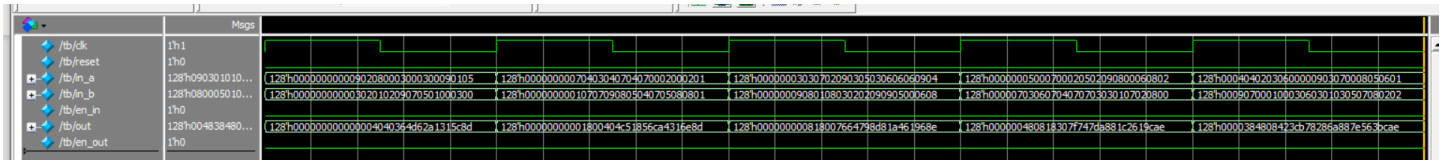
The out signal will output one row (16 elements) per cycle, and is valid when en_out is high.



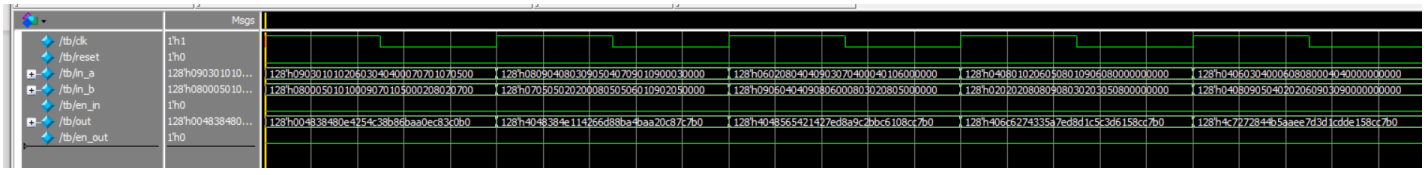

*Picture 2: the first part of waveform*



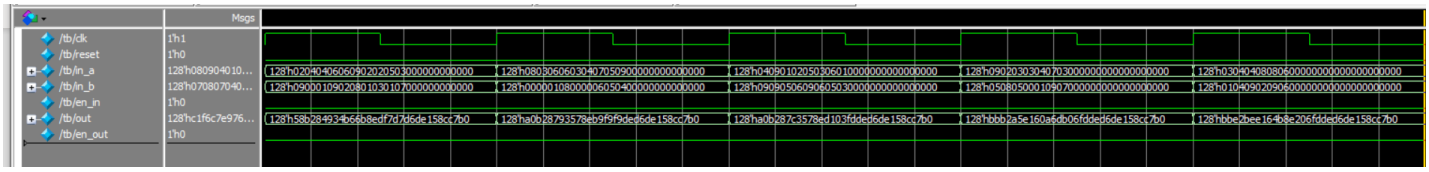

*Picture 3: the second part of waveform*



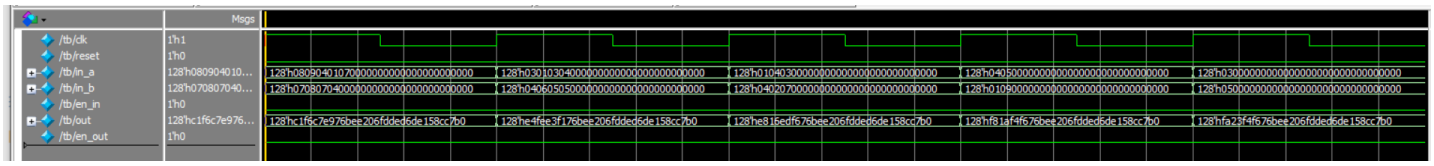

*Picture 4: the third part of waveform*




*Picture 5: the fourth part of waveform*

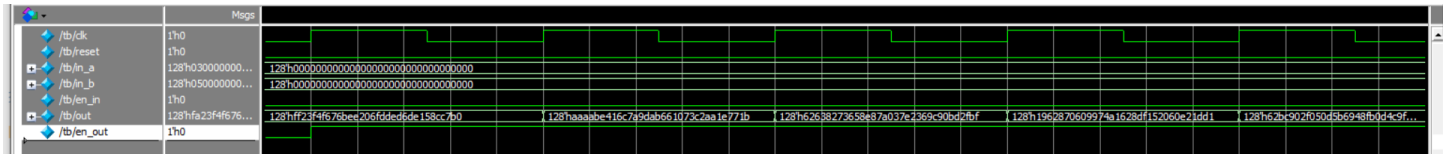



*Picture 6: part 5 of the waveform*

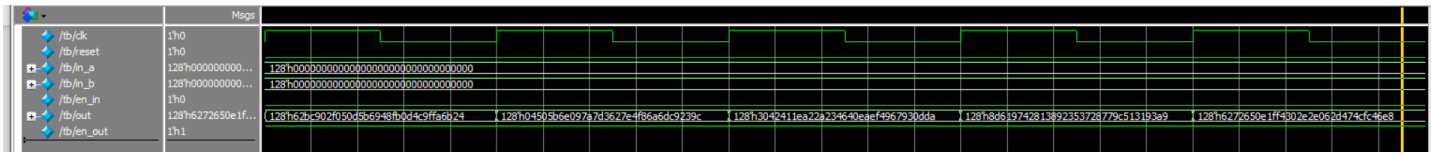



*Picture 7: part 6 of the waveform*

The above are input signals. The following are output signals.

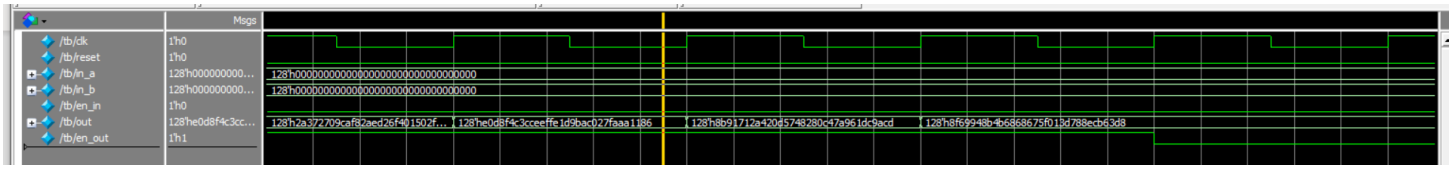



*Picture 8: part 1 of output waveform*




*Picture 9: part 2 of output waveform*


*Picture 10: part 3 of output waveform*

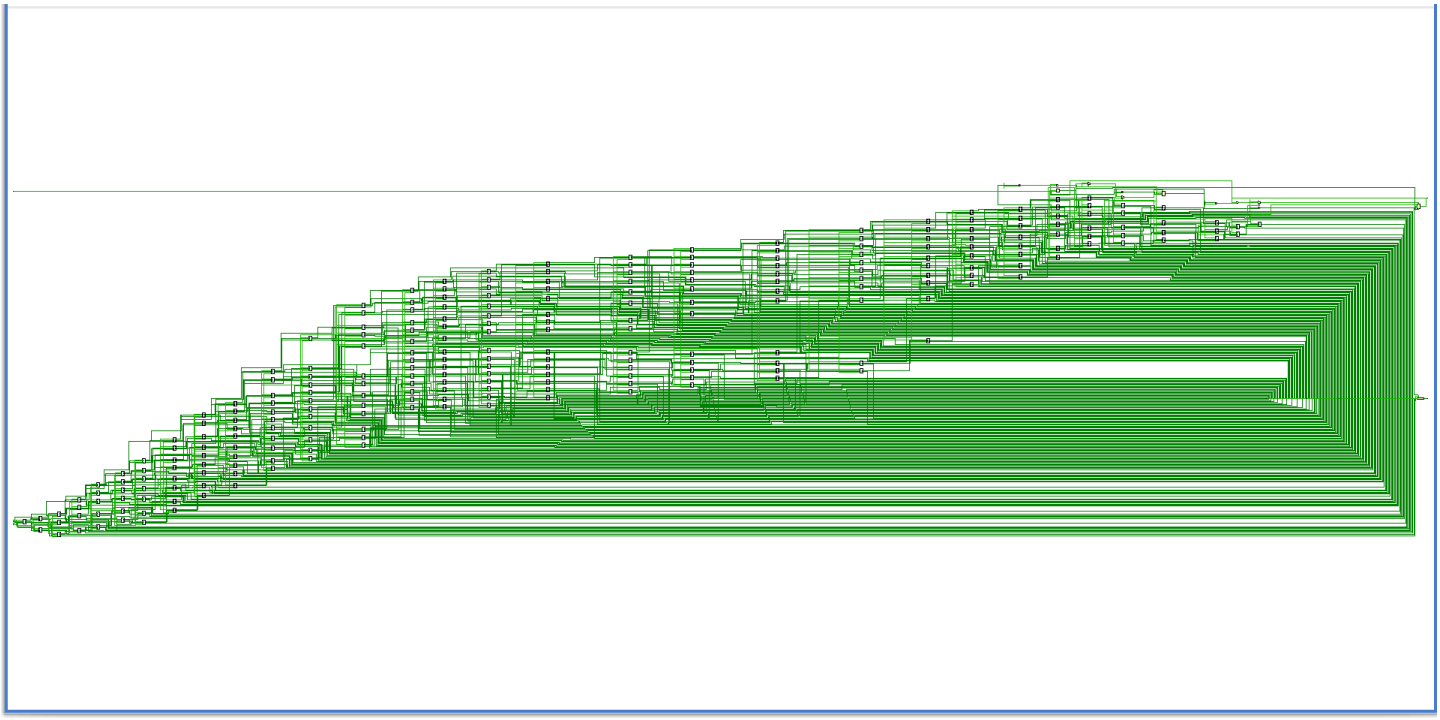



*Picture 11: part 4 of output waveform*

Based on the waveform, we could know our circuits is correct.

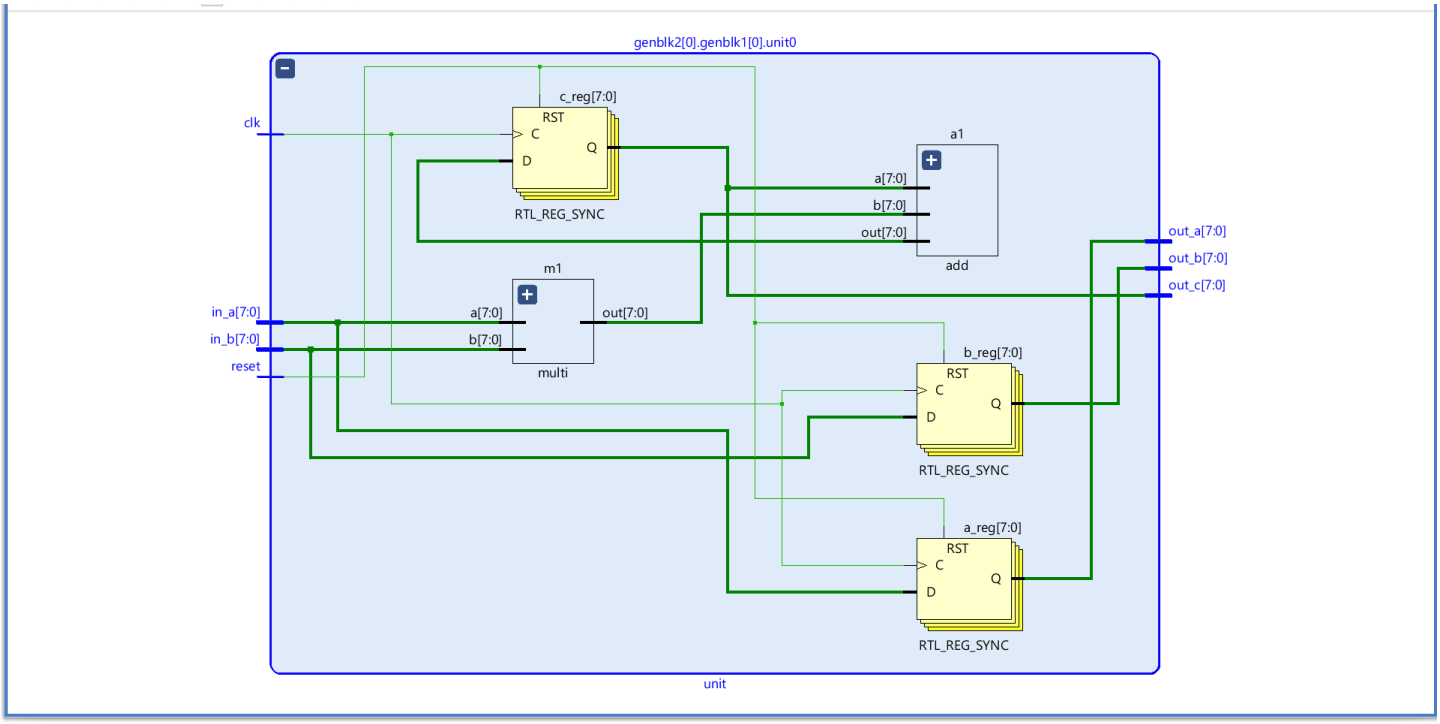
# Part 1: 16 * 16 elements

1. Elaborate design



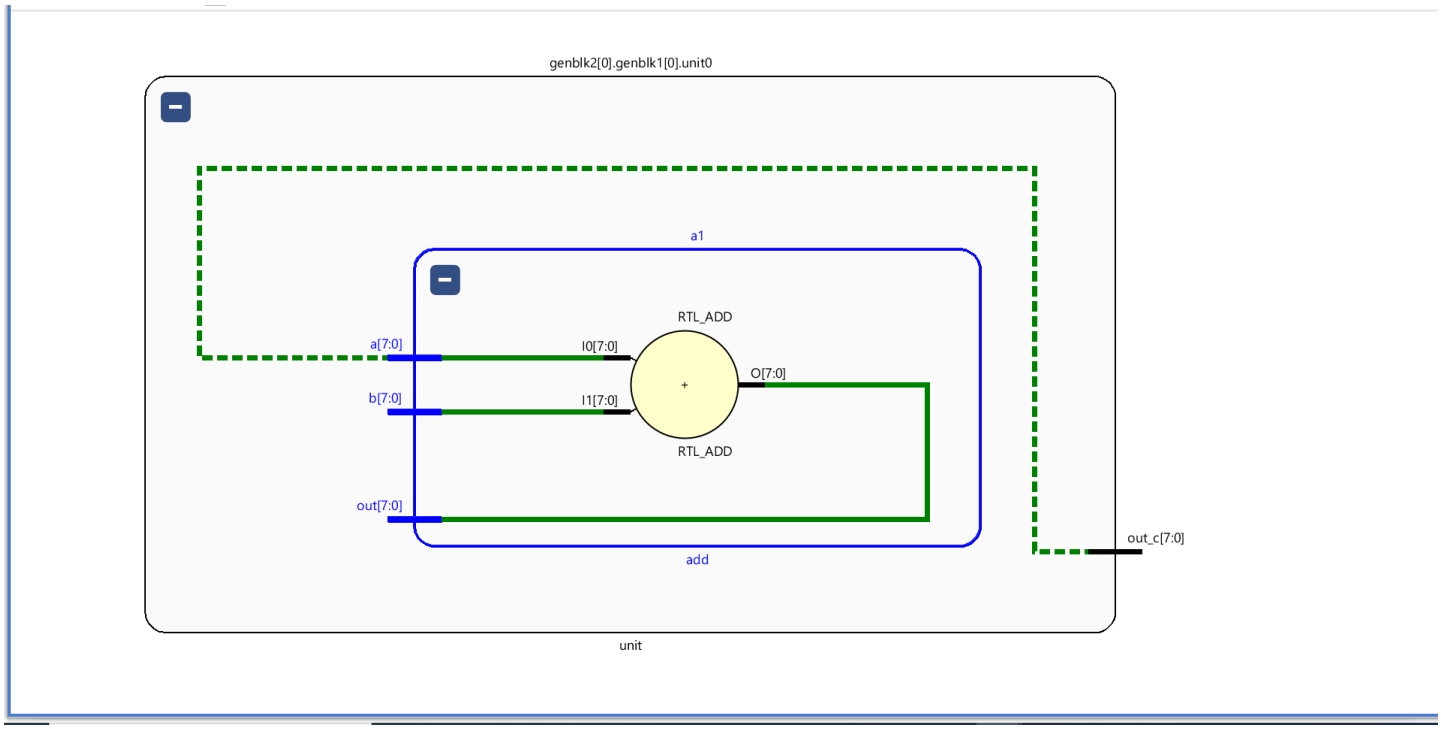
*Picture 1: schematics of Systolic array*

It includes 16*16 PEs.

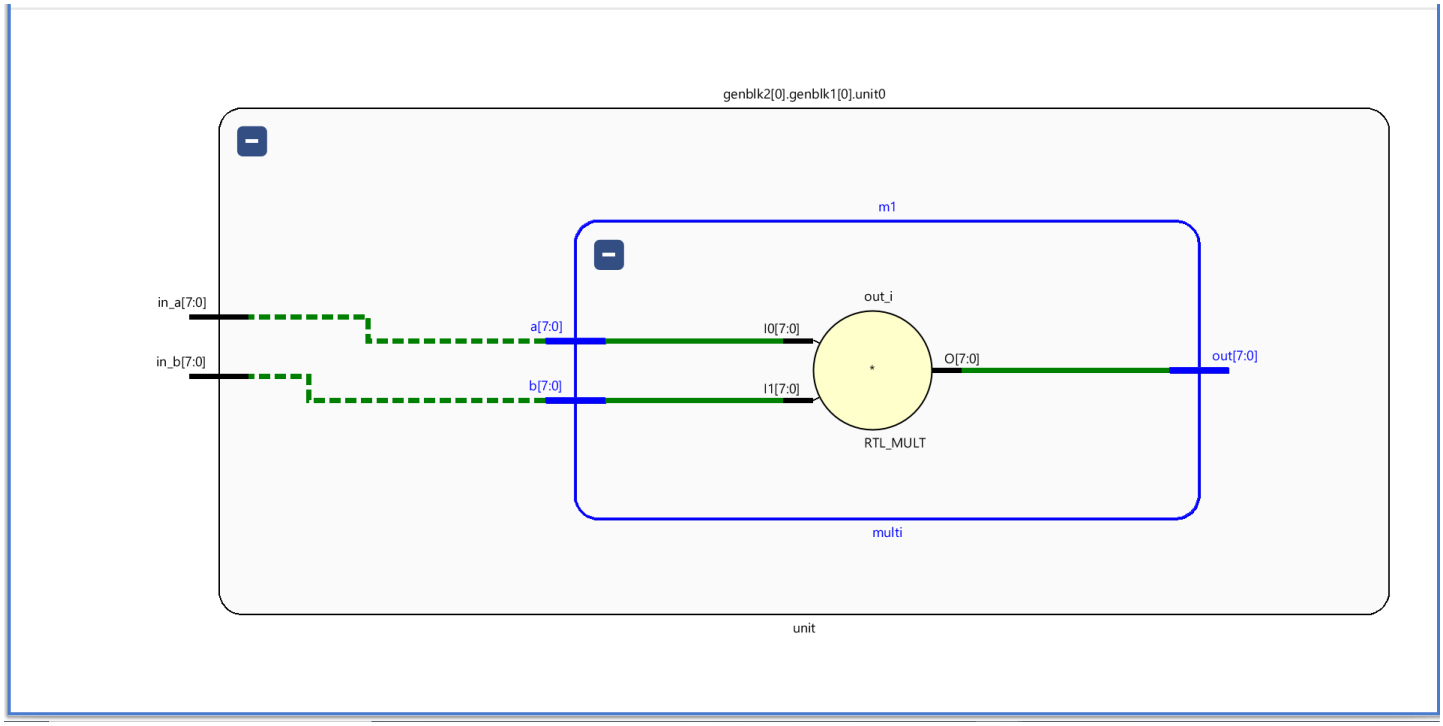



*Picture 2: schematics of PE*

It includes 1 adder and 1 multiply module.

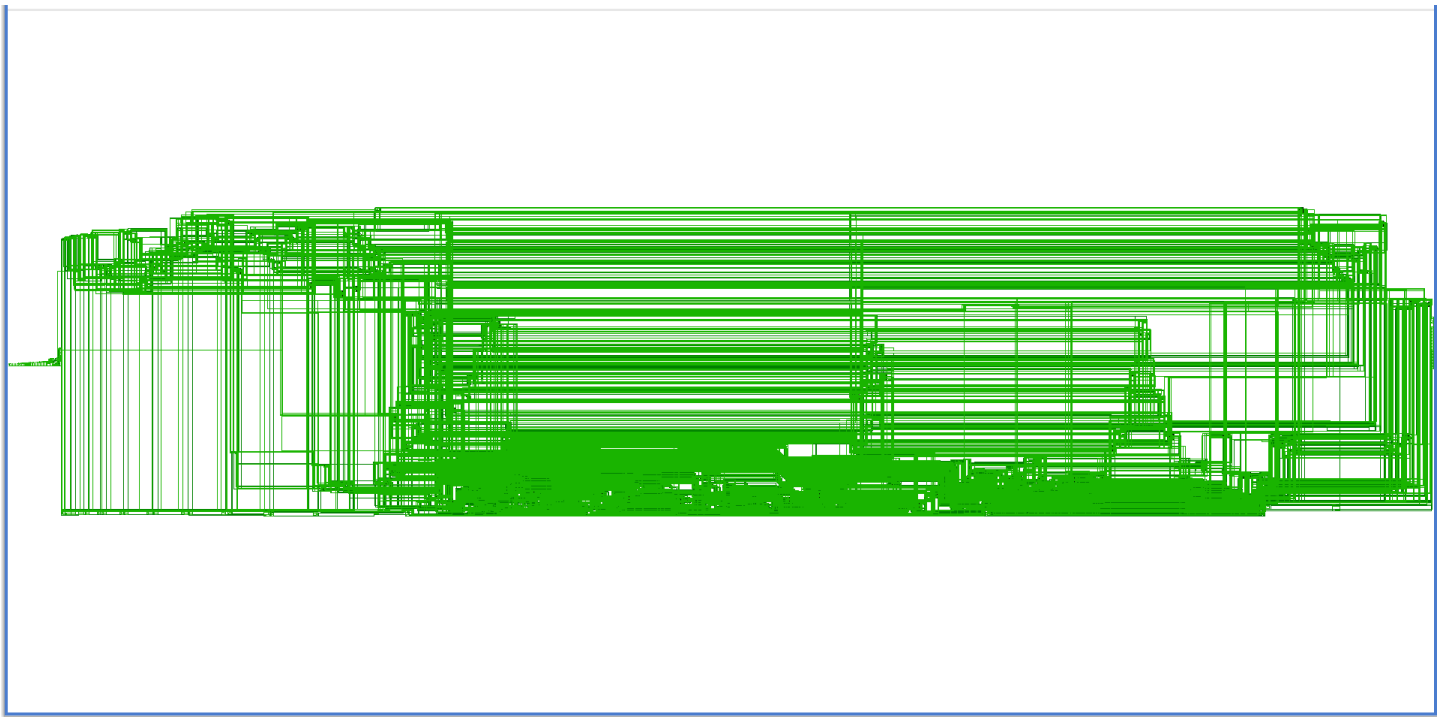



*Picture 3: adder module*

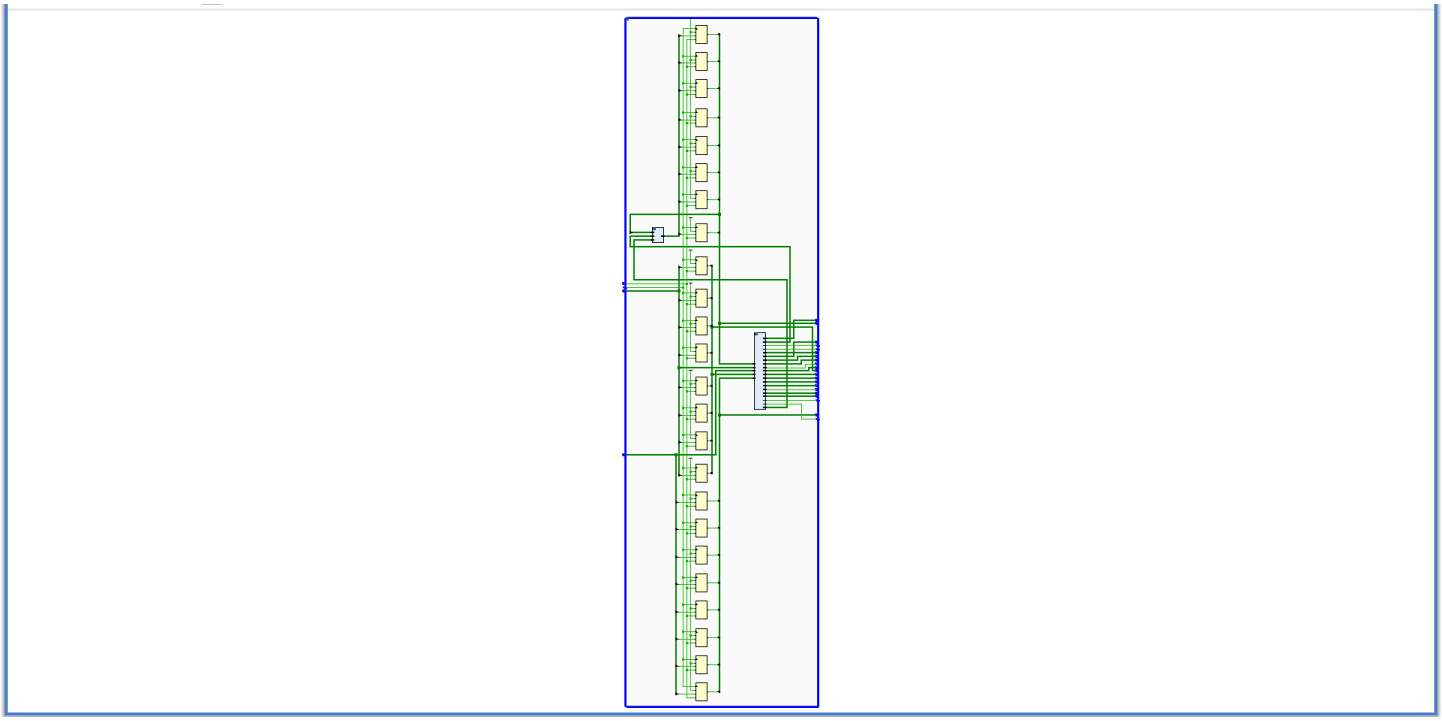



*Picture 4: multiply module*

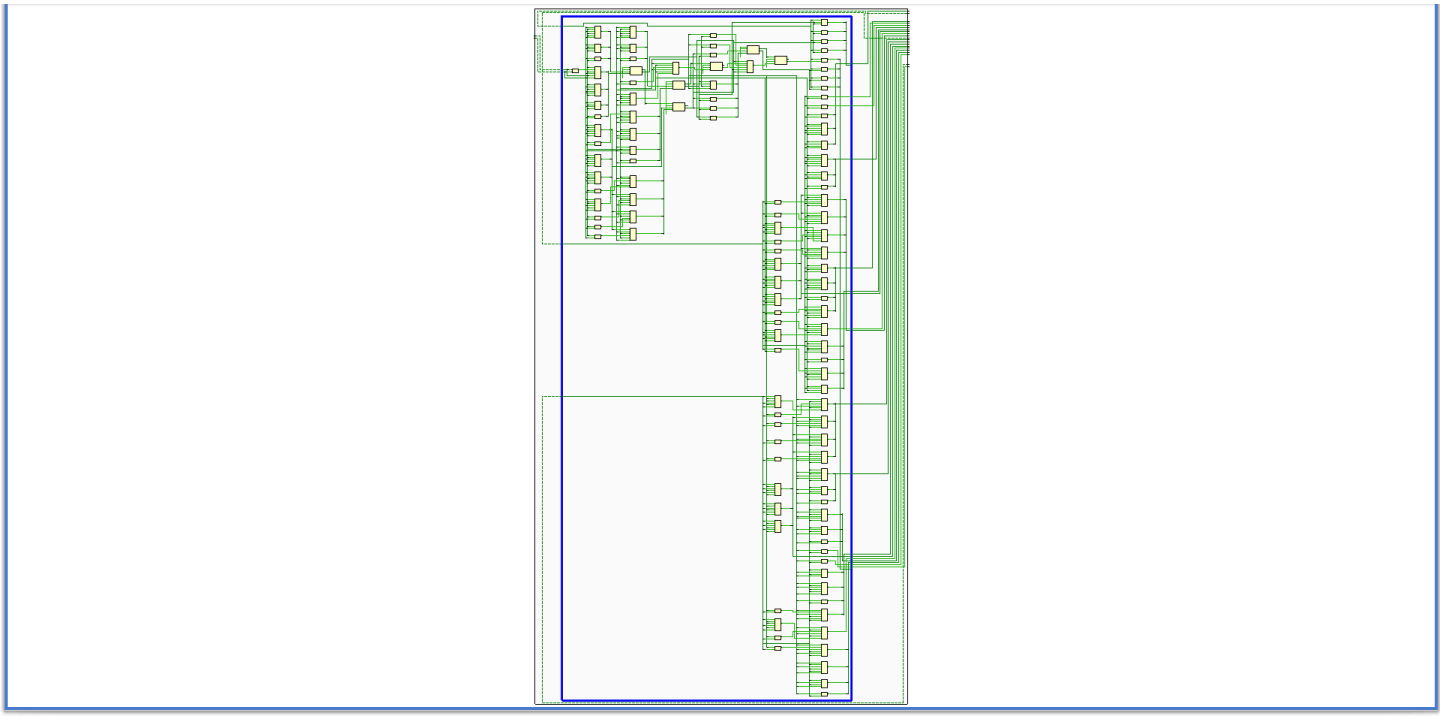
2. Synthesis design



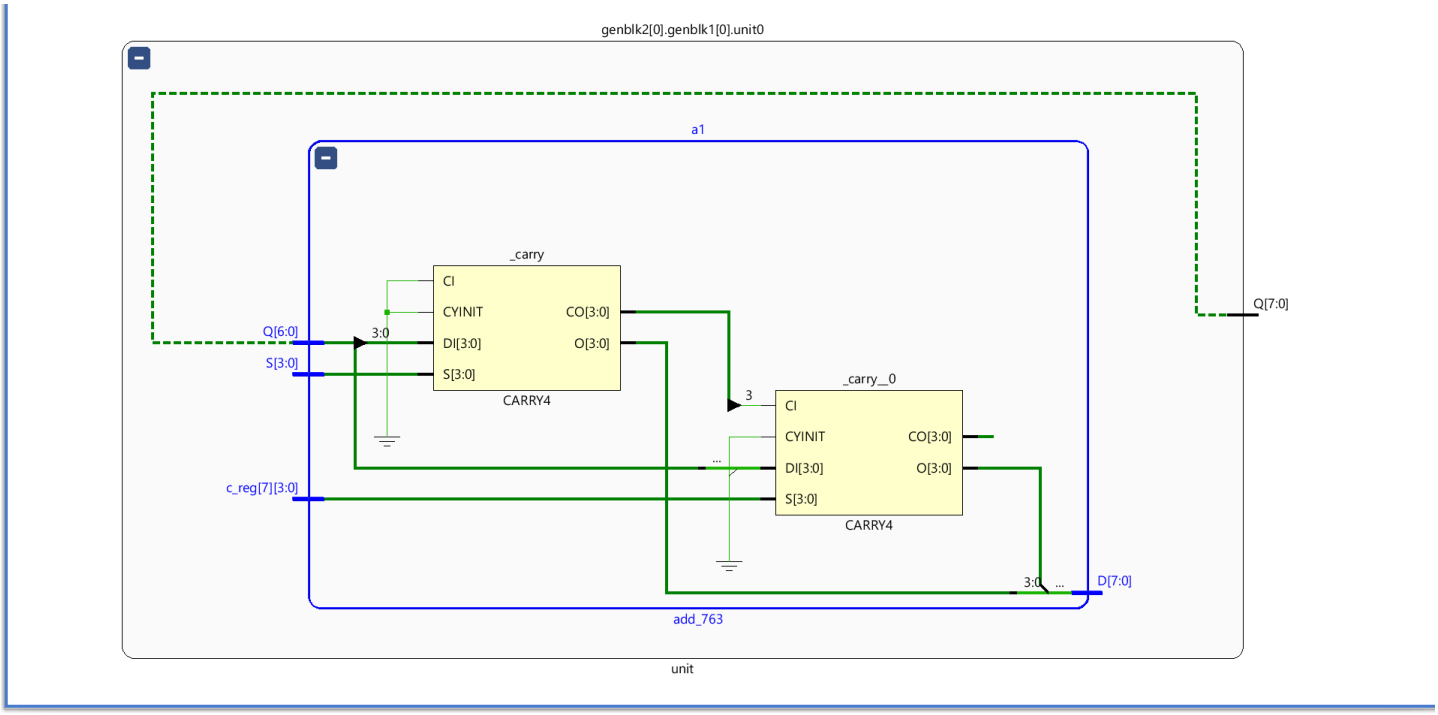
*Picture 1: the schematics of whole design*



*Picture 2: the synthesized schematics of PE*



*Picture 3: the schematics of multiply module*




*Picture 4: the schematics of adder module*

## 3. Estimation

**Utilization** Post-Synthesis | **Post-Implementation**

Graph | **Table**

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 10735 | 14400 | 74.55 |
| FF | 6233 | 28800 | 21.64 |
| IO | 28 | 54 | 51.85 |
| BUFG | 1 | 32 | 3.13 |

*Picture 1: resource estimation*

**Power** **Summary** | On-Chip

| | |
|---|---|
| **Total On-Chip Power:** | **0.189 W** |
| **Junction Temperature:** | **27.2 °C** |
| Thermal Margin: | 57.8 °C (4.9 W) |
| Effective ϑJA: | 11.5 °C/W |
| Power supplied to off-chip devices: | 0 W |
| Confidence level: | Low |

Implemented Power Report

*Picture 2: power estimation*

**Design Timing Summary**

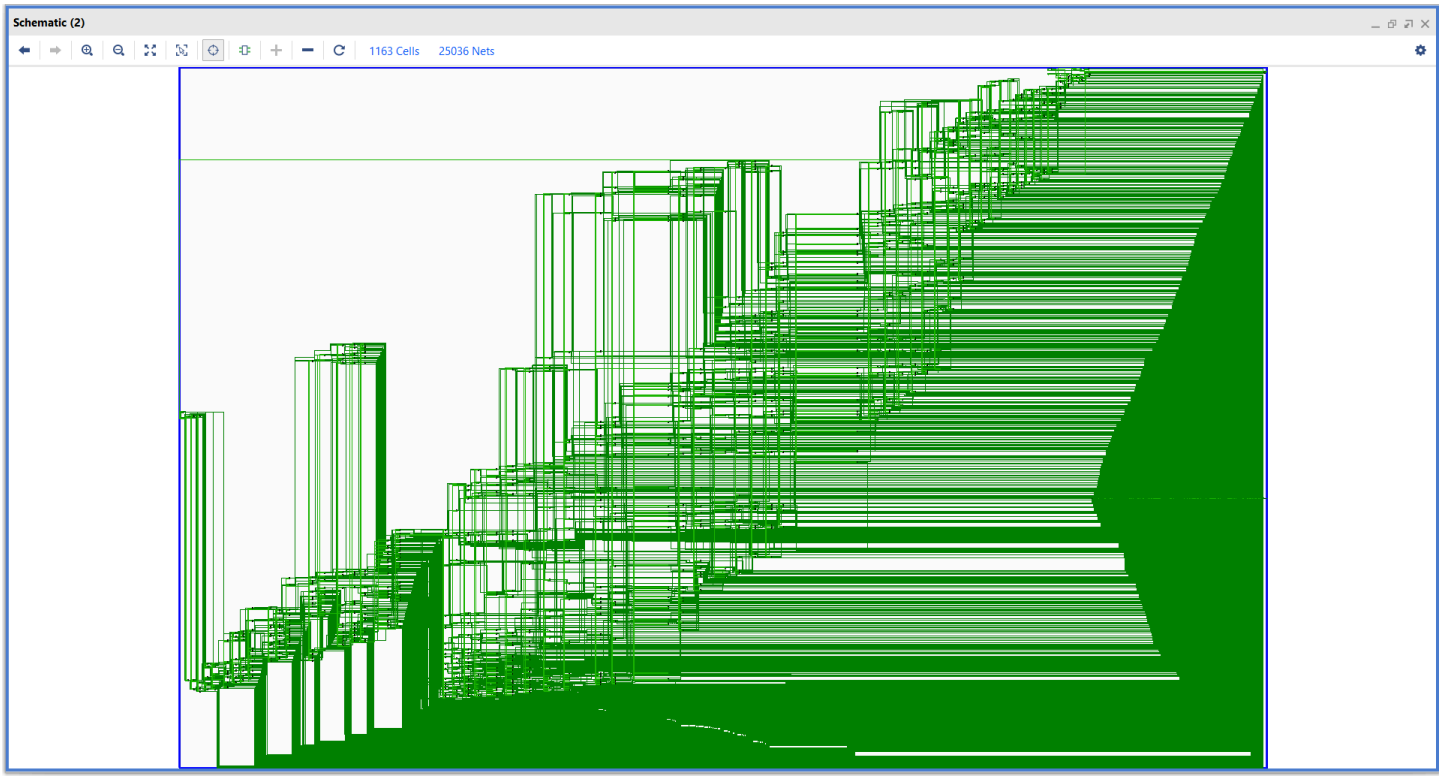
| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | 4.151 ns | Worst Hold Slack (WHS): | 0.061 ns | Worst Pulse Width Slack (WPWS): | 4.500 ns |
| Total Negative Slack (TNS): | 0.000 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 6282 | Total Number of Endpoints: | 6282 | Total Number of Endpoints: | 6234 |

**All user specified timing constraints are met.**

*Picture 3: timing estimation*

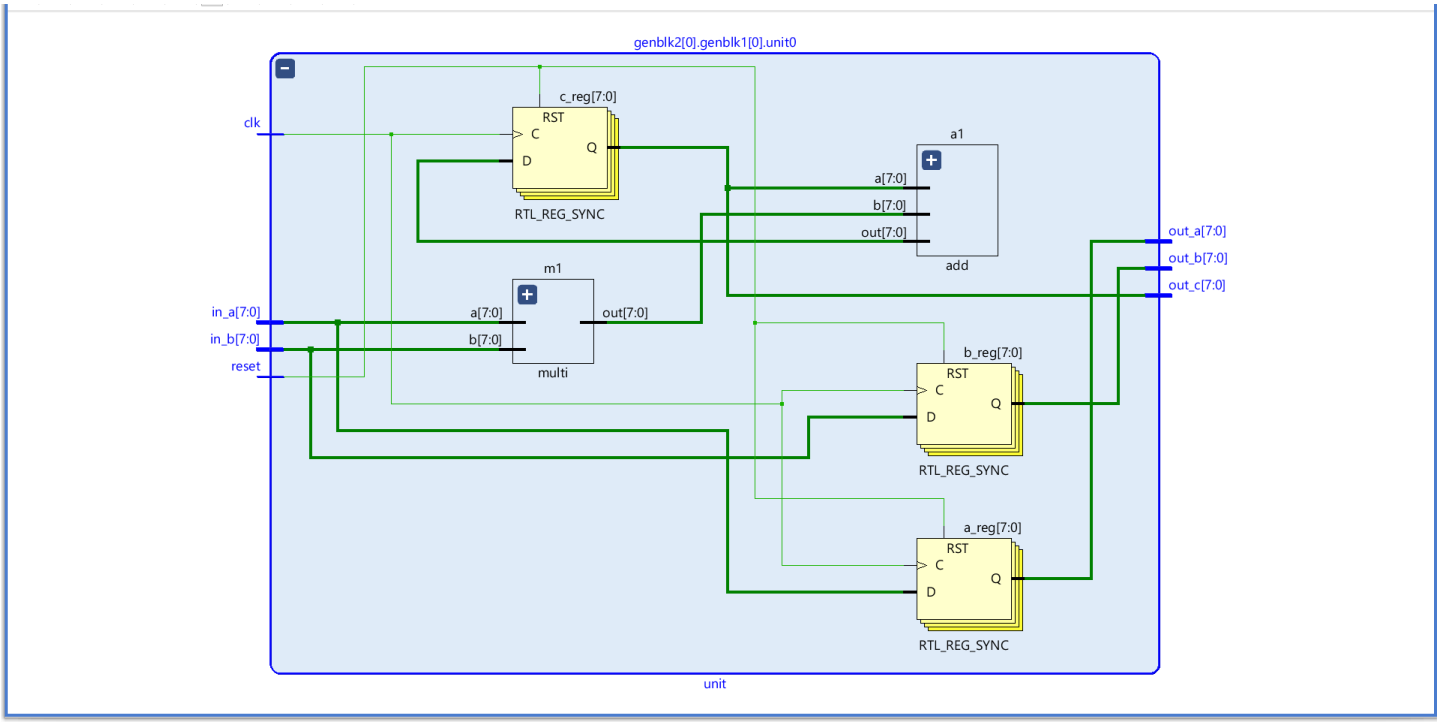
# Part 1: 32 * 32 elements

1. Elaborate design



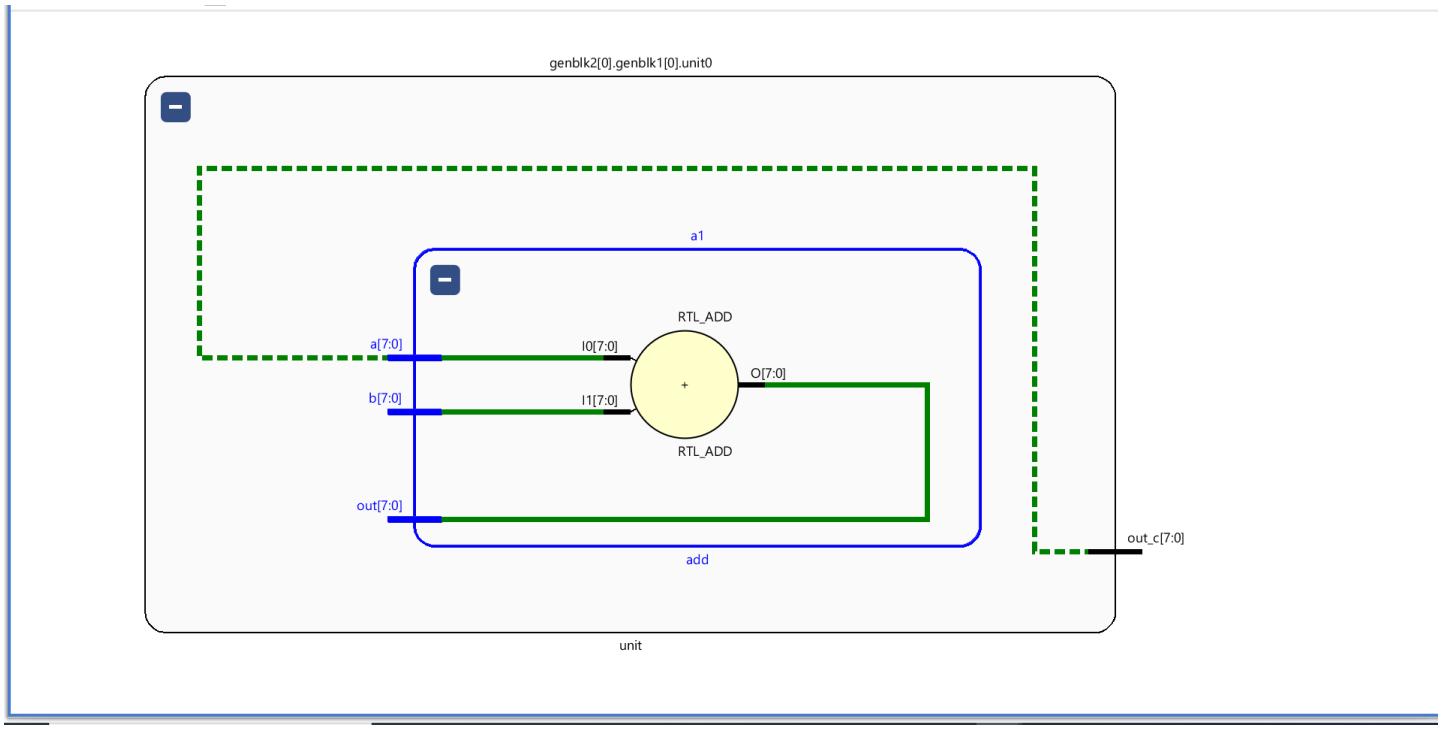

*Picture 1: schematics of Systolic array*

It includes 32*32 PEs.

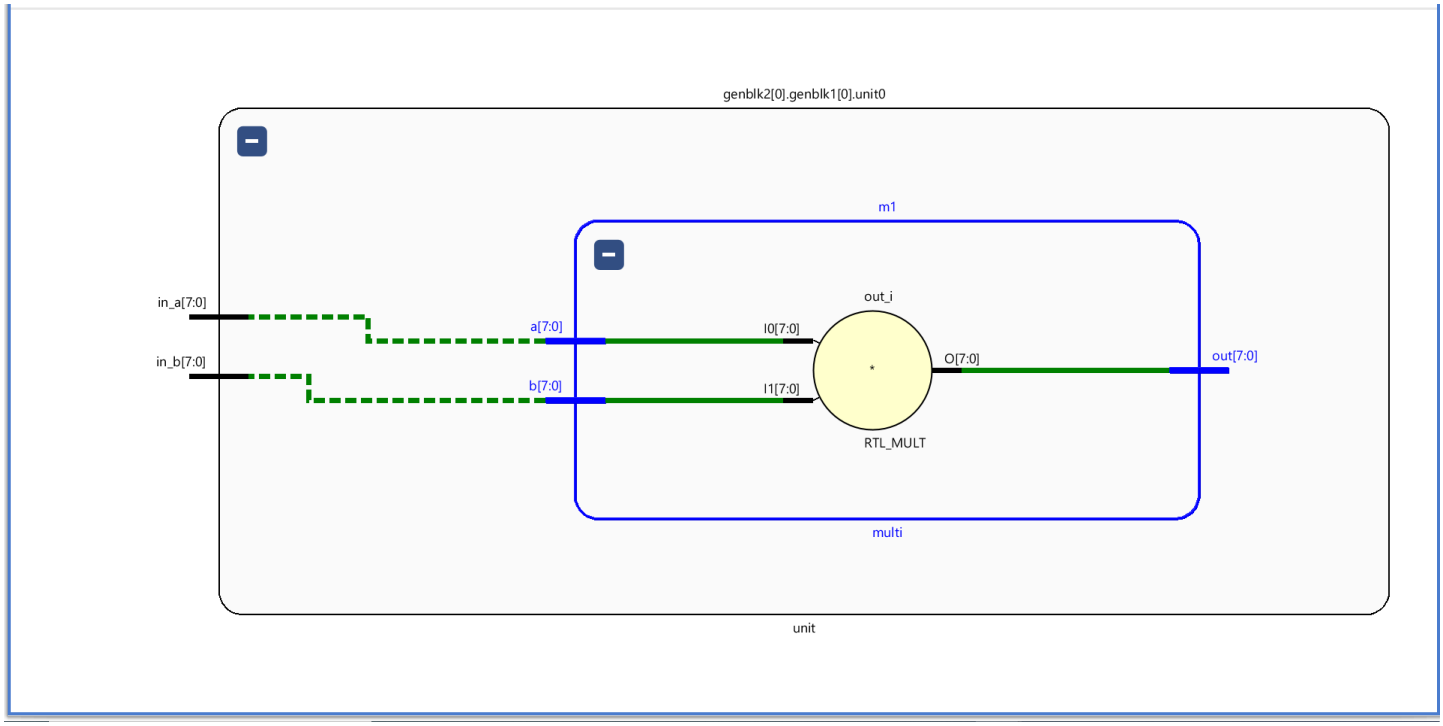



*Picture 2: schematics of PE*

It includes 1 adder and 1 multiply module.

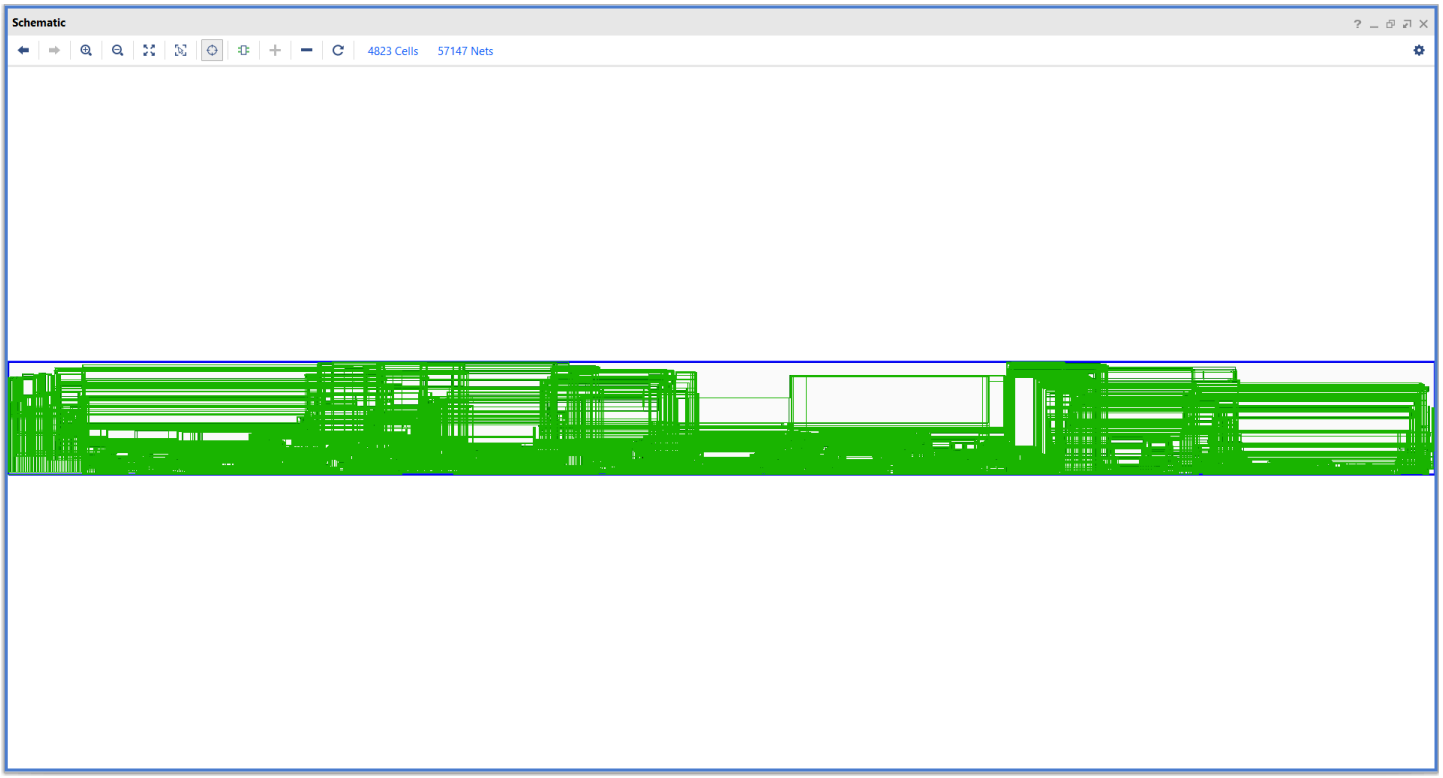



*Picture 3: adder module*

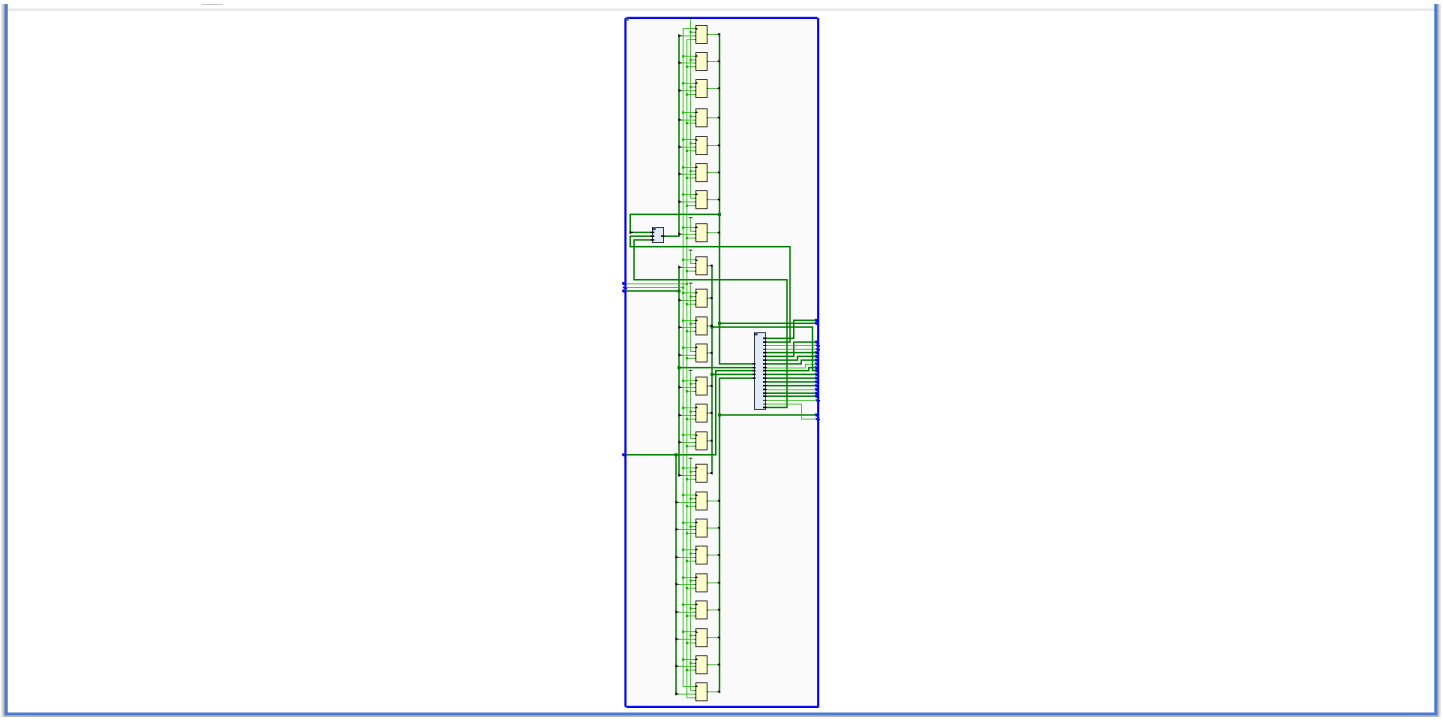



*Picture 4: multiply module*

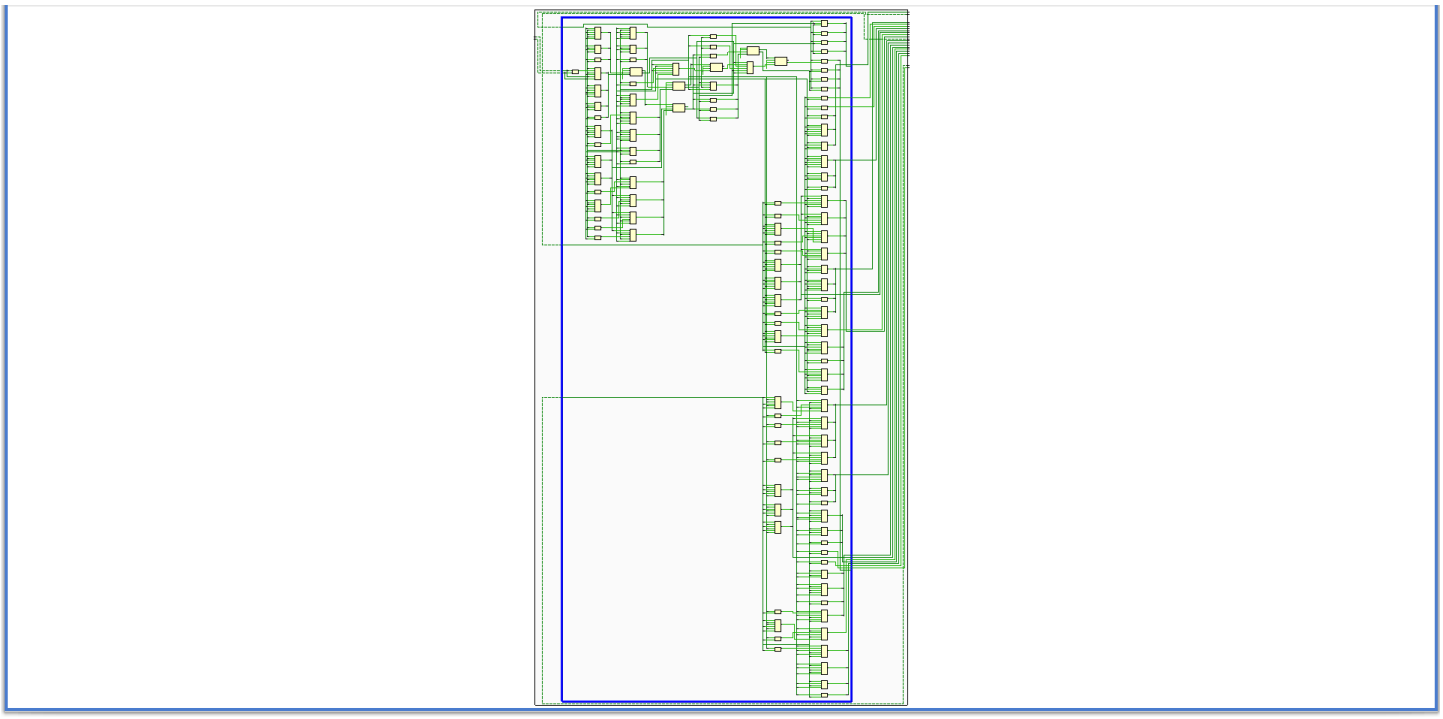
2. Synthesis design



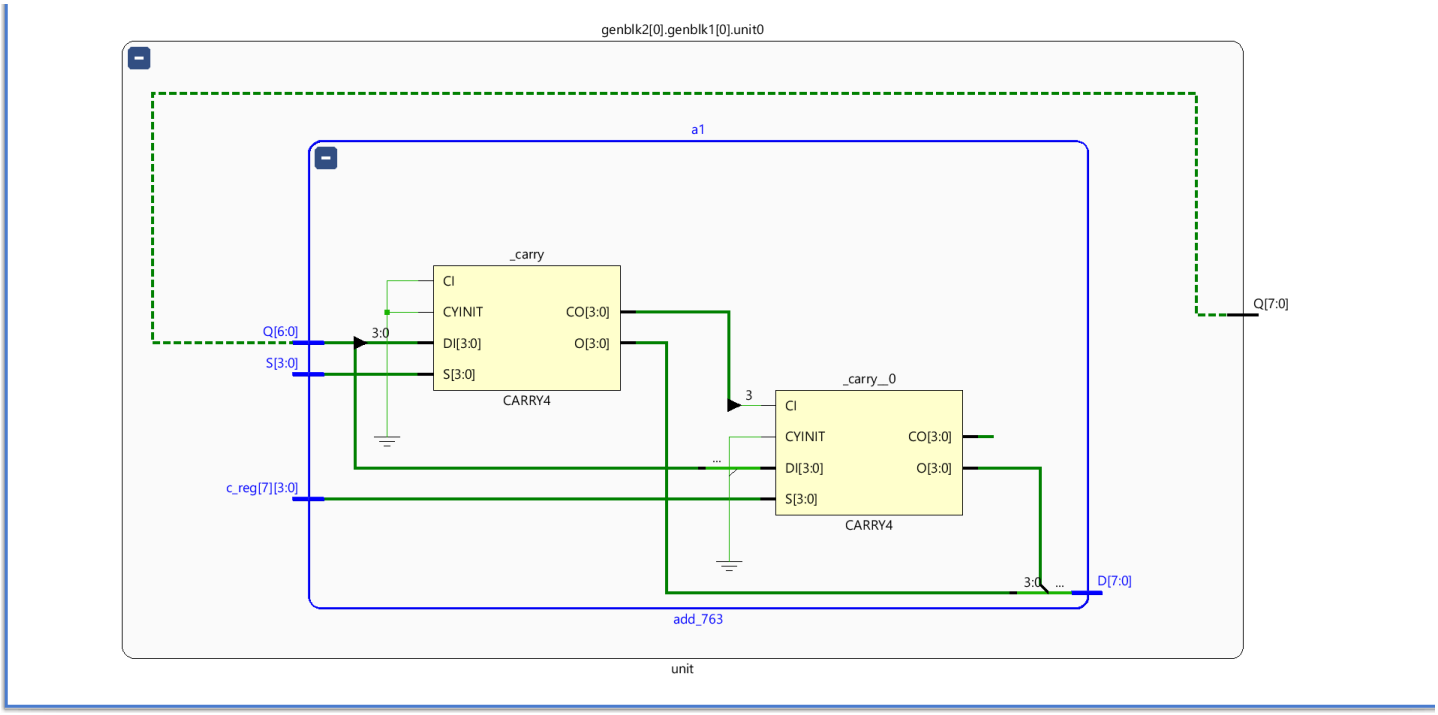

*Picture 1: the schematics of whole design*



*Picture 2: the synthesized schematics of PE*

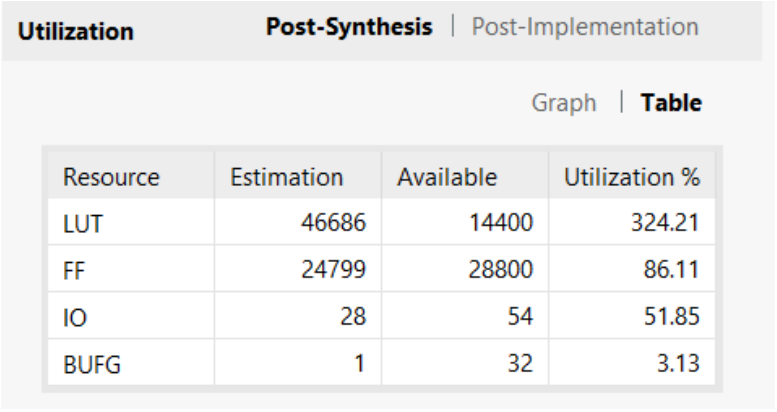


*Picture 3: the schematics of multiply module*




*Picture 4: the schematics of adder module*

## 3. Estimation




| Resource | Estimation | Available | Utilization % |
|---|---|---|---|
| LUT | 46686 | 14400 | 324.21 |
| FF | 24799 | 28800 | 86.11 |
| IO | 28 | 54 | 51.85 |
| BUFG | 1 | 32 | 3.13 |

*Picture 1: resource estimation*

Because the circuit has over-utilized the FPGA resource, the implementation is failed, so, there is no power or timing estimation.