

Deadline: December 4, 2023 at 23:59

Note: You are required to use the L^AT_EX template provided on Brightspace.

Question 1 (10 points)

Design an FSM for a music player with four buttons: stop, play, fast forward, and pause.

- The music player stops playing as soon as the stop button is pressed regardless of whether it is paused, playing or fast forwarding;
- the fast forward button can be used only when the player has been stopped;
- pause has no effect when the player is stopped or is fast forwarding;
- play button can be used when the player is paused or stopped.

Draw the FSM diagram and show the transitions.

Question 2 (15 points)

Assume a combinational logic circuit includes 3 outputs. Using logic gates design a circuit to determine if the majority of the outputs are 1 or 0.

Example:

Majority 1: 101, 110

Majority 0: 000, 001

Figure 1 depicts the diagram of the circuits. The output from the majority detector is 1, if at least 2 of its inputs are 1, and zero otherwise.

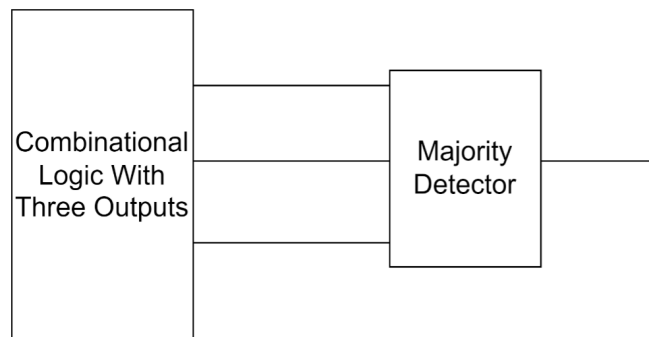


Figure 1

Question 3 (10 points)

Assume a circuit has 8 inputs and we want to select one input at a time. Design an 8-to-1 multiplexer for this application using two 4-to-1 multiplexers and one 2-to-1 multiplexer. Complete the solution shown below in Figure 2 by determining the select inputs of the multiplexers.

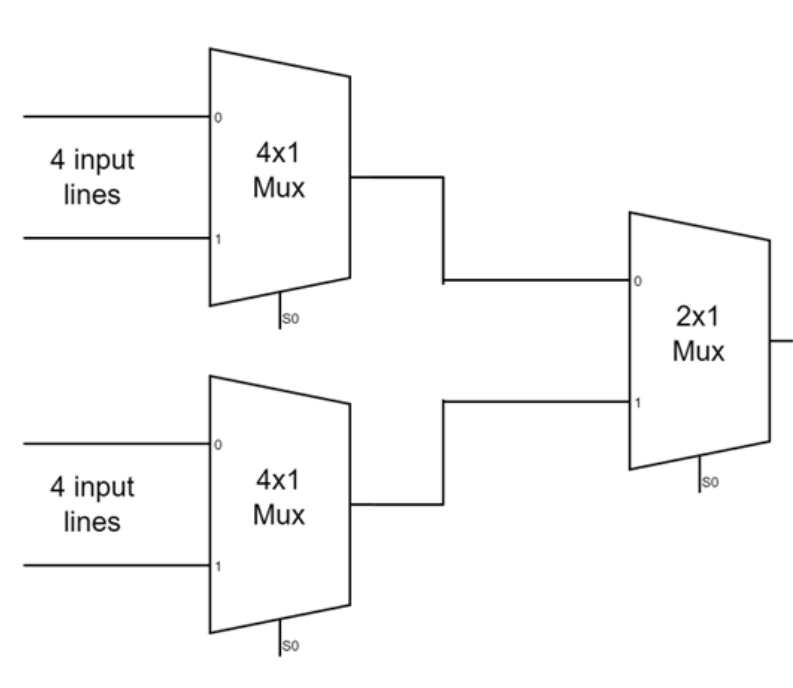


Figure 2

Question 4 (5 points)

The addressability of memory system of a computer is two bytes. You need 18 bits to access a location in memory. What is the total size of the memory in bytes?

Question 5 (15 points)

Even parity is a method of error checking used in digital communication. In the context of parity bits, "even parity" refers to the parity bit being 1 or 0 in a way that the total number of "1" bits (including the parity bit) is an even number.

Assume data is 8 bits. Design a combinational logic circuit to generate the even parity bit for the data.

Question 6 (10 points)

In the shift register in Figure 3, select bits of the multiplexers determine the operation. The register can preserve the current value, shift left with serial input from the least significant bit, shift right with serial input from the most significant bit, and parallel input. Modify the circuit to perform circular shifts instead of serial input shifts. In a left circular shift the most significant bit is placed at the least significant bit position. In a similar way, a right circular shift moves the least significant bit to the most significant bit position.

Example:

Current value: 0011

After left circular shift: 0110

After right circular shift: 1001

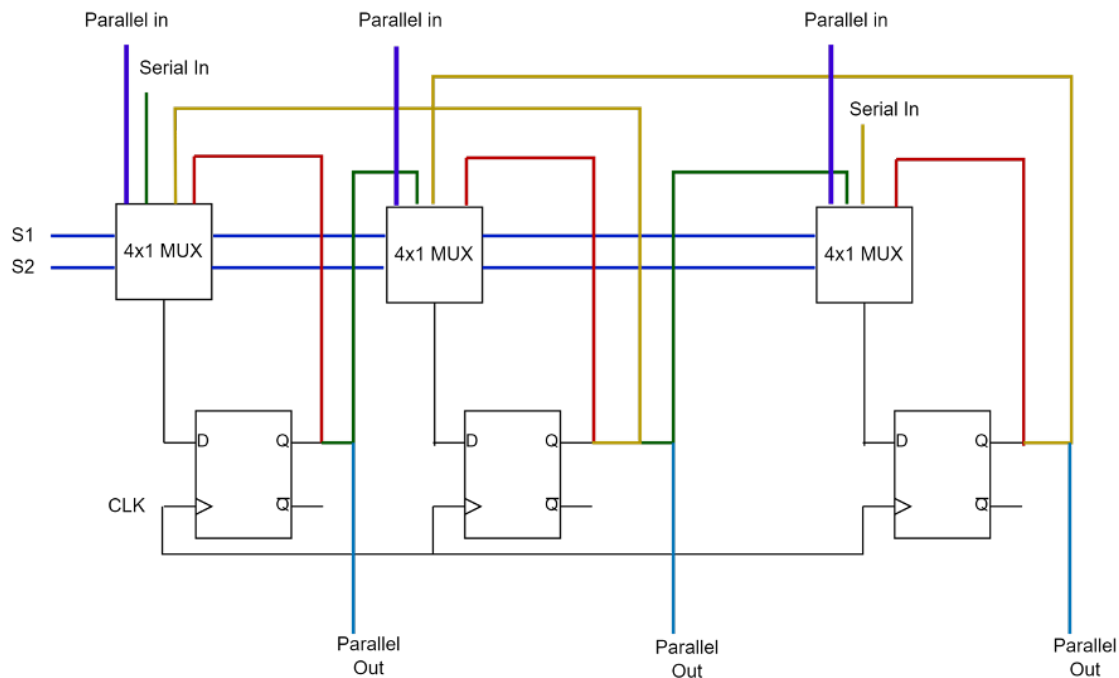


Figure 3

Question 7 (15 points)

Figure 4 depicts a combinational logic circuit of a 2-to-4 decoder (two inputs A_1 and A_0 and 2^2 outputs $F_3F_2F_1F_0$) with an enable input signal E .

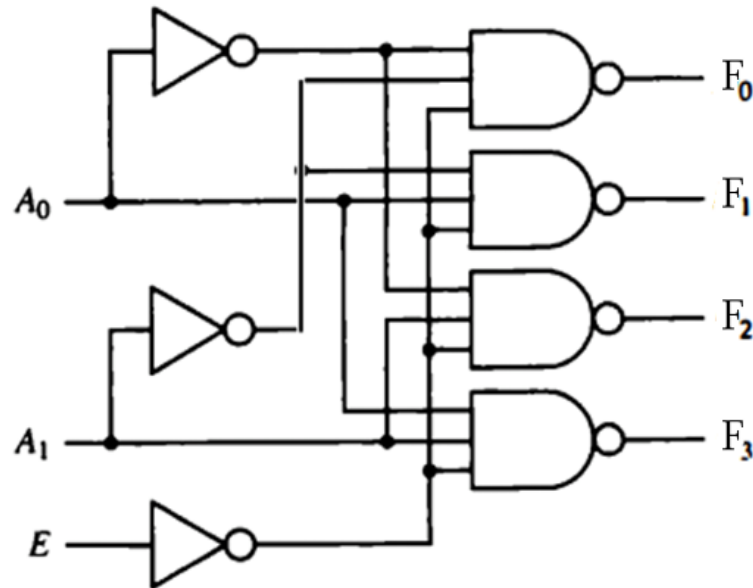


Figure 4

- a) Fill all of the missing values in the following truth table and provide the steps you followed to obtain your answers. Please note that symbol X in the table can represent both 0 or 1 (the so-called “don’t care”).

E	A_1	A_0	F_3	F_2	F_1	F_0
1	X	X				
0	0	0				
0	0	1				
0	1	0				
0	1	1				

- b) How many 2-to-4 decoders are needed to design a 4-to-16 decoder? Explain your answer.

Question 8 (10 points)

The circuit in Figure 5 receives two 4-bit binary numbers (2’s complement). The output of the circuit is 1 if the numbers are equal and 0 otherwise. Design the circuit using logic gates.

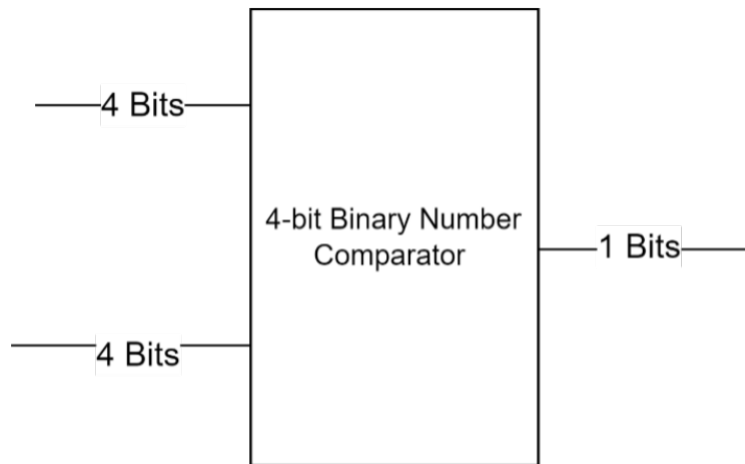


Figure 5

Question 9 (10 points)

The memory depicted in Figure 6 contains 1024 memory locations.

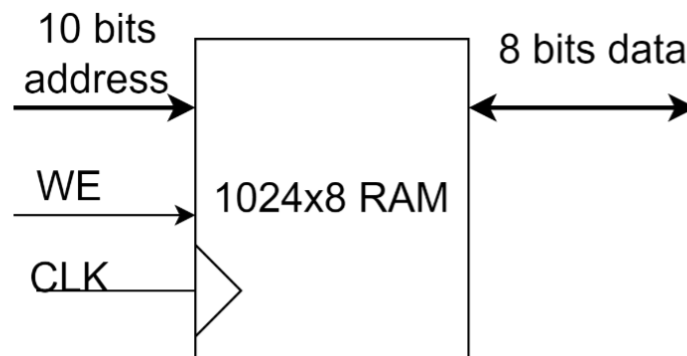


Figure 6

- To increase the capacity of the memory to 2048, two circuits of 1024 locations are used. How many bits are needed to address each location after this extension?
- How should we connect the address/data/WE buses to these memory units? (Draw your solution)