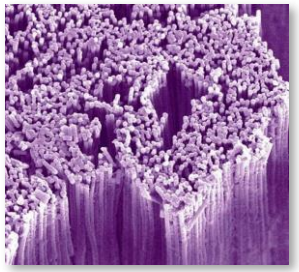
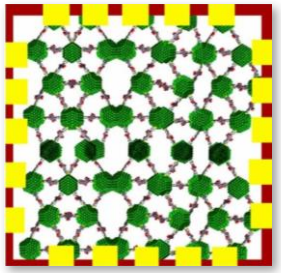
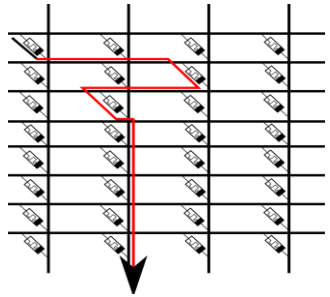
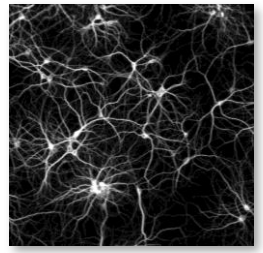
# ECEN 158/258
# Introduction to Neuromorphic Computing

Fr. Dat Tran, S. J.

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Emerging Computing Models and Technologies

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THE STATE UNIVERSITY OF NEW JERSEY
RUTGERS

# Module 1
# Conventional and Bio-inspired Computing

# What is a Computing System?


Computing Systems

# What is a Computing System?

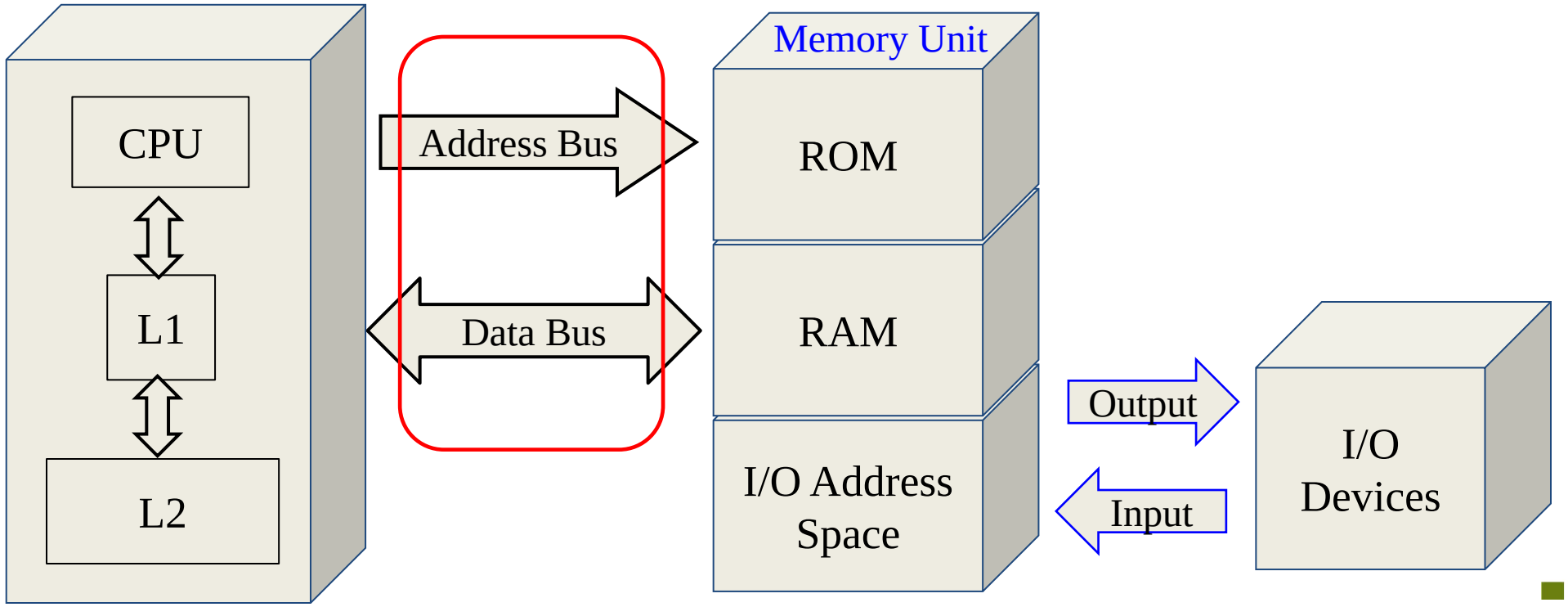
Analog Inputs

https://neurosurgerycnj.com/a-guide-to-brain-cells/

Response

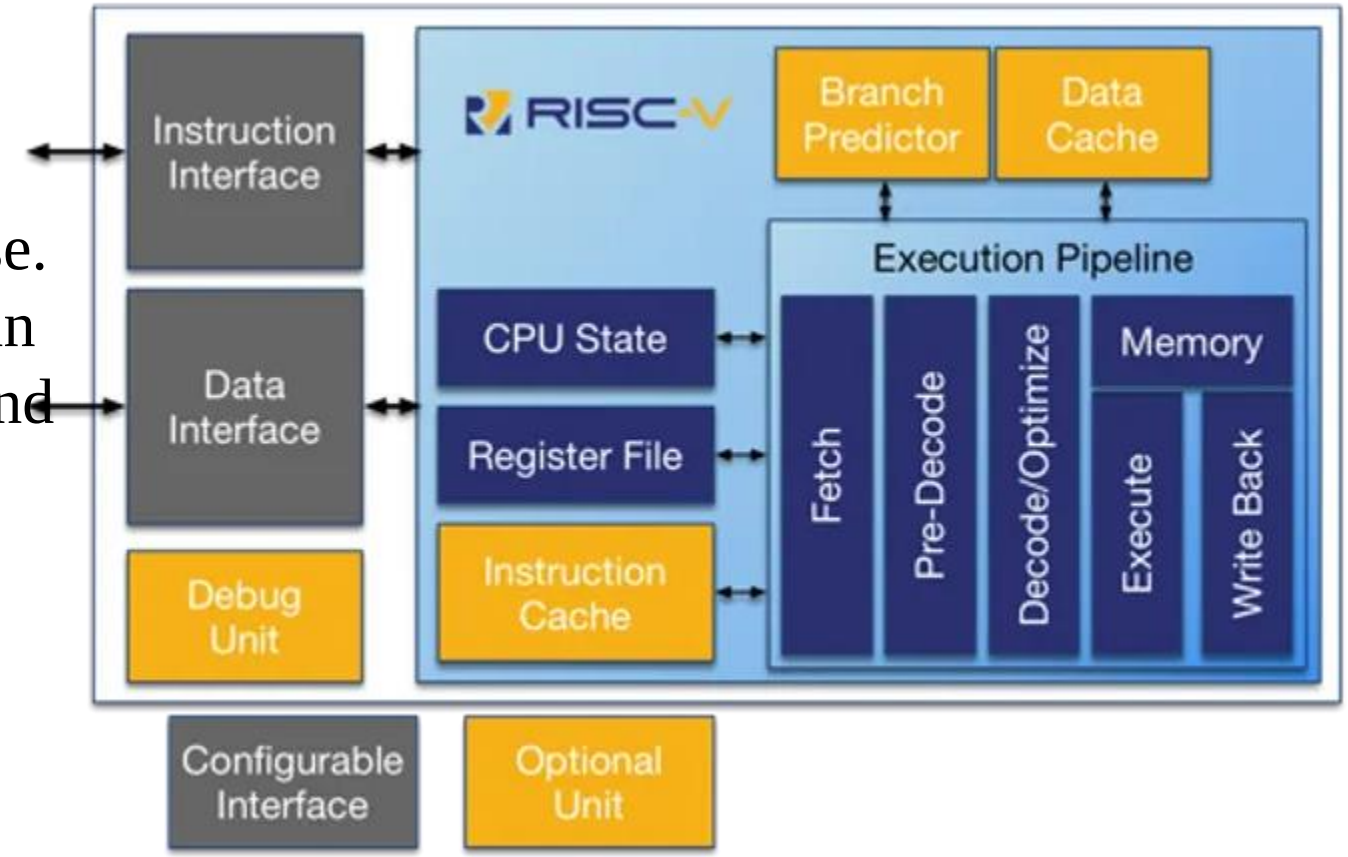
# Von Neumann Computing Architecture

- Conventional Computing System: Central Processing Unit (CPU), Memory Unit, and IO Devices.
- The limited bandwidth of the data path → the bottleneck.



# Reduced Instruction Set Computing (RISC)

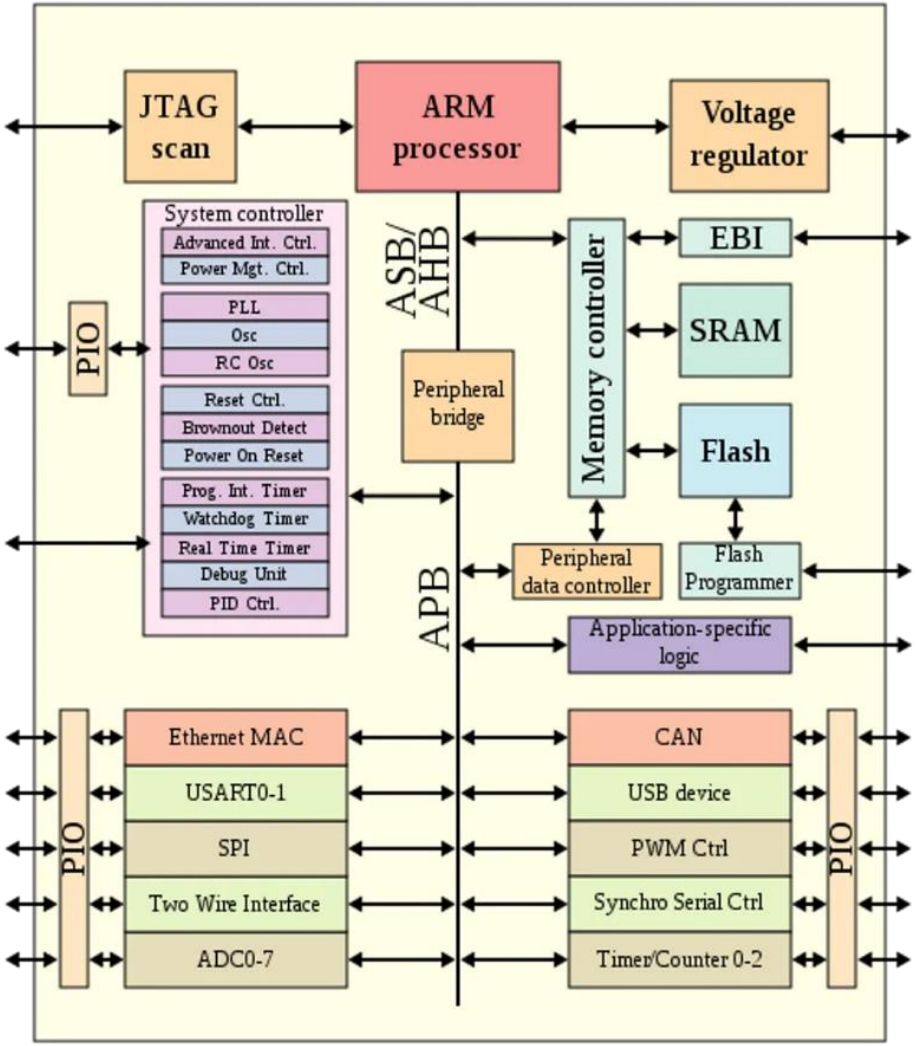
- RISC-V began at the Computer Science Division at UC Berkeley in 2010.
- Load-store ISA (Instruction Set Architecture) and open-source license.
- Standardization of the RISC-V ISA in 2015 → RISC-V-based processors and systems-on-chip (SoCs): Google, NVIDIA, and Western Digital.
- RISC-V Privileged Architecture Specification: In 2017, the RISC-V platform received more complex RISC-V processors and common operating systems (Linux).




https://www.wevolver.com/article/risc-v-vs-arm-a-comprehensive-comparison-of-processor-architectures

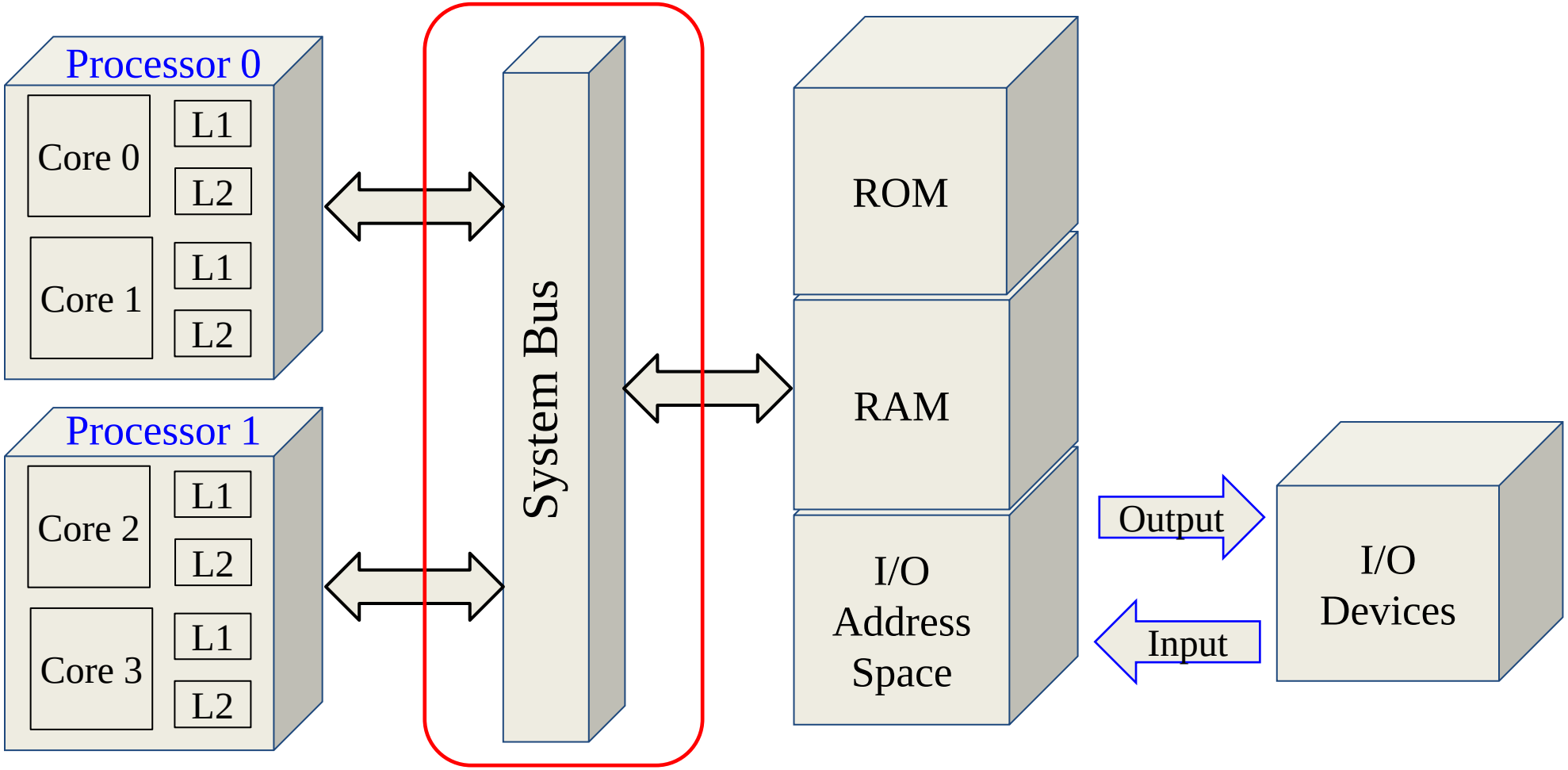
# Advanced RISC Machine (ARM)

- ARM (Advanced RISC Machine)
- License processor.
- Energy-efficient mobile computing devices
- ARM families: Cortex-A (high-performance mobile devices), Cortex-R (real-time systems, fast interrupt response times), and Cortex-M series (microcontrollers, low-power devices, and energy efficiency).
- L1 cache: separate instructions and data; supports (L2) and (L3) caches.



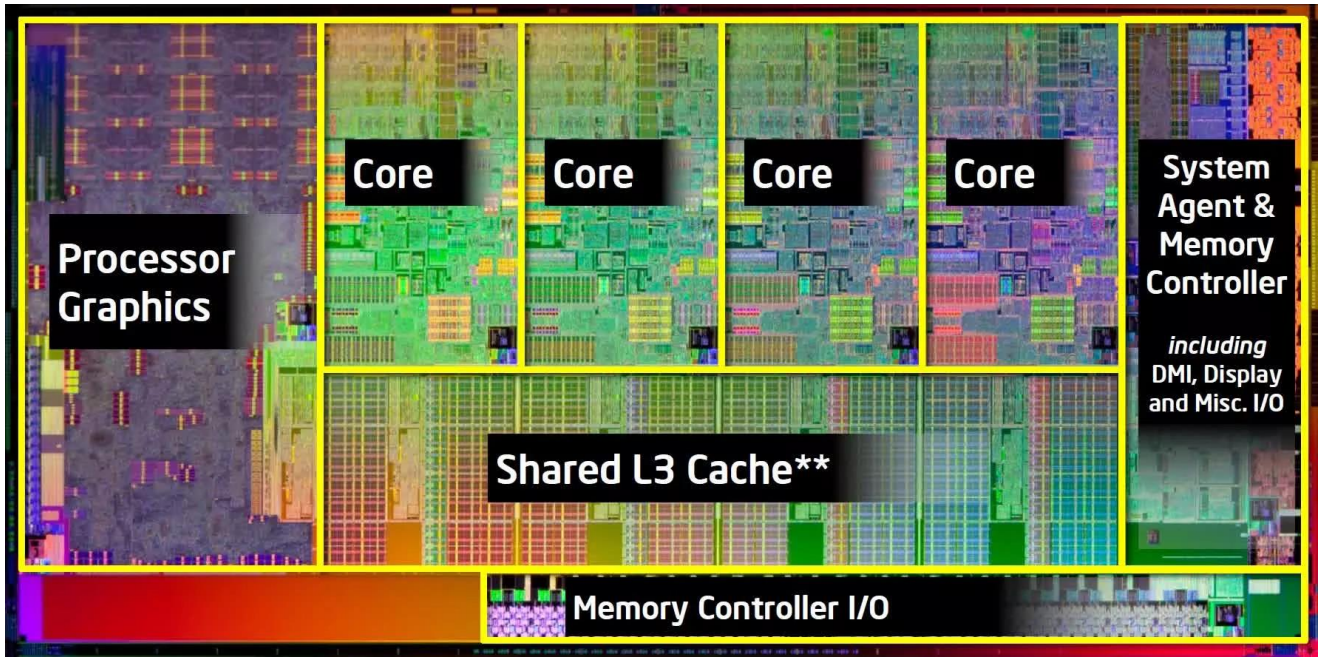

https://www.wevolver.com/article/risc-v-vs-arm-a-comprehensive-comparison-of-processor-architectures

# Multicore Computing System



# Multicore Computing System

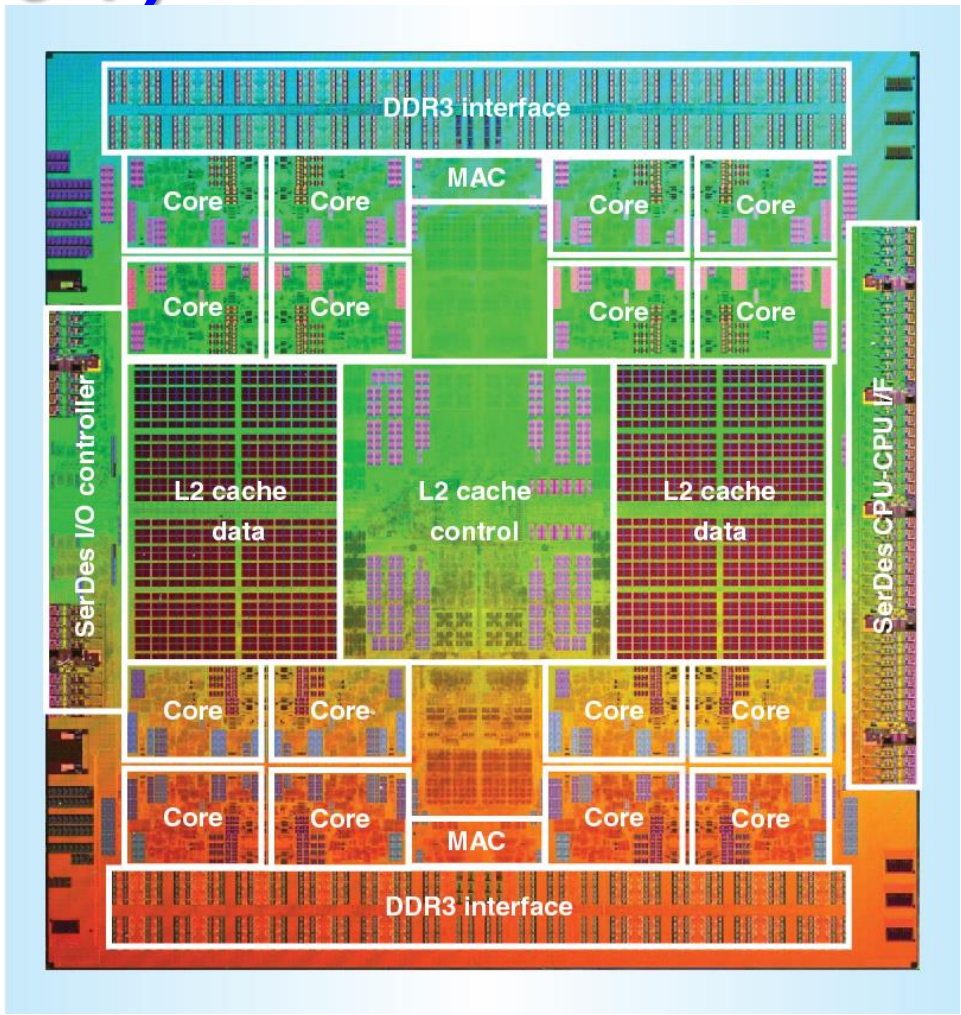
- The multi-core combines more than one core in a processor package and functions as one unit.
- Individual cores share common resources (caches) to speed up program execution.
- A physical core refers to the physical hardware unit that is actualized by the transistors and circuitry that make up the core.
- a logical core refers to the independent thread-execution ability of the core.




https://www.techspot.com/article/2363-multi-core-cpu/

# Scalable Processor ARChitecture (SPARC64)

- A (RISC) instruction set architecture initially developed by Sun Microsystems.
- The multi-core, multi-thread per core and large on-chip cache memory provide a significant boost over single-chip performance.
- A complex inter-core communication network with superscalar implementation.

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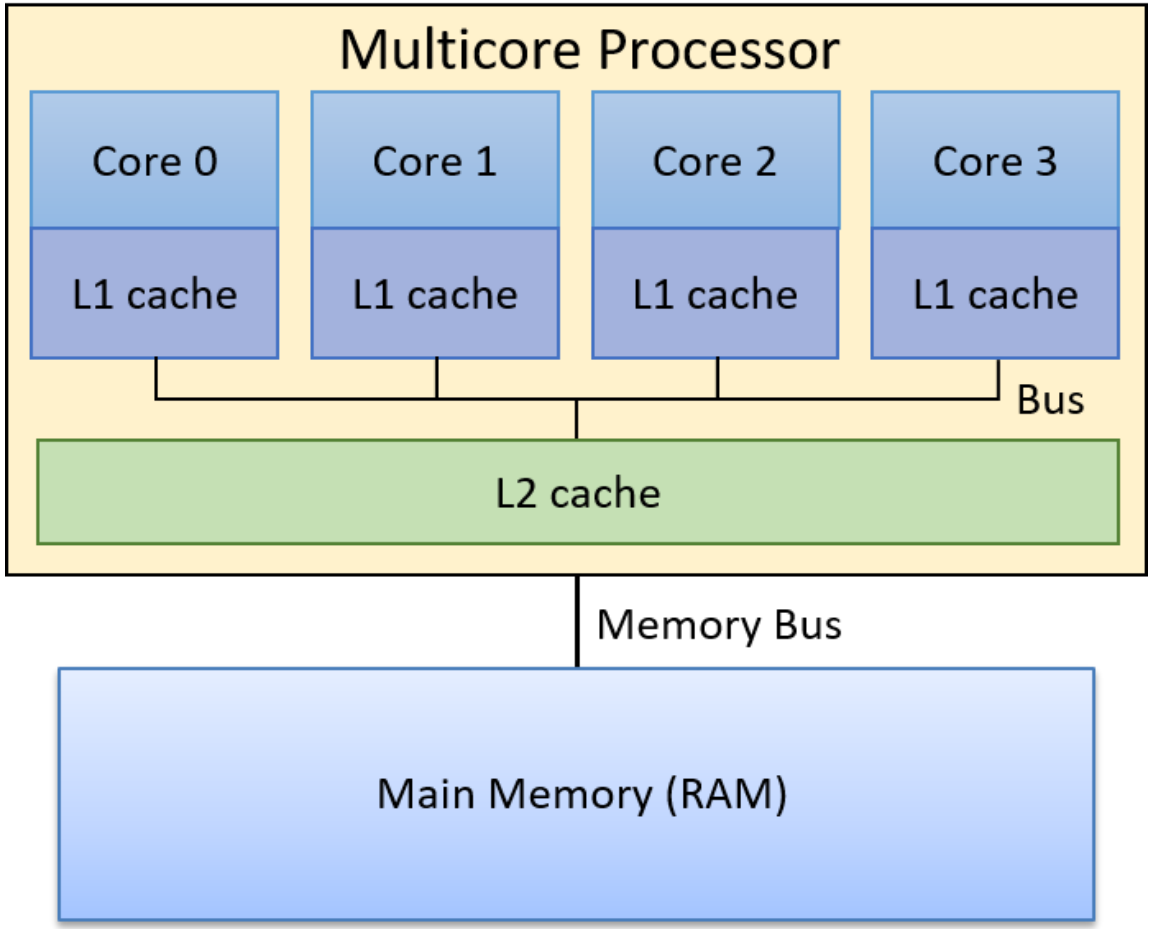
Yoshida, Toshio et al. “Sparc64 X: Fujitsu's New-Generation 16-Core Processor for Unix Servers.” IEEE Micro 33 (2013): 16-24.

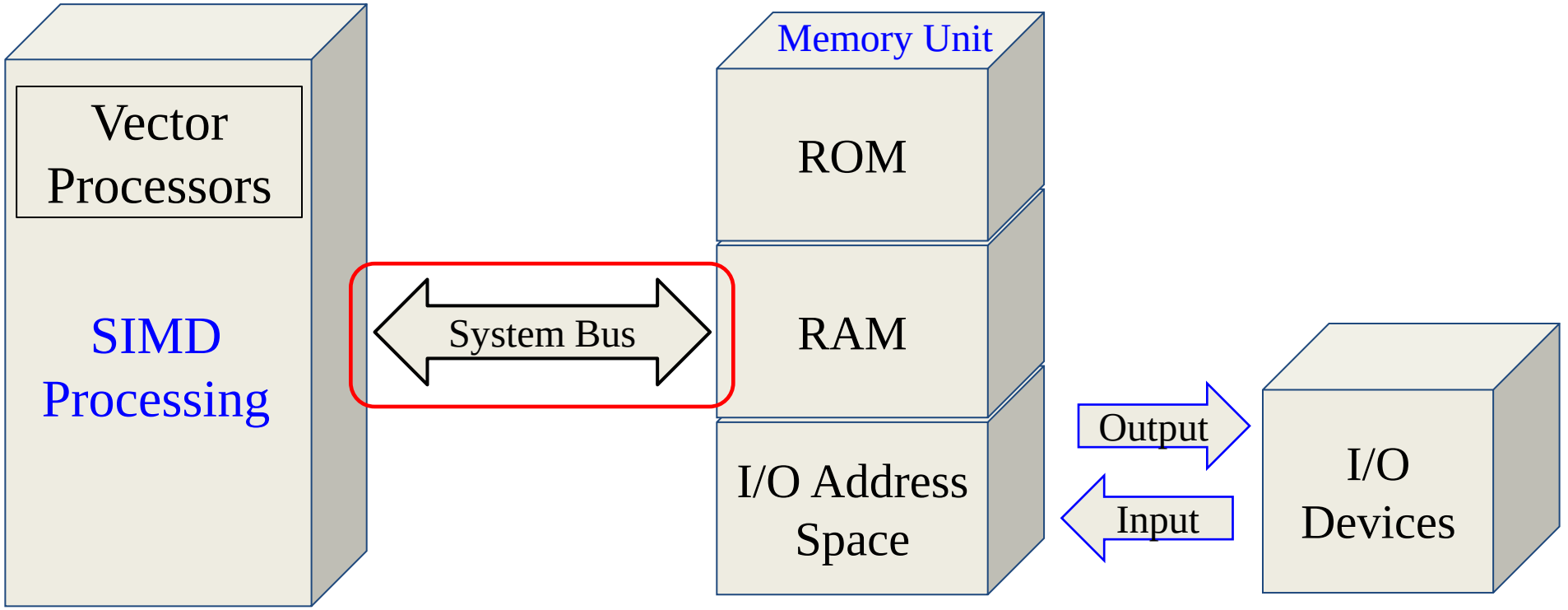
# X86 and AMD 64 Athlon

- x86 (also known as 80x86 or the 8086 family)
- Implementations of x86 and AMD are entirely based on the von Neumann.
- They are the most widely used load-store ISA with complex instruction set computers (CISC) for personal computers.



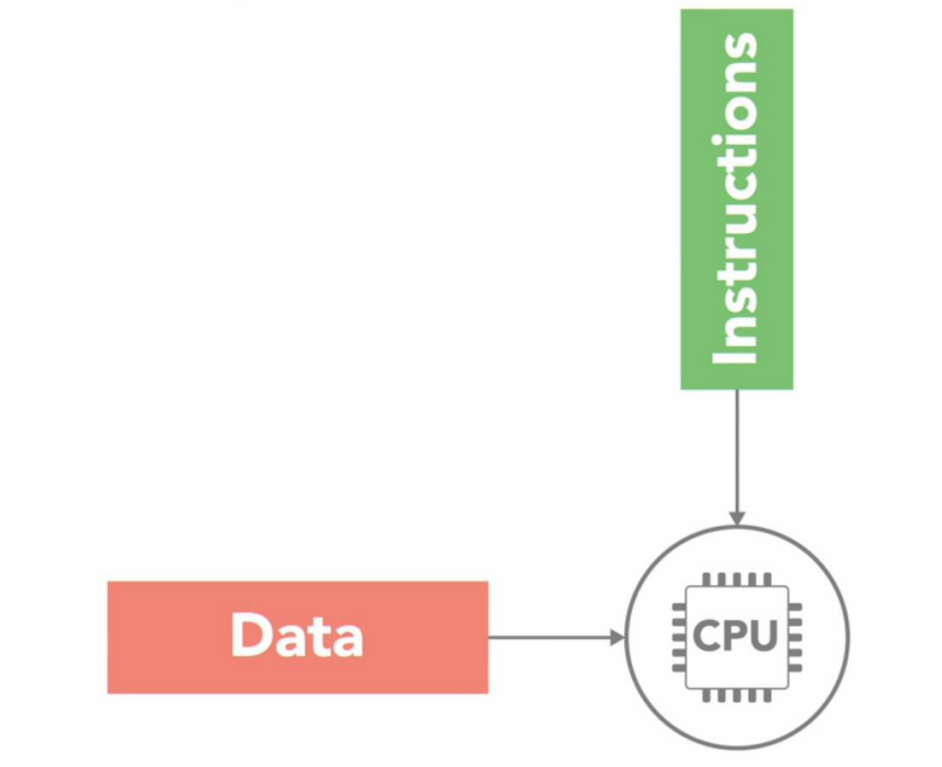

https://diveintosystems.org/book/C11_MemHierarchy/coherency.html

# Vector Processor System

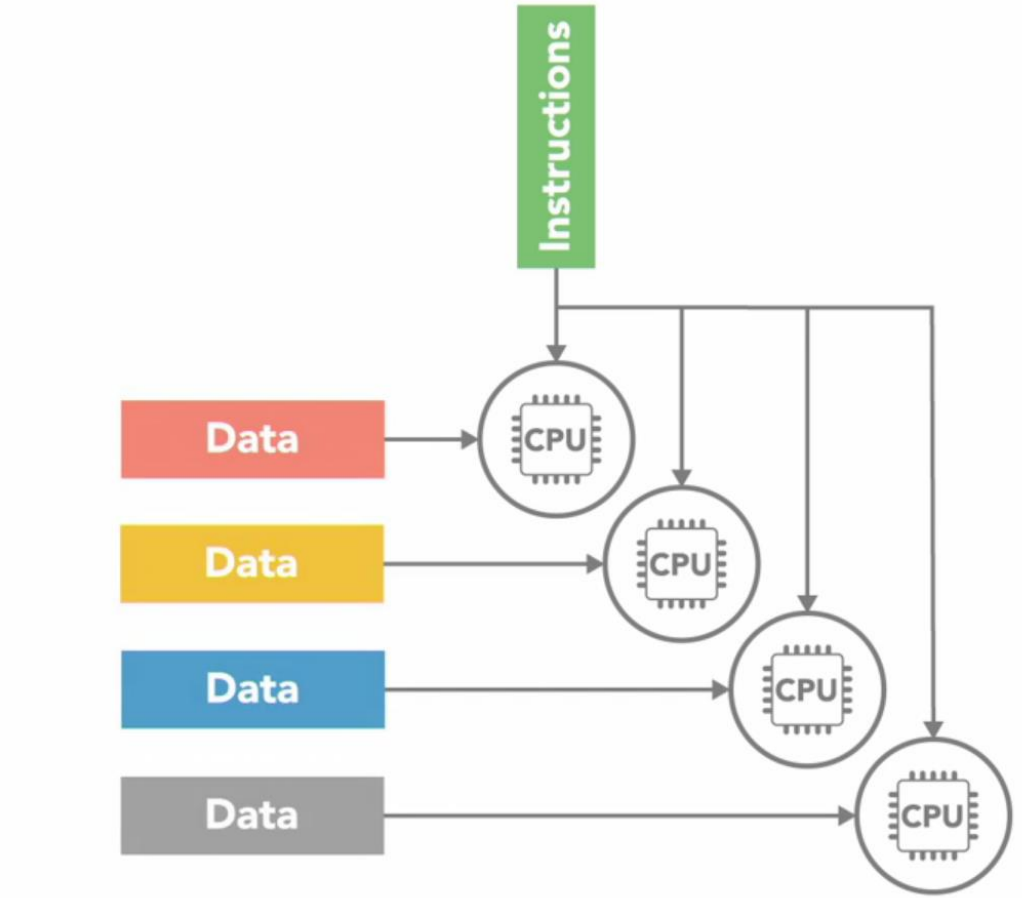


# Vector Processor System

https://www.robinsiwach.com/concurrency/



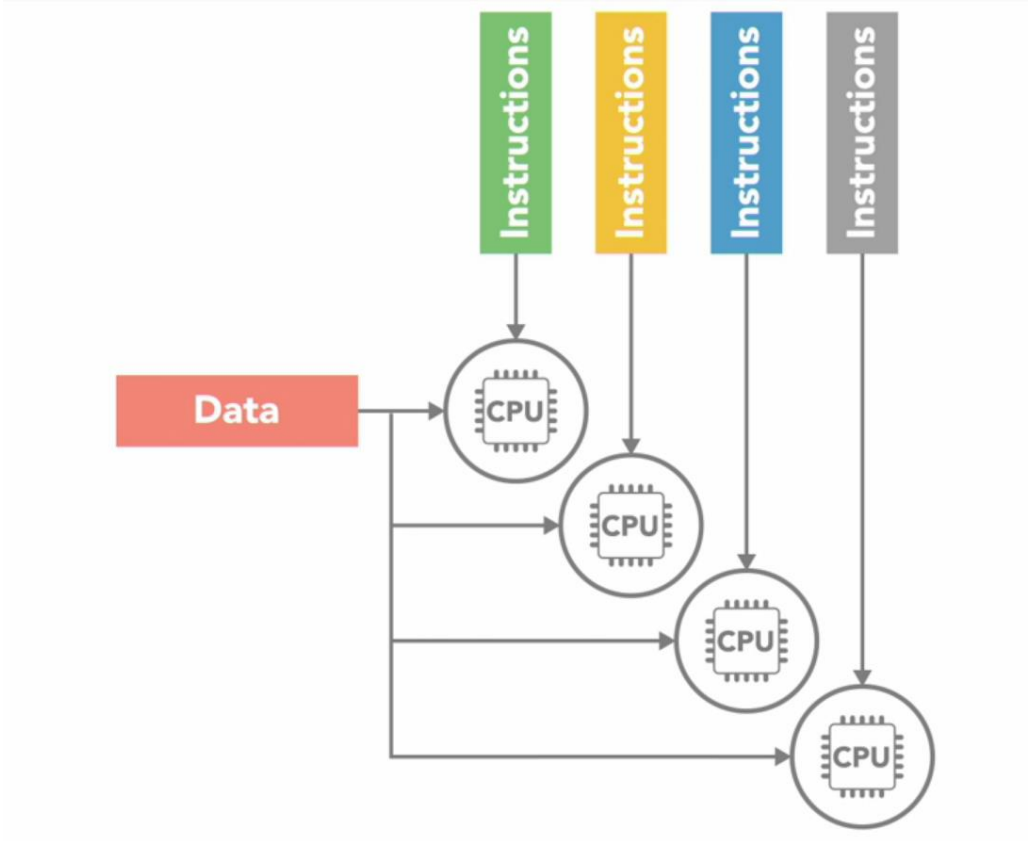

SISD (Single Instruction Single Data)



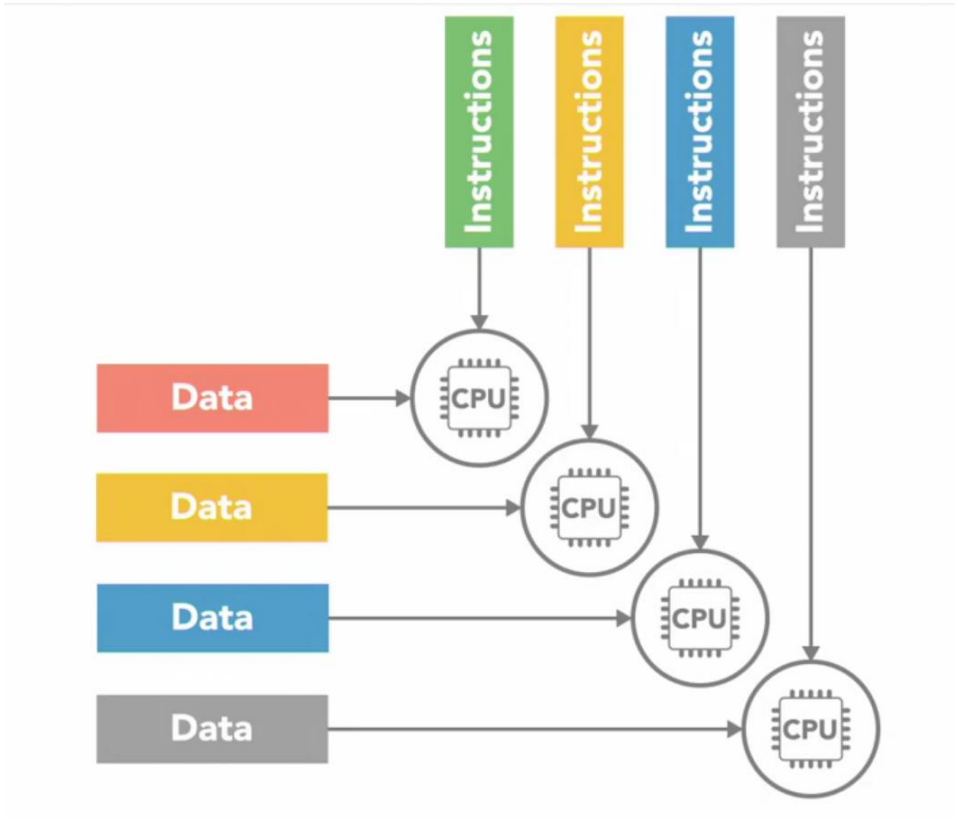

SIMD (Single Instruction Multiple Data)

# Vector Processor System

https://www.robinsiwach.com/concurrency/



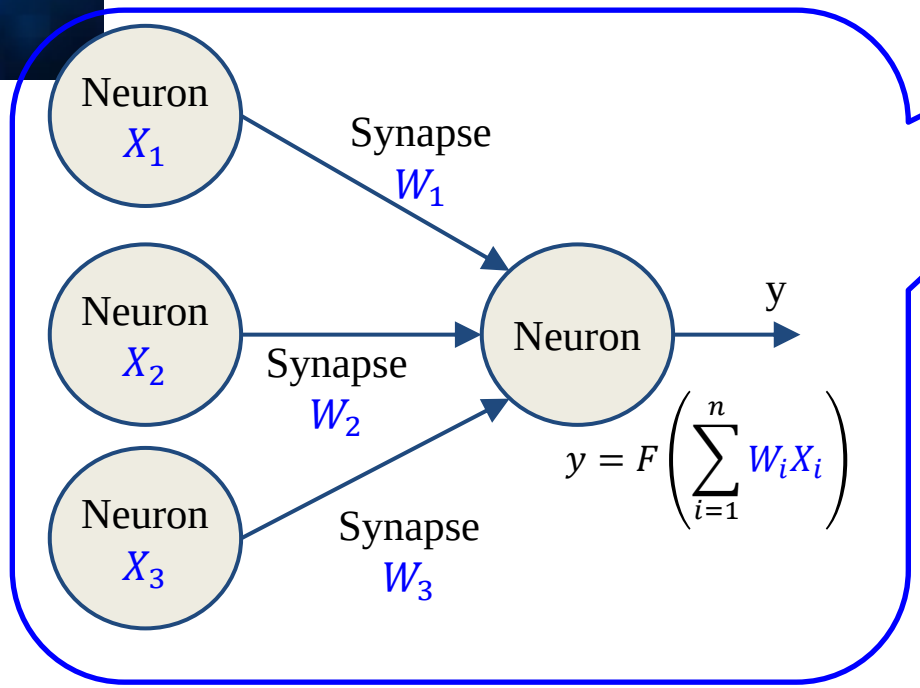

MISD (Multiple Instruction Single Data)

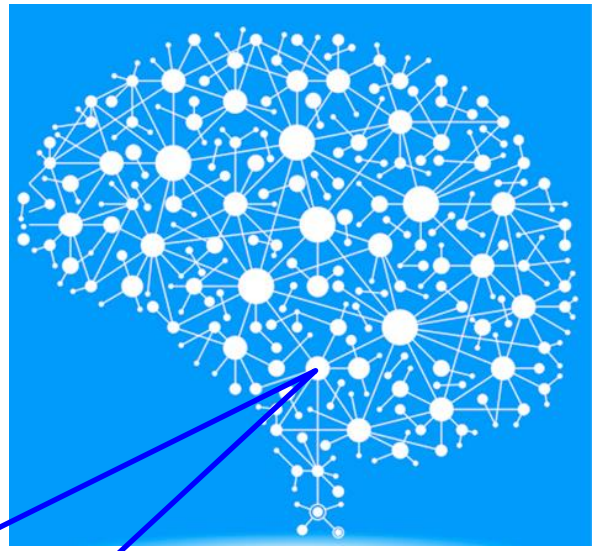



MIMD (Multiple Instruction Multiple Data)

# Human Brain System

https://neurosurgerycnj.com/a-guide-to-brain-cells/



https://www.extremetech.com/extreme/215170-artificial-neural-networks-are-changing-the-world-what-are-they

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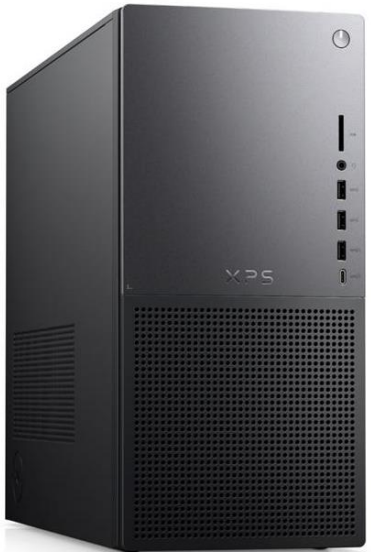
# Neuromorphic Computing



- ~ 1 trillion neurons (~ 1kg)
- ~ 700 trillion of synapses
- ~ 20W

- 10 of the second-fastest supercomputers
- weigh 3,400 metric tons
- ~ 150 MW (100k average households).

"Computing with Brainpower: Merck KGaA, Darmstadt, Germany." Computing with Brainpower | Merck KGaA, Darmstadt, Germany, www.emdgroup.com/en/research/science-space/envisioning-tomorrow/smarter-connected-world/neuromorphic-networks.html. Accessed 24 Jan. 2024.

# What is Neuromorphic Computing?

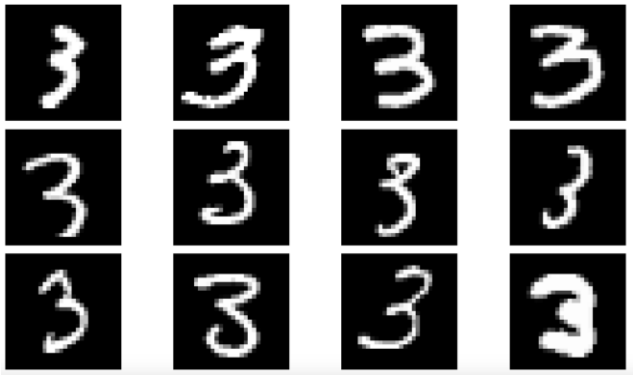
- Neuromorphic computing is brain-inspired computing.
- There are specific tasks where we do better than conventional computing systems.
- Brain network (hardware) is evolving.
- The Human Brain is exceptionally energy-efficient, adaptable, and tolerable.
- Multitasking.

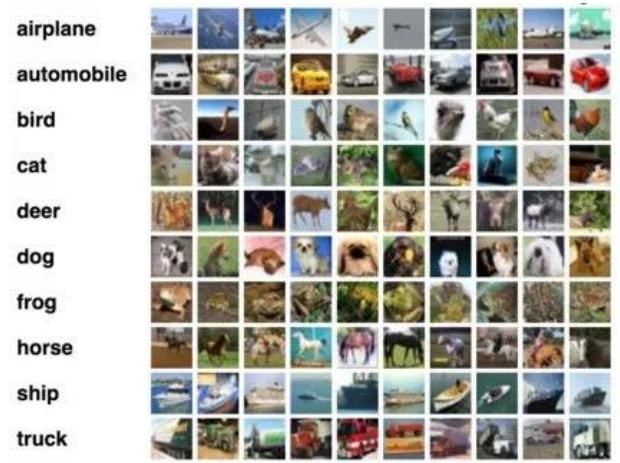
# Neuromorphic Tasks

# Neuromorphic Tasks

# Neuromorphic Tasks

- Digit classification and Class classification.






- Image recognition tasks (16-megapixel)

In 2008

Neuromorphic architectures

Training process

In 2016

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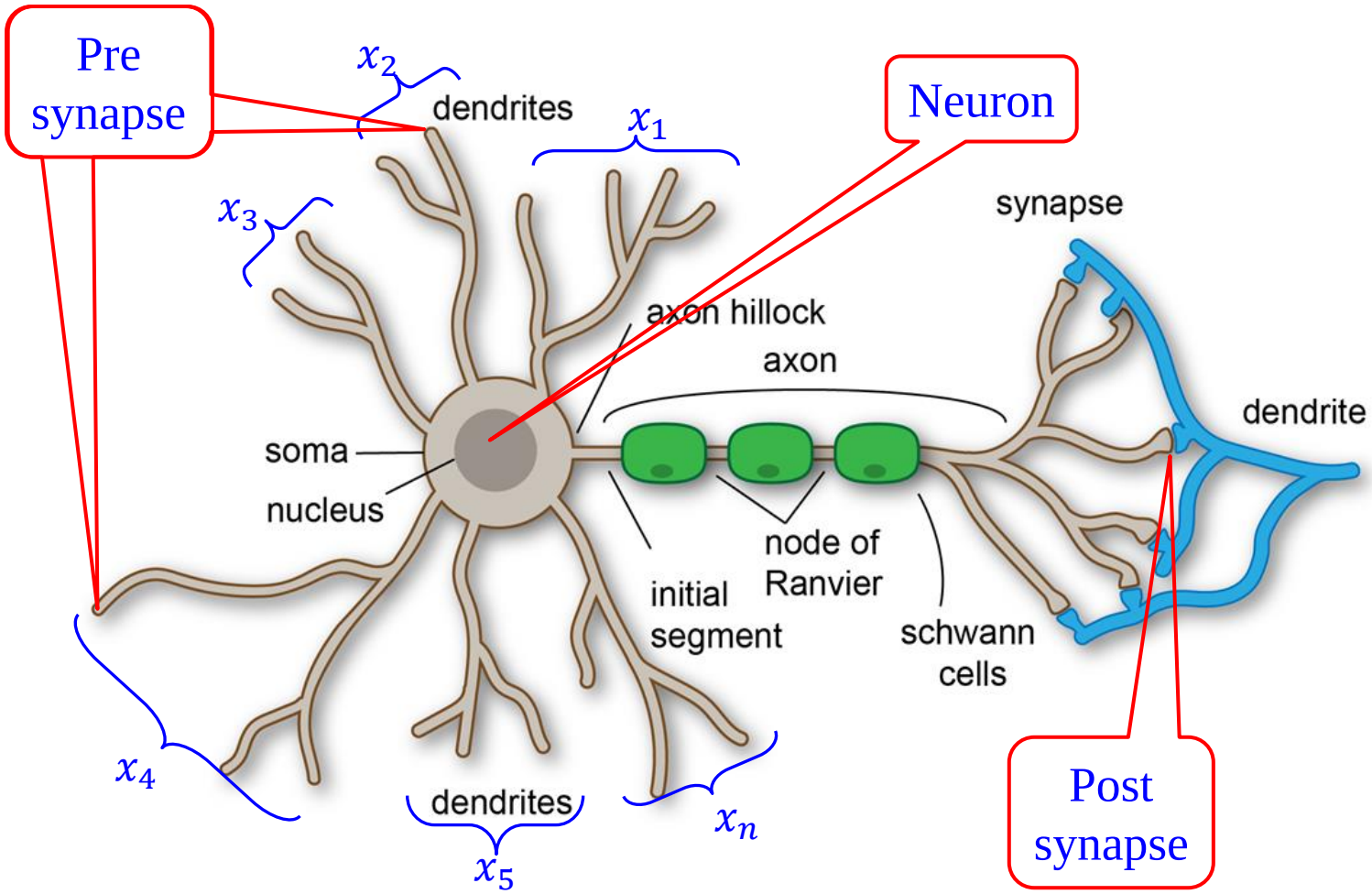
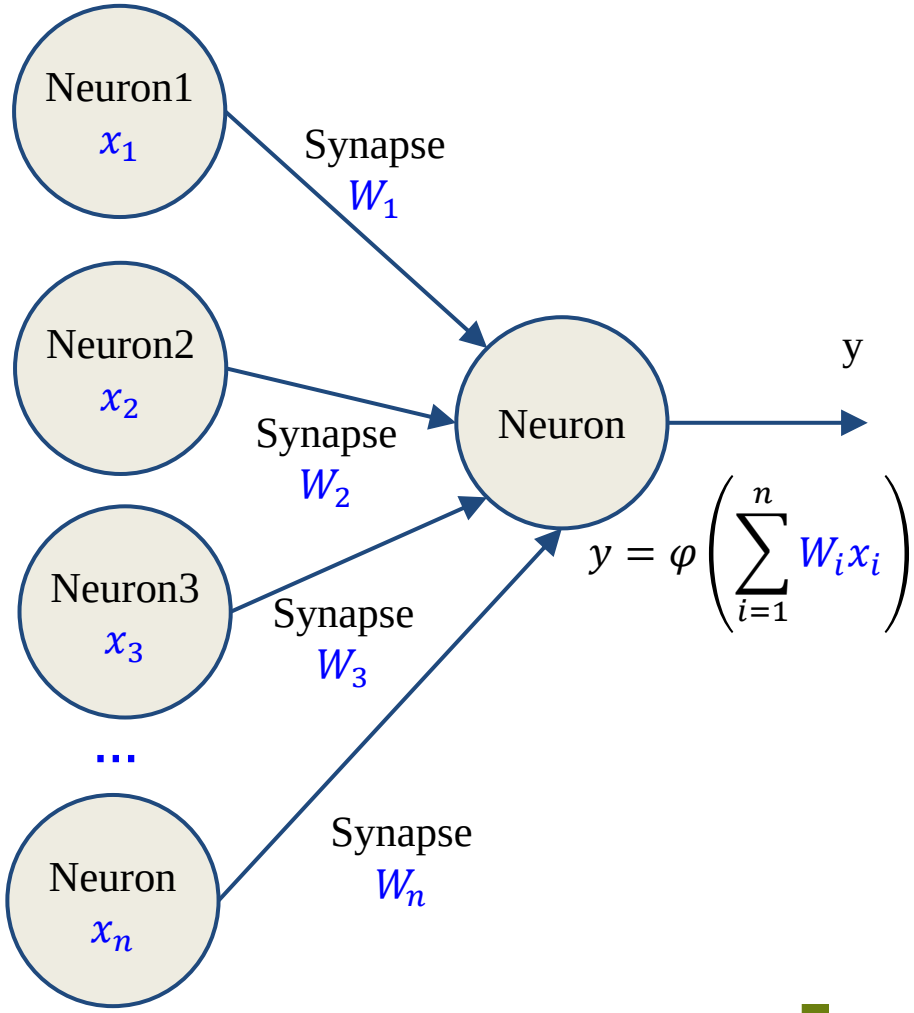
# Neuromorphic Contextual Tasks

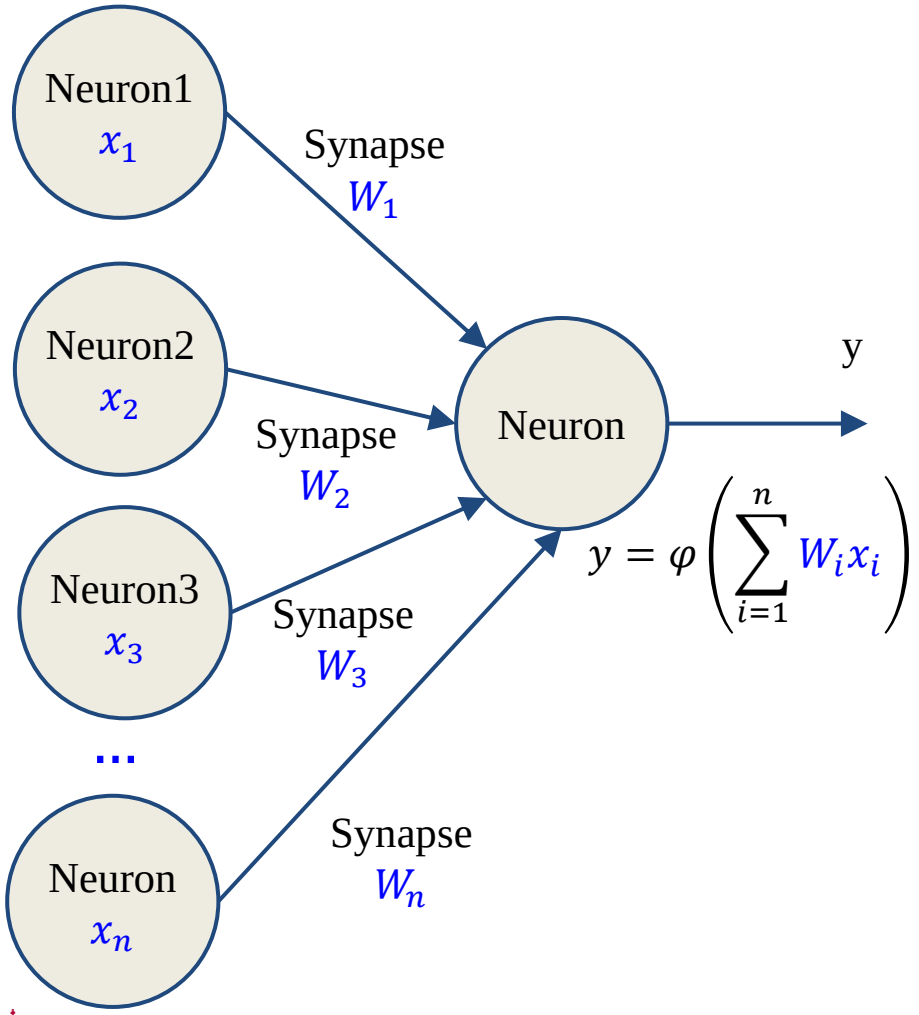
# Biological Neurons and Synapses




https://en.wikipedia.org/wiki/Dendrite

# Artificial Neuron and Synapse




- $\sum_{i=1}^{n} W_i x_i$: linear summation function
- $\varphi()$: activation function
  - Binary Step Function:

$$\varphi(x) = \begin{cases} 0 \; when \; < 0 \\ 1 \; when \; \geq 0 \end{cases}$$

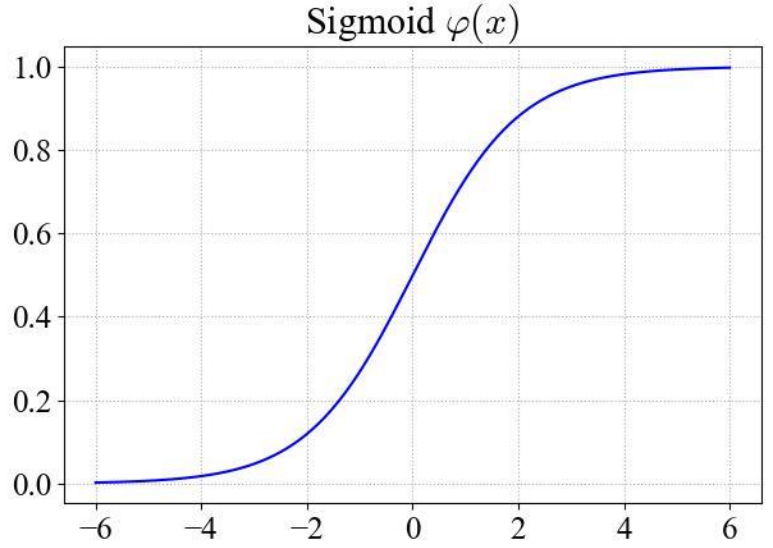
  - Linear Function:

$$\varphi(x) = x$$

# Sigmoid Activation Function

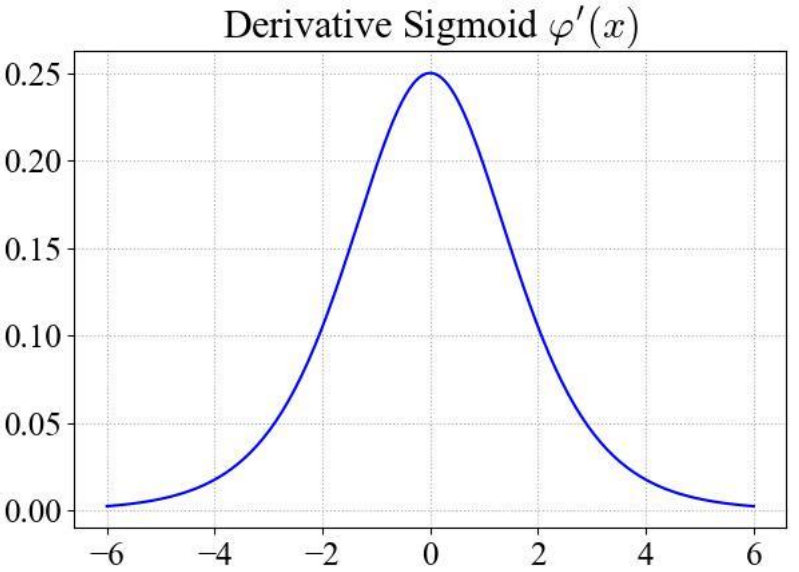
- Sigmoid (Logistic) Function:

$$\varphi(x) = \frac{1}{1 + e^{-x}}$$




- Derivative of sigmoid function:

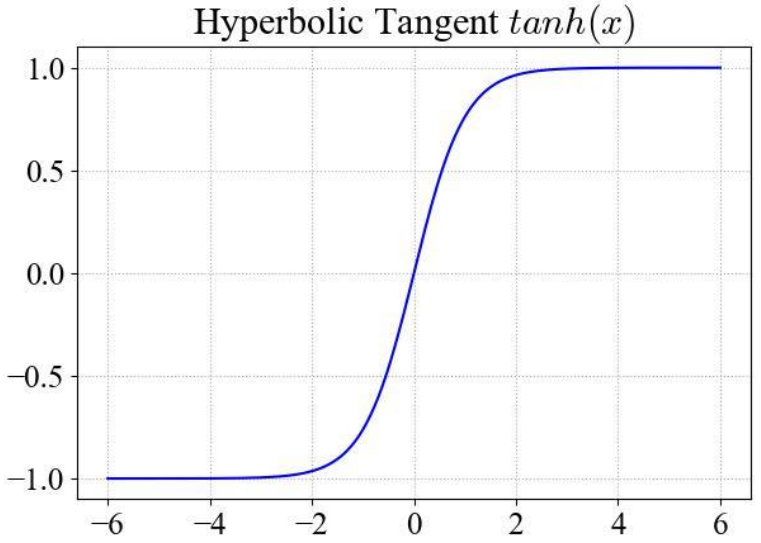
$$\varphi'(x) = \left(\frac{1}{1 + e^{-x}}\right)\left(1 - \frac{1}{1 + e^{-x}}\right)$$



# Hyperbolic Tangent Activation Function

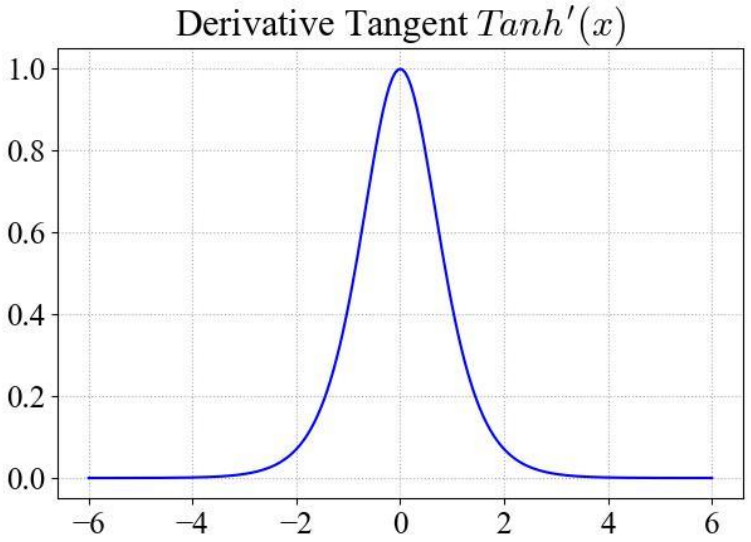
- Hyperbolic Tangent Function:

$$\varphi(x) = \tanh(x)$$




- Derivative of Hyperbolic Tangent Function :

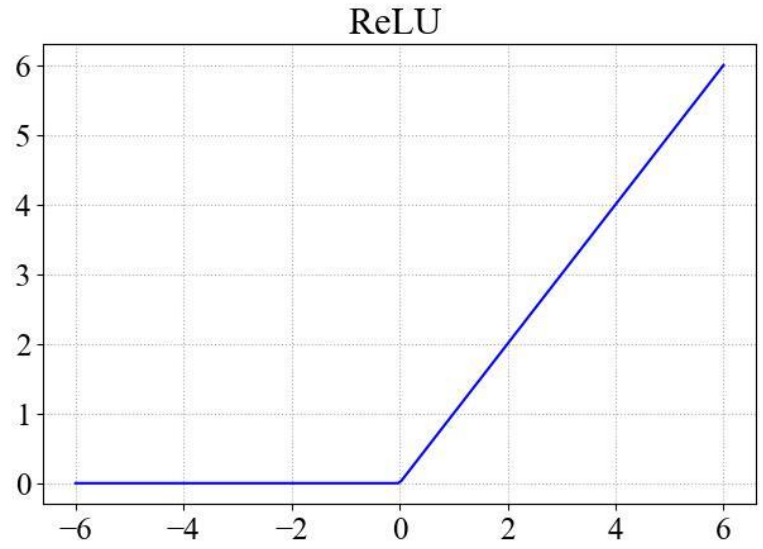
$$\varphi'(x) = 1 - tanh^2(x)$$



# Rectified Linear Unit Function

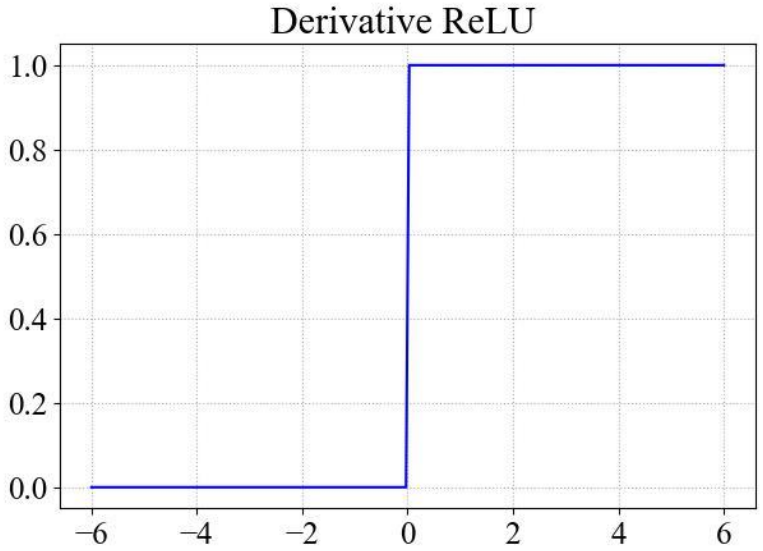
- Rectified Linear Unit (ReLU) Function:

$$\varphi(x) = \begin{cases} 0 \; when \; x < 0 \\ x \;\; when \;\; \geq 0 \end{cases}$$




- Derivative of Rectified Linear Unit :

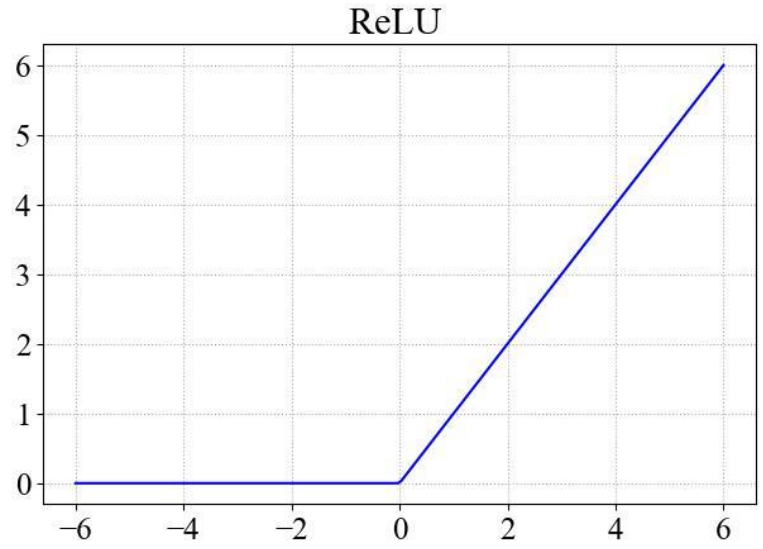
$$\varphi'(x) = \begin{cases} 0 \; when \; x < 0 \\ 1 \;\; when \;\; \geq 0 \end{cases}$$



# Softmax Function

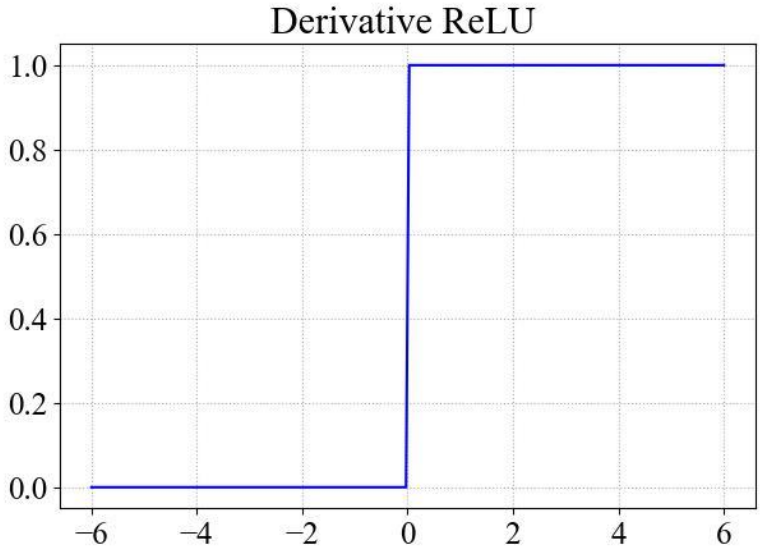
- Rectified Linear Unit (ReLU) Function:

$$\varphi(x) = \begin{cases} 0 \; when \; x < 0 \\ x \;\; when \;\; \geq 0 \end{cases}$$

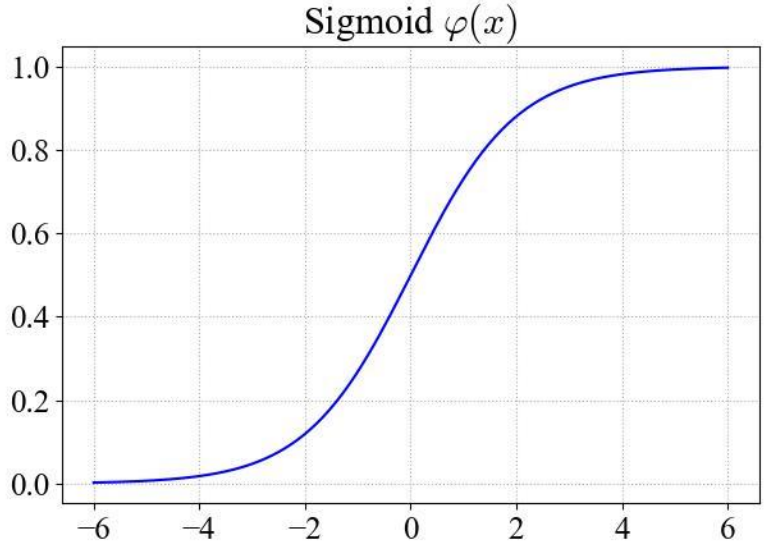



- Derivative of Rectified Linear Unit :

$$\varphi'(x) = \begin{cases} 0 \; when \; x < 0 \\ 1 \;\; when \;\; \geq 0 \end{cases}$$



# Softmax Function




- Sigmoid (Logistic) Function:

$$\varphi(x) = \frac{1}{1 + e^{-x}}$$

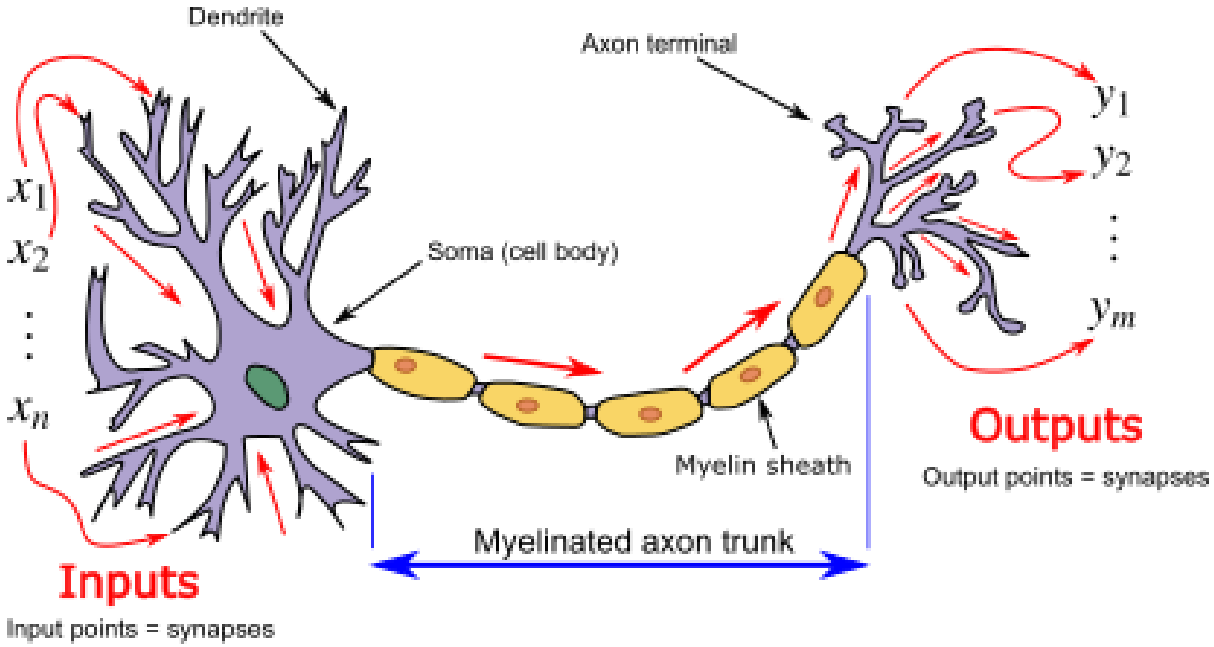
- Softmax Function (Probability Output):

$$\text{SoftMax}(Z_i) = \frac{e^{Z_i}}{\sum_1^n e^{Z_j}}$$

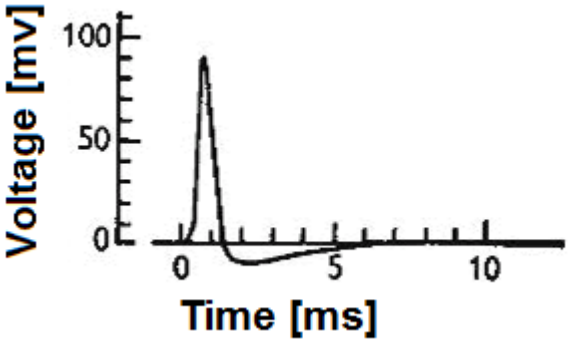
where $Z_i$ is the output of a neuron $i$ and $n$ is the number of classes.

# Biological Spiking Neuron Models

- Information is encoded as a short electrical pulse, or "spike," that travels from inputs at dendrites to outputs at axon terminals.
- A spike is a result of how the membrane potential (the difference in electric potential between the interior and the exterior of a biological cell) across the cell membrane changes over time.
- Information is encoded in both the amplitude and timing of a spike.




https://en.wikipedia.org/wiki/Biological_neuron_model



# Spiking Neuron Model

1. Hodgkin–Huxley:
   - A model of the relationship between ionic currents flow across the neuronal cell membrane and the cell's membrane voltage (HODGKIN AL, HUXLEY AF. A quantitative description of membrane current and its application to conduction and excitation in nerve. J Physiol. 1952 Aug;117(4):500-44. doi: 10.1113/jphysiol.1952.sp004764. PMID: 12991237; PMCID: PMC1392413).
2. Perfect Integrate-and-fire:
   - It is an integrate-and-fire model developed by Louis Lapicque (Abbott, Larry F. "Lapicque's introduction of the integrate-and-fire model neuron (1907)." *Brain research bulletin* 50.5-6 (1999): 303-304).
3. Leaky integrate-and-fire:
   - The leaky integrate-and-fire model was also developed by Louis Lapicque (Abbott, Larry F. "Lapicque's introduction of the integrate-and-fire model neuron (1907)." *Brain research bulletin* 50.5-6 (1999): 303-304).
4. Others

# Spike-timing-dependent plasticity (STDP)

1. A biological process adjusts connection strengths (synapses) between neurons.
2. The adjustment of connection strengths (synapses) depends on the relative timing of a particular neuron's output and input action potentials (or spikes).
3. Under the STDP process:
   - If an input spike to a neuron tends, on average, to occur immediately before that neuron's output spike, then that particular input is made somewhat stronger.
   - If an input spike tends, on average, to occur immediately after an output spike, then that particular input is made somewhat weaker → "spike-timing-dependent plasticity."
4. Artificial Spiking Neural Networks: synapse weight increases if a presynaptic spike occurs before a post-synaptic spike. Otherwise, synapse weight decreases.