ELECTRONIC PROTECTION FOR EXAM PAPER LEAKAGE

A Main Project Report

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CERTIFICATE

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This is to certify that the project report entitled **"Electronic protection for exam paper leakage"** is a bonafide record of work carried out by **G.Rukesh Babu (14X45A0401), K.Kalyan (13X41A0413), K.Saikiran (14X45A0403), MD.Alfar Hussain (14X45A0407)** under my guidance and supervision in partial fulfillment of the requirements for award of the degree of Bachelor of Technology in Electronics and Communication Engineering of Jawaharlal Nehru Technological University, Kakinada is a bonafide record of the work carried out under my guidance and supervision at **S.R.K.INSTITUTE OF TECHNOLOGY**.

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ABSTRACT

The project describes electronic protection for exam paper leakage which is a highly security system. Examination is the important aspect for the educational system to test the skills of student through online, orally on papers .Question paper comes to the college from university in electronic sealed box which is an embedded system designed with ARM processor. An RFID card will be given to the college authorities and password will send to college before 10minutes of exam. By swiping the RFID card with appropriate password, lock of electronic sealed box is open. If anyone tries to open the electronic sealed box before and after RFID swipe duration, message will be send to university board through GSM which indicates exam paper is leaked.

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CHAPTER 1
INTRODUCTION

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An examination is an assessment intended to measure the knowledge, skills, aptitude, physical fitness or classification in many other topics. A test may be administered orally, on paper, on a computer or in a confined area that requires an examinee to physically perform a set of skills. The history of examination is very wide. The first a nationwide standardized test was implemented in China, which was called the imperial examination. The main purpose of this examination was to select able candidates for different governmental positions. The imperial examination was established in 605 AD. And then after different countries adopted the examination systems.England had adopted this examination system in 1806 to select the applicants for positions in Civil Services.

This examination system was later applied to education and became a worldwide standard. Every year news flashes in newspaper and television during the time of examination that the exam is being postponed/cancelled due to the leakage of question papers. Many times the leakage of question papers will not be known to the universities. In such conditions some students get good ranks by these leaked papers and those students who had worked hard have to compromise with less rank. This factor will have negative effect on the growth of the society. Thus by considering the problems faced by the students and society a system has to be implemented which will help to detect and prevent the leakage of question papers.

The question papers are distributed in sealed boxes. This system is being followed since many years. The disadvantages of this system are it may lead to leakage of question papers at various instances in the journey of box from printing location to examination centers. This happens due to easy tampering of sealed boxes and more human interference. Other method involves the e-copy of the question papers mailed from the university to the colleges prior to examination. The colleges take the printouts of the question paper and then are distributed to the examinees. This method also has many disadvantages. The website may be hacked, server may also breakdown and number of colleges had to take printouts which involves the

threats like power failure, system failure and may lead to leakage or problems in conduction of examination.

To open the box, RFID is needed to be swiped with a valid RFID tag at predefined date and time only. The RFID module will compare with EEPROM data such as RFID address, RTC date and time. If the RFID address is wrong, then processor sends “an authentic user” message to the university through a GSM modem and if anybody tries to open the box before the pre-defined date and time with a valid RFID tag also, then processor sends “overruled” message to the university through GSM modem. The box will be open only when swiped with a valid RFID tag at predefined date and time and processor sends “main box opened” message to the university. Then a password is sent from the university to the college to open the particular sub box which contains the question papers. If the person enters the wrong password, then processor sends “wrong password entered” message to the university through GSM modem. If the person enters the correct password, then sub box is opened with the help of the motorized mechanism. Both the sub box and box will then automatically closed after a delay of 10 minutes and 11 minutes respectively and processor sends “box closed” message to the university through GSM modem. After completion of the exam, the university sends “new password” to exam centre. If the box is not closed along with answer papers within the specified time given by the university, then processor sends “overruled” message to the university through GSM modem. Light sensors are mounted inside a box which detects unauthorized tampering.

CHAPTER 2
BASIC TERMINOLOGY

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BASIC TERMINOLOGY

2.1 EMBEDDED SYSTEMS

An Embedded System is a special-purpose computer system designed to perform one or a few dedicated functions, sometimes with real-time computing constraints. It is usually embedded as part of a complete device including hardware

and mechanical parts. In contrast, a general-purpose computer, such as a personal computer, can do many different tasks depending on programming. Embedded systems have become very important today as they control many of the common devices we use.

Since the embedded system is dedicated to specific tasks, design engineers can optimize it, reducing the size and cost of the product, or increasing the reliability and performance. Some embedded systems are mass-produced, benefiting from economies of scale.

In general, "embedded system" is not an exactly defined term, as many systems have some element of programmability. For example, Handheld computers share some elements with embedded systems, such as the operating systems and microprocessors which power them but are not truly embedded systems, because they allow different applications to be loaded and peripherals to be connected.

2.1.1 Applications of Embedded Systems:

An embedded system typically has a specialized function with programs stored on ROM. Examples of embedded systems are chips that monitor automobile functions, including engine controls, antilock brakes, air bags, active suspension systems, environmental systems, security systems, and entertainment systems. Everything needed for those functions is custom designed into specific chips. No external operating system is required.

It’s easy to picture nearly every electronic device as having an embedded system. For example, refrigerators, washing machines, and even coffee brewers will benefit in some way from embedded systems. A critical feature of an embedded system is its ability to communicate, so embedded systems support Ethernet, Bluetooth (wireless), infrared, or other technologies.

A weather station on top of a building may employ an embedded system that gathers information from external sensors. This information can be pushed or pulled. In the push scenario, the data is automatically sent to devices that have requested it. In the pull scenario, users or network devices access the weather station to read the latest information.

If the weather station is connected to the Internet, it may have its own IP address and, ideally, will provide information to anyone that accesses the IP address. In this sense, the weather station is acting as a mini-Web server. In fact, many embedded systems are basically Web servers on a chip.

2.2 GSM TECHNOLOGY

2.2.1 GSM History:

In 1982, the European Conference of Postal and Telecommunications Administrations (CEPT) created the Group Special Mobile (GSM) to develop a standard for a mobile telephone system that could be used across Europe. In 1987, a memorandum of understanding was signed by 13 countries to develop a common cellular telephone system across Europe. Finally the system created by SINTEF lead by Torleiv Maseng was selected. In 1989, GSM responsibility was transferred to the European Telecommunications Standards Institute (ETSI) and phase I of the GSM specifications were published in 1990. The first GSM network was launched in 1991 by Radiolinja in Finland with joint technical infrastructure maintenance from Ericsson. By the end of 1993, over a million subscribers were using GSM phone networks being operated by 70 carriers across 48 countries.

2.2.2 GSM Frequencies:

GSM networks operate in a number of different frequency ranges (separated into GSM frequency ranges for 2G and UMTS frequency bands for 3G). Most 2G GSM networks operate in the 900 MHz or 1800 MHz bands. Some countries in the Americas (including Canada and the United States) use the 850 MHz and 1900 MHz bands because the 900 and 1800 MHz frequency bands were already allocated. Most 3G GSM networks in Europe operate in the 2100 MHz frequency band. The rarer 400 and 450 MHz frequency bands are assigned in some countries where these frequencies were previously used for first-generation systems.

Fig 2.2.2 Global System for Mobile Communications

GSM-900 uses 890–915 MHz to send information from the mobile station to the base station (uplink) and 935–960 MHz for the other direction (downlink), providing 124 RF channels (channel numbers 1 to 124) spaced at 200 kHz. Duplex spacing of 45 MHz is used. In some countries the GSM-900 band has been extended to cover a larger frequency range. This 'extended GSM', E-GSM, uses 880–915 MHz (uplink) and 925–960 MHz (downlink), adding 50 channels (channel numbers 975 to 1023 and 0) to the original GSM-900 band. Time division multiplexing is used to allow eight full-rate or sixteen half-rate speech channels per radio frequency channel. There are eight radio timeslots (giving eight burst periods) grouped into what is called

a TDMA frame. Half rate channels use alternate frames in the same timeslot. The channel data rate for all 8 channels is 270.833 Kbit/s, and the frame duration is 4.615ms. The transmission powers in the handset are limited to a maximum of 2 watts in GSM850/900 and 1 watt in GSM1800/1900.

2.3 RFID SYSTEM

2.3.1 The Elements of an RFID System:

RFID systems fundamentally consist of four elements:

The RFID tags themselves, the RFID readers, the antennas and choice of radio characteristics, and the computer network (if any) that is used to connect the readers.

Tag:

The tag is the basic building block of RFID. Each tag consists of an antenna and a small silicon chip that contains a radio receiver, a radio modulator for sending a response back to the reader, control logic, some amount of memory, and a power system.

Passive Tag and Active Tag:

The power system can be completely powered by the incoming RF signal, in which case the tag is known as a passive tag. Alternatively, the tag's power system can have a battery, in which case the tag is known as an active tag. The primary advantages of active tags are their reading range and reliability. With the proper antenna on the reader and the tag, a 915MHz tag can be read from a distance of 100 feet or more. Passive tags, on the other hand, can be much smaller and cheaper than active ones because they don't have batteries. Another advantage is their longer shelf life: Whereas an active tag's batteries may last only a few years, a passive tag could in principle be read many decades after the chip was manufactured. Between the active and the passive tags are the semi- passive tags. These tags have a battery, like active tags, but still use the reader's power to transmit a message back to the RFID reader using a technique known as backscatter. These tags thus have the read reliability of an active tag but the read range of a passive tag. They also have a longer shelf life than a tag that is fully active.

Readers:

The RFID reader sends a pulse of radio energy to the tag and listens for the tag's response. The tag detects this energy and sends back a response that contains the tag's serial number and possibly other information as well. In simple RFID systems, the reader's pulse of energy functioned as an on-off switch; in more sophisticated systems, the reader's RF signal can contain commands to the tag, instructions to read or write memory that the tag contains, and even passwords. Historically, RFID readers were designed to read only a particular kind of tag, but so-called multimode readers that can read many different kinds of tags are becoming increasingly popular. Like the tags themselves, RFID readers come in many sizes. The largest readers might consist of a desktop personal computer with a special card and multiple antennas connected to the card through shielded cable. Such a reader would typically have a network connection as well so that it could report tags that it reads to other computers. The smallest readers are the size of a postage stamp and are designed to be embedded in mobile telephones.

Antennas and Radio:

The RFID physical layer consists of the actual radios and antennas used to couple the reader to the tag so that information can be transferred between the two. Radio energy is measured by two fundamental characteristics: the frequencies at which it oscillates and the strength or power of those oscillations. Commercial FM broadcast stations in the United States transmit with energy at a frequency between 88MHz and 108MHz, or 1 million isolations per second. The AM spectrum, by contrast, transmits at 500,000 to 1,500,000 oscillations per second, or between 500 kHz and 1500 kHz. Microwave ovens cook with RF energy that vibrates 2.4 billion times each second, which is 2.4GHz.

Most RFID systems use the so-called unlicensed spectrum, which is a specific part of the spectrum set aside for use without a radio license. Popular bands are the low- frequency (LF) band at 125–134.2KHz, the high-frequency band at 13.56MHz, the ultrahigh-frequency (UHF) band at 915MHz (in North America; varies in other regions), and the industrial, scientific, and medical (ISM) band at 2.4GHz.

Advantages:

Efficiency: RFID tags do not require line-of-sight to be deciphered. They can be read through cardboard, plastic, wood and even the human body. RFID tags can easily track moving objects and send the required information back to the reader. This eliminates human errors, reduces labor and provides quick access to a wealth of information.

Return on Investment (ROI): RFID costs more to implement than a barcode system, but provides a good return on investment in the long run, since RFID is significantly more efficient.

Less Susceptible to Damage: RFID tags are less susceptible to damage. An RFID tag is securely placed within an object or embedded in plastic, enabling the system to be used in a variety of harsh environments, such as areas of high temperature or moisture, or with exposure to chemicals or the outdoors.

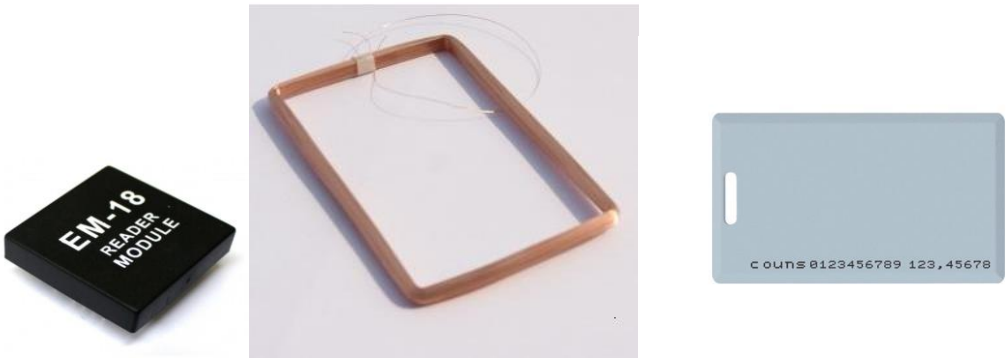

Fig 2.3 RFID System

2.3.2 RFID applications:

1. **Manufacturing and Processing**

a. Inventory and production process monitoring.

b. Warehouse order fulfillment.

2. **Supply Chain Management**

a. Inventory tracking systems.

b. Logistics management.

3. Retail

a. Inventory control and customer insight.

b. Auto checkout with reverse logistics.

4. Security

a. Access control.

b. Counterfeiting and Theft control/prevention.

5. Location Tracking

a. Traffic movement control and parking management.

b. Wildlife/Livestock monitoring and tracking.

2.4 REAL TIME CLOCK (DS1302)

Real-time clock (RTC) counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap-year compensation valid up to 2100.It uses burst mode for reading/writing successive addresses in clock/RAM.

2.4.1Features:

- Setting and retrieving the time, using the burst modes.
- Setting and clearing the Write Protect (WP) flag.
- Setting and clearing the Clock Halt (CH) flag.
- Setting and accessing the 31 bytes of static RAM. Single-byte and multi-byte modes are supported.
- Low-level register access.

CHAPTER 3
BLOCK DIAGRAM

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3.1 Block Diagram

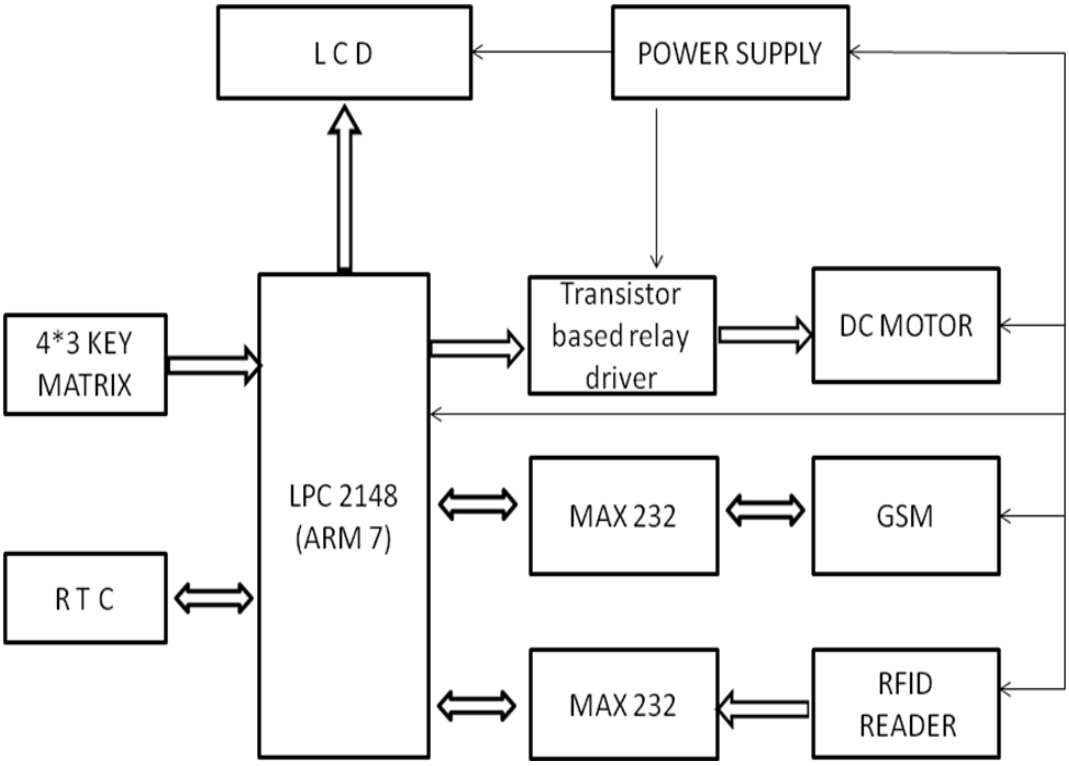

Fig 3.1 Block Diagram of Electronic Protection For Exam Paper Leakage

3.2 Block Diagram Description

The Block Diagram consists of Power supply section, 16X2 LCD Display, 4*3 Matrix, RTC, Microcontroller ARM7, Transistor based relay driver, DC Motor, MAX 232, GSM, RFID Reader.

In the power supply section, the AC power (230-0-230V) from the transformer is converted into 12V dc after passing through full wave rectifier. By switch on the kit, 12v dc is applied to the kit. This 12v is applied to AMS1117 regulator. The output of this regulator is 5V .This 5V is distributed to all devices which are operated with 5V like LPC2148, GSM, RFID, LCD, MAX232 etc.. First of all, LCD is displays "exam paper leakage detection" and then "wait for the time" in RTC. Then we have to set the time in RTC by using s1, s2, s3 switches. If it is time for the exam buzzer on by applying 5V to buzzer from the output of the port0.7 and again LCD displays "enter ur mobile number". Then we have to enter the mobile number through keyboard. By pressing the any number, that particular row and column are activated and send high pulse (5V) to microcontroller. Then the particular microcontroller pin is high and the number is displayed on LCD after that, OTP is generated by the microcontroller as per given logic and send to mobile through GSM. We have to load the password into the microcontroller through keyboard. If it is correct further process is done otherwise lcd displays "invalid otp".If entered otp is correct, lcd displays "show ur valid rfid card". When we placed the rfid tag near the rfid reader, which is operated with13.56mhz frequency in high frequency band. The reader sends a RF signal to the tag. The power system of tag is charged and detected this signal and again sends back the response of tag to rfid. This response contains serial number of card and other related information. The rfid reader will convert this data into digital and send to LPC2148 microcontroller. The microcontroller will compare this number with predefined number of the card. If it is matched, the lock is opened through motor mechanism. The microcontroller output is very low voltage (5v) which is not sufficient to drive the motor. So, 12V transistor based relay is used to run the motor. The output of microcontroller at port0.4 is 5v, which is applied to the base of the transistor, and then the transistor goes into saturation. The output of transistor is 4.5V applied to relay, which is run with 12V. Then the relay is energized and switched ON. Then the motor runs unidirectionaly.Initially, tamper switch is low. If anyone tries to open the box before rfid predefined time. Then the tamper switch becomes high and high pulse (5v) send to microcontroller. Then the buzzer ON. Simultaneously, GSM sends sms to board that "some one tamper ur box please check".

CHAPTER 4
CIRCUIT DIAGRAM

CHAPTER 4

CIRCUIT DIAGRAM

4.1 CIRCUIT DIAGRAM

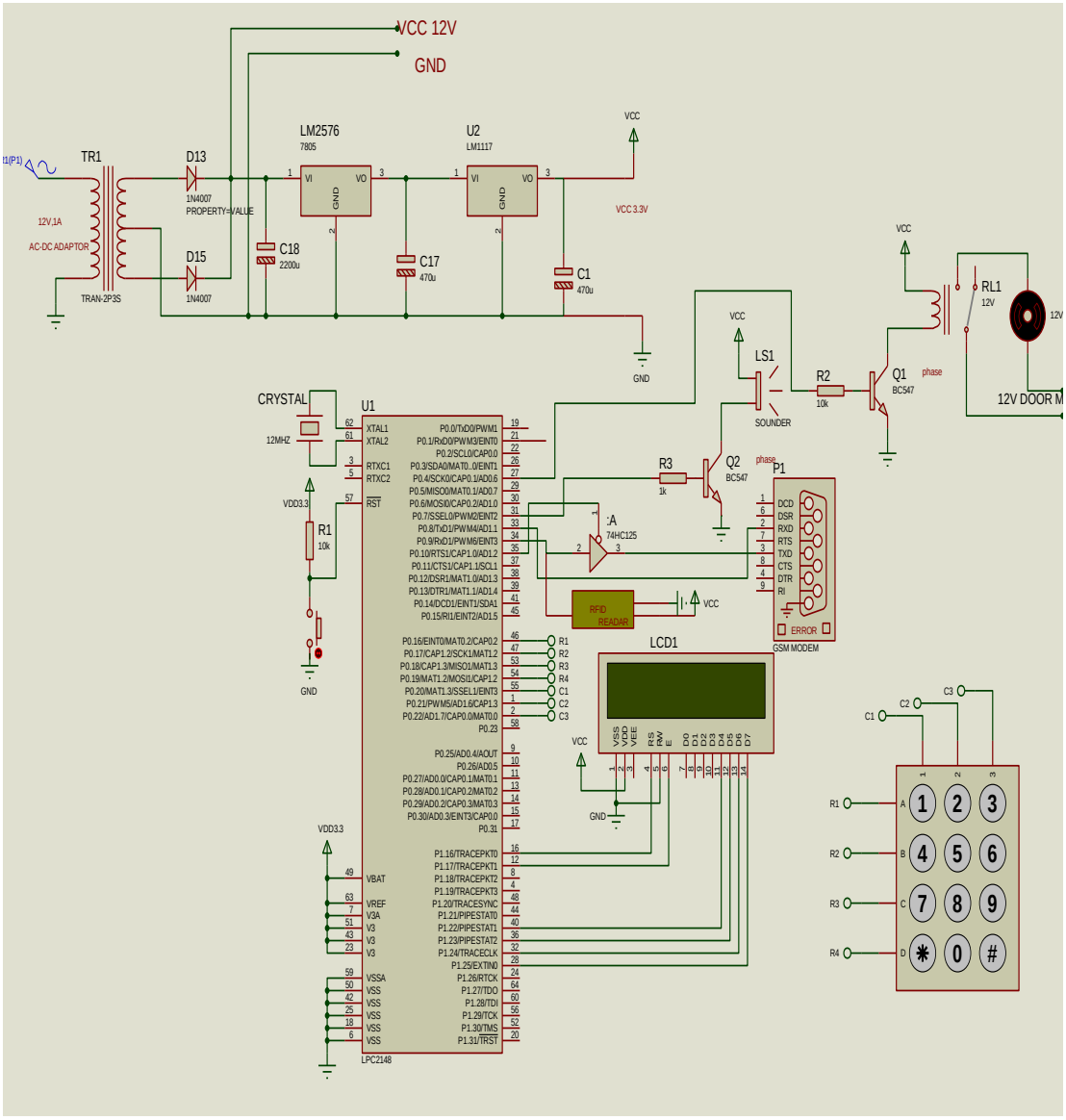

Fig 4.1 Circuit Diagram of Electronic Protection For Exam Paper Leakage

4.2 Components List

ADAPTOR	-	12V, 1A
Diodes D7-D8	-	IN4007
Diode D9	-	LED
IC Regulator	-	LM7805, AMS1117

Resistors:

R1	-	15K
R2, R5, R12	-	2M2
R3	-	270K
R4	-	3K3
R6, R10	-	27K
R7, R11	-	1K5
R8, R9	-	10K
R13	-	2K2

Capacitors:

C1	-	2200uF
C2, C3	-	470uF
C4	-	1000UF/16V

Transistors:

BC547	-	NPN (2)

Micro Controller - ARM7 SeriesLPC2148

- Global System for Mobile communication, Real time clock, RFID Reader & Tag
- 16*2 LCD
- Keyboard
- Buzzer
- 12v Relay
- Tamper switch
- Dc Motor
- 74HC125 Buffer

CHAPTER 5
MICRO-CONTROLLER ARM7 LPC2148

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5.1. General description

The LPC2141/42/44/46/48 microcontrollers are based on a 16-bit/32-bit ARM7TDMI-SCPU with real-time emulation and embedded trace support, that combine microcontroller with embedded high speed flash memory ranging from 32 kB to 512 kB. A 128-bit wide memory interface and unique accelerator architecture enable 32-bit code execution at the maximum clock rate. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty.

Due to their tiny size and low power consumption, LPC2141/42/44/46/48 are ideal for applications where miniaturization is a key requirement, such as access control and point-of-sale. Serial communications interfaces ranging from a USB 2.0 Full-speed device, multiple UARTs, SPI, SSP to I2C-bus and on-chip SRAM of 8 kB up to 40 kB, make these devices very well suited for communication gateways and protocol converters, soft modems, voice recognition and low end imaging, providing both large buffer size and high processing power. Various 32-bit timers, Single or dual 10-bit ADC(s), 10-bit DAC, PWM channels and 45 fast GPIO lines with up to nine edge or level sensitive external interrupt pins make these microcontrollers suitable for industrial control and medical systems.

5.2. Features

5.2.1 Key features:

1) 16-bit/32-bit ARM7TDMI-S microcontroller in a tiny LQFP64 package.

2) 8 kB to 40 kB of on-chip static RAM and 32 kB to 512 kB of on-chip flash memory.128-bit wide interface/accelerator enables high-speed 60MHz operation. In-System Programming/In application Programming (ISP/IAP) via on-chip boot loader software. Single flash sector or full chip erase in 400 ms and programming of 256 bytes in 1ms.

3) Embedded ICE RT and Embedded Trace interfaces offer real-time debugging with the on-chip Real Monitor software and high-speed tracing of instruction execution.

4) USB 2.0 Full-speed compliant device controller with 2 kB of endpoint RAM. In addition, the LPC2146/48 provides 8 kB of on-chip RAM accessible to USB by DMA.

5) One or two (LPC2141/42 vs. LPC2144/46/48) 10-bit ADCs provide a total of 6/14 analog inputs, with conversion times as low as 2.44μs per channel.

6) Single 10-bit DAC provides variable analog output (LPC2142/44/46/48 only).Two 32-bit timers/external event counters (with four capture and four compare channels each), PWM unit (six outputs) and watchdog.

7) Low power Real-Time Clock (RTC) with independent power and 32 kHz clock input.

8) Multiple serial interfaces including two UARTs (16C550), two Fast I2C-bus (400 Kbit/s), SPI and SSP with buffering and variable data length capabilities.

9) Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.

10) Up to 45 of 5 V tolerant fast general purpose I/O pins in a tiny LQFP64 package. Up to 21 external interrupt pins available.

11)60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 μs.

12) On-chip integrated oscillator operates with an external crystal from 1 MHz to 25 MHz.

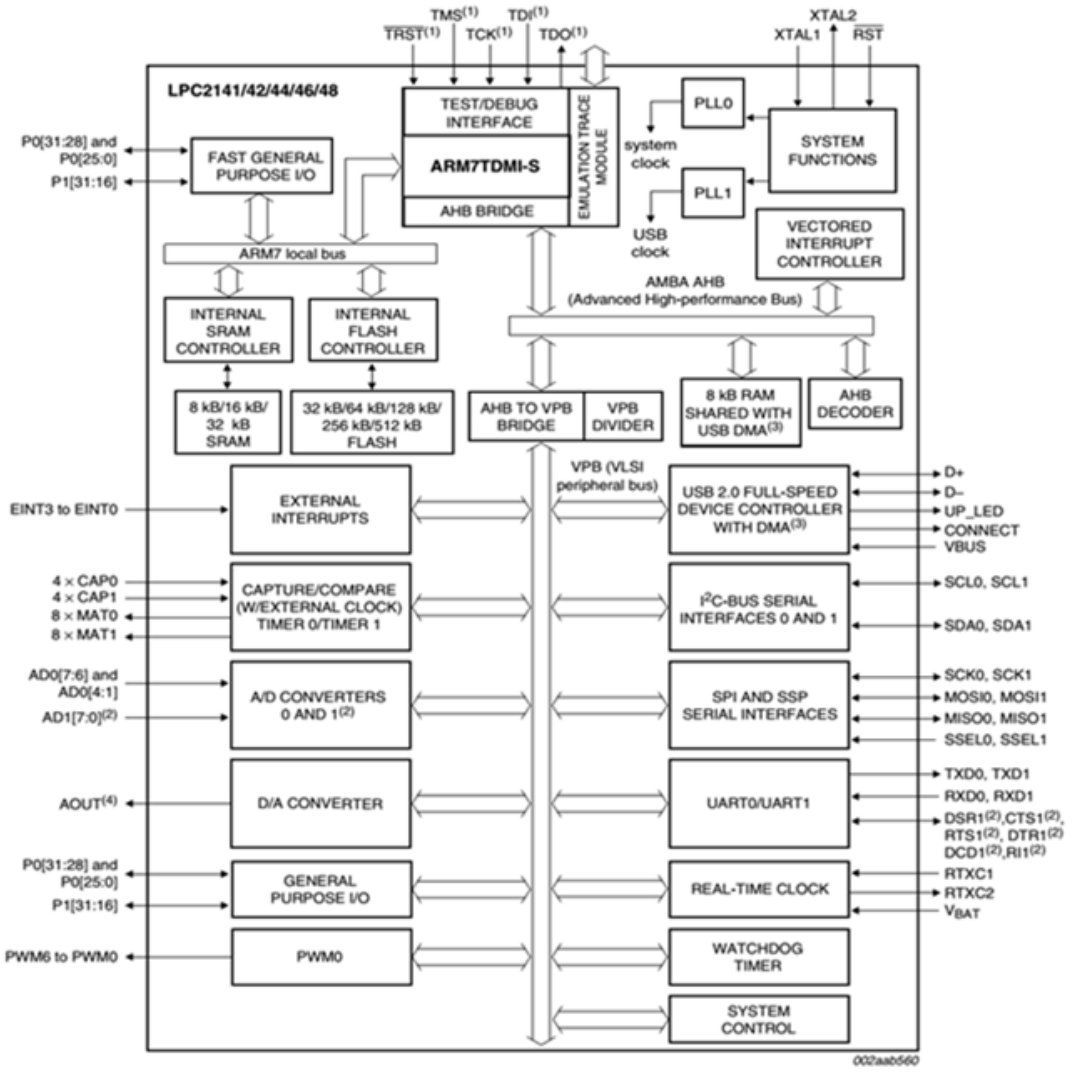
13) Power saving modes include idle and Power-down.

14) Individual enable/disable of peripheral functions as well as peripheral clock scaling for additional power optimization.

15) Processor wake-up from Power-down mode via external interrupt or BOD.

16) Single power supply chip with POR and BOD circuits.

17) CPU operating voltage range of 3.0 V to 3.6 V (3.3 V±10 %) with 5 V tolerant I/O pads.



(1) Pins shared with GPIO.
(2) LPC2144/46/48 only.
(3) USB DMA controller with 8 kB of RAM accessible as general purpose RAM and/or DMA is available in LPC2146/48 only.
(4) LPC2142/44/46/48 only.

Fig 5.2(a) ARM7 LPC2148 Block Diagram

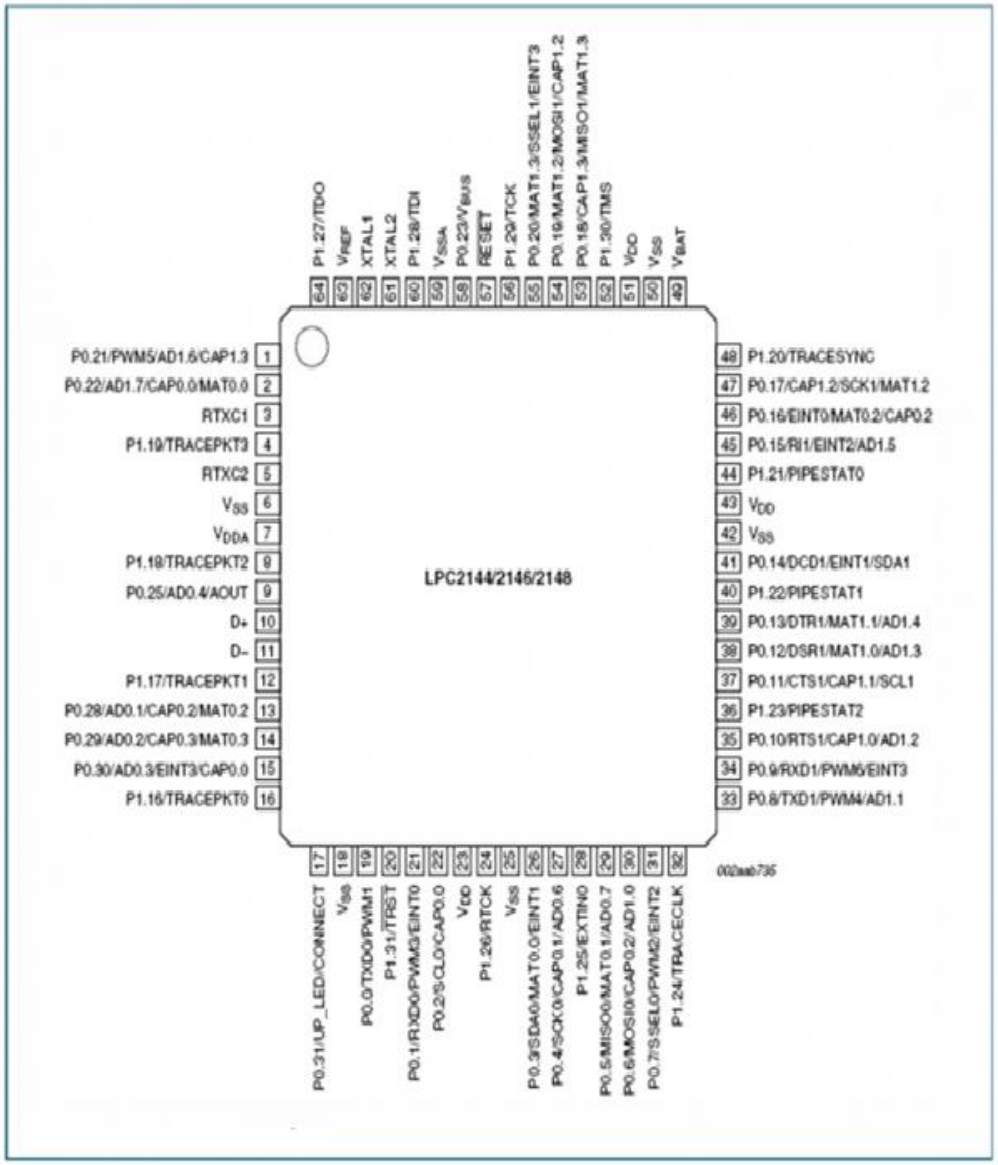


Fig 5.2(b) LPC2148 Pinning

Table 5.2 Pin Description of LPC 2148:

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. Total of 31 pins of the Port 0 can be used as a general purpose bidirectional digital I/Os while P0.31 is output only pin. The operation of port 0 pins depends upon the pin function selected via the pin connect block. Pins P0.24, P0.26 and P0.27 are not available.
P0.0/TXD0/ PWM1	19	I/O	**P0.0 —** General purpose input/output digital pin (GPIO).
		O	**TXD0 —** Transmitter output for UART0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0.1/RXD0/ PWM3/EINT0	21	I/O	**P0.1 —** General purpose input/output digital pin (GPIO).
		I	**RXD0 —** Receiver input for UART0.
		O	**PWM3 —** Pulse Width Modulator output 3.
		I	**EINT0 —** External interrupt 0 input.
P0.2/SCL0/ CAP0.0	22	I/O	**P0.2 —** General purpose input/output digital pin (GPIO).
		I/O	**SCL0 —** I^2C0 clock input/output. Open-drain output
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.3/SDA0/ MAT0.0/EINT1	26	I/O	**P0.3 —** General purpose input/output digital pin (GPIO).
		I/O	**SDA0 —** I^2C0 data input/output. Open-drain output
P0.4/SCK0/ CAP0.1/AD0.6	27	I/O	**P0.4 —** General purpose input/output digital pin (GPIO).
		I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0.1 —** Capture input for Timer 0, channel 1.
		I	**AD0.6 —** ADC 0, input 6.
P0.5/MISO0/ MAT0.1/AD0.7	29	I/O	**P0.5 —** General purpose input/output digital pin (GPIO).
		I/O	**MISO0 —** Master In Slave Out for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0.1 —** Match output for Timer 0, channel 1.
		I	**AD0.7 —** ADC 0, input 7.
P0.6/MOSI0/ CAP0.2/AD1.0	30	I/O	**P0.6 —** General purpose input/output digital pin (GPIO).
		I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
		I	**AD1.0 —** ADC 1, input 0. Available in LPC2144/46/48 only.
P0.7/SSEL0/ PWM2/EINT2	31	I/O	**P0.7 —** General purpose input/output digital pin (GPIO).
		I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
		I	**EINT2 —** External interrupt 2 input.
P0.8/TXD1/ PWM4/AD1.1	33	I/O	**P0.8 —** General purpose input/output digital pin (GPIO).
		O	**TXD1 —** Transmitter output for UART1.
		O	**PWM4 —** Pulse Width Modulator output 4.
		I	**AD1.1 —** ADC 1, input 1. Available in LPC2144/46/48 only.
P0.9/RXD1/ PWM6/EINT3	34	I/O	**P0.9 —** General purpose input/output digital pin (GPIO).
		I	**RXD1 —** Receiver input for UART1.
		O	**PWM6 —** Pulse Width Modulator output 6.
		I	**EINT3 —** External interrupt 3 input.
P0.10/RTS1/ CAP1.0/AD1.2	35	I/O	**P0.10 —** General purpose input/output digital pin (GPIO).
		O	**RTS1 —** Request to Send output for UART1. LPC2144/46/48 only.
		I	**CAP1.0 —** Capture input for Timer 1, channel 0.
		I	**AD1.2—**ADC 1, input 2. Available in LPC2144/46/48 Only.

Symbol	Pin	Type	Description
P0.11/CTS1/ CAP1.1/SCL1	37	I/O	**P0.11 —** General purpose input/output digital pin (GPIO).
		I	**CTS1 —** Clear to Send input for UART1.
		I	**CAP1.1 —** Capture input for Timer 1, channel 1.
		I/O	**SCL1 —** I^2C1 clock input/output. Open-drain output)
P0.12/DSR1/ MAT1.0/AD1.3	38	I/O	**P0.12 —** General purpose input/output digital pin (GPIO).
		I	**DSR1 —** Data Set Ready input for UART1.
		O	**MAT1.0 —** Match output for Timer 1, channel 0.
		I	**AD1.3 —** ADC 1 input 3. Available in LPC2144/46/48 only.
P0.13/DTR1/ MAT1.1/AD1.4	39	I/O	**P0.13 —** General purpose input/output digital pin (GPIO).
		O	**DTR1 —** Data Terminal Ready output for UART1.
		O	**MAT1.1 —** Match output for Timer 1, channel 1.
		I	**AD1.4 —** ADC 1 input 4. Available in LPC2144/46/48 only.
P0.14/DCD1/ EINT1/SDA1	41	I/O	**P0.14 —** General purpose input/output digital pin (GPIO).
		I	**DCD1 —** Data Carrier Detect input for UART1. LPC2144/46/48 only.
		I	**EINT1 —** External interrupt 1 input.
I/O **SDA1 —** I^2C1 data input/output. Open-drain output			
P0.15/RI1/ EINT2/AD1.5	45	I/O	**P0.15 —** General purpose input/output digital pin (GPIO).
		I	**RI1 —** Ring Indicator input for UART1.
		I	**EINT2 —** External interrupt 2 input.
		I	**AD1.5 —** ADC 1, input 5. Available in LPC2144/46/48 only.
P0.16/EINT0/ MAT0.2/CAP0.2	46	I/O	**P0.16 —** General purpose input/output digital pin (GPIO).
		I	**EINT0 —** External interrupt 0 input.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.17/CAP1.2/ SCK1/MAT1.2	47	I/O	**P0.17 —** General purpose input/output digital pin (GPIO).
		I	**CAP1.2 —** Capture input for Timer 1, channel 2.
		I/O	**SCK1 —** Serial Clock for SSP.
		O	**MAT1.2 —** Match output for Timer 1, channel 2.
P0.18/CAP1.3/ MISO1/MAT1.3	53	I/O	**P0.18 —** General purpose input/output digital pin (GPIO).
		I	**CAP1.3 —** Capture input for Timer 1, channel 3.
		I/O	**MISO1 —** Master In Slave Out for SSP.
		O	**MAT1.3 —** Match output for Timer 1, channel 3.
P0.19/MAT1.2/ MOSI1/CAP1.2	54	I/O	**P0.19 —** General purpose input/output digital pin (GPIO).
		O	**MAT1.2 —** Match output for Timer 1, channel 2.
		I/O	**MOSI1 —** Master Out Slave In for SSP.
		I	**CAP1.2 —** Capture input for Timer 1, channel 2.
P0.20/MAT1.3/ SSEL1/EINT3	55	I/O	**P0.20 —** General purpose input/output digital pin (GPIO).
		O	**MAT1.3 —** Match output for Timer 1, channel 3.
		I	**SSEL1 —** Slave Select for SSP.
		I	**EINT3 —** External interrupt 3 input.
P0.21/PWM5/ AD1.6/CAP1.3	1	I/O	**P0.21 —** General purpose input/output digital pin (GPIO).
		O	**PWM5 —** Pulse Width Modulator output 5.
		I	**AD1.6 —** ADC 1, input 6. Available in LPC2144/46/48 only.
		I	**CAP1.3 —** Capture input for Timer 1, channel 3.
P0.22/AD1.7/ CAP0.0/MAT0.0	2	I/O	**P0.22 —** General purpose input/output digital pin (GPIO).
		I	**AD1.7 —** ADC 1, input 7. Available in LPC2144/46/48 only.
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
		O	**MAT0.0 —** Match output for Timer 0, channel 0.

Symbol	Pin	Type	Description
P0.23/V_{BUS}	58	I/O	**P0.23 —** General purpose input/output digital pin (GPIO).
		I	**V_{BUS} —** Indicates the presence of USB bus power.
P0.25/AD0.4/ AOUT	9	I/O	**P0.25 —** General purpose input/output digital pin (GPIO).
		I	**AD0.4 —** ADC 0, input 4.
		O	**AOUT —** DAC output. Available in LPC2142/44/46/48 only.
P0.28/AD0.1/ CAP0.2/MAT0.2	13	I/O	**P0.28 —** General purpose input/output digital pin (GPIO).
		I	**AD0.1 —** ADC 0, input 1.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.
P0.29/AD0.2/ CAP0.3/MAT0.3	14	I/O	**P0.29 —** General purpose input/output digital pin (GPIO).
		I	**AD0.2 —** ADC 0, input 2.
		I	**CAP0.3 —** Capture input for Timer 0, channel 3.
		O	**MAT0.3 —** Match output for Timer 0, channel 3.
P0.30/AD0.3/ EINT3/CAP0.0	15	I/O	**P0.30 —** General purpose input/output digital pin (GPIO).
		I	**AD0.3 —** ADC 0, input 3.
		I	**EINT3 —** External interrupt 3 input.
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.31/UP_LED/ CONNECT	17	O	**P0.31 —** General purpose output only digital pin (GPO).
		O	**UP_LED —**It is HIGH when the device is not configured or during global suspend.
		O	**CONNECT —** Signal used to switch an external 1.5 kW resistor under the software control. Used with the Soft Connect USB feature.
P1.0 to P1.31		I/O	**Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit.
P1.16/ TRACEPKT0	16	I/O	**P1.16 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**TRACEPKT0 —** Trace Packet, bit 0.
P1.17/ TRACEPKT1	12	I/O	**P1.17 —** General purpose input/output digital pin (GPIO).
		O	**TRACEPKT1 —** Trace Packet, bit 1.
P1.18/ TRACEPKT2	8	I/O	**P1.18 —** General purpose input/output digital pin (GPIO).
		O	**TRACEPKT2 —** Trace Packet, bit 2.
P1.19/ TRACEPKT3	4	I/O	**P1.19 —** General purpose input/output digital pin (GPIO).
		O	**TRACEPKT3 —** Trace Packet, bit 3.
P1.20/ TRACESYNC	48	I/O	**P1.20 —** General purpose input/output digital pin (GPIO).
		O	**TRACESYNC —** Trace Synchronization.
P1.21/ PIPESTAT0	44	I/O	**P1.21 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**TRACESYNC —** Trace Synchronization.
P1.21/ PIPESTAT0	44	I/O	**P1.21 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**PIPESTAT0 —** Pipeline Status, bit 0.
P1.22/ PIPESTAT1	40	I/O	**P1.22 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**PIPESTAT1 —** Pipeline Status, bit 1.
P1.23/ PIPESTAT2	36[6]	I/O	**P1.23 —** General purpose input/output digital pin (GPIO).

		O	**PIPESTAT2 —** Pipeline Status, bit 2.
P1.24/ TRACECLK	32[6]	I/O	**P1.24 —** General purpose input/output digital pin (GPIO).
		O	**TRACECLK —** Trace Clock.
P1.25/EXTIN0	28	I/O	**P1.25 —** General purpose input/output digital pin (GPIO).
		I	**EXTIN0 —** External Trigger Input.
P1.26/RTCK	24	I/O	**P1.26 —** General purpose input/output digital pin (GPIO).
I/O **RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up.			
P1.27/TDO	64	I/O	**P1.27 —** General purpose input/output digital pin (GPIO).
		O	**TDO —** Test Data out for JTAG interface.
P1.28/TDI	60	I/O	**P1.28 —** General purpose input/output digital pin (GPIO).
		I	**TDI —** Test Data in for JTAG interface.
P1.29/TCK	56	I/O	**P1.29 —** General purpose input/output digital pin (GPIO).
		I	**TCK —** Test Clock for JTAG interface. This clock must be slower than $^{1}?_{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
P1.30/TMS	52	I/O	**P1.30 —** General purpose input/output digital pin (GPIO).
		I	**TMS —** Test Mode Select for JTAG interface.
P1.31/TRST (GPIO).	20	I/O	**P1.31 —** General purpose input/output digital pin
		I	**TRST —** Test Reset for JTAG interface.
D+	10	I/O	USB bidirectional D+ line.
D-	11	I/O	USB bidirectional D- line.
RESET	57	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	62	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	61	O	Output from the oscillator amplifier.
RTCX1	3	I	Input to the RTC oscillator circuit.
RTCX2	5	O	Output from the RTC oscillator circuit.
V_{SS}	6, 18, 25, 42, 50	I	**Ground:** 0 V reference.
		I	**Analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
V_{DD} .	23, 43, 51	I	**3.3V power supply:** This is the power supply voltage for the core and I/O p
V_{DDA}	7	I	**Analog 3.3 V power supply:** This should be nominally the same voltage as V_{DD} but should be isolated to minimize noise and error. This voltage is only used to power the on-chip ADC(s) and DAC.
VREF	63	I	**ADC reference voltage:** This should be nominally less than or equal to the V_{DD} voltage but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC(s) and DAC.
VBAT	49	I	**RTC power supply voltage:** 3.3 V on this pin supplies the power to the RTC.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[2] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns.

[3] Open-drain 5 V tolerant digital I/O I^2C-bus 400 kHz specification compatible pad. It requires external pull-up to provide an output functionality.

[4] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns. When configured as an ADC input, digital section of the pad is disabled.

[5] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[6] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistor's value typically ranges from 60 kΩ to 300 kΩ.

[7] Pad is designed in accordance with the Universal Serial Bus (USB) specification, revision 2.0 (Full-speed and Low-speed mode only).

[8] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.

[9] Pad provides special analog functionality.

5.3. FUNCTIONAL DESCRIPTION

5.3.1 Architectural overview:

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of micro programmed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core. Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory. The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue. The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set,
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage

over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code. Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system. The particular flash implementation in the LPC2141/42/44/46/48 allows for full speed execution also in ARM mode. It is recommended to program performance critical and short code sections (such as interrupt service routines and DSP algorithms) in ARM mode. Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system. The particular flash implementation in the LPC2141/42/44/46/48 allows for full speed execution also in ARM mode. It is recommended to program performance critical and short code sections (such as interrupt Service routines and DSP algorithms) in ARM mode. The impact on the overall code size will be minimal but the speed can be increased by 30% over Thumb mode.

5.3.2 On-chip flash program memory:

The LPC2141/42/44/46/48 incorporates a 32 kB, 64 kB, 128 kB, 256 kB and 512 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. Due to the architectural solution chosen for an on-chip boot loader, flash memory available for user's code on LPC2141/42/44/46/48 is 32 kB, 64 kB, 128 kB, 256 kB and 500 kB respectively.

The LPC2141/42/44/46/48 flash memory provides a minimum of 100,000 erase/write cycles and 20 years of data-retention.

5.3.3 On-chip static RAM:

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2141, LPC2142/44 and LPC2146/48 provide 8 kB, 16 kB and 32 kB of static RAM respectively. In case of LPC2146/48 only, an 8 kB SRAM block intended to be utilized mainly by the USB can also be used as a general purpose RAM for data storage and code storage and execution.

5.3.4 Memory map:

The LPC2141/42/44/46/48 memory map incorporates several distinct regions, as shown in Figure 5. In addition, the CPU interrupt vectors may be remapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in below diagram as shown.

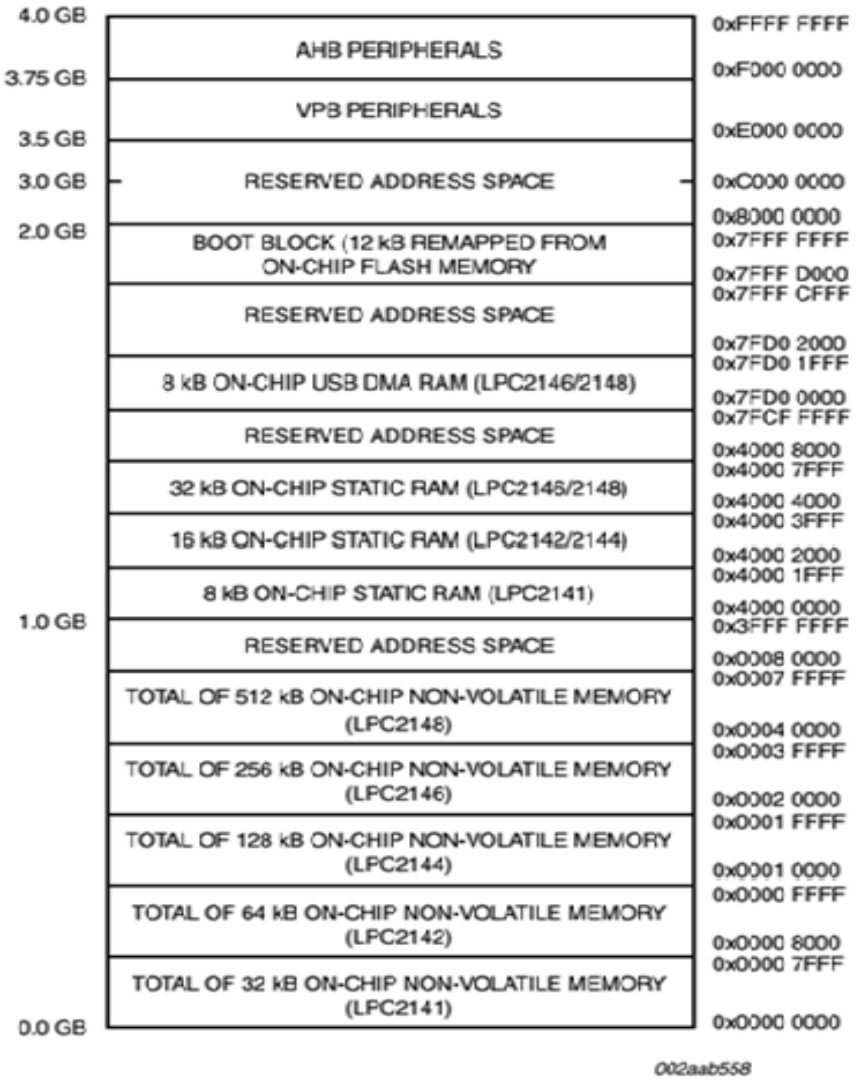


Table 5.3.4 LPC2148 Memory Map

5.4 Interrupt Controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt Request (FIQ), vectored Interrupt Request (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted. Fast interrupt request (FIQ) has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest

possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine does not need to branch into the interrupt service routine but can run from the interrupt vector location. If more than one request is assigned to the FIQ class, the FIQ service routine will read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest. Non-vectored IRQs have the lowest priority. The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are pending, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

5.5 Interrupt Sources

Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

5.6 PIN CONNECT BLOCK

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined. The Pin Control Module with its pin select registers defines the functionality of the microcontroller in a given hardware environment. After reset all pins of Port 0 and 1 are configured as input with the following exceptions: If debug is enabled, the JTAG pins will assume their

JTAG functionality; if trace is enabled, the Trace pins will assume their trace functionality. The pins associated with the I2C0 and I2C1 interface are open drain.

5.7 ADC OPERATIONS

5.7.1 10-BIT ADC:

The LPC2141/42 contains one and the LPC2144/46/48 contains two analog to digital converters. These converters are single 10-bit successive approximation analog to digital converters. While ADC0 has six channels, ADC1 has eight channels. Therefore, total number of available ADC inputs for LPC2141/42 is 6 and for LPC2144/46/48 is 14.

5.7.2 Features:

• 10 bit successive approximation analog to digital converter.

• Measurement range of 0 V to VREF (2.0 V ≤VREF ≤VDDA).

• Each converter capable of performing more than 400,000 10-bit samples per second.

• Every analog input has a dedicated result register to reduce interrupt overhead.

• Burst conversion mode for single or multiple inputs.

• Optional conversion on transition on input pin or timer match signal.

• Global Start command for both converters (LPC2142/44/46/48 only).

5.8 UARTs: [UNIVERSAL ASYNCHRONOUS RECEIVE TRANSMISION]

The LPC2141/42/44/46/48 each contains two UARTs. In addition to standard transmit and receive data lines. The LPC2144/46/48 UART1 also provides a full modem control handshake interface. Compared to previous LPC2000 microcontrollers, UARTs in LPC2141/42/44/46/48 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 with any crystal frequency above 2 MHz In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware (UART1 in LPC2144/46/48 only).

5.8.1 Features:

• 16 byte Receive and Transmit FIFO.

• Register locations conform to 550 industry standard.

• Receiver FIFO triggers points at 1, 4, 8, and 14 bytes

• Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.

• Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.

• LPC2144/46/48 UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

5.9 GENERAL PURPOSE TIMERS/EXTERNAL EVENT COUNTERS

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signals transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with ‘or’ and ‘and’, as well as ‘broadcast’ functions among them. The LPC2141/42/44/46/48 can count external events on one of the capture inputs if the minimum external pulse is equal or longer than a period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs, or used as external interrupts.

5.9.1 Features:

• A 32-bit timer/counter with a programmable 32-bit presaler.

• External event counter or timer operation.

• Four 32-bit capture channels per timer/counter that can take a snapshot of the timer value when an input signals transitions. A capture event may also optionally generate an interrupt.

• Four 32-bit match registers that allow:

– Continuous operation with optional interrupt generation on match.

– Stop timer on match with optional interrupt generation.

– Reset timer on match with optional interrupt generation.

• Four external outputs per timer/counter corresponding to match registers, with the Following capabilities:

- Set LOW on match.
- Set HIGH on match.
- Toggle on match.
- Do nothing on match.

5.10 REAL-TIME CLOCK

The RTC is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

5.10.1Features:

• Measures the passage of time to maintain a calendar and clock.

• Ultra-low power design to support battery powered systems.

• Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.

• Can use either the RTC dedicated 32 kHz oscillator input or clock derived from the external crystal/oscillator input at XTAL1.Programmable reference clock divider allows fine adjustment of the RTC.

• Dedicated power supply pin can be connected to a battery or the main 3.3 V.

5.11 SYSTEM CONTROL

5.11.1 Crystal oscillator:

On-chip integrated oscillator operates with external crystal in range of 1 MHz to 25 MHz .The oscillator output frequency is called foscand the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. foscand CCLK are the same value unless the PLL is running and connected. Refer to Section 6.19.2 “PLL”for additional information.

5.12 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLLs a clock source. The PLL settling time is 100µs.

5.13 RESET AND WAKE-UP TIMER

Reset has two sources on the LPC2141/42/44/46/48: the RESET pin and watch dog reset. The RESET pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values. The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

The Wake-up Timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of VDD ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

5.14 EXTERNAL INTERRUPT INPUTS

The LPC2141/42/44/46/48 include up to nine edge or level sensitive External Interrupt Inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The External Interrupt Inputs can optionally be used to wake-up the processor from Power-down mode. Additionally capture input pins can also be used as external interrupts without the option to wake the device up from Power-down mode.

5.15 Power Supply Unit

In every project we need different voltages for different Circuits. So we need to construct different power supply circuits of different voltages employing different voltage transformers, rectifier circuits, filter circuits and regulator circuits.

This type of construction requires many components (transformers, capacitors, regulators, etc,). So the size of the power supply module becomes bulky and costly. To overcome these disadvantages we use regulator IC's for different voltages [12V, 9V, 5V...] can be obtained with only one transformer.

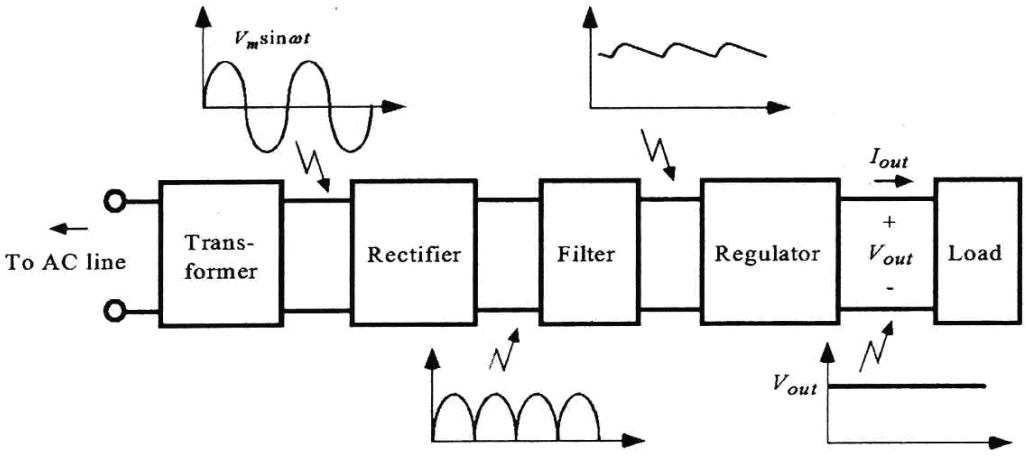


Fig 5.15 Components of a typical linear Power Supply

The circuit diagram of power supply module is as shown in the figure. The function of each component of the circuit is explained below. It consists of following stages.

- Transformers
- Rectifiers
- Filters and
- Regulator

5.15.1 Transformer:

It is an electrical device which transfers the power from one winding with isolation. All the electronic gadgets work for less voltage [normally 3V to 12V]. So an step down transformer is used, whose function is to step down the A.C voltage from 230V to required voltage depending on the need. In our project 12V-0-12V is used the output of the transformer is connected to the diodes for rectification.

5.15.2 Rectifier Circuit:

It employs 2 diodes, which converts A.C voltage into D.C voltage. The output of rectifier circuit is not a pure D.C. It also consists of some A.C components, which is called Ripples. In order to remove these A.C components, filter circuits are employed. So the output of rectifier circuit is fed to the filter circuit [capacitor].

5.15.3 Filter Circuit:

Filter circuit employs electrolytic capacitors in order to remove the A.C the components. As we know the capacitors does not allow the D.C components to pass through it because it offers high reactance to the D.C components and offers less reactance to the A.C components. So all A.C components will be bi-pass through the ground.

5.15.4 Regulator:

Regulator is an electronic circuit, whose function is to keep its output constant, though the input is varied. In this project the three terminal I.C regulators of 7805 is used for providing output D.C voltages. E.g. 7805, the number 78 represents the positive regulator I.C and 05 represents the output voltage i.e. output is 5V.

CHAPTER 6
ICS AND HARDWARE COMPONENTS

CHAPTER 6
ICS AND HARDWARE COMPONENTS

6.1 Regulator (LM7805)

A variable regulated power supply, also called a variable bench power supply, is one where you can continuously adjust the output voltage to your requirements. Varying the output of the power supply is the recommended way to test a project after having double checked parts placement against circuit drawings and the parts placement guide. This type of regulation is ideal for having a simple variable bench power supply. Actually this is quite important because one of the first projects a hobbyist should undertake is the construction of a variable regulated power supply. While a dedicated supply is quite handy e.g. 5V or 12V, it's much handier to a variable supply on hand, especially for testing.

Most digital logic circuits and processors need a 5 volt power supply. To use these parts we need to build a regulated 5 volt source. Usually you start with an unregulated power supply ranging from 9 volts to 24 volts DC. To make a 5 volt power supply, we use a LM7805 voltage regulator IC (Integrated Circuit). The IC is shown below. The LM7805 is simple to use. You simply connect the positive lead of your unregulated DC power supply (anything from 9VDC to 24VDC) to the Input pin, connect the negative lead to the Common pin and then when you turn on the power, you get a 5 volt supply from the Output pin.

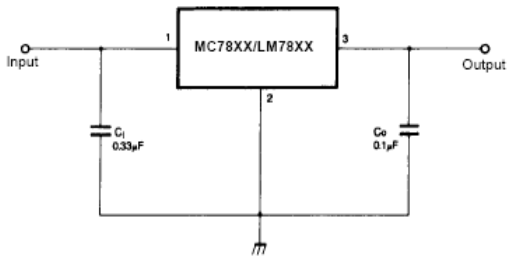


Fig 6.1 (a) Regulator (LM7805) Circuit Diagram

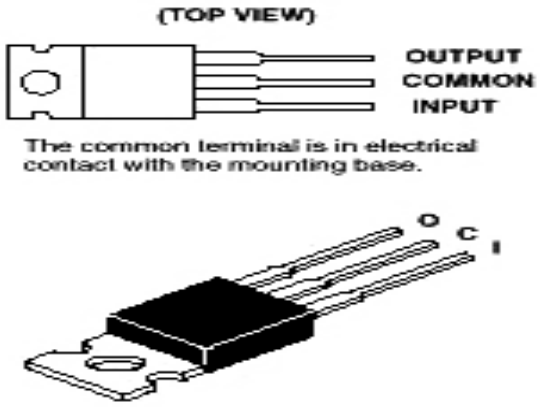


Fig 6.1(b) Regulator (LM7805)

Circuit Features:

Brief description of operation: Gives out well regulated +5V output, output current capability of 100 mA.

Circuit protection: Built-in overheating protection shuts down output when regulator IC gets too hot.

Circuit complexity: Very simple and easy to build.

Circuit performance: Very stable +5V output voltage, reliable operation.

Availability of components: Easy to get, uses only very common basic components.

Design testing: Based on datasheet example circuit, I have used this circuit successfully as part of many electronics projects.

Applications: Part of electronics devices, small laboratory power supply.

Power supply voltage: Unregulated DC 8-18V power supply.

Power supply current: Needed output current + 5 mA.

Component costs: Few dollars for the electronics components + the input transformer cost.

6.2 Resistor

A **resistor** is a two-terminal electronic component designed to oppose an electric current by producing a voltage drop between its terminals in proportion to the current, that is, in accordance with Ohm's law: V = IR

Resistors are used as part of electrical networks and electronic circuits. They are extremely commonplace in most electronic equipment. Practical resistors can be

made of various compounds and films, as well as resistance wire (wire made of a high-resistivity alloy, such as nickel/chrome).

6.3 Capacitor

In October 1745, Ewald Georg von Kleist of Pomerania in Germany found that charge could be stored by connecting a generator by a wire to a volume of water in a hand-held glass jar. The following year, the Dutch physicist Pieter van Musschenbroek invented a similar capacitor, which was named the Leyden jar, after the University of Leyden where he worked.

A capacitor or condenser is a passive electronic component consisting of a pair of conductors separated by a dielectric. When a voltage potential difference exists between the conductors, an electric field is present in the dielectric. This field stores energy and produces a mechanical force between the plates. The effect is greatest between wide, flat, parallel, narrowly separated conductors.

Energy storage i (t) = c dv(t)/dt.

6.4 Diode

When P-type Semiconductor material pieces are joined together, the contact surface is called Pn junction. P-n junction makes a very useful device and also known as a Semiconductor diode as shown in figure.

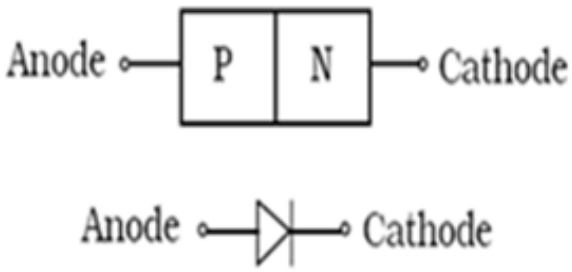


Fig 6.4 Diode

6.4.1 Working:

P-N Junction with No Bias:

P-N junction is just formed as follows. Initially only P-type carriers are sent to the left of junction and only n-type carriers to the right of the junction. As soon as a junction is formed following changes will take place. Holes from P-region diffuse into n-region and Vice-Versa due to this recombination of holes and electrons takes place. A restraining force is setup automatically due to which further diffusion is prevented. It is because now positive charge one-side and negative charge on P-type repels corresponding holes and electrons. The total recombination of holes and electrons cannot take places in entire diode.

P-N Junction with forward Biasing:

When the applied voltage to P-N junction is in such as direction that it reduces the potential burrier and permits the flow of current through device is called forward biasing.

P-N Junction with reverse Biasing:

When the applied voltage to a P-N junction is in such a direction that it increases the potential barrier and prevents the flow of current through device is called reverse biasing.

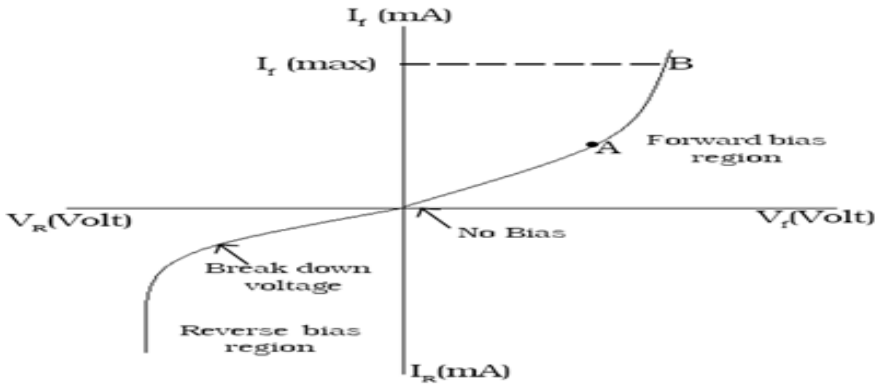


Fig 6.4.1 V-I Characteristics

6.5 Transistor

A Transistor consists of two P-N junctions formed by sandwiching either P-type or n-type semiconductor between a pair of opposite type. There are two types of transistor namely,

(1) N-P-N transistor

(2) P-N-P transistor

1. These are two P-N junctions. Therefore, a transistor may be regarded as a combination of two diodes connected back to back.

2. There are three terminals, taken from each type of Semiconductor

3. The middle section is a very thin layer. This is the most important faction in the function of a transistor.

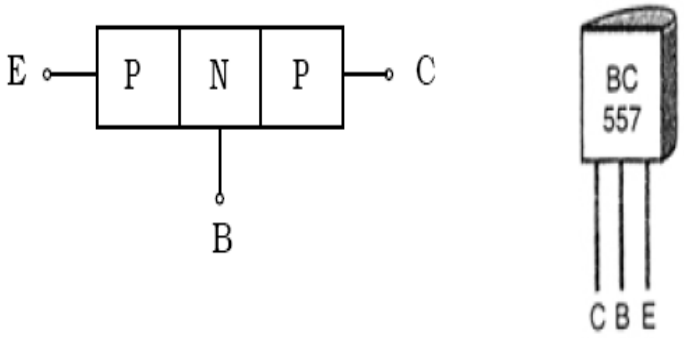


Fig 6.5 Transistor

A transistor has three sections of doped Semiconductors. The section on one side is the 'EMITTER' and the section on the opposite side is the 'COLLECTOR'. The middle section is called the 'BASE' and forms two junctions between the emitter and collector.

Emitter:

The section on one side that supplies charge carriers (electrons or holes) is called the emitter. The emitter is always forward biased with respect to base so that it

can supply a large number of majority carriers. The emitter of P-N-P transistor is forward biased and supplies hole charges to its junction with the base.

Collector:

The section on the other side that collects the charges is called the collector. The collector is always reverse biased. Its function is to remove charges from its junction with the base. The collector of PNP transistor has a reverse bias and receives hole charges that flow in the output Circuit.

Base:

The middle section which forms two P-N junctions between the emitter and collector is called the base. The base-emitter junction is forward biased, allowing low resistance for the emitter circuit. The base-collector junction is reverse biased and provides high resistance in the collector circuit.

6.5.1 Applications:

- Transistors are widely used in electronic circuits.
- These are mainly use to amplifying weak signals.
- It can use as an ON and OFF switch.
- It is used in Oscillator circuits.

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6.6 LED

It is a semiconductor diode having radioactive recombination. It requires a definite amount of energy to generate an electron-hole pair. The same energy is released when an electron recombines with a hole. This released energy may result in the emission of photon and such a recombination. Hear the amount of energy released when the electro reverts from the conduction band to the valence band appears in the form of radiation. Alternatively the released energy may result in a series of photons causing lattice vibration. Finally the released energy may be transferred to another electron. The recombination radiation may be lie in the infra-red and visible light

spectrum. In forward is peaked around the band gap energy and the phenomenon is called injection luminescence. In a junction biased in the avalanche break down region, there results a spectrum of photons carrying much higher energies. Almost White light then gets emitted from micro-plasma breakdown region in silicon junction. Diodes having radioactive recombination are termed as Light Emitting Diode, abbreviated as LEDs.

In gallium arsenide diode, recombination is predominantly a radiation recombination and the probability of this radioactive recombination far exceeds that in either germanium or silicon. Hence GaAs LED has much higher efficiency in terms of Photons emitted per carrier. The internal efficiency of GaAs LED may be very close to 100% but because of high index of refraction, only a small fraction of the internal radiation can usually come out of the device surface. In spite of this low efficiency of actually radiated light, these LEDs are efficiency used as light emitters in visual display units and in optically coupled circuits, the efficiency of light generation increases with the increase of injected current and with decreases in temperature. The light so generated is concentrated near the junction since most of the charge carriers are obtained within one diffusion length of the diode junction. These are the merits of LEDs over conventional incandescent and other types of lamps

- Low Working voltages and currents
- Less power consumption
- Very fast action
- Emission of monochromatic light
- Small size and weight
- No effect of mechanical vibrations
- Extremely long life.

Typical LED uses a forward voltage of about 2V and current of 5 to 10mA.GaAs LED produces infra-red light while red, green and orange lights are produced by gallium arsenide phosphide (GaAsP) and gallium phosphide (GaP).

6.7 PCB Fabrication Details Soldering methods of PCB:

There are basically two soldering methods:

- Manuals soldering with iron
- Mass soldering

Manual soldering with iron:

The surface to be soldered is cleaned and fluxed. The soldering iron is switched on and allowed to attain soldering temperature. The solder in the form of wire is applied near the component to be soldered and heated with iron. The surfaces to be soldered or filled. Iron is removed and the joint is cooled without disturbing.

Cleaning the PCB after soldering:

This method is used when cleaning is required after soldering with flux solder paste. The cleaning process should be done by hand using a soft brush. Simply and gently brush the cleaning agent on the area needing to be cleaned.

6.8 Liquid Crystal Display

A Liquid Crystal Display is a thin, flat display device made up of any number of color or monochrome pixels arrayed in front of a light source or reflector. Each pixel consists of a column of liquid crystal molecules suspended between two transparent electrodes, and two polarizing filters, the axes of polarity of which are perpendicular to each other. Without the liquid crystals between them, light passing through one would be blocked by the other. The liquid crystal twists the polarization of light entering one filter to allow it to pass through the other.

Many microcontroller devices use 'smart LCD' displays to output visual information. LCD displays designed around Hitachi's LCD HD44780 module, are inexpensive, easy to use, and it is even possible to produce a readout using the 8x80 pixels of the display. They have a standard ASCII set of characters and mathematical symbols.

For an 8-bit data bus, the display requires a +5V supply plus 11 I/O lines. For a 4-bit data bus it only requires the supply lines plus seven extra lines. When the LCD display is not enabled, data lines are tri-state and they do not interfere with the operation of the microcontroller.

Data can be placed at any location on the LCD. For 16×2 LCD, the address location are:

First line	**80**	**81**	**82**	**83**	**84**	**85**	**86**	**through**	**8F**
Second line	**C0**	**C1**	**C2**	**C3**	**C4**	**C5**	**C6**	**through**	**CF**

Address locations for a 2x16 line LCD

Signals to the LCD

The LCD also requires 3 control lines from the microcontroller:

1) Enable (E)

This line allows access to the display through R/W and RS lines. When this line is low, the LCD is disabled and ignores signals from R/W and RS. When (E) line is high, the LCD checks the state of the two control lines and responds accordingly.

2) Read/Write (R/W)

This line determines the direction of data between the LCD and microcontroller.When it is low data is written to the LCD. When it is high, data is read from the LCD.

3) Register selects (RS)

With the help of this line, the LCD interprets the type of data on data lines. When it is low, an instruction is being written to the LCD. When it is high, a character is being written to the LCD.

Logic status on control lines:

- E - 0 Access to LCD disabled
  - 1 Access to LCD enabled
- R/W - 0 Writing data to LCD
  - 1 Reading data from LCD
- RS - 0 Instructions
  - 1 Character

Writing and reading the data from the LCD:

Writing data to the LCD is done in several steps:

1) Set R/W bit to low

2) Set RS bit to logic 0 or 1 (instruction or character)

3) Set data to data lines (if it is writing)

4) Set E line to high

5) Set E line to low

Read data from data lines (if it is reading):

1) Set R/W bit to high

2) Set RS bit to logic 0 or 1 (instruction or character)

3) Set data to data lines (if it is writing)

4) Set E line to high

5) Set E line to low

6.8.1 Pin Description:

Most LCDs with 1 controller has 14 Pins and LCDs with 2 controller has 16 Pins(two pins are extra in both for back-light LED connections)

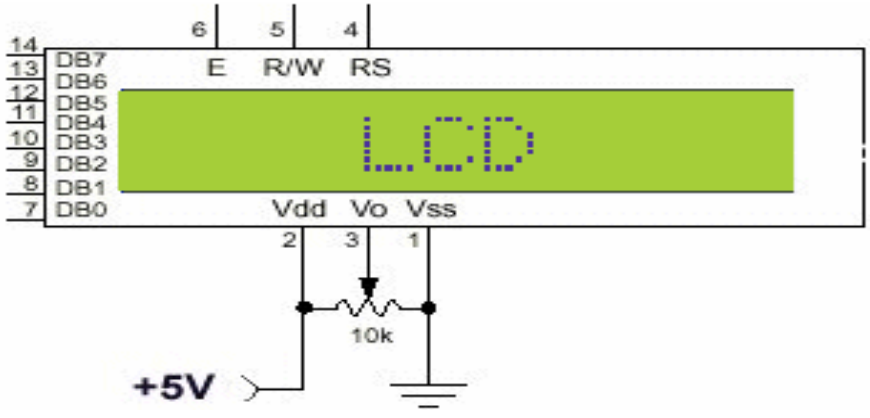


Fig 6.9.1 Pin diagram of 2x16 line LCD

Pin No.	Name	Description
Pin no. 1	**VSS**	Power supply (GND)
Pin no. 2	**VCC**	Power supply (+5V)
Pin no. 3	**VEE**	Contrast adjust
Pin no. 4	**RS**	0 = Instruction input 1 = Data input
Pin no. 5	**R/W**	0 = Write to LCD module 1 = Read from LCD module
Pin no. 6	**EN**	Enable signal
Pin no. 7	**D0**	Data bus line 0 (LSB)
Pin no. 8	**D1**	Data bus line 1
Pin no. 9	**D2**	Data bus line 2
Pin no. 10	**D3**	Data bus line 3
Pin no. 11	**D4**	Data bus line 4
Pin no. 12	**D5**	Data bus line 5
Pin no. 13	**D6**	Data bus line 6
Pin no. 14	**D7**	Data bus line 7 (MSB)

Table 6.8.1 Pin description of the LCD

6.9 MAX232

The MAX232 is an integrated circuit first created in 1987 by Maxim Integrated Products that converts signals from a TIA-232 (RS-232) serial port to signals suitable for use in TTL-compatible digital logic circuits. The MAX232 is a dual transmitter / dual receiver that typically is used to convert the RX, TX, CTS, RTS signals. The drivers provide TIA-232 voltage level outputs (about ±7.5 volts) from a single 5-volt supply by on-chip charge pumps and external capacitors. This makes it useful for implementing TIA-232 in devices that otherwise do not need any other voltages. The receivers reduce TIA-232 inputs, which may be as high as ±25 volts, to standard 5 volt TTL levels. These receivers have a typical threshold of 1.3 volts and a typical hysteresis of 0.5 volts. The MAX232 replaced an older pair of chips MC1488 and MC1489 that performed similar RS-232 translation. The MC1488 quad transmitter chip required 12 volt and -12 volt power, and MC1489 quad receiver chip required 5 volt power. The main disadvantages of this older solution was the +/-

12 volt power requirement, only supported 5 volt digital logic, and two chips instead of one.

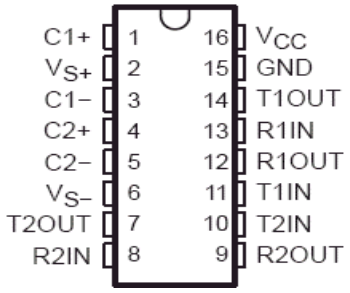
6.9.1 Voltage levels

When a MAX232 IC receives a TTL level to convert, it changes a TTL logic 0 to between +3 and +15 V, and changes TTL logic 1 to between −3 and −15 V, and vice versa for converting from TIA-232 to TTL. This can be confusing when you realize that the TIA-232 data transmission voltages at a certain logic state are opposite from the TIA-232 control line voltages at the same logic state. To clarify the matter, see the table below. For more information, see RS-232 voltage levels

TIA-232 line type and logic level	TIA-232 voltage	TTL voltage to/from MAX232
Data transmission (Rx/Tx) logic0	+3 V to +15 V	0 V
Data transmission (Rx/Tx) logic1	−3 V to −15 V	5V
Control signals (RTS/CTS/DTR/DSR) logic 0	−3 V to −15 V	5 V
Control signals (RTS/CTS/DTR/DSR) logic 1	+3 V to +15 V	0 V

Table 6.9.1Voltage levels of MAX232

6.9.2 MAX 232 pin description



6.9.2 Pin diagram of MAX232

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V

inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC library.

Pin No	Function	Name
1	Capacitor connection pins	Capacitor 1 +
2		Capacitor 3 +
3		Capacitor 1 -
4		Capacitor 2 +
5		Capacitor 2 -
6		Capacitor 3 -
7	Output pin; outputs the serially transmitted data at RS232 logic level; connected to receiver pin of PC serial port	T_2 Out
8	Input pin; receives serially transmitted data at RS 232 logic level; connected to transmitter pin of PC serial port	R_2 In
9	Output pin; outputs the serially transmitted data at TTL logic level; connected to receiver pin of controller.	R_2 Out
10	Input pins; receive the serial data at TTL logic level; connected to serial transmitter pin of controller.	T_2 In
11		T_1 In
12	Output pin; outputs the serially transmitted data at TTL logic level; connected to receiver pin of controller.	R_1 Out
13	Input pin; receives serially transmitted data at RS 232 logic level; connected to transmitter pin of PC serial port	R_1 In
14	Output pin; outputs the serially transmitted data at RS232 logic level; connected to receiver pin of PC serial port	T_1 Out
15	Ground (0V)	Ground
16	Supply voltage; 5V (4.5V – 5.5V)	Vcc

Table 6.9.2 Pin description of MAX232

6.10 Alarm Circuitry

6.10.1 Buzzer:

Buzzer is an audio signaling device, which may be mechanical, electro mechanical or piezoelectric. Typical uses of buzzers and beepers include alarm devices, timers, and confirmation of user input such as a mouse click or keystroke. It is connected to the control unit through the transistor that acts as an electronic switch for it. When the switch forms a closed path to the buzzer, it sounds a warning in the form of a continuous or intermittent buzzing or beeping sound.

6.10.2 Buzzer Driver:

The transistor acts as a normal controlled by the base connection. It switches ON when a positive voltage from the control unit is applied to the base. If the positive voltage is less than 0.6V, the transistor switches OFF. No current flows through the buzzer in this case and it will not buzz. As can be seen in the buzzer circuitry given below, a protection resistor of 10k ohm is used in order to protect the transistor from being damaged in case of excessive current flow. In our system, the buzzer is designed to give a small beep whenever one of the devices such as a cooler or a bulb turns on in order to alert the user.

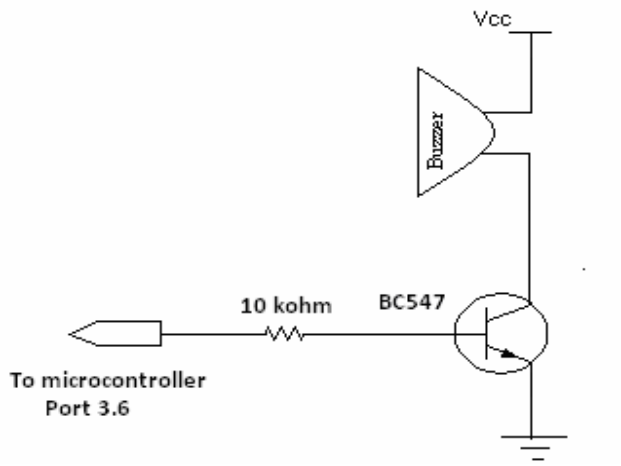


Fig 6.10.1 Buzzer Circuitry

The circuit is designed to control the buzzer. The buzzer ON and OFF is controlled by the pair of switching transistors (BC 547). The buzzer is connected in the Q2 transistor collector terminal. When high pulse signal is given to base of the Q1 transistors, the transistor is conducting and close the collector and emitter terminal so zero signals is given to base of the Q2 transistor. Hence Q2 transistor and buzzer is turned OFF state. When low pulse is given to base of transistor Q1, the transistor is turned OFF. Now 12V is given to base of Q2 transistor so the transistor is conducting and buzzer is energized and produces the sound signal.

6.11 RTC DS1302

The DS1302 Trickle Charge Timekeeping Chip contains a real time clock/calendar and 31 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is

automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24–hour or 12–hour format with an AM/PM indicator.

6.11.1 Operation

The main elements of the Serial Timekeeper are shown in Figure 1: shift register, control logic, oscillator, real time clock, and RAM. To initiate any transfer of data, RST is taken high and 8 bits are loaded into the shift register providing both address and command information. Data is serially input on the rising edge of the SCLK. The first 8 bits specify which of 40 bytes will be accessed, whether a read or write cycle will take place, and whether a byte or burst mode transfer is to occur. After the first eight clock cycles have loaded the command word into the shift register, additional clocks will output data for a reader input data for a write. The number of clock pulses equals 8 plus 8 for byte mode or 8 plus up to 248 for burst mode.

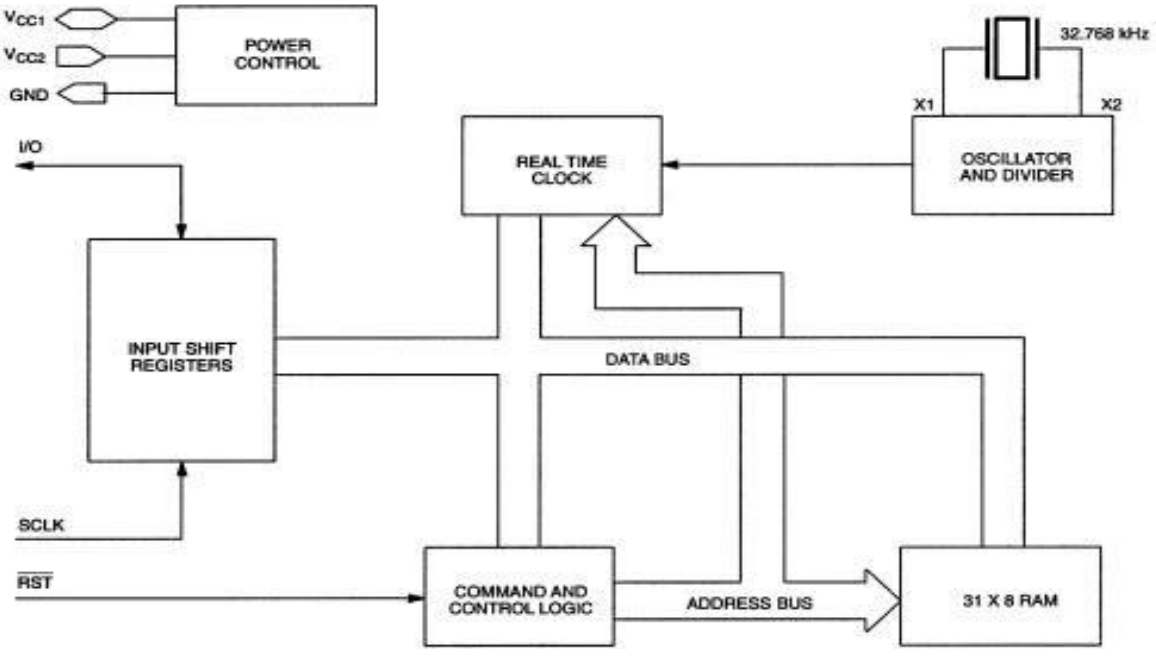


Fig 6.11.1 RTC DS1302 Block Diagram

6.11.2 Signal Descriptions

VCC1 – VCC1 provides low power operation in single supply and battery operated systems as well as low power battery backup. In systems using the trickle charger, the rechargeable energy source is connected to this pin.

VCC2 – Vcc2 is the primary power supply pin in a dual supply configuration. VCC1 is connected to a backup source to maintain the time and date in the absence of primary power. The DS1302 will operate from the larger of VCC1 or VCC2. When VCC2 is greater than VCC1 + 0.2V, VCC2 will power the DS1302. When VCC2 is less than VCC1, VCC1 will power the DS1302.

SCLK (Serial Clock Input) – SCLK is used to synchronize data movement on the serial interface.

I/O (Data Input/output) – The I/O pin is the bi-directional data pin for the 3-wire interface.

RST (Reset) – The reset signal must be asserted high during a read or a write.

X1, X2 – Connections for a standard 32.768 kHz quartz crystal. The internal oscillator is designed for operation with a crystal having a specified load capacitance of 6pF. For more information on crystal selection and crystal layout considerations, please consult Application, "Crystal Considerations with Real Time Clocks." The DS1302 can also be driven by an external 32.768 kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

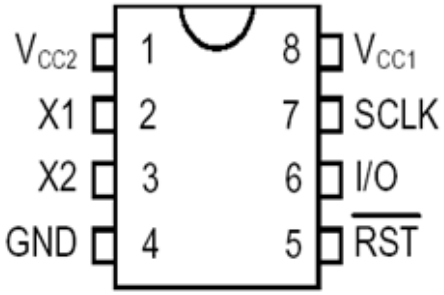


Fig 6.11.2 RTC DS1302 Pin diagram

6.12 Linear DC Motor

A linear motor is an electric motor that has had its stator and rotor "unrolled" so that instead of producing a torque (rotation) it produces a linear force along its length. However, linear motors are not necessarily straight. Characteristically, a linear motor's active section has ends, whereas more conventional motors are arranged as a continuous loop. The most common mode of operation is as a Lorentz-type actuator, in which the applied force is linearly proportional to the current and the magnetic field .

Fig 6.12 Linear DC Motor

6.12.1 Working

In a traditional DC electric motor, a central core of tightly wrapped magnetic material (known as the rotor) spins at high speed between the fixed poles of a magnet (known as the stator) when an electric current is applied. In an AC induction motor, electromagnets positioned around the edge of the motor are used to generate a rotating magnetic field in the central space between them. This "induces" (produces) electric currents in a rotor, causing it to spin. In an electric car, DC or AC motors like these are used to drive gears and wheels and convert rotational motion into motion in a straight line

A linear motor is effectively an AC induction motor that has been cut open and unwrapped. The "stator" is laid out in the form of a track of flat coils made from aluminum or copper and is known as the "primary" of a linear motor. The "rotor" takes the form of a moving platform known as the "secondary." When the current is switched on, the secondary glides past the primary supported and propelled by a magnetic field. Linear motors have a number of advantages over ordinary motors. Most obviously, there are no moving parts to go wrong. As the platform rides

above the track on a cushion of air, there is no loss of energy to friction or vibration (but because the air-gap is greater in a linear motor, more power is required and the efficiency is lower). The lack of an intermediate gearbox to convert rotational motion into straight-line motion saves energy. Finally, as both acceleration and braking are achieved through electromagnetism, linear motors are much quieter than ordinary motors.

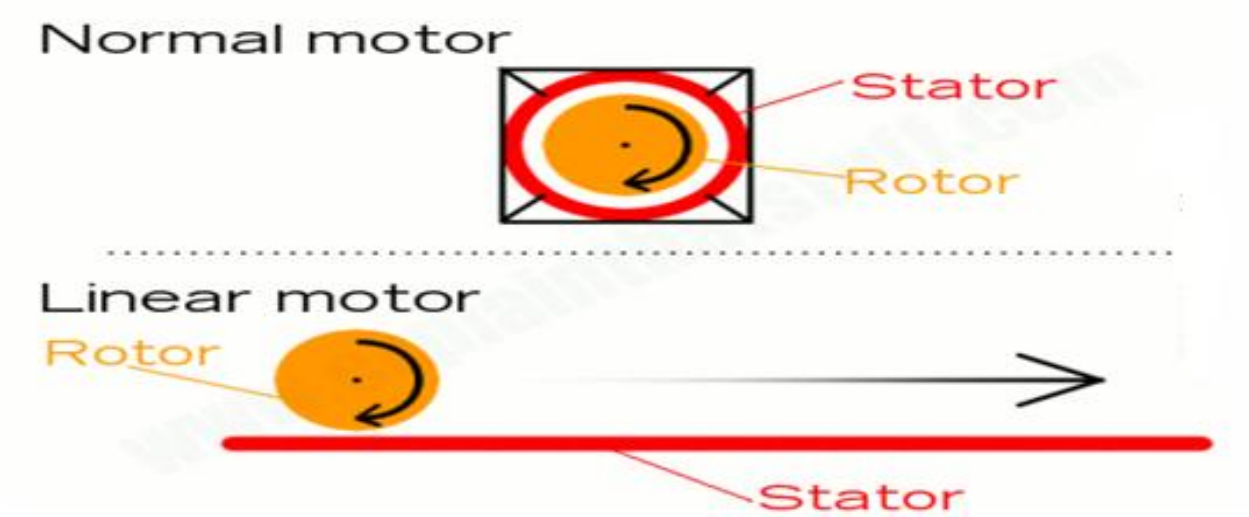


Fig 6.12.1 Linear DC Motor Working

6.12.2 Advantages & Disadvantages

Advantages:

- Highest force available per unit volume
- Efficient Cooling
- Lower cost
- Low Weight
- Small Size

Disadvantages:

- High attractive force between forcer & magnet track.
- Cogging: Iron forcer affects thrust force as it passes over each magnet.

6.13 Transistor based relay driver

A relay is an electrical switch that opens and closes under the control of another electrical circuit. In the original form, the switch is operated by an electromagnet to open or close one or many sets of contacts. It was invented by Joseph Henry in 1835. Because a relay is able to control an output circuit of higher power than the input circuit, it can be considered to be, in a broad sense, a form of an electrical amplifier.

Fig 6.13(a) Sugar cube relay

Despite the speed of technological developments, some products prove so popular that their key parameters and design features remain virtually unchanged for years. One such product is the 'sugar cube' relay, shown in the figure above, which has proved useful to many designers who needed to switch up to 10A, whilst using relatively little PCB area.

Since relays are switches, the terminology applied to switches is also applied to relays. A relay will switch one or more poles, each of whose contacts can be thrown by energizing the coil in one of three ways:

1. Normally - open (NO) contacts connect the circuit when the relay is activate d; the circuit is disconnected when the relay is inactive. It is also called a FORM A contact or "make" contact.

2. Normally - closed (NC) contacts disconnect the circuit when the relay is activated ; the circuit is connected when relay is inactive. It is also called FORM B contact or" break" contact.

3. **Change-over or double-throw** contacts control two circuits; one normally open contact and one normally –closed contact with a common terminal. It is also called a Form C "transfer "contact.

The following types of relays are commonly encountered:

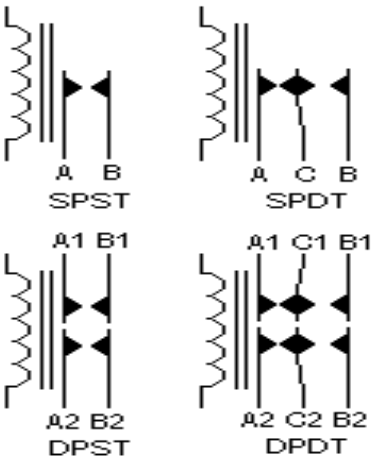


Fig 6.13 (b) SPDT AND DPDT

"C" denotes the common terminal in SPDT and DPDT types

6.13.1 Different types of Relays:

SPST - Single Pole Single Throw: These have two terminals which can be connected or disconnected. Including two for the coil, such a relay has four terminals in total. It is ambiguous whether the pole is normally open or normally closed. The terminology "SPNO" and "SPNC" is sometimes used to resolve the ambiguity.

SPDT - Single Pole Double Throw: A common terminal connects to either of two others. Including two for the coil, such a relay has five terminals in total.

DPST - Double Pole Single Throw: These have two pairs of terminals. Equivalent to two SPST switches or relays actuated by a single coil. Including two for the coil, such a relay has six terminals in total. It is ambiguous whether the poles are normally open, normally closed, or one of each.

DPDT - Double Pole Double Throw: These have two rows of change-over terminals. Equivalent to two SPDT switches or relays actuated by a single coil. Such a relay has eight terminals, including the coil.

QPDT - Quadruple Pole Double Throw: Often referred to as Quad Pole Double Throw, or 4PDT. These have four rows of change-over terminals. Equivalent to four SPDT switches or relays actuated by a single coil or two DPDT relays. In total, fourteen terminals including the coil.

The Relay interfacing circuitry used in the application.

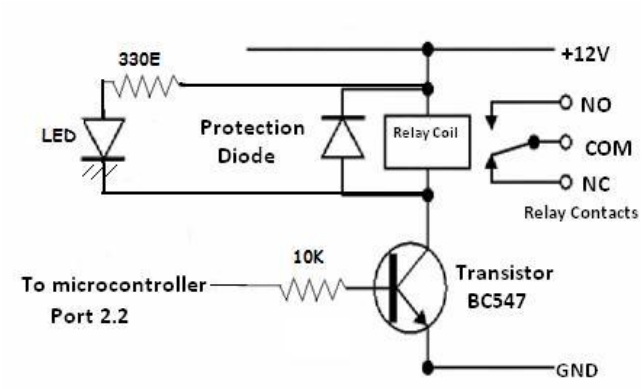


Fig 6.13.1 Relay Circuitry

6.14 Miniature snap-action switch

A miniature snap-action switch, also trademarked and frequently known as a micro switch, is an electric switch that is actuated by very little physical force, through the use of a tipping-point mechanism, sometimes called an "over-center" mechanism.

Fig 6.14 Miniature snap-action switch

In one type of micro switch, internally there are two conductive springs. A long flat spring is hinged at one end of the switch (the left, in the photograph) and has electrical contacts on the other. A small curved spring, preloaded (i.e., compressed during assembly) so it attempts to extend itself (at the top, just right of center in the photo), is connected between the flat spring near the contacts and a fulcrum near the midpoint of the flat spring. An actuator nub presses on the flat spring near its hinge point. Because the flat spring is anchored and strong in tension the curved spring

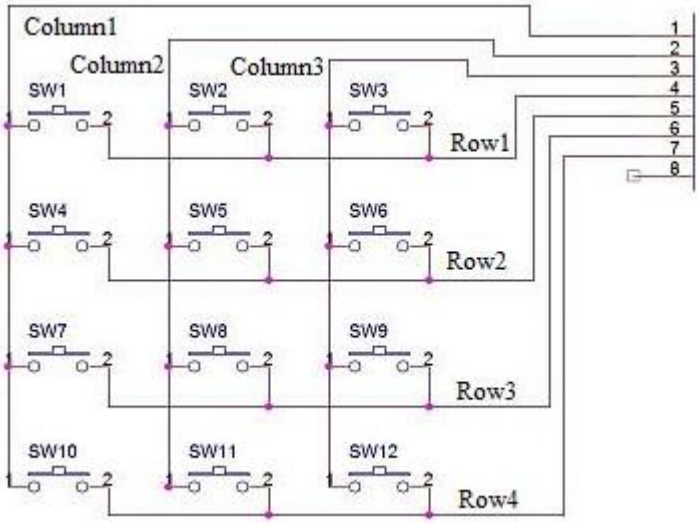
cannot move it to the right. The curved spring presses, or pulls, the flat spring upward, that is away, from the anchor point. Owing to the geometry, the upward force is proportional to the displacement which decreases as the flat spring moves downward. As the actuator depresses it flexes the flat spring while the curved spring keeps the electrical contacts touching. When the flat spring is flexed enough it will provide sufficient force to compress the curved spring and the contacts will begin to move. As the flat spring moves downward the upward force of the curved spring reduces causing the motion to accelerate even in the absence of further motion of the actuator until the flat spring impacts the normally-open contact. Even though the flat spring unflexes as it moves downward, the switch is designed so the net effect is acceleration. This "over-center" action produces a very distinctive clicking sound and a very crisp feel.

In the actuated position the curved spring provides some upward force. If the actuator is released this will move the flat spring upward. As the flat spring moves, the force from the curved spring increases. This results in acceleration until the normally-closed contacts are hit. Just as in the downward direction, the switch is designed so that the curved spring is strong enough to move the contacts, even if the flat spring must flex, because the actuator does not move during the changeover.

6.15 3*4 Key Board

Keypad is a commonly used device to get user′ input. Although simple push switches can be used to get user input, as we have done so, this would require 1 I/O line per switch. Keypads are collection of push switches however′ arranged in the form of a matrix. So there are rows and columns of switches. The two connections of a switch are also connected in the matrix, so that the row has common connection and column has a common connection. Thus when a button is pressed a row and a column, where the button is pressed gets connected internally. The keypads are usually available as telephone type 3 x4keypad. This one has three columns and 4 rows, or a 4 x 4 keypad having 4 rows and 4 columns .The first step is to make the row 1 line low, logical 0. Then to scan all the column lines for a logical 0. If all the column lines are high the no key in this row is being pressed. Let’s say key 2 was being pressed, the column 2 pin of microcontroller would go low and other column pins would remain high. The same process is repeated for row2 and row3 and row4. Every time one row is taken

low and all columns are canned. The key being pressed depends upon the column which gets low, and the row being scanned.

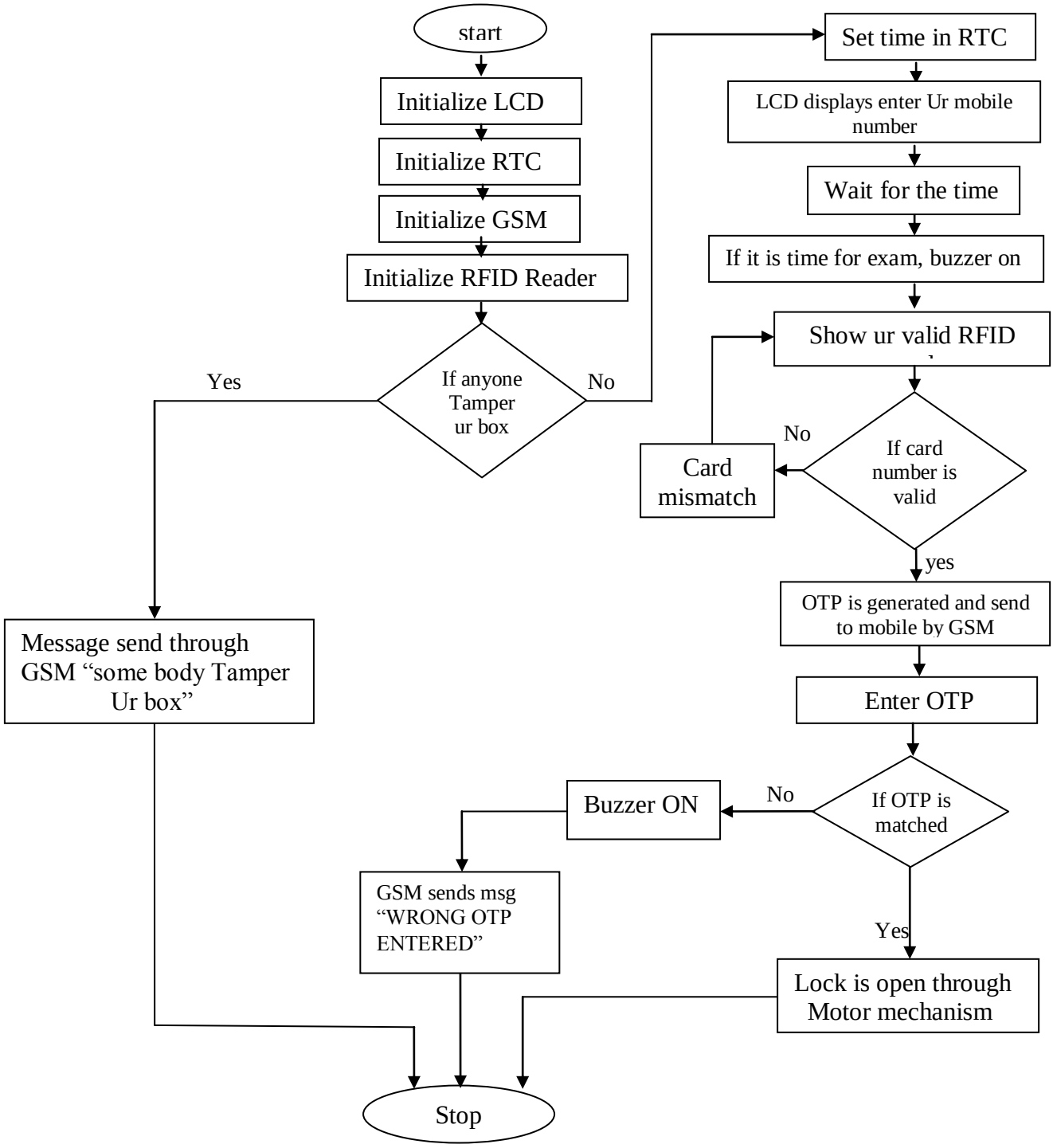


6.15 Internal Structure of 3*4 Keyboard

CHAPTER 7
SOFTWARE

CHAPTER 7
SOFTWARE

7.1Flow Chart



7.2 Project Code:

```
#include <lpc214x.h>

#include<string.h>

#include"gpio.h"

#include"lcd.h"

#include"uart0.h"

#include"uart1.h"

#include"keypad.h"

#include"gsm_uart1.h"

#define in1  P0_4

#define in2  P0_5

//#define tampersw P0_2

//#define timesw P0_3

#definetampersw (0x00000004&IOPIN0)                // P0.6 accident bumbper switch sensor

#definetimesw   (0x00000008&IOPIN0) //inbuilt p0.3 switch

#define rfid P0_10

#define gsm  P0_11

#define buzz P0_7

//unsigned char fp[20],i=0,j=0,id;

unsigned char rec=0x00,chk_sum=0x0f;

char rx_data[13],fail=0;
```

```
unsigned char uc_count=0,newcard=0,id;

void gsm_init(void);

void door_open()

{

 IODIR0|=in1|in2; IOSET0=in1; IOSET0=in2;          delay(1100);  IOCLR0=in1;
IOCLR0=in2;

}

void door_close()

{

 IODIR0|=in1|in2; IOCLR0=in2;  IOCLR0=in1;  delay(1100);  IOCLR0=in1;
IOCLR0=in2;

}

void gsm_enable()

{

 IODIR0|=gsm|rfid;

 IOCLR0=gsm;

 IOSET0=rfid;

}

void rfid_enable()

{

 IODIR0|=gsm|rfid;

 IOCLR0=rfid;
```

```
 IOSET0=gsm;
}
void buzz_on()
{
 IODIR0|=buzz;
 IOSET0=buzz;
}
void buzz_off()
{
 IODIR0|=buzz;
 IOCLR0=buzz;
}
/*void fp_read(void)  __irq
{
 fp[j]=uart0_getch();
 j++;
 VICVectAddr= 0x00000000;
}*/
void UART1_ISR (void)        __irq
{

 while (!(U1LSR & 0x01));                    // Wait RXD Receive Data Ready
```

```
 rx_data[uc_count]=U1RBR;
 uc_count++;
 if(uc_count==12)
 {
  rx_data[11]='\0';
            rx_data[12]='\0';
           rx_data[0]='A';
  lcd_cmd(0x01);
  lcd_puts(rx_data);
  delay(1000);
  uc_count=0;
  newcard=1;
  //U1IER=0x00;
 }
 VICVectAddr          =          0x00000000;      //Dummy write to signal end of
interrupt
}

/*
void uart0_interrupt(void)
{
 VICVectCntl0 =  0x00000026;
```

```
 VICVectAddr0 = (unsigned) fp_read;
 VICIntEnable |=  0x00000040;
 U0IER       =  0x01;
}*/
void uart1_irq_init(void)
{
 VICVectCntl1 = 0x00000027;
 VICVectAddr1 = (unsigned)UART1_ISR;
 VICIntEnable |= 0x00000080;
 U1IER=0x05;
}
/********************** MAIN FUNCTION ***********/
int main()
{
 unsigned  char c_no,mno[11];
 unsigned int ot=1000;
 char pass[5],otp[5];
IO0SET=tampersw;
IO0SET=timesw;
 buzz_off();
door_close();
```

```
lcd_init();  lcd_puts("    EXAM PAPER"); delay(500);

 uart1_init(); uart0_init();

 gsm_enable();buzz_off();

 lcd_cmd(0x01); lcd_puts("Leakage Detectio"); lcd_cmd(0xc0); lcd_puts("
SYSTEM ");delay(2000);

 gsm_check();   gsm_init();      gsm_clear_msg(1);

 lcd_cmd(0x01);           lcd_puts("Enter mobile no:");

 lcd_cmd(0xc0);

 mno [0] =keypad (); buzz_on (); delay (50); buzz_off ();

 lcd_data(mno[0]); delay(400);

 mno [1]=keypad();    buzz_on ();  delay(50); buzz_off();

 lcd_data(mno[1]);   delay (400);

 mno[2]=keypad();    buzz_on();  delay(50); buzz_off();

 lcd_data(mno[2]);       delay(400);

 mno[3]=keypad();  buzz_on();  delay(50); buzz_off();

 lcd_data(mno[3]); delay(400);

 mno[4]=keypad();  buzz_on();  delay(50); buzz_off();

 lcd_data(mno[4]); delay(400);

 mno[5]=keypad();  buzz_on();  delay(50); buzz_off();

 lcd_data(mno[5]); delay(400);

 mno[6]=keypad();  buzz_on();  delay(50); buzz_off();

 lcd_data(mno[6]); delay(400);
```

```
 mno[7]=keypad();  buzz_on();  delay(50); buzz_off();
 lcd_data(mno[7]); delay(400);
 mno[8]=keypad();  buzz_on();  delay(50); buzz_off();
 lcd_data(mno[8]); delay(400);
 mno[9]=keypad();  buzz_on();  delay(50); buzz_off();
 lcd_data(mno[9]); delay(400);
 mno[10]='\0';
 back1:
 lcd_cmd(0x01);
 lcd_cmd(0x80);
 lcd_puts("wait for Time");
 delay(500);
 if(timesw==0)
 {
        goto back;
 }
else if(tampersw)
{
lcd_cmd(0x01);
lcd_cmd(0x80);
lcd_puts("Sending SMS...");
buzz_on();
```

```
U1IER=0x00;
gsm_enable();
gsm_send_num_mesg(mno,"Someone Tampered b0xno 11W10 Please check!");
buzz_off();
goto back1;
}
else
{
goto back1;
}
 back:
 rfid_enable();
 uart1_irq_init();   delay(100);
 lcd_cmd(0x01);         lcd_puts("show ur card");
 U1IER=0x05;  uc_count=0;
 while(1)
 {
  ot++;
  if(ot>=9999)
  ot=1200;
  if(newcard==1)
  {
```

```
 U1IER=0x00;


        if(rx_data[10]=='B')
                {
lcd_cmd(0x01); lcd_puts("UR ID: 00"); delay(1000);
        newcard=0;
        U1IER=0x05;
        c_no=0;
 }
 else
 {
buzz_on();
        lcd_cmd(0x01); lcd_puts("UnAuthorized..."); delay(1000);
        buzz_off();
        newcard=0;
        goto back;
}
 if(c_no==id)
 delay(1);
 else
 {
buzz_on();
```

```
 lcd_cmd(1);  lcd_puts("card miss match");
        delay(2000);
        buzz_off();
        goto back;
 }
 lcd_cmd(0x01);       lcd_puts("Sending OTP...");    delay(1500);
 gsm_enable(); U1IER=0x00;
 otp[0]=ot/1000+48;
 otp[1]=(ot/100)%10+48;
 otp[2]=(ot/10)%10+48;
 otp[3]=ot%10+48;
 otp[4]='\0';
 gsm_send_num_mesg(mno,(unsigned char *)otp);
 delay(2000);
 lcd_cmd(1);  lcd_puts("Enter ur OTP");
 lcd_cmd(0xc0);
pass[0]=keypad();  buzz_on();  delay(50); buzz_off();
 lcd_data(pass[0]); delay(400);
 pass[1]=keypad();  buzz_on();  delay(50); buzz_off();
 lcd_data(pass[1]);  delay(400);
 pass[2]=keypad();  buzz_on();  delay(50); buzz_off();
 lcd_data(pass[2]);  delay(400);
```

```
  pass[3]=keypad();  buzz_on();  delay(50); buzz_off();
  lcd_data(pass[3]); delay(400);
  pass[4]='\0';
  if(!strcmp(otp,pass))
  {
   lcd_cmd(0x01);      lcd_puts("Locker open");
                door_open();
                delay(1000); delay(1000);  delay(1000);
                lcd_cmd(0x01);          lcd_puts("Locker close");
                door_close();
  }
  else
  {
 buzz_on();
        lcd_cmd(0x01); lcd_puts("miss match OTP");
lcd_cmd(0xc0);  lcd_puts("MSG Sending..");
 U1IER=0x00; gsm_enable();
gsm_send_num_mesg(mno,"Wrong OTP Entered ");
        delay(2000);
 buzz_off();
        delay(2000);
  }
```

```
   goto back;
  }}}
/*void gsm_init()
{
 uart1_puts("AT");
 uart1_putch(13);
    uart1_putch(10);
delay(1000);
 uart1_puts("ATE0");
 uart1_putch(13);
    uart1_putch(10);
 delay(1000);
 uart1_puts("AT+CMGF=1");
 uart1_putch(13);
 uart1_putch(10);
delay(1000);
} */
}
```

CHAPTER 8
RESULTS & DISCUSSION

CHAPTER 8

RESULTS AND DISCUSSION

8.1Results

This prototype consists of ARM controller, RFID Reader and RFID Tag, Real Time Clock, DC Motor, Motor Driver, 3*4 Key Matrix and GSM module, Miniature snap-action switch.

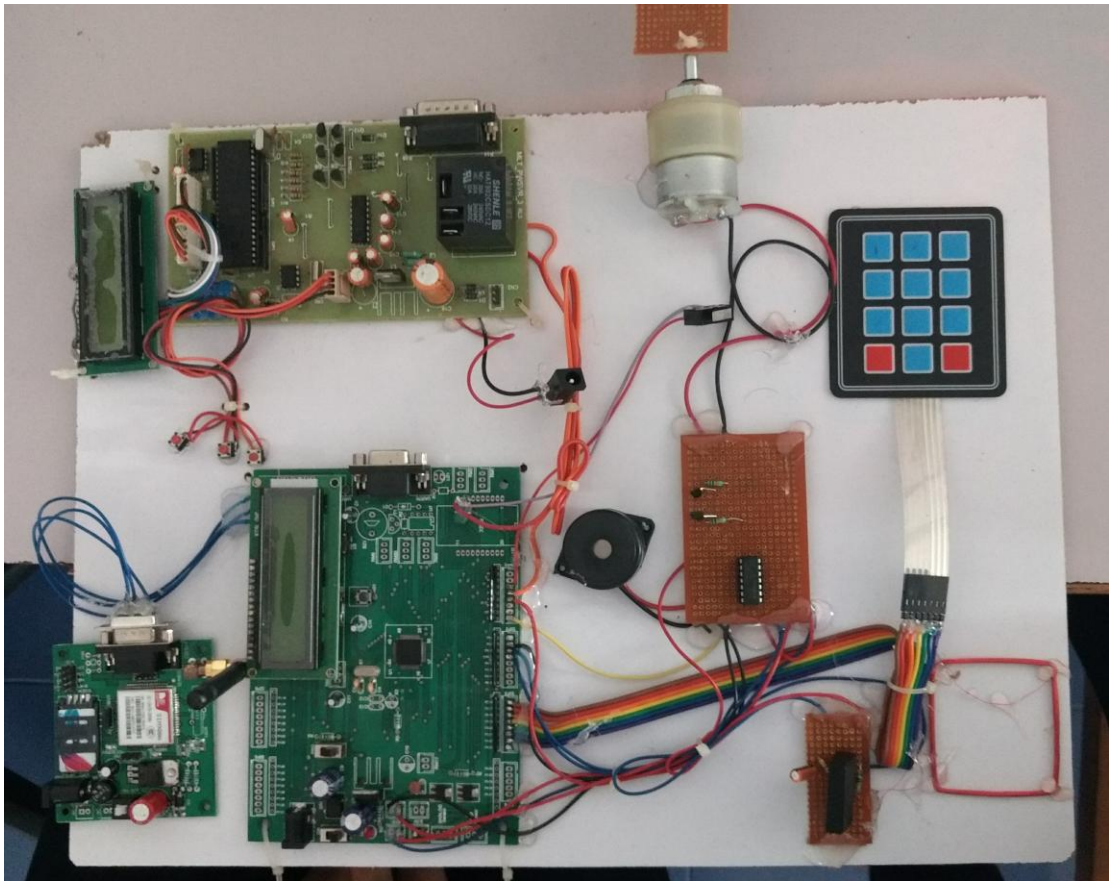


Fig 8.1(a) Electronic Protection for Exam Paper Leakage

- Real time clock is used to store time and date .we has to set the time and date in real time clock through s1, s2, s3 switches.
- RFID Reader sends signal to RFID tag, when we placed the tag near to it. The tag receives it and detects the signal and sends back again to the reader .The reader will converts into digital and send to the microcontroller.
- 12V DC motor used to open the lock of the embedded system .The output voltage of microcontroller is very low voltage which is not sufficient to drive the motor so motor driver is used.

- Miniature snap-action switch is used to send the message to the board whenever anybody try to open the box

LCD output during the startup of the embedded kit as shown below:

The LCD display should be show the message of the Electronic Protection for Exam Paper Leakage after the switch on the experiment kit.

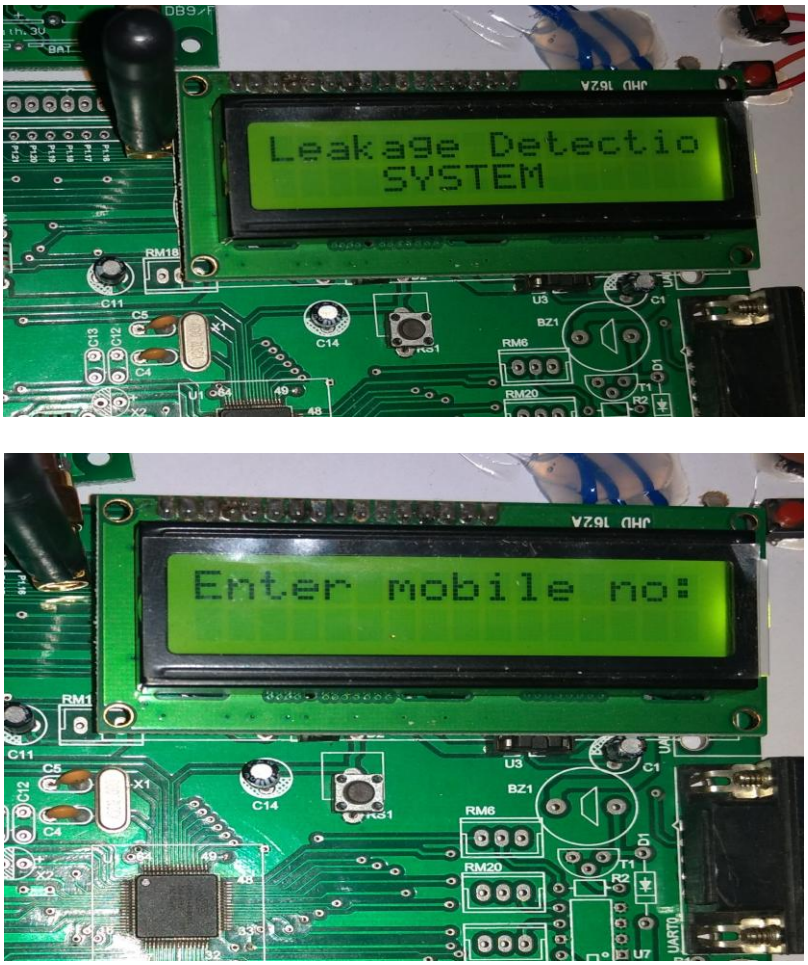


Fig 8.1 (b) LCD displays enter mobile number

LCD displaying the output during controller waits for the time which is set in RTC:

The LCD Display should be show the message waits for the time in LCD of the controller, when we set the time in real time clock using s1, s2, s3.

Fig 8.1 (c) LCD displays wait for the time

LCD displaying the output during controller asks for show Ur RFID card as shown below:

The LCD Display the message show Ur RFID card when it is time for exam in the LCD of the controller.

Fig 8.1 (d) LCD displays show Ur RFID card

LCD displaying the output during controller sending OTP to Authorized person as shown below:

The LCD Display the message sending OTP to the authorized person through GSM which is created in controller by the logic code.

.

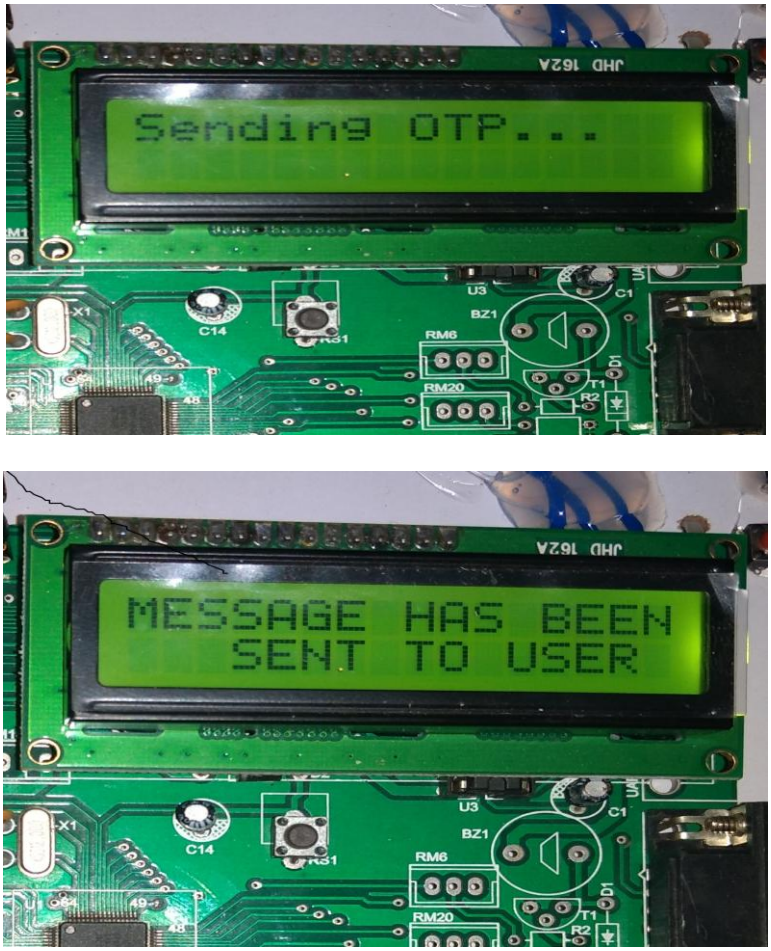


Fig 8.1(e) LCD displays sending OTP to authorized person

LCD displaying the output during controller asks for Enter Ur OTP as shown below:

The OTP which is get to authorized person is loaded into the microcontroller through 3*4 key matrix.

Fig 8.1(f) LCD displays enter ur OTP

LCD displaying the output during Lock of the box is open through motor mechanism as shown below:

Whenever entered OTP is valid, then lock will be open through motor mechanism. Otherwise GSM sends wrong OTP entered to authorized person.

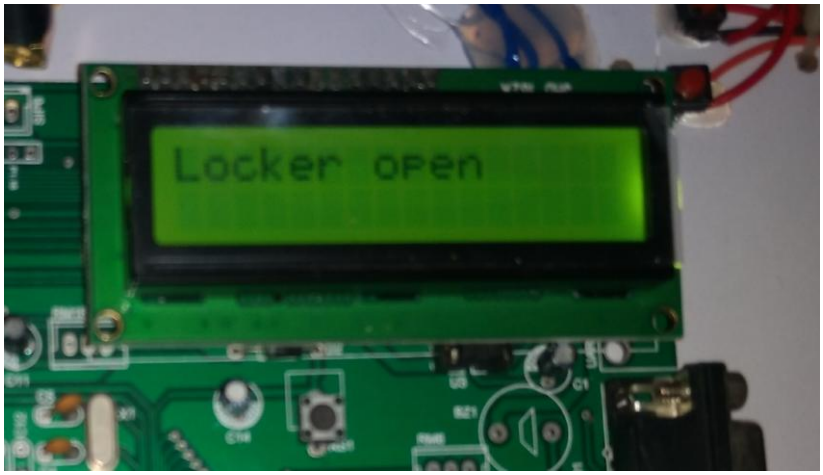


Fig 8.1(g) LCD displays locker open

Messages to authorized person from the controller as shown below:

Output to authorized person during Lock of the box is open, when wrong OTP entered, when OTP mismatch messages from GSM to mobile

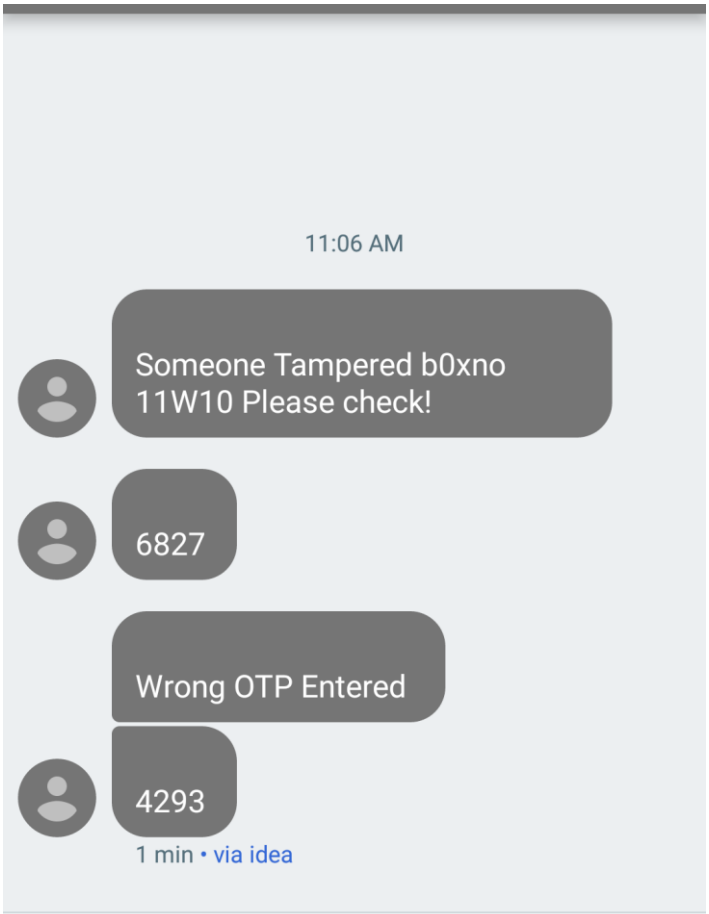


Fig 8.1(h) Output Results

CHAPTER 9
APPLICATIONS & ADVANTAGES

CHAPTER 9

APPLICATIONS & ADVANTAGES

9.1 Applications

- This project is implemented to detect and prevent the leakage of question papers in various university and civil service exams.
- It can be modified to protect some secret and confidential information papers related to our country.
- Electronic lockers in bank.
- Home security systems.
- Office security systems and other security enhanced electronic systems

9.2 Advantages

- Provides better security.
- Remote monitoring.
- No need of manual monitoring

CONCLUSION AND FUTURE SCOPE

CONCLUSION

An Effective system is proposed here which uses RFID, GSM and Real Time Synchronized clock. Examination section of university can deliver the question papers to the examination centers by password protected electronic security system. All these question papers will have next level security using RFID. Using GSM each activity involving opening and closing the box can be monitored in real time by university examination centre

FUTURE SCOPE

- This project can be extended by including biometric of the college authorities
- This project can be extended by placing gas sensor, which is used to detect the gas whenever anybody want to cut the box by using cutter
- This project also can be extended by placing vibration sensor in the box, which detects vibrations, whenever, anybody want to break the box with hammer.

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