Computer Organization

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1. Architecture diagrams:

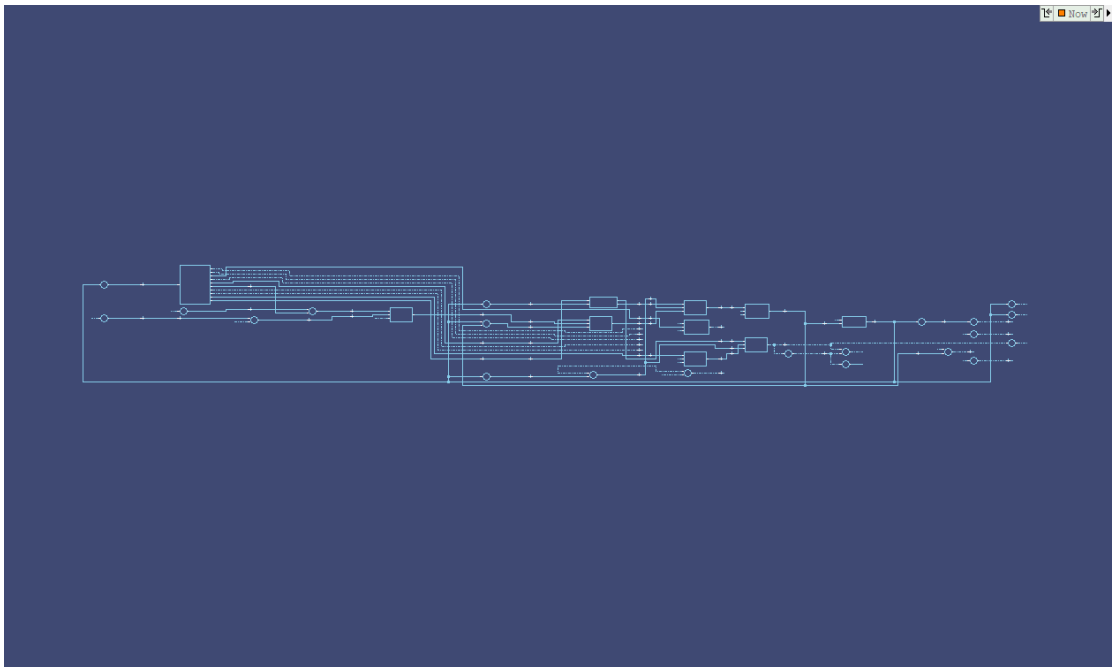

圖 1.1:Dataflow

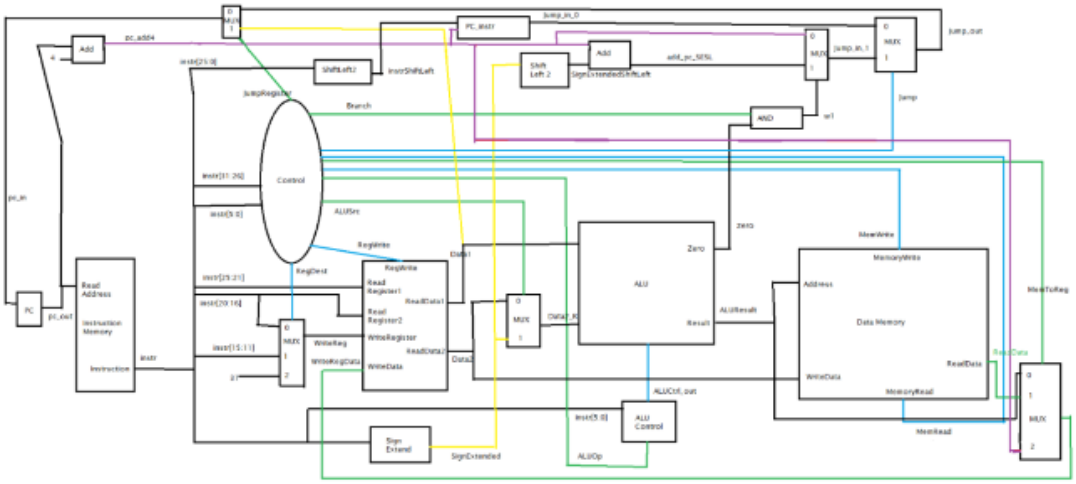

圖 1.2:Diagram

2. Hardware module analysis:

Lab3 跟 Lab2 在許多元件設計上均相同，少數不同的地方在於新增一些指令(J,

JAL, JR, LW, SW 還有 BEQ 的幾個延伸指令)，其中 JR 在 ALU_CTRL 時多了控制信號去決定 PC 的值，以及 BEQ 的延伸指令需要設計 4to1 MUX 的控制信號，大部分都是基於 LAB2 進行小改動。

3. Result:

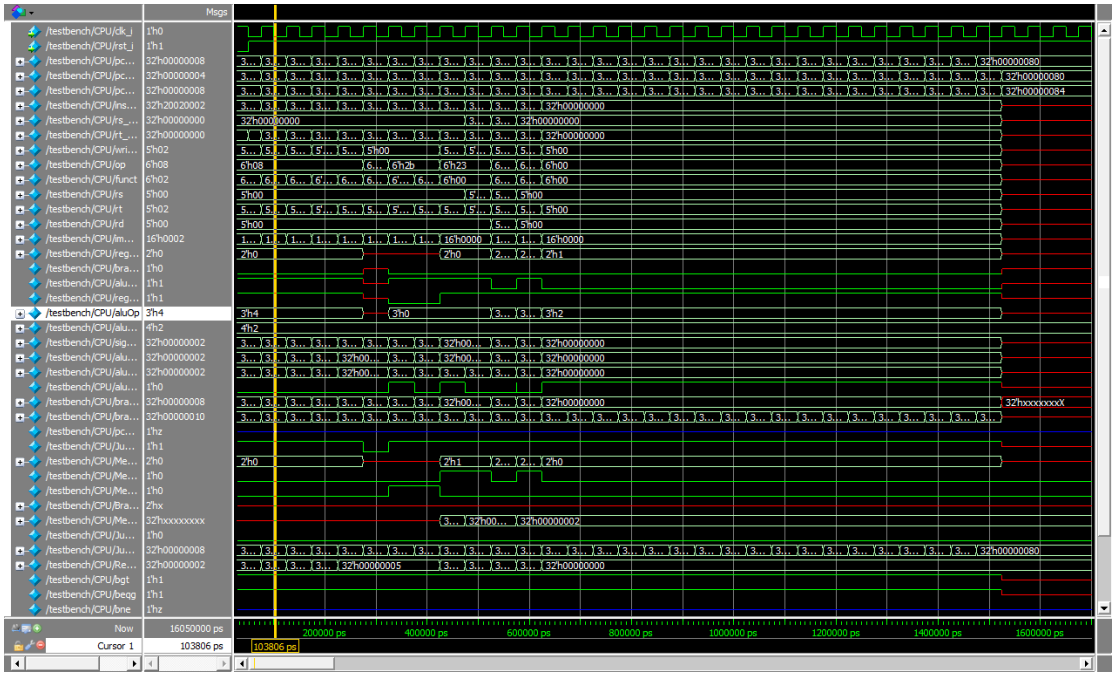

圖 3.1: test1 波形圖

```
# PC =        128
# Data Memory =          1,          2,          0,          0,          0,          0,          0,          0
# Data Memory =          0,          0,          0,          0,          0,          0,          0,          0
# Data Memory =          0,          0,          0,          0,          0,          0,          0,          0
# Data Memory =          0,          0,          0,          0,          0,          0,          0,          0
# Registers
# R0 =          0, R1 =          1, R2 =          2, R3 =          3, R4 =          4, R5 =          5, R6 =          1, R7 =
2
# R8 =          4, R9 =          2, R10 =          0, R11 =          0, R12 =          0, R13 =          0, R14 =          0, R15 =
0
# R16 =          0, R17 =          0, R18 =          0, R19 =          0, R20 =          0, R21 =          0, R22 =          0, R23 =
0
# R24 =          0, R25 =          0, R26 =          0, R27 =          0, R28 =          0, R29 =        128, R30 =          0, R31 =
0
# ** Note: $stop    : C:/Users/office01/Desktop/DCP3362/lab3/code/testbench.v(36)
#    Time: 16050 ns  Iteration: 0  Instance: /testbench
# Break in Module testbench at C:/Users/office01/Desktop/DCP3362/lab3/code/testbench.v line 36
```

圖 3.2: test1 結果圖

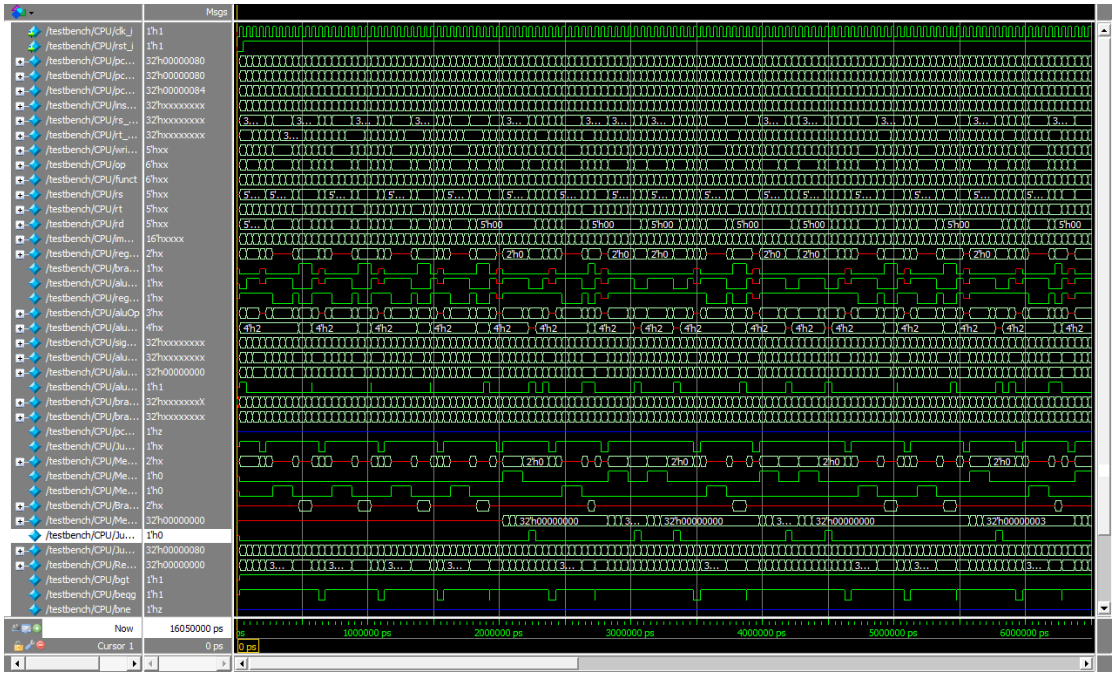

圖 3.3: test2 波形圖

```
# PC =        128
# Data Memory =          0,          0,          0,          0,          0,          0,          0,          0
# Data Memory =          0,          0,          0,          0,          0,          0,          0,          0
# Data Memory =          0,          0,          0,          0,         68,          2,          1,         68
# Data Memory =          2,          1,         68,          4,          3,         16,          0,          0
# Registers
# R0 =          0, R1 =          0, R2 =          5, R3 =          0, R4 =          0, R5 =          0, R6 =          0, R7 =
0
# R8 =          0, R9 =          1, R10 =          0, R11 =          0, R12 =          0, R13 =          0, R14 =          0, R15 =
0
# R16 =          0, R17 =          0, R18 =          0, R19 =          0, R20 =          0, R21 =          0, R22 =          0, R23 =
0
# R24 =          0, R25 =          0, R26 =          0, R27 =          0, R28 =          0, R29 =        128, R30 =          0, R31 =
16
# ** Note: $stop    : C:/Users/office01/Desktop/DCP3362/lab3/code/testbench.v(36)
#    Time: 16050 ns  Iteration: 0  Instance: /testbench
# Break in Module testbench at C:/Users/office01/Desktop/DCP3362/lab3/code/testbench.v line 36
```

圖 3.4: test2 結果圖

4. Summary:

LAB3 的電路設計較 LAB2 複雜很多，在 test2 的實驗中，說明文檔只有說 reg2 最終為 5，但不確定其他值是否需要為 0，在我的設計裡，並沒有將其他值復位為 0。