MEMORY MANAGEMENT UNIT

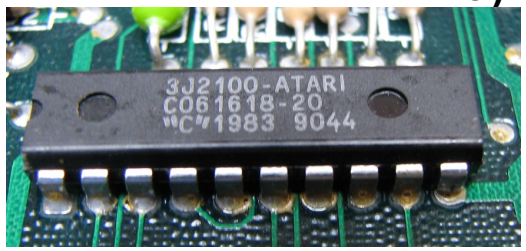
소프트웨어융합 2019102098 방민수

CONTENTS

MMU - Hardware

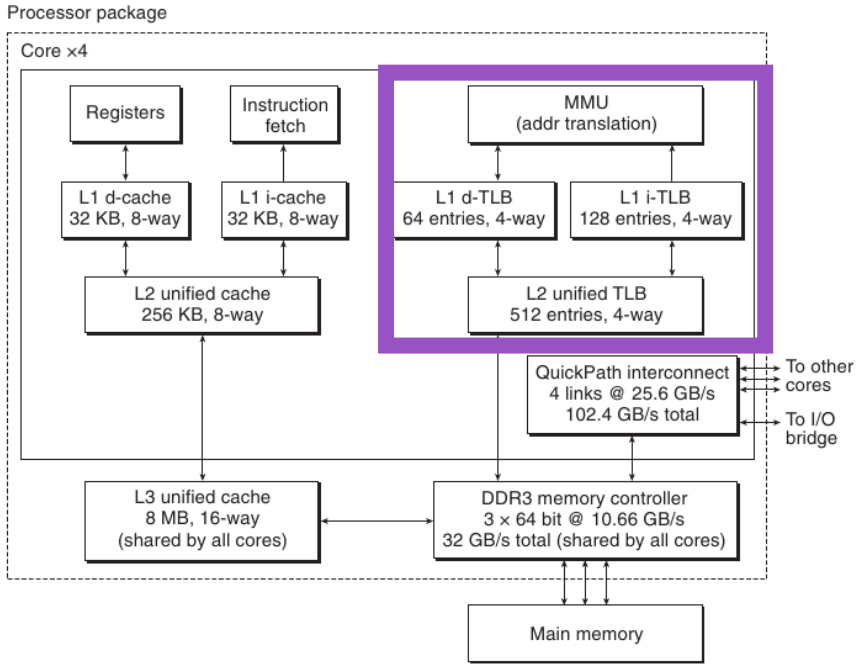
PAST – External Hardware

68451 MMU (used with Motorola 6801 0)



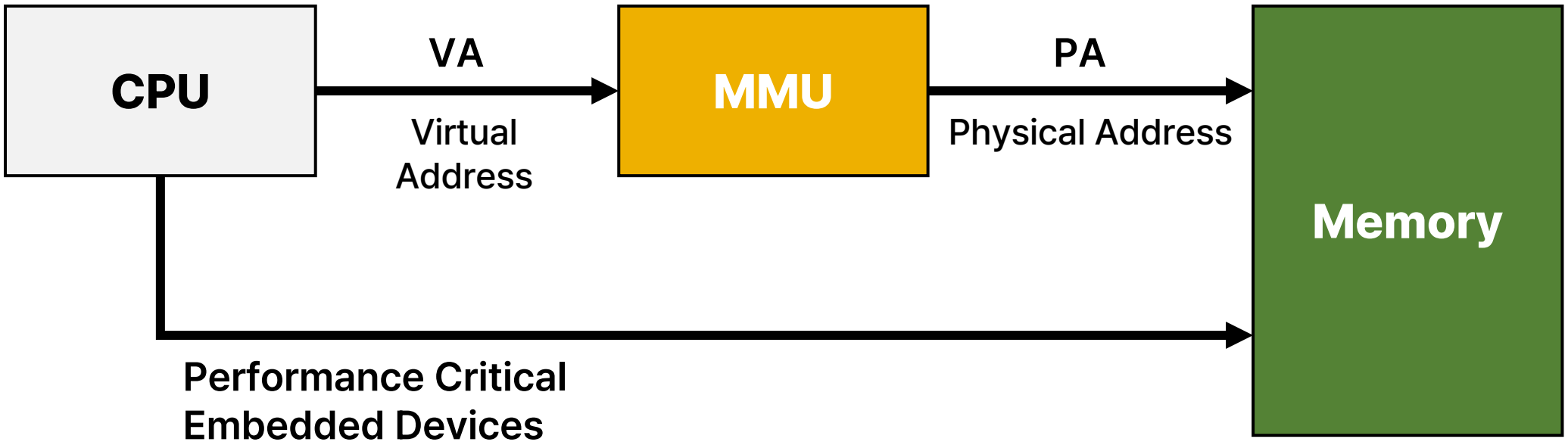
Atari MMU (for the Atari 8-bit computers)

RECENT – Integrate with CPU

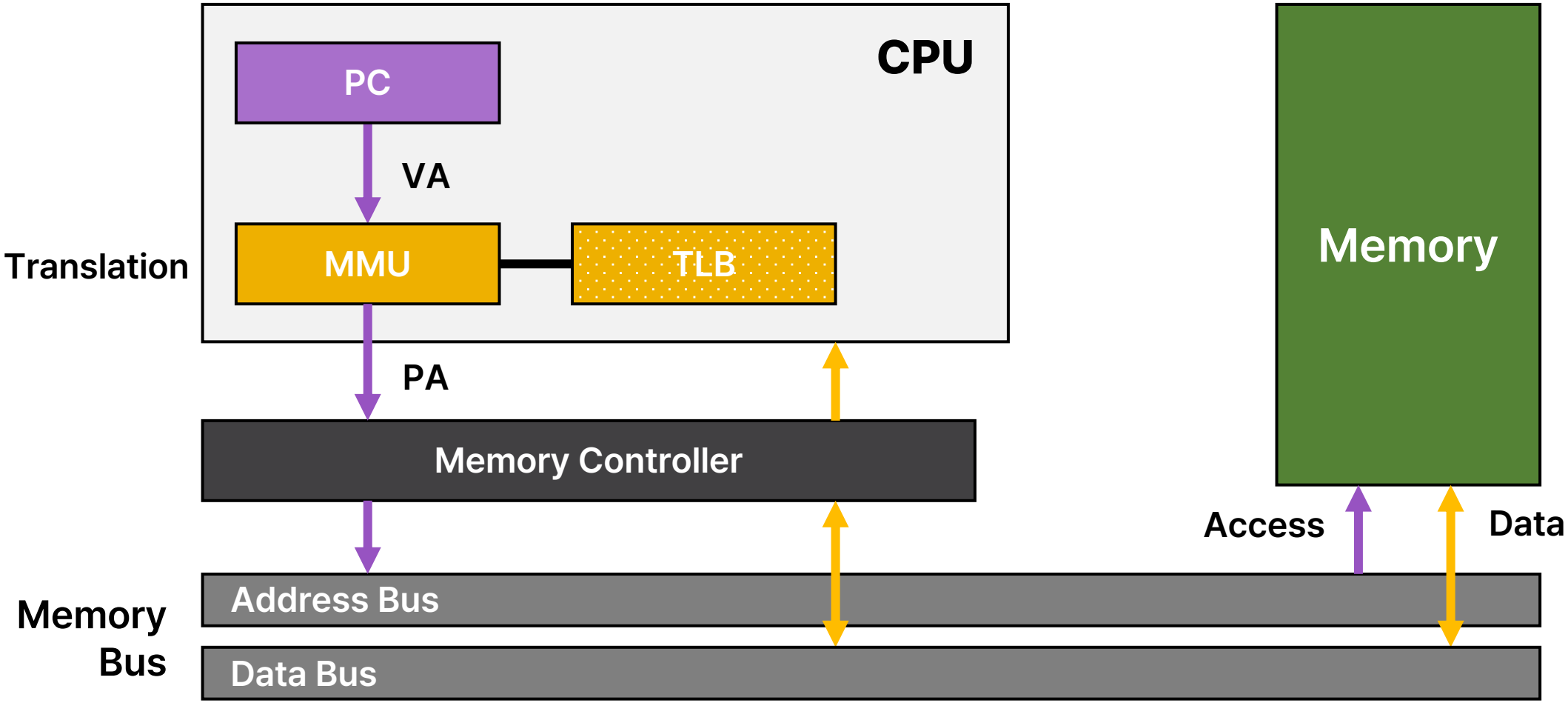


Intel Core i7 Memory System

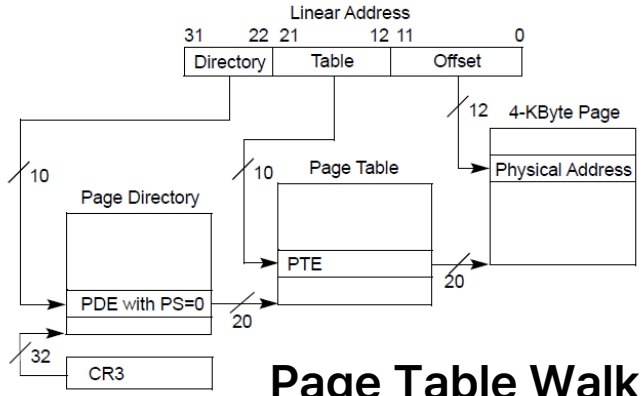
MMU – Translation (Remind)



MMU - Architecture

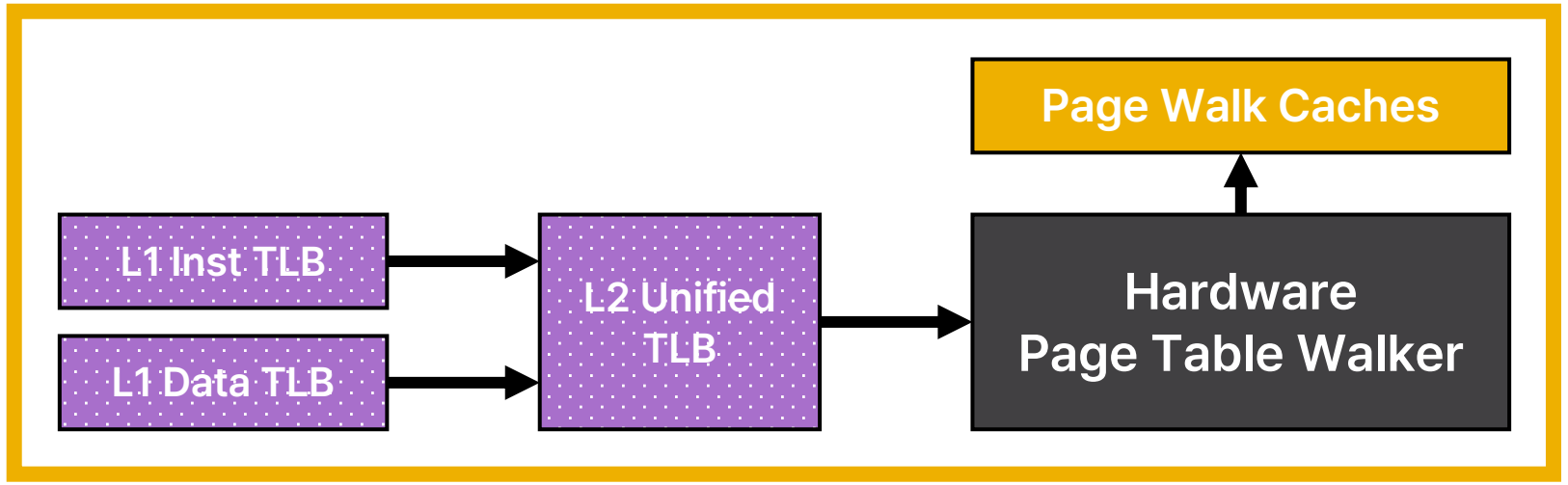


Inside MMU (Intel Skylake)

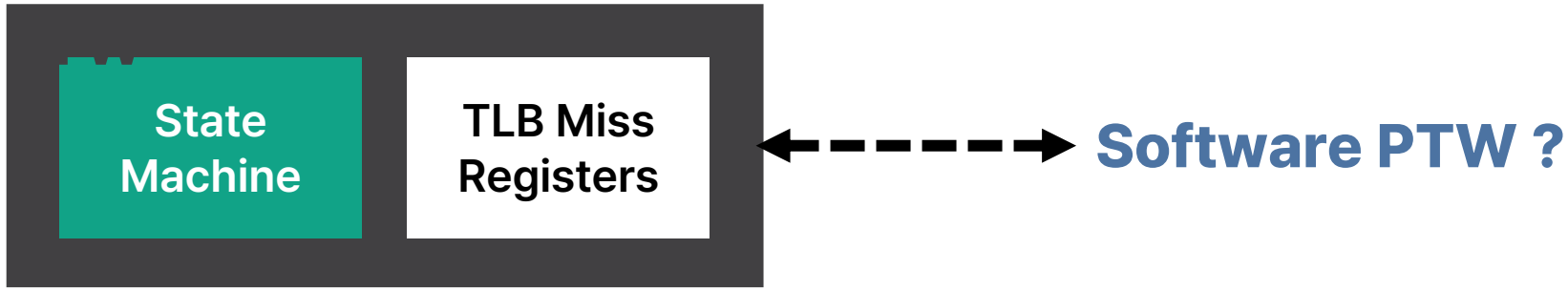


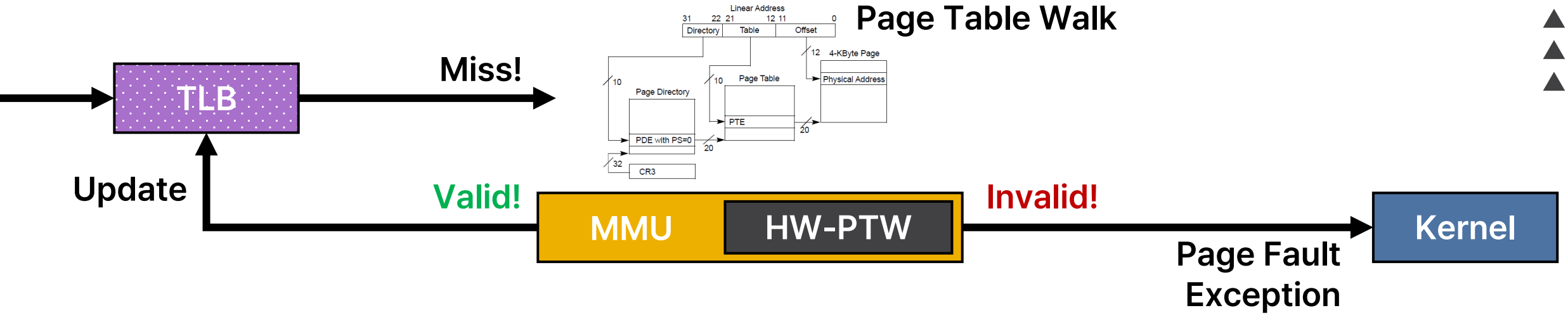
Page Table Walk

MMU



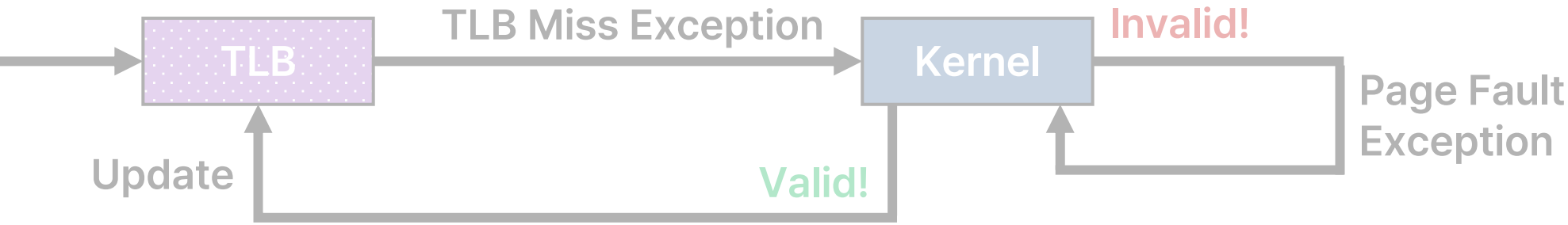
Hardware

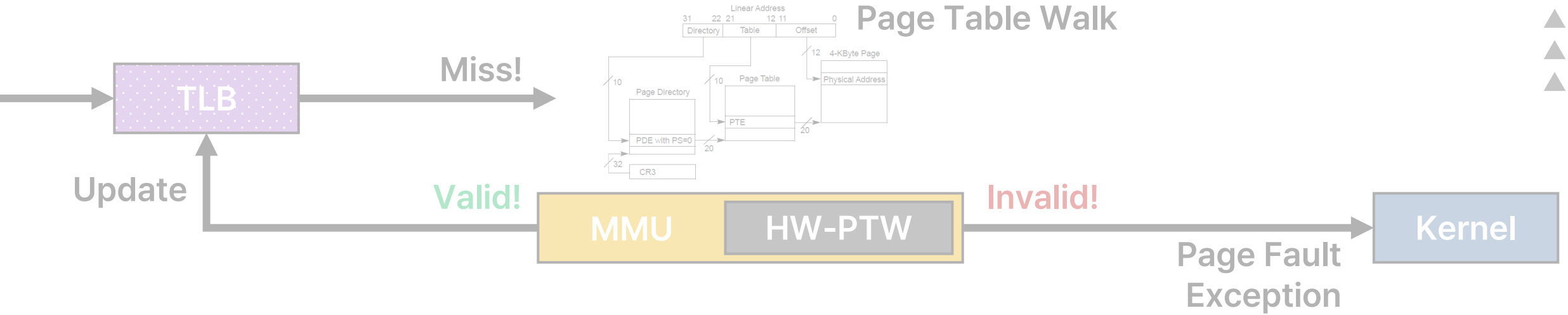




HW Managed PTW

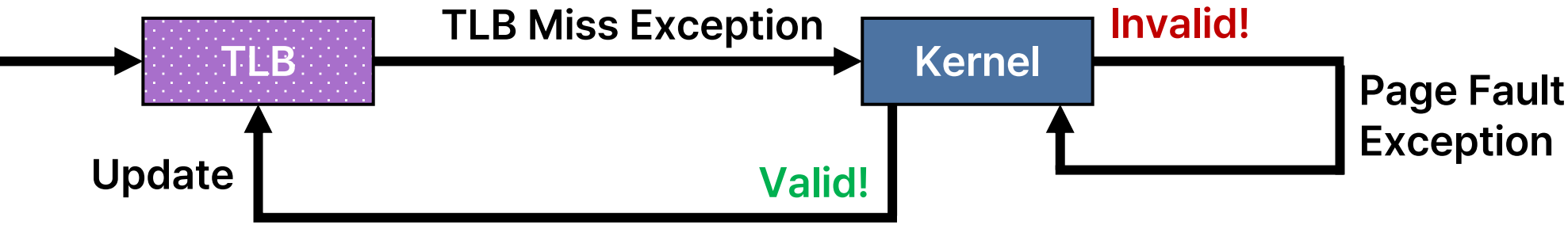
SW Managed PTW





HW Managed PTW

SW Managed PTW



x86 CR3, CR2

31(63) 0

Page-Directory Base | PCD | PWT

CR3

Start Address of Page Directory

Used at Page Walk

31(63) 0

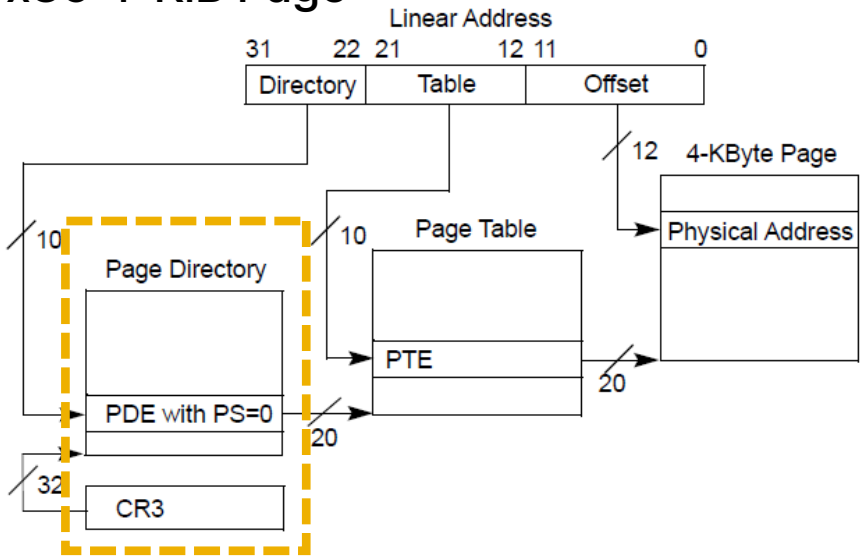
Page-Fault Linear Address

CR2

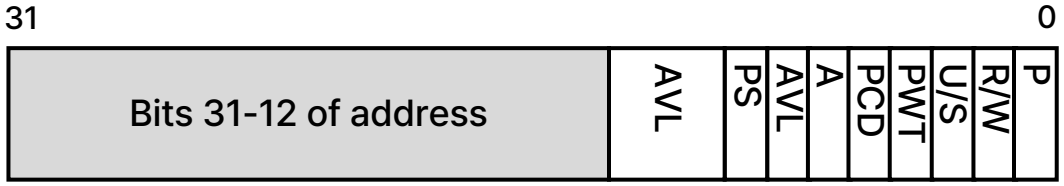
Linear address of program attempted to access

Used at Page Fault Exception Handling

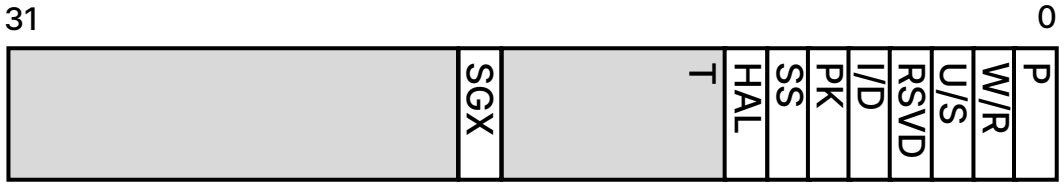
x86 4-KiB Page



Page Fault Exception

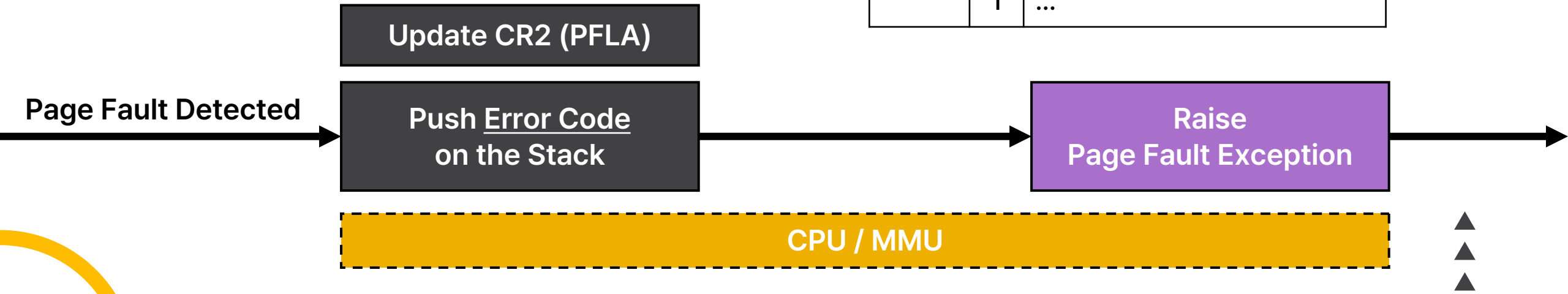


x86 4KiB-Page PDE

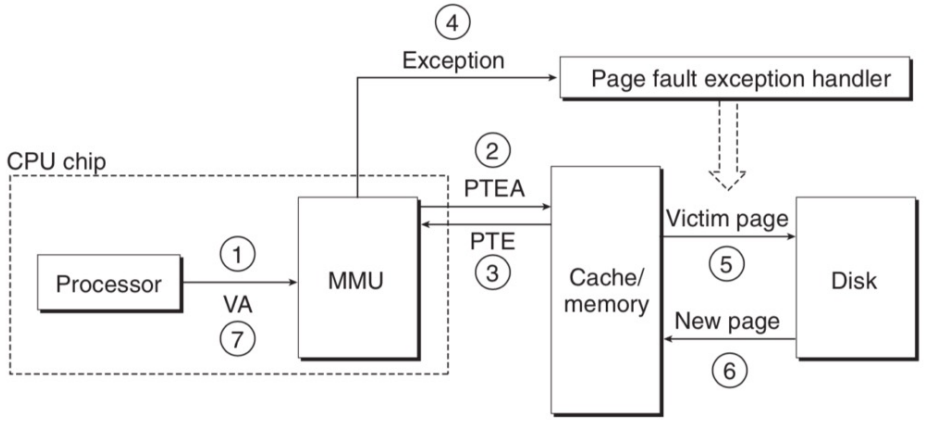


Page Fault Error Code (Pushed on Stack)

P	0	Non-Present Page
	1	Protection Violation
W/R	0	Access was a Read
	1	Access was a Write
U/S	0	Supervisor-Mode Access
	1	User-Mode Access
...	0	...
	1	...



Page Fault Exception



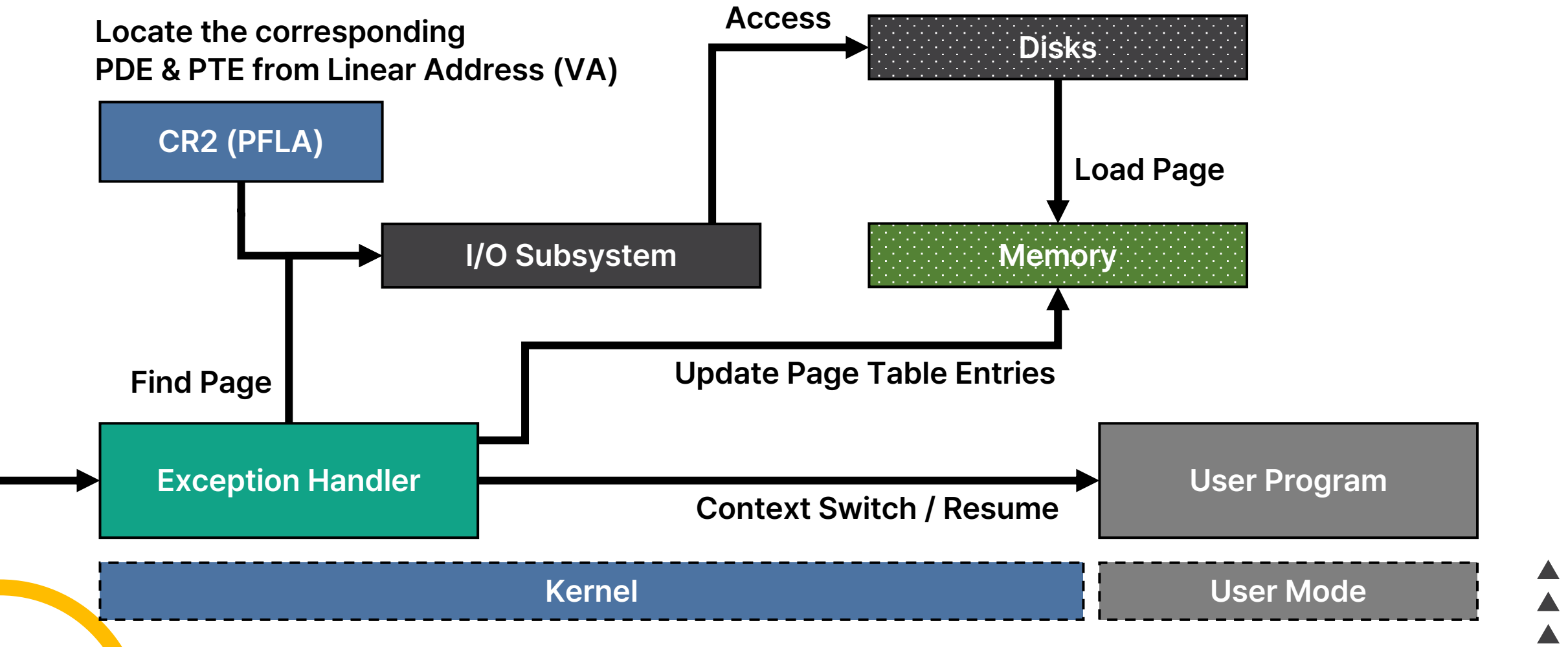
Interrupt Vector Table

IVT Offset	INT #	Description
0x0000	0x00	Divide by 0
0x0004	0x01	Reserved
...	...	...
0x0038	**0x0E**	**Page Fault**
...	...	...

Raise Page Fault Exception → **Context Switch** → **Exception Handler**

CPU / MMU | **Kernel**

Page Fault Exception



Thank you for Listening